

N - CHANNEL ENHANCEMENT MODE "ULTRA HIGH DENSITY" POWER MOS TRANSISTOR

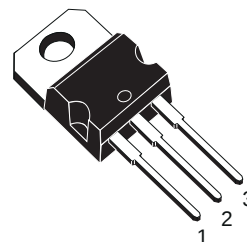
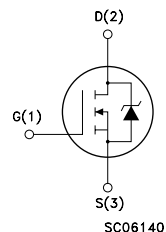
PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP40N03L-20	30 V	< 0.02 Ω	40 A

- TYPICAL R_{DS(on)} = 0.016 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- HIGH CURRENT CAPABILITY
- 175°C OPERATING TEMPERATURE
- HIGH dV/dt CAPABILITY
- APPLICATION ORIENTED CHARACTERIZATION

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- POWER MOTOR CONTROL
- DC-DC & DC-AC CONVERTERS
- SYNCHRONOUS RECTIFICATION


TO-220
INTERNAL SCHEMATIC DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 kΩ)	30	V
V _{GS}	Gate-source Voltage	± 15	V
I _D	Drain Current (continuous) at T _c = 25 °C	40	A
I _D	Drain Current (continuous) at T _c = 100 °C	28	A
I _{DM} (•)	Drain Current (pulsed)	160	A
P _{tot}	Total Dissipation at T _c = 25 °C	90	W
	Derating Factor	0.6	W/°C
dV/dt(1)	Peak Diode Recovery voltage slope	6	V/ns
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(•) Pulse width limited by safe operating area

STP40N03L-20

THERMAL DATA

R _{thj-case}	Thermal Resistance Junction-case	Max	1.66	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	Max	62.5	°C/W
R _{thc-sink}	Thermal Resistance Case-sink	Typ	0.5	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max, $\delta < 1\%$)	40	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 25 V)	300	mJ
E _{AR}	Repetitive Avalanche Energy (pulse width limited by T _j max, $\delta < 1\%$)	75	mJ
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (T _c = 100 °C, pulse width limited by T _j max, $\delta < 1\%$)	28	A

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μ A V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating x 0.8 T _c = 125 °C			250 1000	μ A μ A
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 15 V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μ A	1	1.6	2	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V I _D = 20 A V _{GS} = 10V I _D = 20 A T _c = 100°C V _{GS} = 5V I _D = 20 A		0.016 0.019	0.02 0.023	Ω Ω Ω
I _{D(on)}	On State Drain Current	V _{DS} > I _{D(on)} x R _{DS(on)max} V _{GS} = 10 V	40			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} > I _{D(on)} x R _{DS(on)max} I _D = 20 A	15	22		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25 V f = 1 MHz V _{GS} = 0		1800 450 180	2300 580 230	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	$V_{DD} = 15\text{ V}$ $I_D = 10\text{ A}$		20	30	ns
t_r	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$ (see test circuit, figure 3)		80	100	ns
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 24\text{ V}$ $I_D = 20\text{ A}$ $R_G = 50\ \Omega$ $V_{GS} = 5\text{ V}$ (see test circuit, figure 5)		200		A/ μ s
Q_g	Total Gate Charge	$V_{DD} = 24\text{ V}$ $I_D = 20\text{ A}$ $V_{GS} = 5\text{ V}$		40	60	nC
Q_{gs}	Gate-Source Charge			10		nC
Q_{gd}	Gate-Drain Charge			20		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 24\text{ V}$ $I_D = 20\text{ A}$		42	55	ns
t_f	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$		45	60	ns
t_c	Cross-over Time	(see test circuit, figure 5)		76	100	ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				40	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				160	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 40\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 20\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 24\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, figure 5)		65		ns
Q_{rr}	Reverse Recovery Charge			0.12		μC
I_{RRM}	Reverse Recovery Current			4		A

(*) Pulsed: Pulse duration = 300 μ s, duty cycle 1.5 %

(\bullet) Pulse width limited by safe operating area

(1) $I_{SD} \leq 40\text{ A}$, $di/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

STP40N03L-20

PSPICE PARAMETERS

SUBCIRCUIT COMPONENTS

Symbol	Parameter	Value	Unit
S1	(V14_16<0) (See Power Mosfet Model Subcircuit)	ON	
S2	(V16_11<0) (See Power Mosfet Model Subcircuit)	ON	
LD	Drain Inductance	8	nH
LG	Gate Inductance	10	nH
LS	Source Inductance	10	nH
RDRAIN	Drain Resistance	$1.9E^{-2}$	Ω
RGATE	Gate Resistance	1	Ω
CGD	Gate Drain Capacitance	3.92	nF
CGS	Gate Source Capacitance	1.9	nF
ALFA	Drift Coefficient	$1E^{-3}$	V^{-1}
RGN	Negative Bias Resistance	10	K Ω

DIODE DRAIN GATE (Depletion Capacitance)

Symbol	Parameter	Value	Unit
CJO	Zero Bias p-n Capacitance	2.7	nF
VJ	p-n Potential	0.35	V
M	p-n Grading Coefficient	0.55	

DIODE DRAIN SOURCE

Symbol	Parameter	Value	Unit
CJO	Zero Bias p-n Capacitance	10	nF
VJ	p-n Potential	0.35	V
M	p-n Grading Coefficient	0.55	
TT	Transit Time	20	nsec

N MOSFET

Symbol	Parameter	Value	Unit
L	Channel Length	1	μ Meter
W	Channel Width	1	μ Meter
LEVEL	Model Index	3	
TOX	Oxide Thickness	1	Meter
VTO	Zero Bias Threshold Voltage	3.25	V
U0	Surface Mobility	600	cm^2/Vs
THETA	Mobility Modulation	0.005	V^{-1}
Vmax	Maximum Drift Velocity	0	Meter/sec
KP	Trans Conductance Coefficient	15	Amp/ V^2

For Transient Simulation Applicate U.I.C. (Use Initial Condition) Option

PSPICE NETLIST OF THE SUBCIRCUIT

.SUBCKT STP40N03L-20 1 2 3

*VALUE OF THE PACKAGE INDUCTANCES

LS 1 11 10n

LG 2 12 10n

LD 3 13 7n

*RESISTANCE OF THE GATE

POLYSILICON

RG 12 16 1

*EPY AND DRIFT RESISTANCES

RD 13 14 1.9e-02

EDRI 14 15 POLY(2) (13 14) (13 11) 0 0 0 0
1e-3

*CAPACITANCE GATE SOURCE

CGS 16 11 1.90n

*OPTIONAL FOR NEGATIVE GATE BIAS

*S2 51 11 11 16 SWITCH

*CGN 51 16 3.92n

*RGN 51 16 10k

*MILLER CAPACITANCE

CGD 16 17 3.92n

* DEPLETION CAPACITANCE

DGD 17 14 DGD

S1 17 14 16 14 SWITCH

.MODEL DGD D +IS=

+CJO=2.6n

+Vj=.1

+M=.6

.MODEL SWITCH VSWITCH

+RON=1m

+ROFF=1MEG

+VON=0.1

* OUTPUT CAPACITANCE AND BODY DRAIN DIODE

DBD 11 14 DBD

.MODEL DBD D

+TT=20n

+CJO=7.8n

+VJ=.1

+M=.6

* MODEL OF THE MOSFET

MMAIN 15 16 11 11 MMAIN L=1u W=1u

.MODEL MMAIN NMOS

+LEVEL=3

+TOX=1

+VTO=3.25

+uo=600

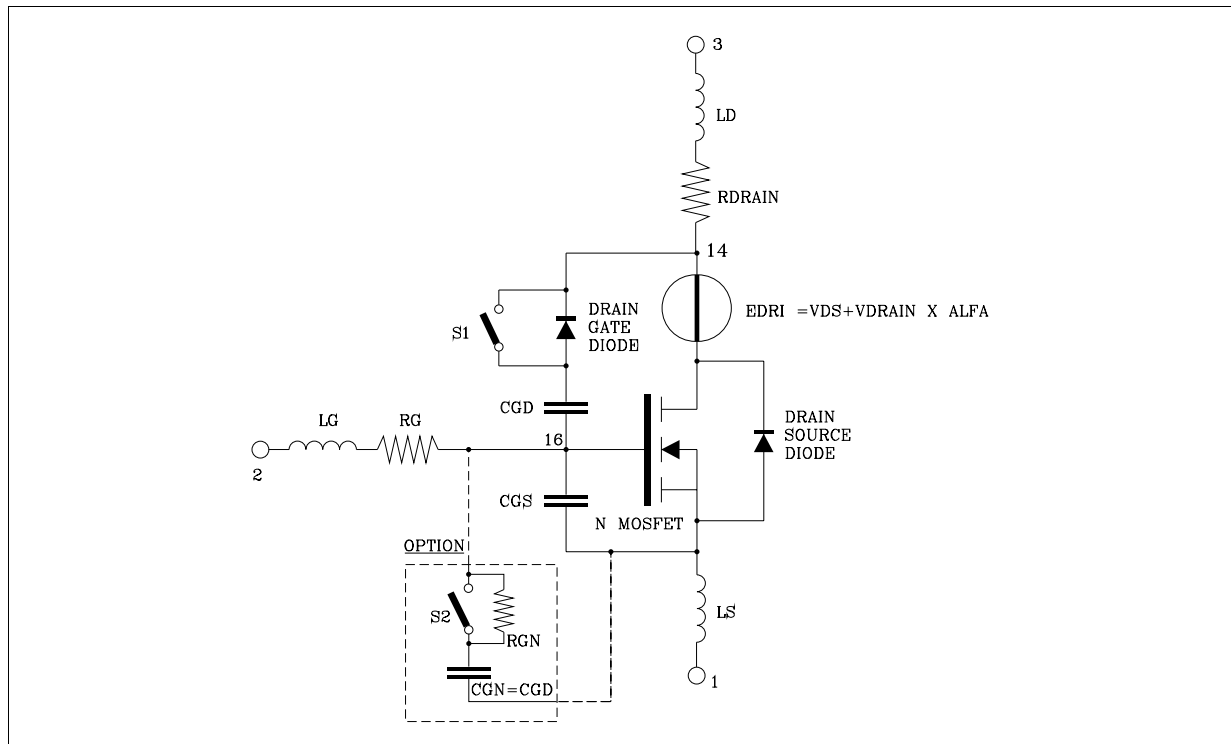
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+VMAX=5e7

+KP=28

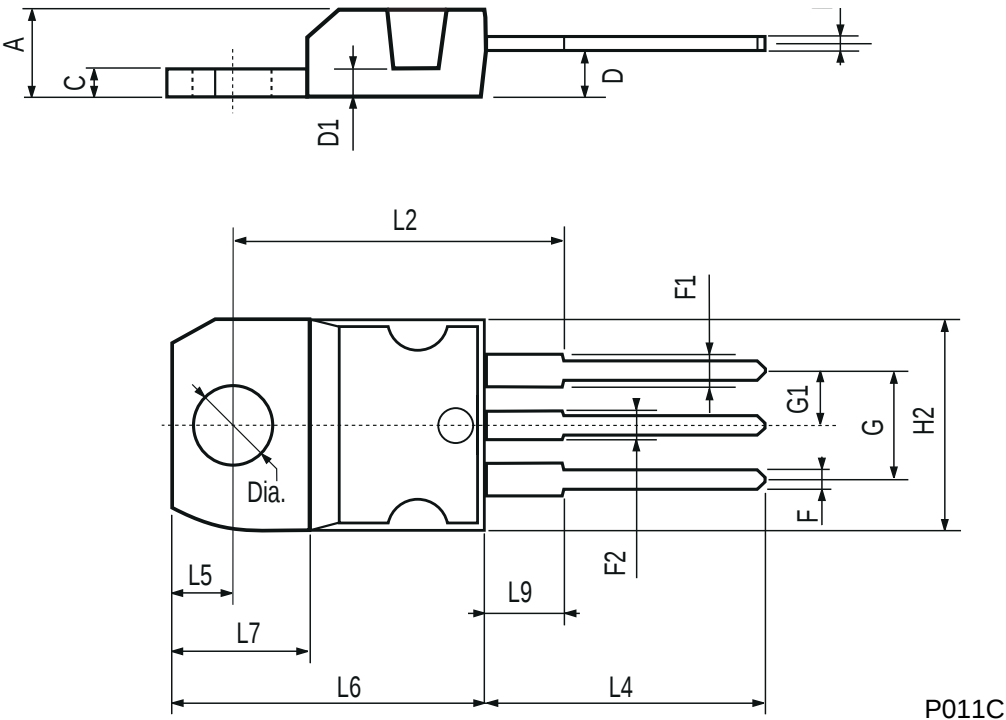
.ENDS

Power Mosfet Model Subcircuit



TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



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