

STN7NF10

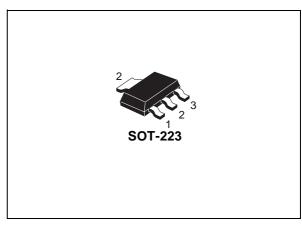
N-CHANNEL 100V - 0.055 Ω - 5A SOT-223 LOW GATE CHARGE STripFET™ II POWER MOSFET

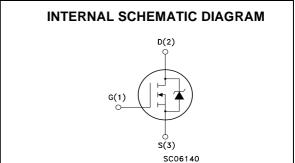
TYPE	V _{DSS}	R _{DS(on)}	I _D
STN7NF10	100 V	< 0.065 Ω	5 A

- TYPICAL $R_{DS}(on) = 0.055 \Omega$
- APPLICATION ORIENTED CHARACTERIZATION



This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.





APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	100	V
V _G S	Gate- source Voltage	±20	V
ID	Drain Current (continuous) at T _C = 25°C	5	Α
I _D	Drain Current (continuous) at T _C = 100°C	3.4	А
I _{DM} (●)	Drain Current (pulsed)	20	А
P _{TOT}	Total Dissipation at T _C = 25°C	3.3	W
	Derating Factor	0.026	W/°C
T _{stg}	Storage Temperature	-55 to 150	°C
Tj	Operating Junction Temperature	-55 to 150	

(•) Pulse width limited by safe operating area

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THERMAL DATA

Rthj-PCB	Thermal Resistance Junction-PCB Max(*)	38	°C/W
Rthj-PCB	Thermal Resistance Junction-PCB Max(**)	100	°C/W
Tı	Maximum Lead Temperature For Soldering Purpose (1.6 mm from case,for 10s)	260	°C

Note: (*) When mounted on 1 in² FR-4 BOARD,2 oz Cu, t<10s.

Note: (**) When mounted on minimum footprint.

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25 \, ^{\circ}C$ UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0$	100			V
I _{DSS}	Zero Gate Voltage	V _{DS} = Max Rating			1	μA
	Drain Current (V _{GS} = 0)	V _{DS} = Max Rating, T _C = 125 °C			10	μΑ
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 1.5 A		0.055	0.065	Ω

DYNAMIC

Symbol	Parameter	Test Conditions Min.		Тур.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 15 V , I _D = 1.5 A		12		S
C _{iss}	Input Capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		870		pF
Coss	Output Capacitance			125		pF
C _{rss}	Reverse Transfer Capacitance			52		pF

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ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on Delay Time	V _{DD} = 50 V, I _D = 12 A		58		ns
t _r	Rise Time	$R_G = 4.7\Omega V_{GS} = 10 V$ (see test circuit, Figure 3)		45		ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 80 V, I _D = 24 A, V _{GS} = 10 V		30 6 10	41	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(off)}	Turn-off-Delay Time Fall Time	$V_{DD} = 50 \text{ V}, I_D = 12 \text{ A},$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		49 17		ns ns

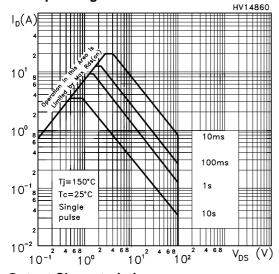
SOURCE DRAIN DIODE

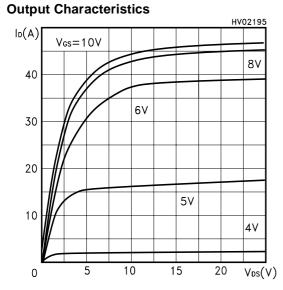
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain Current				5	Α
I _{SDM} (1)	Source-drain Current (pulsed)				20	Α
V _{SD} (2)	Forward On Voltage	I _{SD} = 5 A, V _{GS} = 0			1.3	V
t _{rr} Q _{rr} IRRM	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 5 A, di/dt = 100A/µs, V_{DD} = 30 V, T_j = 150°C (see test circuit, Figure 5)		100 375 7.5		ns nC A

Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

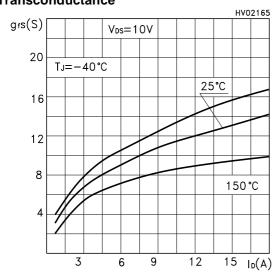
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Safe Operating Area

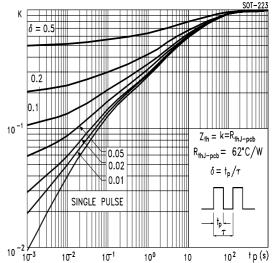




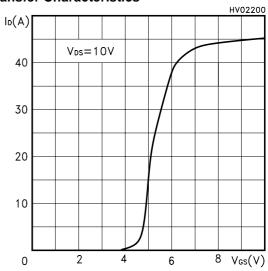
Transconductance



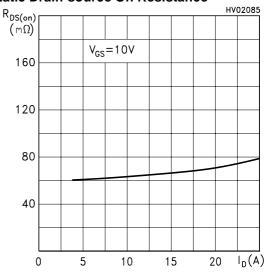
Thermal Impedence



Transfer Characteristics

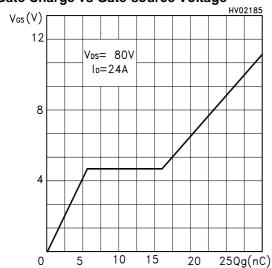


Static Drain-source On Resistance

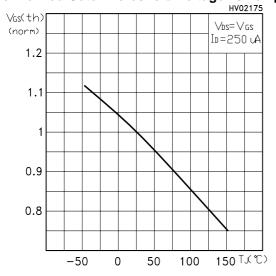


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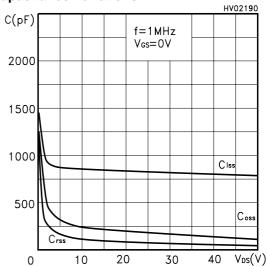
Gate Charge vs Gate-source Voltage



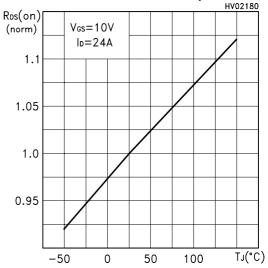
Normalized Gate Thereshold Voltage vs Temp.



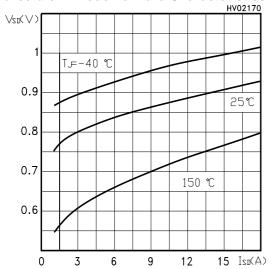
Capacitance Variations



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



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Fig. 1: Unclamped Inductive Load Test Circuit

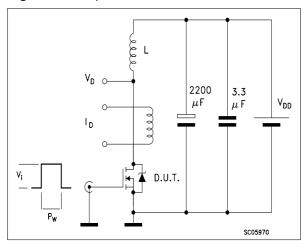


Fig. 3: Switching Times Test Circuit For Resistive Load

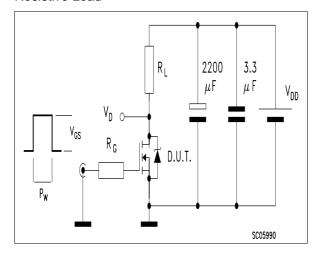


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

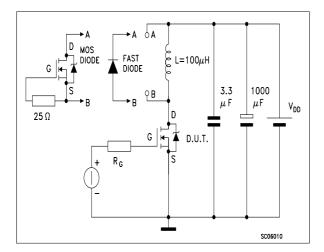


Fig. 2: Unclamped Inductive Waveform

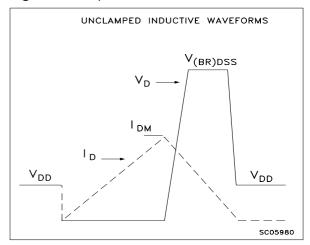
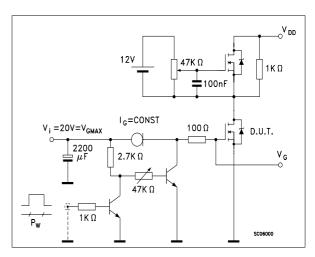


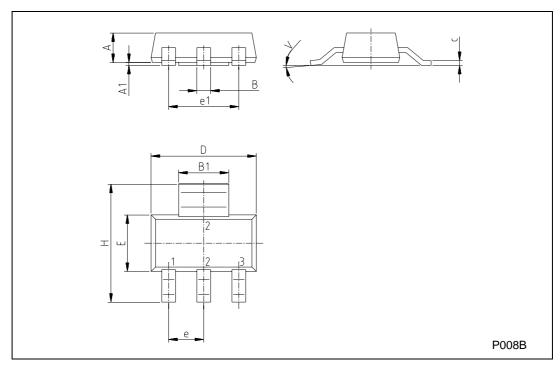
Fig. 4: Gate Charge test Circuit



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SOT-223 MECHANICAL DATA

DIM.		mm			inch	
Diwi.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А			1.80			0.071
В	0.60	0.70	0.80	0.024	0.027	0.031
B1	2.90	3.00	3.10	0.114	0.118	0.122
С	0.24	0.26	0.32	0.009	0.010	0.013
D	6.30	6.50	6.70	0.248	0.256	0.264
е		2.30			0.090	
e1		4.60			0.181	
Е	3.30	3.50	3.70	0.130	0.138	0.146
Н	6.70	7.00	7.30	0.264	0.276	0.287
V			10°			10°
A1		0.02				



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