



STN2NE10L

N-CHANNEL 100V - 0.33Ω - 2A SOT-223 STripFET™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STN2NE10L	100 V	< 0.4 Ω	1.8 A

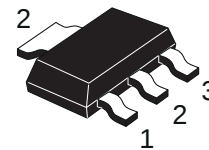
- TYPICAL R_{DS(on)} = 0.33 Ω
- EXCEPTIONAL dv/dt CAPABILITY
- AVALANCHE RUGGED TECHNOLOGY
- 100 % AVALANCHE TESTED
- LOW THRESHOLD DRIVE

DESCRIPTION

This Power Mosfet is the latest development of STMicroelectronics unique "Single Feature Size™" stip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

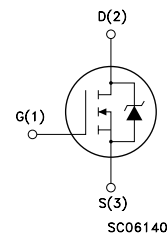
APPLICATIONS

- DC MOTOR CONTROL (DISK DRIVES, etc.)
- DC-DC & DC-AC CONVERTERS
- SYNCHRONOUS RECTIFICATION



SOT-223

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100	V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 kΩ)	100	V
V _{GS}	Gate-source Voltage	± 20	V
I _D	Drain Current (continuous) at T _c = 25 °C	1.8	A
I _D	Drain Current (continuous) at T _c = 100 °C	1.3	A
I _{DM} (•)	Drain Current (pulsed)	7.2	A
P _{tot}	Total Dissipation at T _c = 25 °C	2.5	W
	Derating Factor	0.02	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	6	V/ns
T _{stg}	Storage Temperature	-65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 7.2 A, di/dt ≤ 200 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}

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THERMAL DATA

$R_{thj-pcb}$	Thermal Resistance Junction-PC Board	Max	50	$^{\circ}\text{C/W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient (Surface Mounted)	Max	60	$^{\circ}\text{C/W}$
T_l	Maximum Lead Temperature For Soldering Purpose		260	$^{\circ}\text{C}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	1.8	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 25\text{ V}$)	20	mJ

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0$	100			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\text{ }\mu\text{A}$	1	1.7	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$ $I_D = 1\text{ A}$ $V_{GS} = 5\text{ V}$ $I_D = 1\text{ A}$		0.33 0.38	0.4 0.45	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\text{ V}$	1.8			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 1\text{ A}$	1	3		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0\text{ V}$		345 45 20		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 50\text{ V}$ $I_D = 3.5\text{ A}$		7		ns
t_r	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$ (Resistive Load, see fig. 3)		17		ns
Q_g	Total Gate Charge	$V_{DD} = 80\text{ V}$ $I_D = 7\text{ A}$ $V_{GS} = 5\text{ V}$		10	14	nC
Q_{gs}	Gate-Source Charge			5		nC
Q_{gd}	Gate-Drain Charge			4		nC

SWITCHING OFF

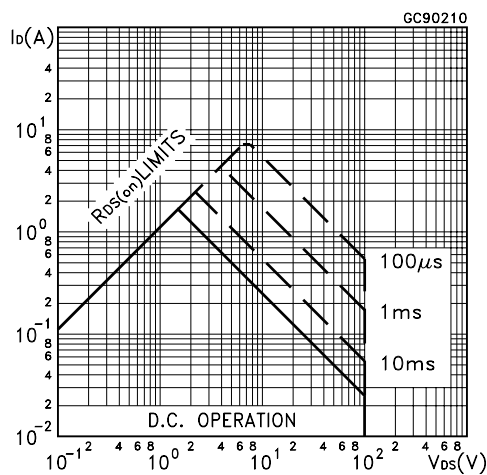
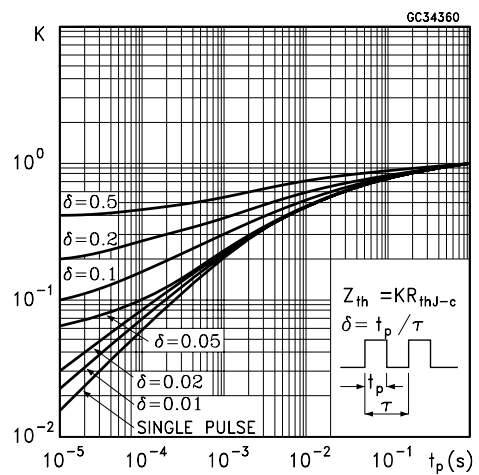
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 80\text{ V}$ $I_D = 3.5\text{ A}$		22		ns
t_f	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$ (Resistive Load, see fig. 3)		8		ns
$t_r(V_{off})$	Off-voltage Rise Time	$V_{DD} = 80\text{ V}$ $I_D = 7\text{ A}$		8		ns
t_f	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$		9		ns
t_c	Cross-over Time	(Inductive Load, see fig. 5)		19		ns

SOURCE DRAIN DIODE

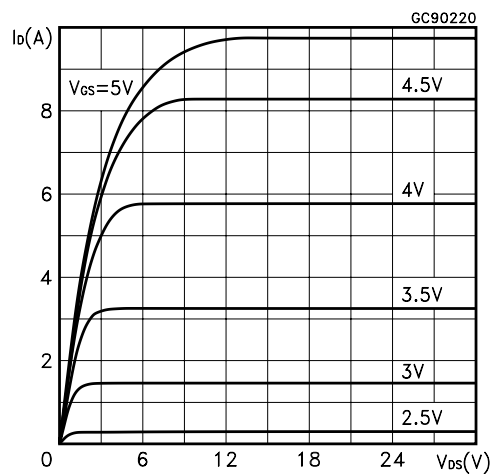
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				2	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				8	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 2\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 7\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ (see test circuit, fig. 5)		75		ns
Q_{rr}	Reverse Recovery Charge			190		μC
I_{RRM}	Reverse Recovery Current			5		A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

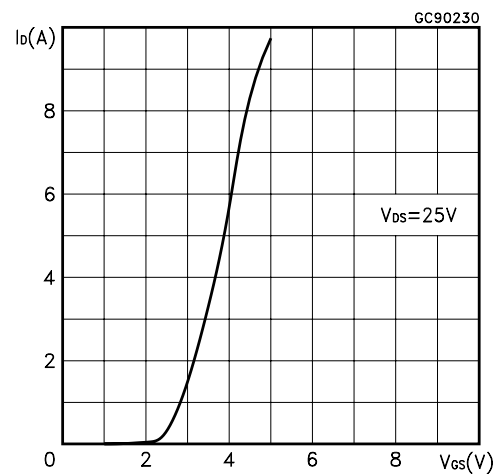
(•) Pulse width limited by safe operating area

Safe Operating Area**Thermal Impedance**

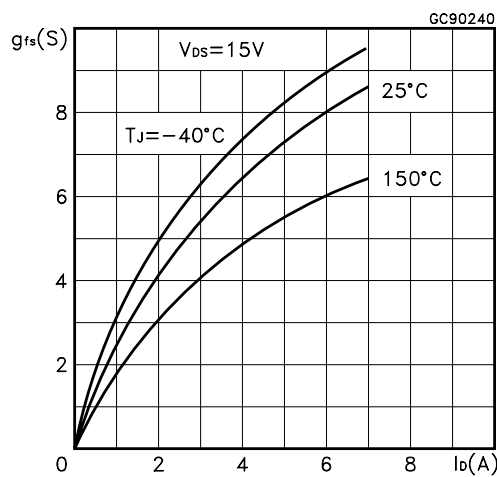
Output Characteristics



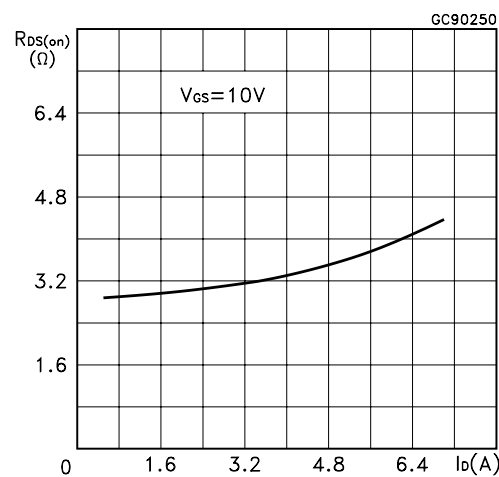
Transfer Characteristics



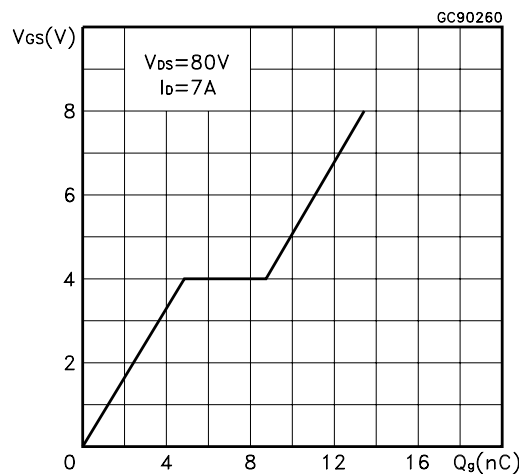
Transconductance



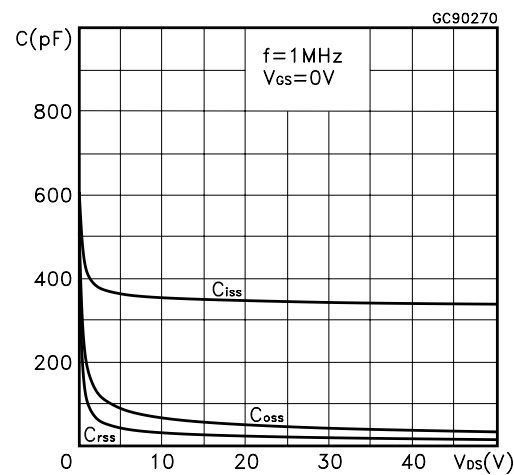
Static Drain-source On Resistance



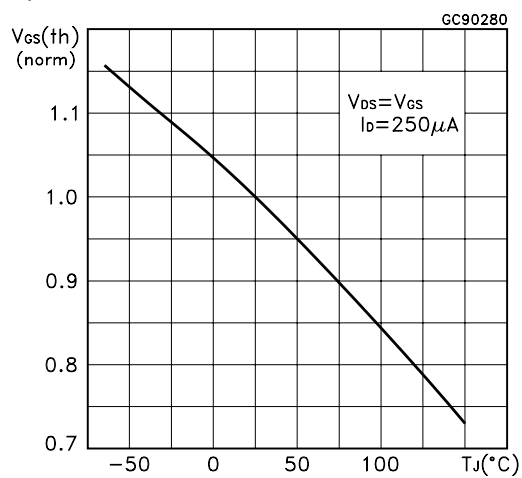
Gate Charge vs Gate-source Voltage



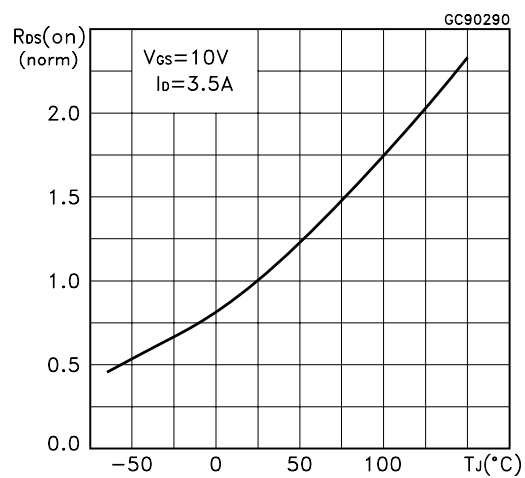
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

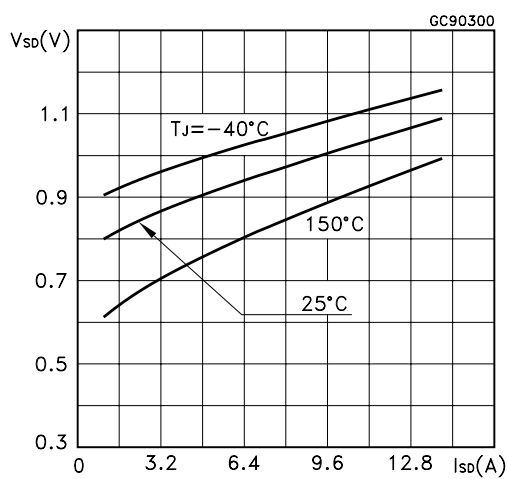


Fig. 1: Unclamped Inductive Load Test Circuit



Fig. 2: Unclamped Inductive Waveform

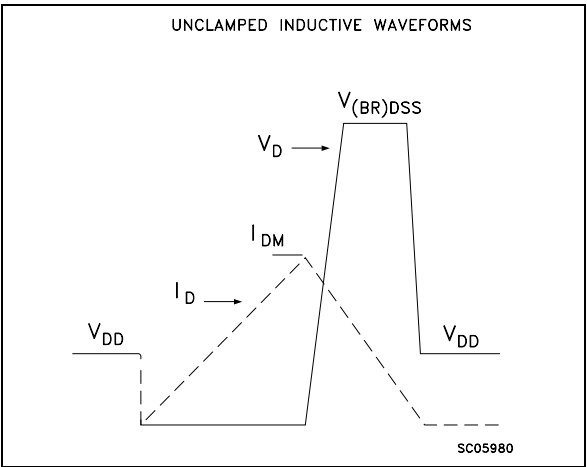


Fig. 3: Switching Times Test Circuits For Resistive Load



Fig. 4: Gate Charge test Circuit

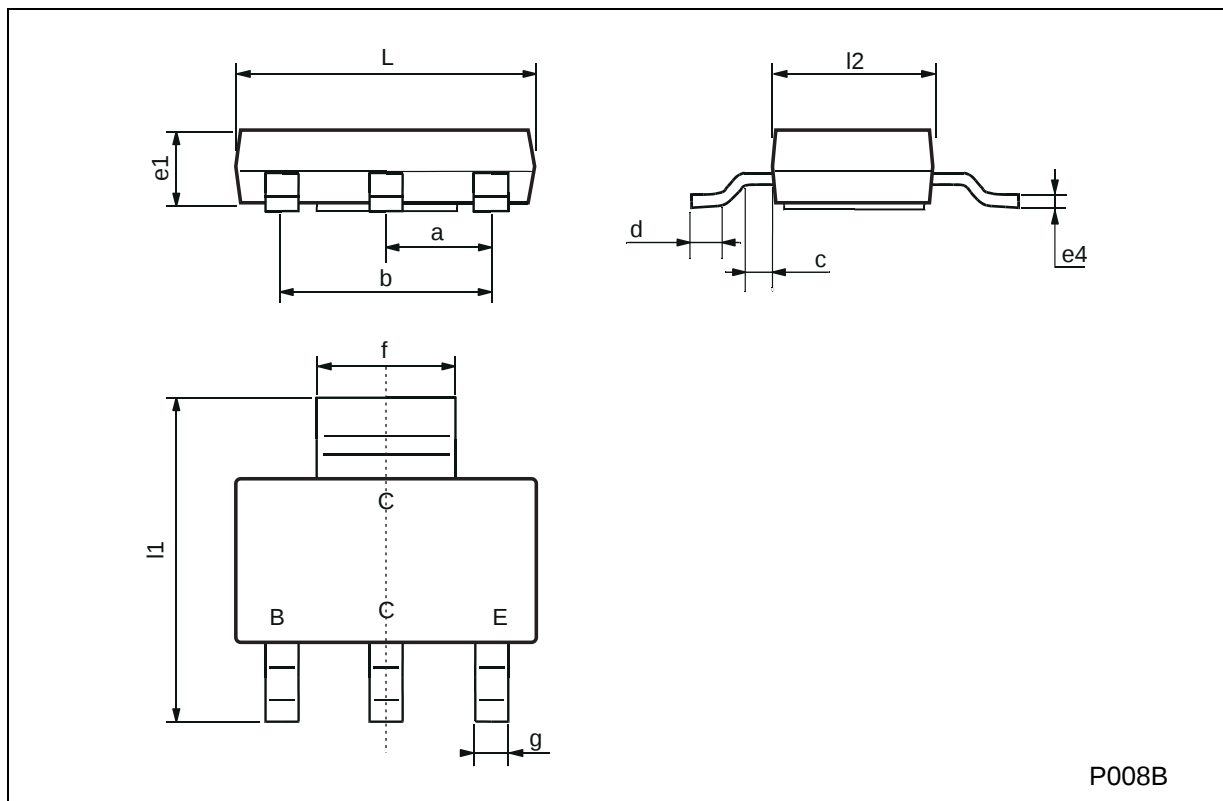


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



SOT-223 MECHANICAL DATA

DIM.	mm			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a	2.27	2.3	2.33	89.4	90.6	91.7
b	4.57	4.6	4.63	179.9	181.1	182.3
c	0.2	0.4	0.6	7.9	15.7	23.6
d	0.63	0.65	0.67	24.8	25.6	26.4
e1	1.5	1.6	1.7	59.1	63	66.9
e4			0.32			12.6
f	2.9	3	3.1	114.2	118.1	122.1
g	0.67	0.7	0.73	26.4	27.6	28.7
l1	6.7	7	7.3	263.8	275.6	287.4
l2	3.5	3.5	3.7	137.8	137.8	145.7
L	6.3	6.5	6.7	248	255.9	263.8



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