



# STL28NF3LL

## N-CHANNEL 30V - 0.0055Ω - 28A PowerFLAT™ LOW GATE CHARGE STripFET™ MOSFET

PRELIMINARY DATA

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STL28NF3LL	30 V	< 0.0065 Ω	28 A

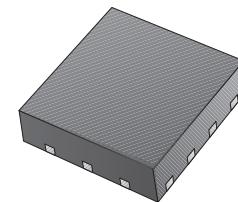
- TYPICAL R<sub>DS(on)</sub> = 0.0055Ω
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE

### DESCRIPTION

This Power MOSFET is the second generation of STMicroelectronics unique "STripFET™" technology. The resulting transistor shows extremely low on-resistance and minimal gate charge. The new PowerFLAT™ package allows a significant reduction in board space without compromising performance.

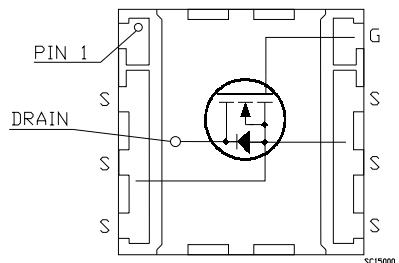
### APPLICATIONS

- DC-DC CONVERTERS



PowerFLAT™(5x5)  
(Chip Scale Package)

### INTERNAL SCHEMATIC DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	30	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	30	V
V <sub>GS</sub>	Gate- source Voltage	± 16	V
I <sub>D(#)</sub>	Drain Current (continuos) at T <sub>C</sub> = 25°C Drain Current (continuos) at T <sub>C</sub> = 100°C	28 17.5	A A
I <sub>DM(•)</sub>	Drain Current (pulsed)	112	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	80	W
	Derating Factor	0.64	W/°C
E <sub>AS</sub> (1)	Single Pulse Avalanche Energy	2	J
T <sub>stg</sub>	Storage Temperature	−55 to 150	°C
T <sub>j</sub>	Max. Operating Junction Temperature		

(●) Pulse width limited by safe operating area

(1) Starting T<sub>j</sub> = 25°C, I<sub>D</sub> = 14A, V<sub>DD</sub> = 18V

(#) Limited by Wire Bonding

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### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1.56	°C/W
Rthj-pcb (#)	Thermal Resistance Junction-ambient Max	31.2	°C/W

(\*) When mounted on 1inch<sup>2</sup> FR4 Board, 2oz of Cu, t ≤ 10 sec.

### ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 16V			±100	nA

### ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1			V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 14 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 14A		0.0055 0.0065	0.0065 0.0095	Ω Ω

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 14 A		32		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0		2780		pF
C <sub>oss</sub>	Output Capacitance			890		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			195		pF

**ELECTRICAL CHARACTERISTICS (CONTINUED)****SWITCHING ON**

<b>Symbol</b>	<b>Parameter</b>	<b>Test Conditions</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Unit</b>
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15 \text{ V}$ , $I_D = 14 \text{ A}$		25		ns
$t_r$	Rise Time	$R_G = 4.7\Omega$ $V_{GS} = 4.5 \text{ V}$ (see test circuit, Figure 3)		82		ns
$Q_g$	Total Gate Charge	$V_{DD} = 15 \text{ V}$ , $I_D = 28 \text{ A}$ ,		32		nC
$Q_{gs}$	Gate-Source Charge	$V_{GS} = 5 \text{ V}$		13		nC
$Q_{gd}$	Gate-Drain Charge			18		nC

**SWITCHING OFF**

<b>Symbol</b>	<b>Parameter</b>	<b>Test Conditions</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Unit</b>
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 15 \text{ V}$ , $I_D = 14 \text{ A}$ ,		42		ns
$t_f$	Fall Time	$R_G = 4.7\Omega$ , $V_{GS} = 4.5 \text{ V}$ (see test circuit, Figure 3)		35		ns

**SOURCE DRAIN DIODE**

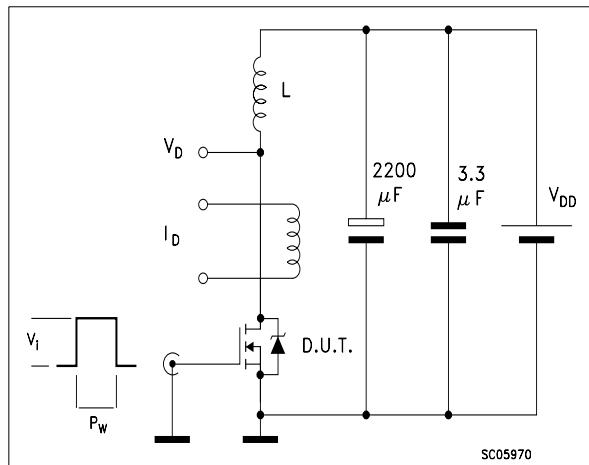
<b>Symbol</b>	<b>Parameter</b>	<b>Test Conditions</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Unit</b>
$I_{SD}$	Source-drain Current				28	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				112	A
$V_{SD}(1)$	Forward On Voltage	$I_{SD} = 28 \text{ A}$ , $V_{GS} = 0$			1.2	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 28 \text{ A}$ , $dI/dt = 100A/\mu s$ ,		50		ns
$Q_{rr}$	Reverse Recovery	$V_{DD} = 25 \text{ V}$ , $T_j = 150^\circ\text{C}$		82		nC
$I_{RRM}$	Charge Reverse Recovery Current	(see test circuit, Figure 5)		3.3		A

Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

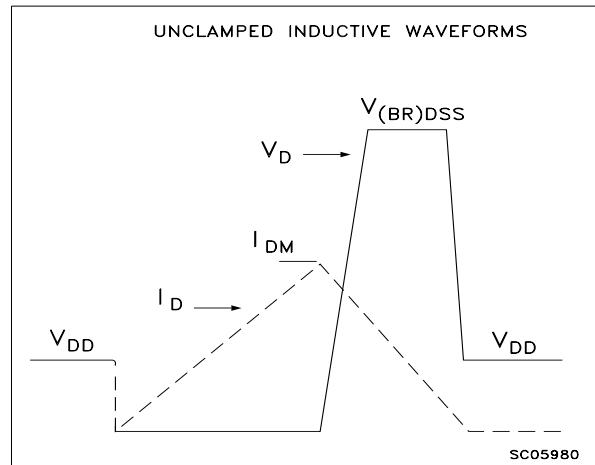
2. Pulse width limited by safe operating area.

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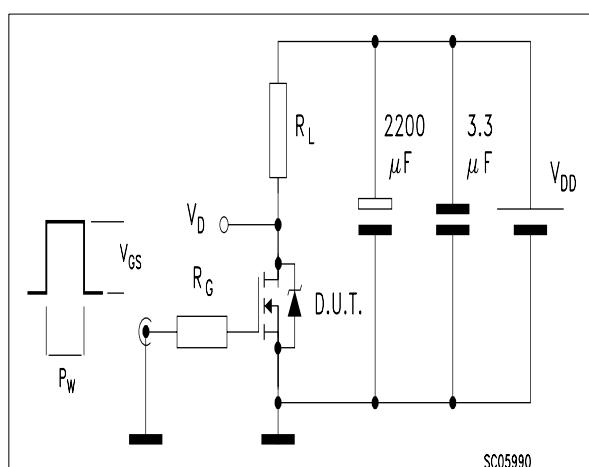
**Fig. 1:** Unclamped Inductive Load Test Circuit



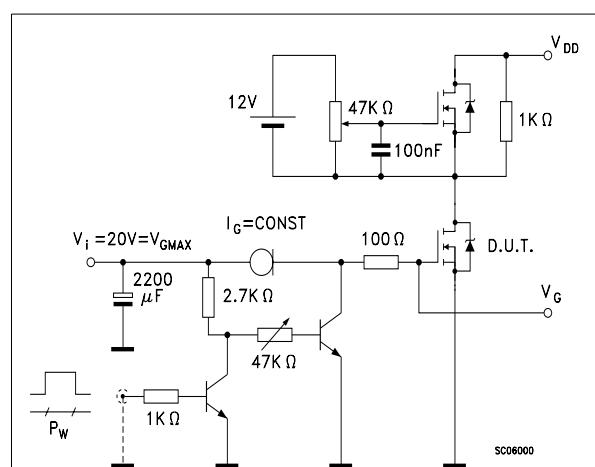
**Fig. 2:** Unclamped Inductive Waveform



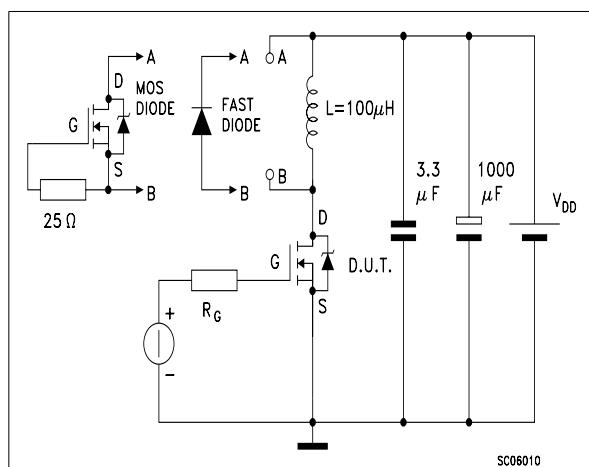
**Fig. 3:** Switching Times Test Circuit For Resistive Load



**Fig. 4:** Gate Charge test Circuit

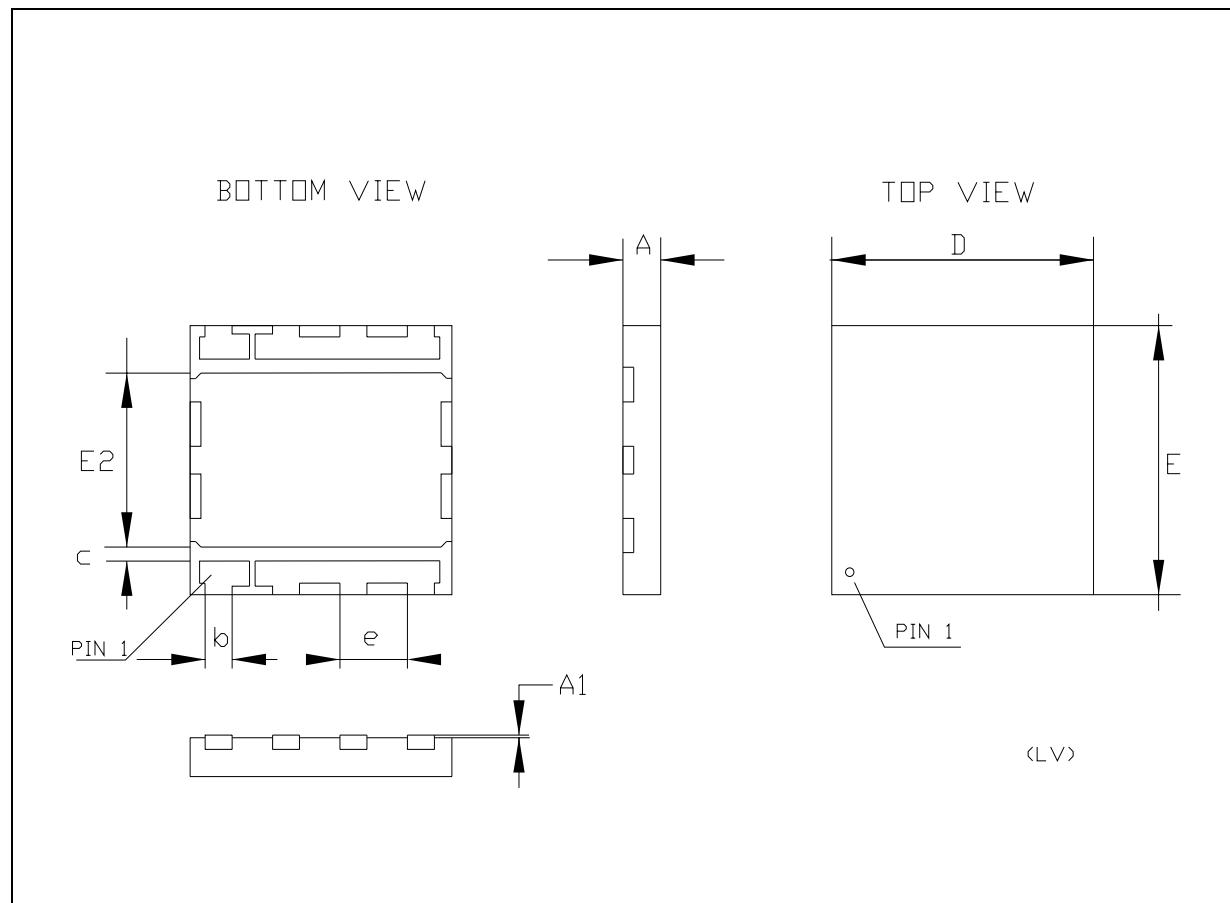


**Fig. 5:** Test Circuit For Inductive Load Switching And Diode Recovery Times



**PowerFLAT™(5x5) MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		0.90	1.00		0.035	0.039
A1		0.02	0.05		0.001	0.002
b	0.43	0.51	0.58	0.017	0.020	0.023
c	0.33	0.41	0.48	0.013	0.016	0.019
D		5.00			0.197	
E		5.00			0.197	
E2	3.10	3.18	3.25	0.122	0.125	0.128
e		1.27			0.050	



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