

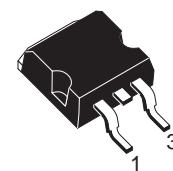


# STGB7NB40LZ

## N-CHANNEL CLAMPED 14A - D<sup>2</sup>PAK INTERNALLY CLAMPED PowerMESH™ IGBT

TYPE	V <sub>CES</sub>	V <sub>CE(sat)</sub>	I <sub>C</sub>
STGB7NB40LZ	CLAMPED	< 1.50 V	14 A

- POLYSILICON GATE VOLTAGE DRIVEN
- LOW THRESHOLD VOLTAGE
- LOW ON-VOLTAGE DROP
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- HIGH VOLTAGE CLAMPING FEATURE



D<sup>2</sup>PAK

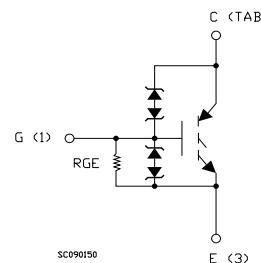
### DESCRIPTION

Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The built in collector-gate zener exhibits a very precise active clamping while the gate-emitter zener supplies an ESD protection.

### APPLICATIONS

- AUTOMOTIVE IGNITION

### INTERNAL SCHEMATIC DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CES</sub>	Collector-Emitter Voltage (V <sub>GS</sub> = 0)	CLAMPED	V
V <sub>ECR</sub>	Reverse Battery Protection	20	V
V <sub>GE</sub>	Gate-Emitter Voltage	CLAMPED	V
I <sub>C</sub>	Collector Current (continuous) at 100°C	14	A
R <sub>G</sub>	Minimum External Gate Resistor	500	Ω
P <sub>TOT</sub>	Total Dissipation at T <sub>c</sub> = 25°C	100	W
	Derating Factor	0.66	W/°C
E <sub>CL</sub>	Single Pulse Collector to Emitter Avalanche Energy I <sub>C</sub> = 13 A ; T <sub>j</sub> = 150°C (see fig.1-2)	130	mJ
E <sub>ECAV</sub>	Reverse Avalanche Energy I <sub>C</sub> = 7 A ; f = 100 Hz ; T <sub>c</sub> = 25°C	10	mJ
T <sub>stg</sub>	Storage Temperature	−55 to 175	°C
T <sub>j</sub>	Operating Junction Temperature		

## STGB7NB40LZ

### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max (free air)	62.5	°C/W

### ELECTRICAL CHARACTERISTICS ( $T_{CASE} = 25^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$\text{BV}_{(\text{CES})}$	Collector-Emitter Clamped Voltage	$I_C = 10 \text{ mA}$ , $V_{GE} = 0$ , $T_c = -40^\circ\text{C}$ to $150^\circ\text{C}$ ; $R_G = 1 \text{ k}\Omega$	370	400	430	V
$\text{BV}_{(\text{ECS})}$	Emitter Collector Break-down Voltage	$I_{EC} = 75 \text{ mA}$ , $V_{GE} = 0$ ,	20	27		V
$\text{BV}_{GE}$	Gate Emitter Break-down Voltage	$I_G = \pm 2 \text{ mA}$	12		16	V
$I_{CES}$	Collector-Emitter Leakage Current	$V_{GE} = 200 \text{ V}$ , $V_{GE} = 0$ , $R_G = 1 \text{ k}\Omega$ $T_c = 25^\circ\text{C}$ $T_c = 150^\circ\text{C}$			25 250	$\mu\text{A}$ $\mu\text{A}$
$I_{GES}$	Gate-Emitter Leakage Current ( $V_{CE} = 0$ )	$V_{GE} = \pm 10 \text{ V}$ , $V_{CE} = 0$			1000	$\mu\text{A}$

### ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GE(\text{th})}$	Gate Threshold Voltage	$V_{CE} = V_{GE}$ , $I_C = 1 \text{ mA}$ , $T_c = 25^\circ\text{C}$ $V_{CE} = V_{GE}$ , $I_C = 1 \text{ mA}$ , $T_c = 150^\circ\text{C}$	1.2 0.75		2.2 1.8	V V
$V_{CE(\text{SAT})}$	Collector-Emitter Saturation Voltage	$V_{GE} = 4.5 \text{ V}$ , $I_C = 7 \text{ A}$ , $T_j = 25^\circ\text{C}$ $V_{GE} = 5.0 \text{ V}$ , $I_C = 14 \text{ A}$ , $T_c = 25^\circ\text{C}$		1.3	1.50 1.9	V V
$R_{GE}$	Gate Emitter Resistance		10	20	30	$\text{k}\Omega$

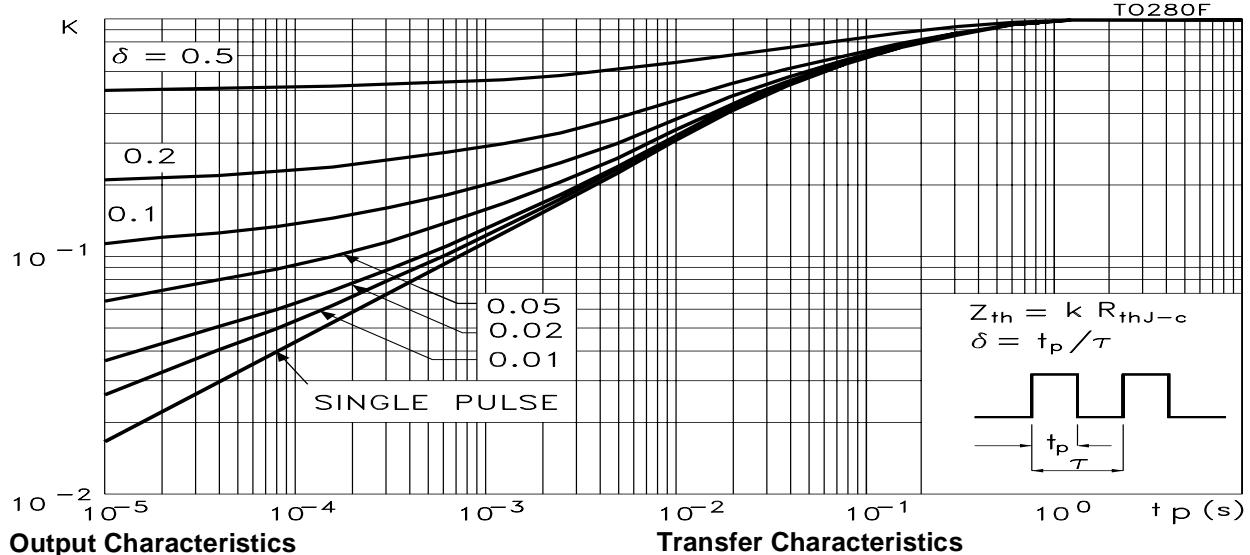
### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$C_{ies}$	Input Capacitance	$V_{CE} = 25 \text{ V}$ , $f = 1 \text{ MHz}$ , $V_{GE} = 0$		910		pF
$C_{oes}$	Output Capacitance			80		pF
$C_{res}$	Reverse Transfer Capacitance			15		pF
$Q_g$	Gate Charge	$V_{CE} = 40 \text{ V}$ , $I_C = 7 \text{ A}$ , $V_{GE} = 5 \text{ V}$		22		nC

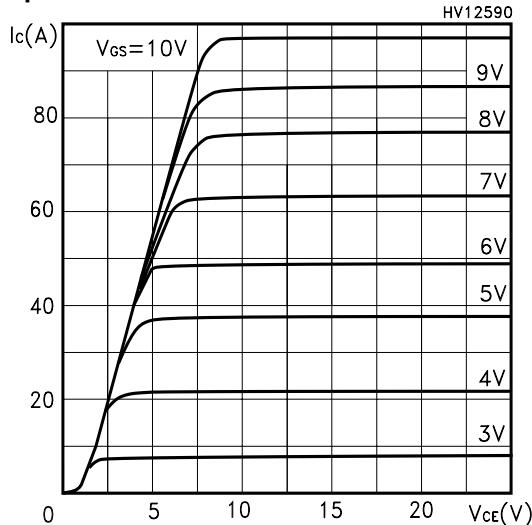
### SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Delay Time Current Rise Time	$V_{CE} = 14 \text{ V}$ , $R_G = 1 \text{ k}\Omega$ , $R_L = 1 \Omega$ , $V_{GE} = 5 \text{ V}$		0.9 4.5		$\mu\text{s}$ $\mu\text{s}$
$t_{d(off)}$ $t_f$	Delay Time Current Fall Time	$V_{CE} = 300 \text{ V}$ , $R_G = 1 \text{ k}\Omega$ , $R_L = 46 \Omega$ , $V_{GE} = 5 \text{ V}$		4.4 3.6		$\mu\text{s}$ $\mu\text{s}$

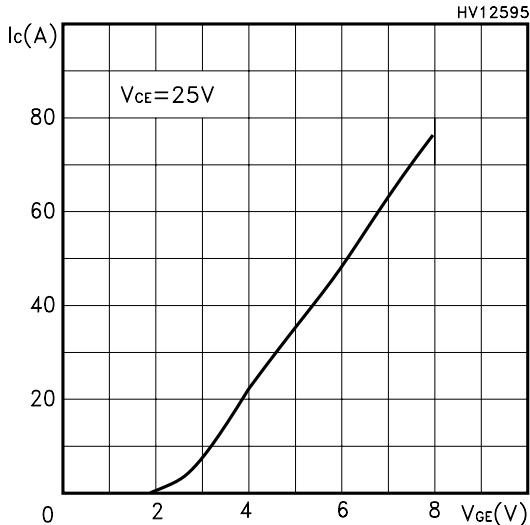
**Thermal Impedance**



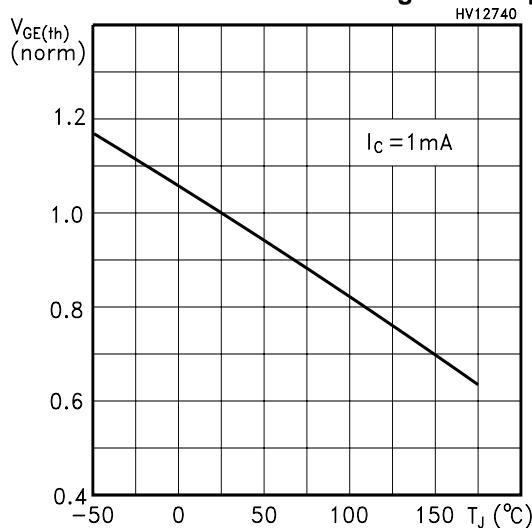
**Output Characteristics**



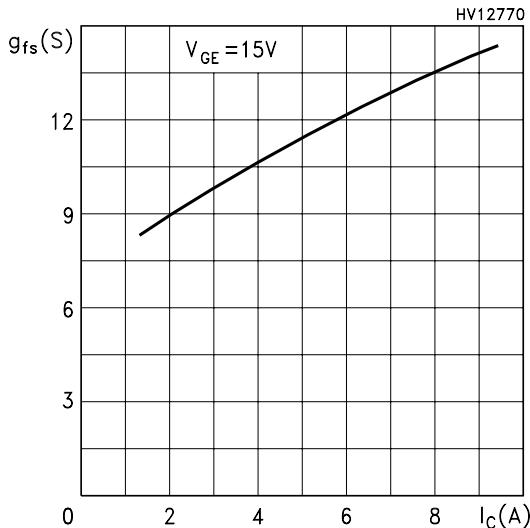
**Transfer Characteristics**



**Normalized Gate Threshold Voltage vs Temp.**

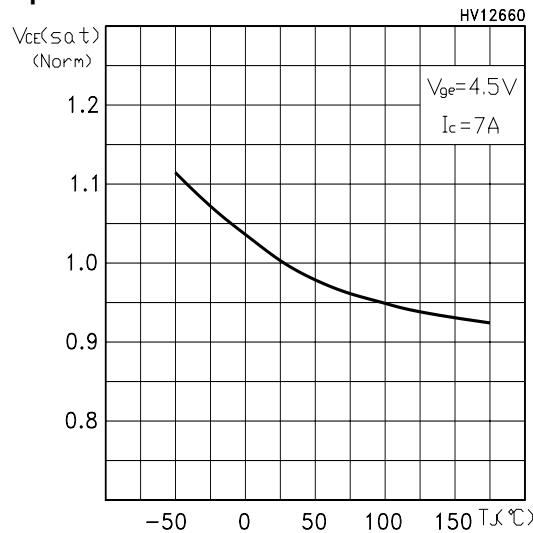


**Transconductance**

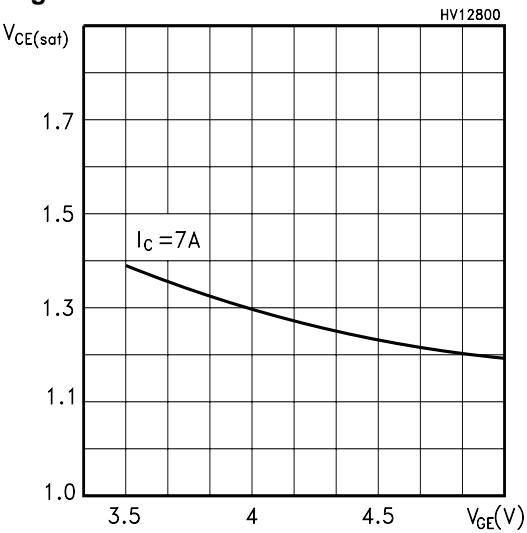


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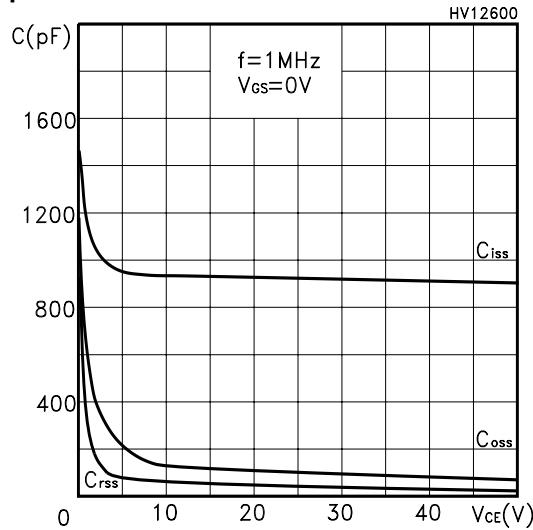
**Normalized Collector-Emitter On Voltage vs Temperature**



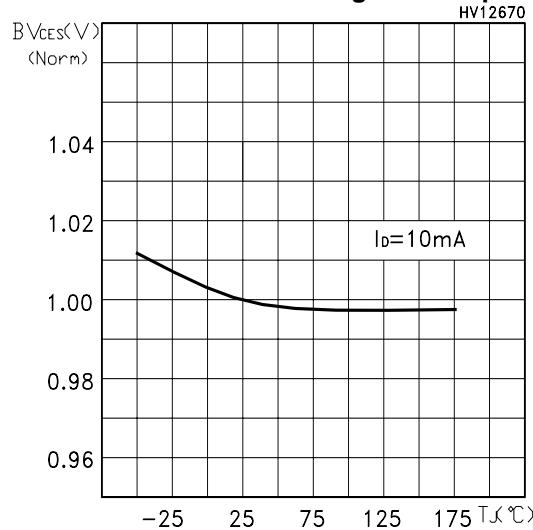
**Collector-Emitter On Voltage vs Gate-Emitter Voltage**



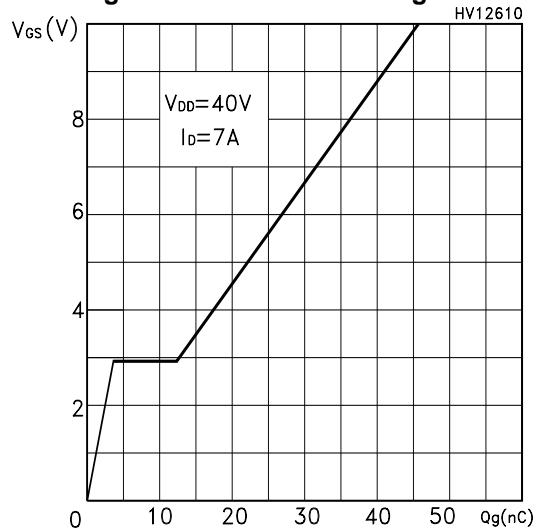
**Capacitance Variations**



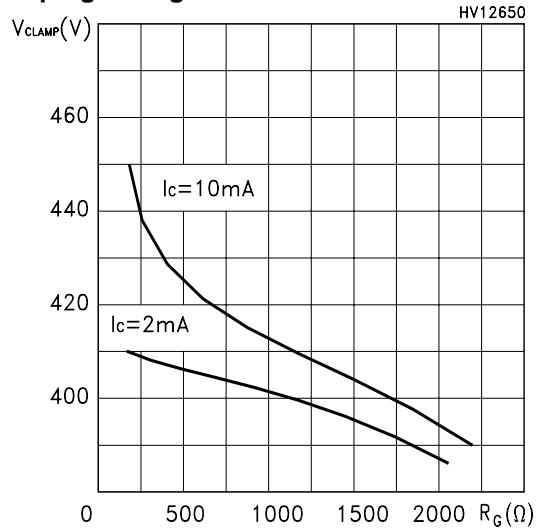
**Normalized Break-down Voltage vs Temp.**



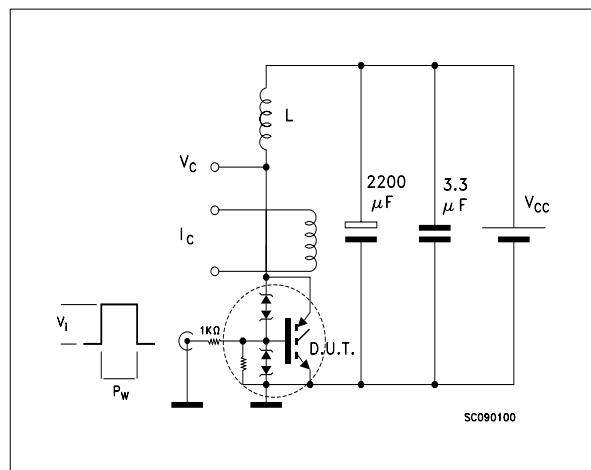
**Gate-Charge vs Gate-Emitter Voltage**



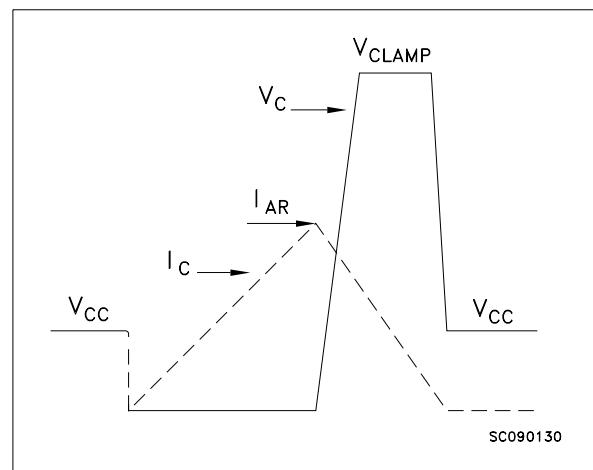
**Clamping Voltage vs Gate Resistance**



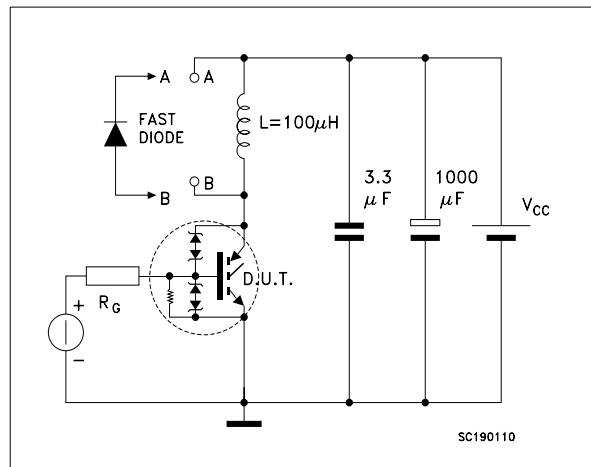
**Fig. 1:** Unclamped Inductive Load Test Circuit



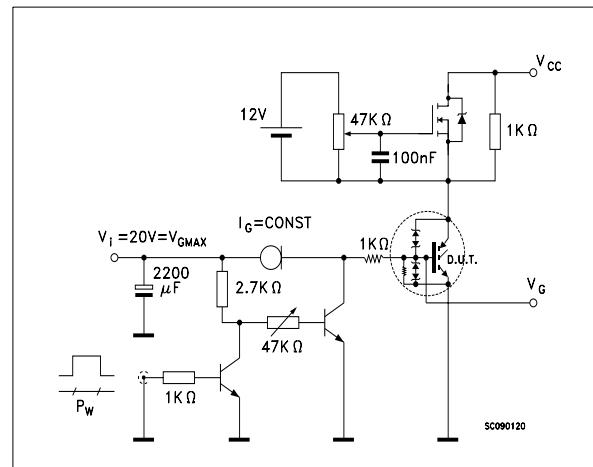
**Fig. 2:** Unclamped Inductive Waveform



**Fig. 3:** Test Circuit For Inductive Load Switching And Diode Recovery Times

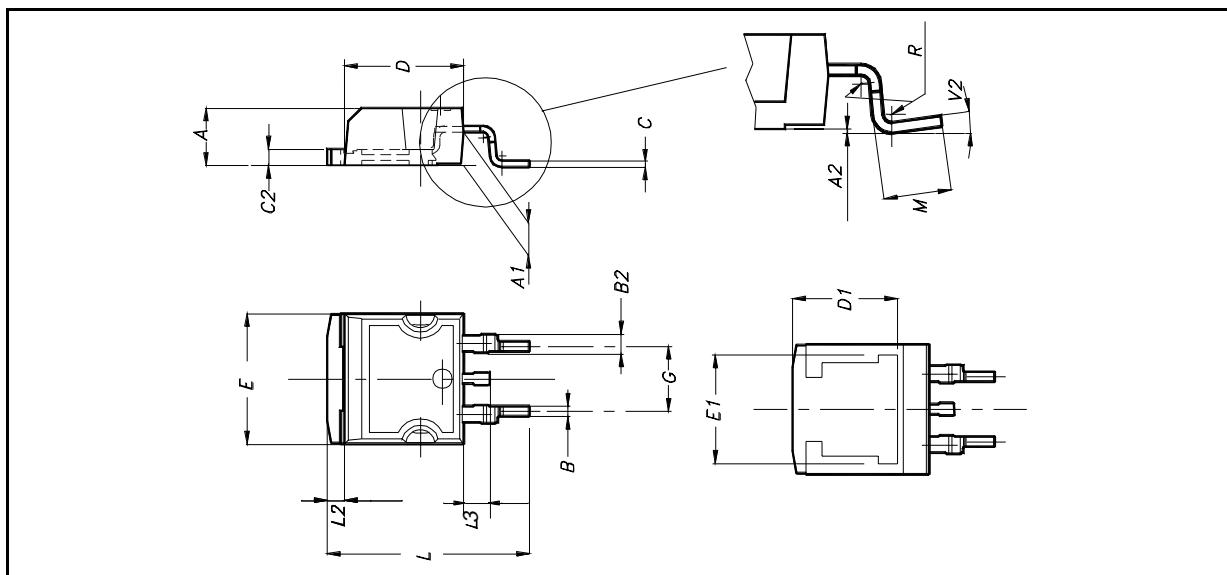


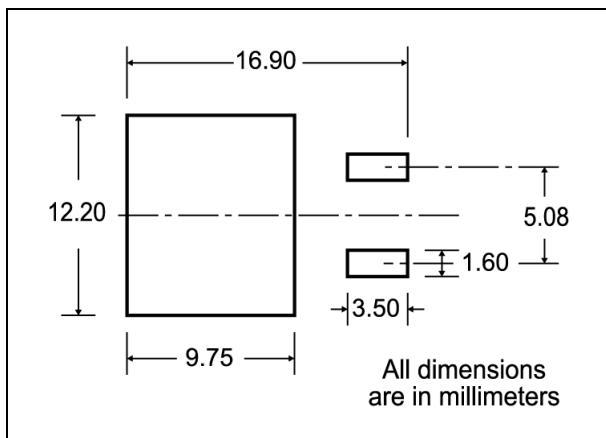
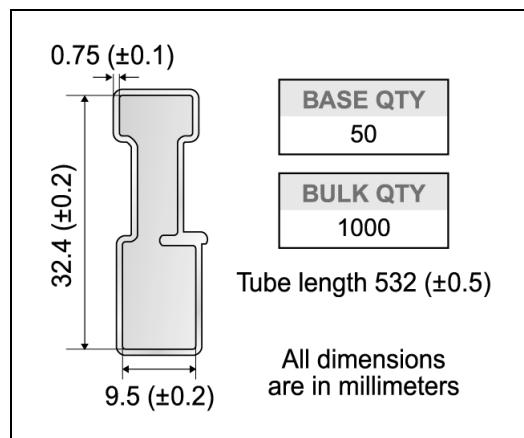
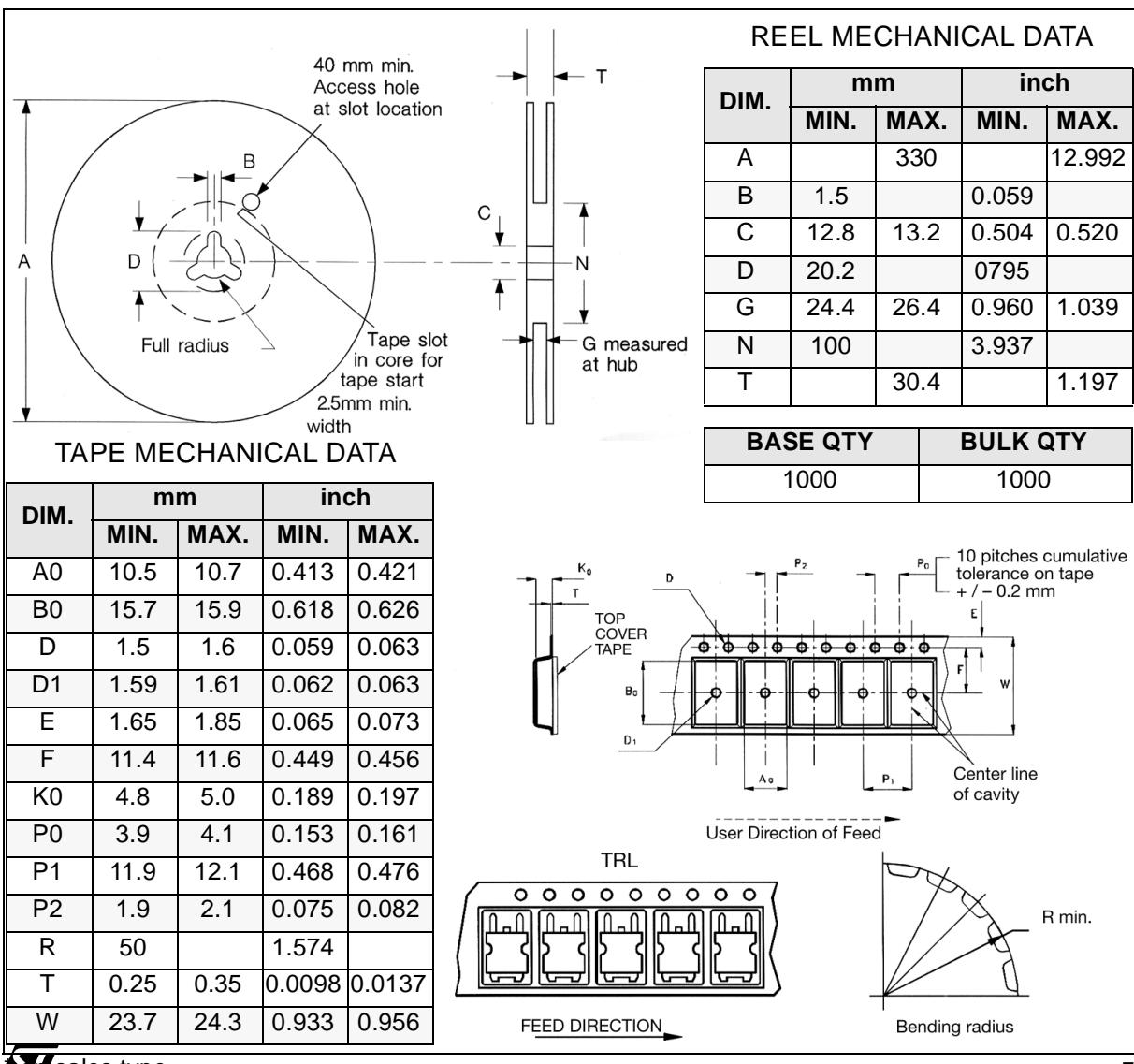
**Fig. 4:** Gate Charge test Circuit



D<sup>2</sup>PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°			



**D<sup>2</sup>PAK FOOTPRINT****TUBE SHIPMENT (no suffix)\*****TAPE AND REEL SHIPMENT (suffix "T4")\***

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