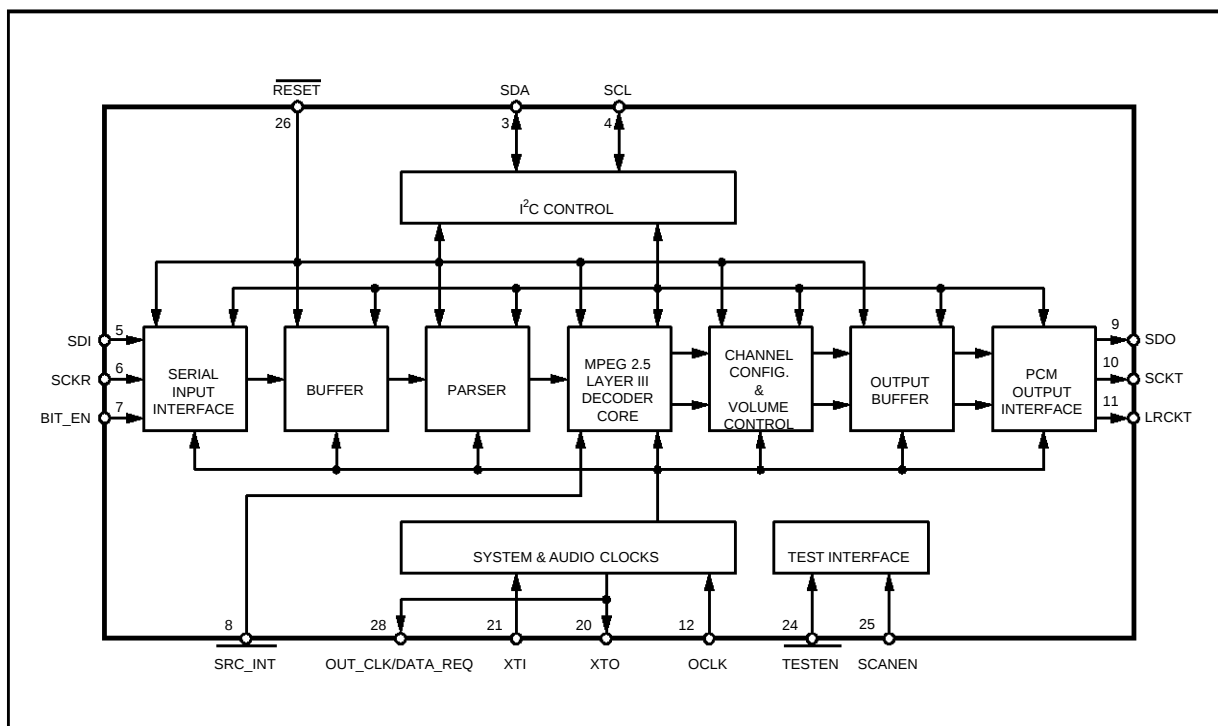


IC INFORMATION

Function	Mpeg 2.5 Layer 3 Audio Decoder	STA013		1/2	E
Type	C MOS	Model	XR-VS400		

● Block Diagram



IC INFORMATION

STA013

2/2

E

Function Mpeg 2.5 Layer 3 Audio Decoder

Type C MOS

Model XR-VS400

●Pin Function

SO28	TQFP44	LFBGA64	Pin Name	Type	Function	PAD Description
1	29	B5	VDD_1		Supply Voltage	
2	30	B4	VSS_1		Ground	
3	31	A4	SDA	I/O	I ² C Serial Data + Acknowledge	CMOS Input Pad Buffer CMOS 4mA Output Drive
4	32	B3	SCL	I	I ² C Serial Clock	CMOS Input Pad Buffer
5	34	A1	SDI	I	Receiver Serial Data	CMOS Input Pad Buffer
6	36	B2	SCKR	I	Receiver Serial Clock	CMOS Input Pad Buffer
7	38	D4	BIT_EN	I	Bit Enable	CMOS Input Pad Buffer with pull up
8	40	D1	$\overline{\text{SRC_INT}}$	I	Interrupt Line For S.R. Control	CMOS Input Pad Buffer
9	42	E2	SDO	O	Transmitter Serial Data (PCM Data)	CMOS 4mA Output Drive
10	44	F2	SCKT	O	Transmitter Serial Clock	CMOS 4mA Output Drive
11	2	H1	LRCKT	O	Transmitter Left/Right Clock	CMOS 4mA Output Drive
12	3	H3	OCLK	I/O	Oversampling Clock for DAC	CMOS Input Pad Buffer CMOS 4mA Output Drive
13	5	F3	VSS_2		Ground	
14	6	E4	VDD_2		Supply Voltage	
15	7	G4	VSS_3		Ground	
16	8	G5	VDD_3		Supply Voltage	
17	10	F5	PVDD		PLL Power	
18	11	G6	PVSS		PLL Ground	
19	12	G7	FILT	O	PLL Filter Ext. Capacitor Conn.	
20	13	G8	XTO	O	Crystal Output	CMOS 4mA Output Drive
21	15	F7	XTI	I	Crystal Input (Clock Input)	Specific Level Input Pad (see paragraph 2.1)
22	19	E7	VSS_4		Ground	
23	21	C8	VDD_4		Supply Voltage	
24	22	D7	$\overline{\text{TESTEN}}$	I	Test Enable	CMOS Input Pad Buffer with pull up
25	24	A7	SCANEN	I	Scan Enable	CMOS Input Pad Buffer
26	25	B6	$\overline{\text{RESET}}$	I	System Reset	CMOS Input Pad Buffer with pull up
27	26	A5	VSS_5		Ground	
28	27	C5	OUT_CLK/ DATA_REQ	O	Buffered Output Clock/ Data Request Signal	CMOS 4mA Output Drive

Note: SRC_INT signal is used by STA013 internal software in Broadcast Mode only; in Multimedia mode SRC_INT must be connected to V_{DD}. In functional mode TESTEN must be connected to VDD, SCANEN to ground.