

## FEATURES

- Complete DTMF Receiver
- Low Power Consumption
- Internal Gain Setting Amplifier
- Adjustable Guard Time
- Central Office Quality
- Power-Down Mode
- Inhibit Mode
- Pin-To-Pin and Functional Compatible with Mitel MT8870

## GENERAL DESCRIPTION

The ST88C870 (U.S. only) and ST88C870E (European only) are complete DTMF receivers integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high and

low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three state bus interface.

## ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
ST88C870CP18	18 Lead 300 Mil PDIP	0° C to + 70°C
ST88C870CF18	18 Lead 300 Mil JEDEC SOIC	0° C to + 70°C

## BLOCK DIAGRAM

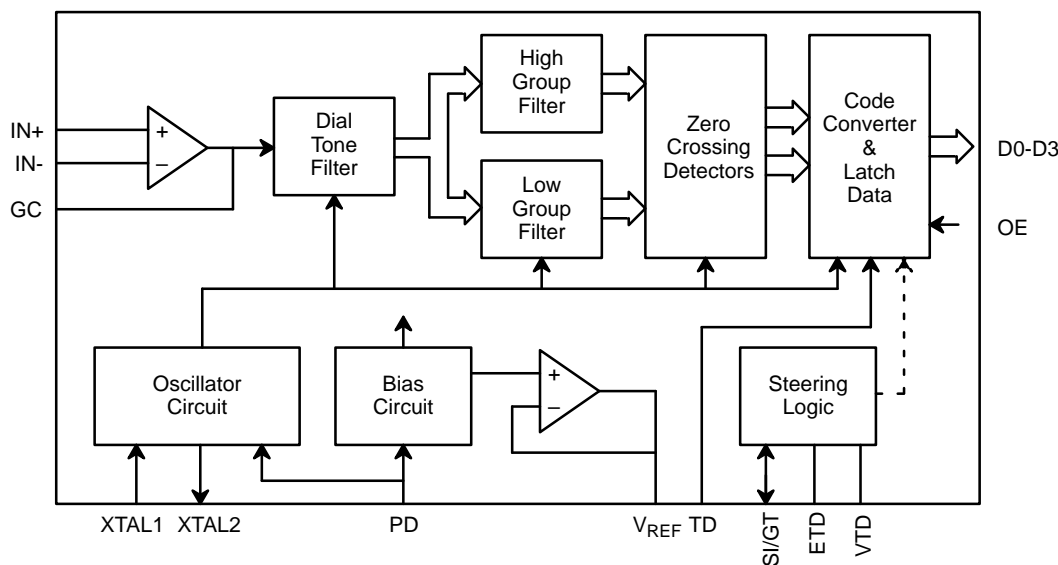
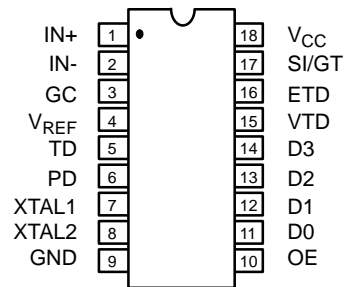
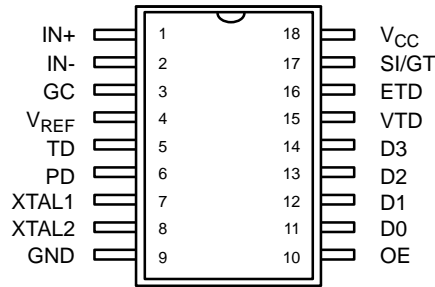


Figure 1. Block Diagram

## PIN CONFIGURATION



18 Lead PDIP (0.300")



18 Lead SOIC (Jedec, 0.300")

## PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	IN+	I	Non-Inverting Op-Amp input.
2	IN-	I	Inverting Op-Amp input.
3	GC	I	Gain adjustment. Op-Amp output of front end differential amplifier for connection of feedback resistor.
4	V <sub>REF</sub>	O	Reference Voltage Output, Nominally set to half supply voltage, is used to bias inputs at mid-rail
5**	TD	I	Tone disable. Logic high inhibits the detection of tones representing characters A, B, C and D.
6**	PD	I	Power Down (active high). Powers down the device and inhibits the oscillator.
7	XTAL1	I	Crystal oscillator, or External clock input pin. A 3.579545 MHz crystal connected between XTAL1 and XTAL2 completes the internal oscillator circuit.
8	XTAL2	O	Crystal oscillator output pin.
9	GND	—	Supply ground pin.
10*	OE	I	Output Enable (active high). To enable / disable the D0-D3 outputs.
11-14	D0-D3	O	Data outputs. When enabled by OE, provide the code corresponding to the last valid tone pair received. When OE is low, the data outputs are three stated.
15	VTD	O	Valid Tone detection signal. Presents a logic high when a received tone pair has been registered and the output latch updated, returns to Logic low when the voltage on SI/GT falls below V <sub>tst</sub> .
16	ETD	O	Early Tone detection. Presents a logic high once the digital algorithm has detected a valid tone pair. Any momentary loss of signal condition will cause ETD to return to a logic low.
17	SI/GT	I/O	Steering Input / Guard time (Output) Bidirectional. A voltage greater than V <sub>tst</sub> detected at SI causes the device to register the detected tone pair and up date the output latch. A voltage less than V <sub>tst</sub> frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant; its state is a function of ETD and the voltage on SI.
18	V <sub>CC</sub>	—	Most positive power supply. Typically 5 Volts.

\* = Internal pull-up resistor

\*\* = Internal pull-down resistor

## DC ELECTRICAL CHARACTERISTICS

Test Conditions:  $T_A = 0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$  Unless Otherwise Specified

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$V_{ILCK}$	Clock input low level	-0.5		0.6	V	
$V_{IHCK}$	Clock input high level	3.0		$V_{CC}$	V	
$V_{IL}$	Input low level	-0.5		0.8	V	
$V_{IH}$	Input high level	2.2		$V_{CC}$	V	
$V_{OL}$	Output low level on all outputs			0.4	V	$I_{OL} = 6\text{ mA}$
$V_{OH}$	Output high level	2.4			V	$I_{OH} = -6\text{ mA}$
$I_{CC}$	Avg. power supply current		5	10	mA	
$I_{STD}$	Standby current		10	25	$\mu\text{A}$	
$I_{CL}$	Clock leakage			+10	$\mu\text{A}$	
$I_{IL}$	Input leakage current		0.1		$\mu\text{A}$	
$I_{UP}$	Input pull-up current		10	20	$\mu\text{A}$	
$I_{DN}$	Input pull-down current		15	40	$\mu\text{A}$	
$R_{IN}$	Input impedance		10		$\text{M}\Omega$	
$V_{VT}$	Threshold voltage	2.2	2.4	2.5	V	
$V_{REF}$	$V_{REF}$ output voltage	2.3	2.5	2.7	V	
$R_{REF}$	$V_{REF}$ output resistance		1		$\text{k}\Omega$	

## AC ELECTRICAL CHARACTERISTICS

Test Conditions:  $T_A = 0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$  Unless Otherwise Specified

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$F_C$	Input clock frequency		3.5795		MHz	
	Input clock duty cycle	40	50	60	%	
$T_3$	Clock rise/fall time			110	ns	
$T_6$	Propagation delay SI to D0-D3		8	16	$\mu\text{s}$	
$T_7$	Propagation delay D0-D3 to STD		8	16	$\mu\text{s}$	
$T_8$	Power down time		20		ms	
$T_9$	Power up time		30		ms	
$T_{10}$	Propagation delay SI to STD		12	16	$\mu\text{s}$	
$T_{12}$	Tone present detect time	5	11	14	ms	
$T_{13}$	Tone absent detect time	0.5	4	8.5	ms	
$T_{14}$	Tone duration accept			40	ms	
$T_{15}$	Tone duration reject	20			ms	
$T_{16}$	Interdigit pause accept			40	ms	
$T_{17}$	Interdigit pause reject	20			ms	
$T_{19}$	Propagation delay		8	16	$\mu\text{s}$	

## AC ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions:  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$  Unless Otherwise Specified

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$T_{21}$	Output data setup time		3.4		$\mu\text{s}$	
$T_{22}$	Propagation delay OE to D0-D3 disable		300		ns	
$T_{23}$	Propagation delay OE to D0-D3 enable		50		ns	

## RECEIVER INPUT SENSITIVITY

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
	Valid input signal levels (each tone of composite signal) (ST88C870)	-29		+1	dBm	Into 600 $\Omega$ load
		27.5		869	mV <sub>RMS</sub>	
	Valid input signal levels (each tone of composite signal) (ST88C870E)	-31		+1	dBm	Into 900 $\Omega$ load
		21.8		869	mV <sub>RMS</sub>	

### \*NOTES

1. dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration=40 ms, tone pause=40ms.
6. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by  $\pm 1.5\% \pm 2$  Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 400 Hz)  $\pm 2\%$ .
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Guaranteed by design and characterization.

## ABSOLUTE MAXIMUM RATINGS

Supply Range ..... 7 Volts  
Voltage at any pin ..... GND-0.3V to  $V_{CC} + 0.3\text{V}$

Operating Temperature .....  $0^\circ\text{C}$  to  $+70^\circ\text{C}$   
Storage Temperature .....  $-40^\circ\text{C}$  to  $+150^\circ\text{C}$   
Package Dissipation ..... 500 mW

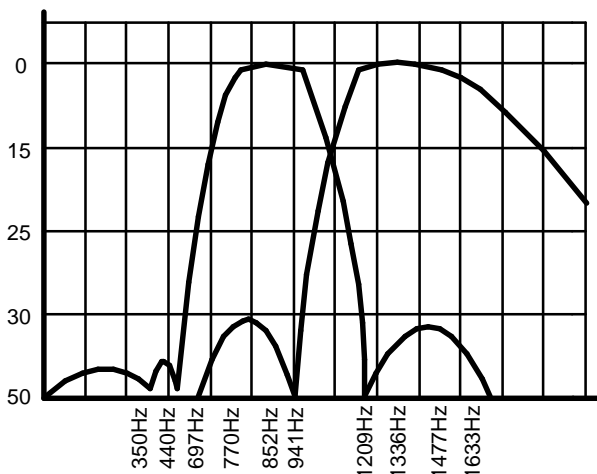
## FILTER SECTION

Separation of the low group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection. Each filter output is followed by a single order RC smoothing filter section which smoothes the signals prior to limiting. Limiting is performed by high gain compactors which are provided with hysteresis to prevent detection of unwanted low level signals. The outputs of the compactors provide full rail logic swings at the frequencies of the incoming DTMF signals. See Figure 2. for the Filter Frequency Response.

## DECODER SECTION

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies and noise.

When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the ETD output will go to an active state. Any subsequent loss of signal condition will cause ETD to assume an inactive state.



**Figure 2. Filter Frequency Response**

## FUNCTIONAL DECODING TABLE:

Key	Oe	Ce	Etd	D3	D2	D1	D0	Fl	Fh
Any	L	X	H	Z	Z	Z	Z		
1	H	X	H	0	0	0	1	697	1209
2	H	X	H	0	0	1	0	697	1336
3	H	X	H	0	0	1	1	697	1477
4	H	X	H	0	1	0	0	770	1209
5	H	X	H	0	1	0	1	770	1336
6	H	X	H	0	1	1	0	770	1477
7	H	X	H	0	1	1	1	852	1209
8	H	X	H	1	0	0	0	852	1336
9	H	X	H	1	0	0	1	852	1477
0	H	X	H	1	0	1	0	941	1209
*	H	X	H	1	0	1	1	941	1336
#	H	X	H	1	1	0	0	941	1477
A	H	L	H	1	1	0	1	697	1633
B	H	L	H	1	1	1	0	770	1633
C	H	L	H	1	1	1	1	852	1633
D	H	L	H	0	0	0	0	941	1633
A	H	H	L	The output code will remain the same as the previous detected code					
B	H	H	L						
C	H	H	L						
D	H	H	L						

## STEERING CIRCUIT

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ETD. A logic high on ETD causes  $V_{CX}$  (Figure 3. and Figure 4.) to rise as the capacitor discharges. Provided signal condition is maintained (ETD remains high) for the validation period (T12)  $V_{CX}$  reaches the threshold (ETD) of the steering logic to register the tone pair, latching its corresponding 4-bit code into the output latch. At this point the GT output is activated and drives  $V_{CX}$  to  $V_{CC}$ . GT continues to drive high as long as ETD remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag STD goes high, signaling that a received tone pair has been registered.

The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (OE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

## GUARD TIME ADJUSTMENTS

In many situations not requiring selection of tone duration and interdigit pause, the simple steering circuit shown in is applicable.

Component values are chosen according to the formula:

$$T_{14} = T_{12} + T_4$$

$$T_{16} = T_{13} + T_5$$

$$T_4 = (R_p C_x) \ln [V_{CC} / (V_{CC} - V_{cx})]$$

$$T_5 = (R_1 C_x) \ln (V_{CC} / V_{cx})$$

$$R_p = (R_1 R_2) / (R_1 + R_2)$$

- Decreasing  $T_4$  ( $T_4 < T_5$ ) Fig. 2
- Decreasing  $T_5$  ( $T_4 > T_5$ ) Fig. 1

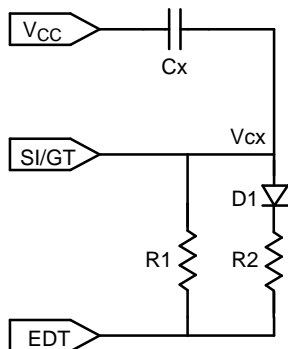


Figure 3. RC Timing

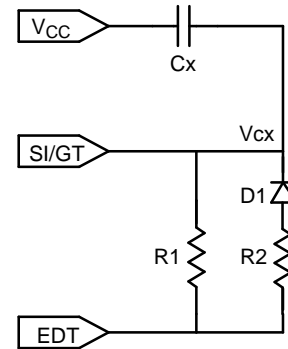


Figure 4. RC Timing

The value of  $T_{12}$  is a device parameter and  $T_{14}$  is the minimum signal duration to be recognized by the receiver (see timing diagram). A value for  $C$  of 0.1F is recommended for most applications, leaving  $R$  to be selected by the designer.

Different steering arrangements may be used to select independently the guard times for tone present ( $T_4$ ) and tone absent ( $T_5$ ). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing  $T_{14}$  improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, relatively short  $T_{14}$  with a long  $T_{17}$  would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required.

## POWER DOWN MODE

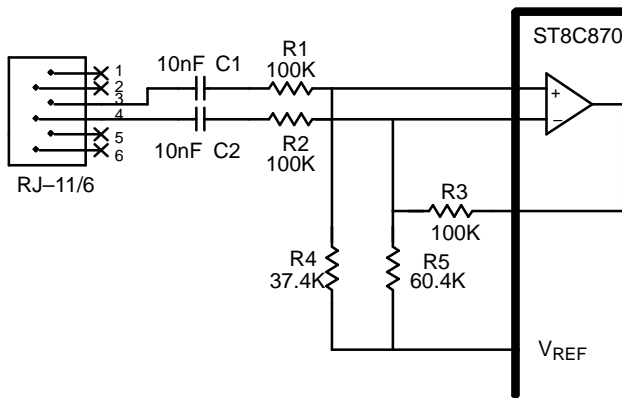
A logic high applied to PD will power down the device to minimize the power consumption in a standby mode. It stops the oscillator and the functions of the filters.

Inhibit mode is enabled by a logic high input to the TD. It inhibits the detection of tones representing characters A, B, C, and D. The output code will remain the same as the previous detected code.

## DIFFERENTIAL INPUT CONFIGURATION

The input arrangement of the ST88C870 provides a differential input operational amplifier as well as a bias source ( $V_{REF}$ ) which is used to bias the inputs at mid rail. Provision is made for connection of a feedback resistor to the op-amp output (GC) for adjustment of gain. In a single ended configuration, the input pins are connected as shown in *Figure 7*. with the op-amp connected for unity gain and  $V_{REF}$  biasing the input at  $V_{CC}/2$ .

*Figure 5*. shows the differential configuration, which permits the adjustment of gain with the feedback resistor R3.



**Figure 5. Typical Input Circuitry**

$$R4 = (R3R5) / (R3 + R5)$$

$$\text{Voltage gain} = R3 / R2$$

$$2 \cdot \sqrt{R^2 + \left(\frac{1}{\omega}\right)^2}$$

## CRYSTAL OSCILLATOR CIRCUIT

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal and is normally connected as shown in *Figure 6*. (Single-Ended Input Configuration). However it is possible to configure several ST88C870 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30pF capacitor to the oscillator input (XTAL1) of the next device shown in *Figure 8*. Subsequent devices are connected in a similar fashion. The problems associated with unbalanced loading are not a concern with the arrangement shown, i.e., precision balancing capacitors are not required.

## CRYSTAL OSCILLATOR SPECIFICATIONS

$$F = \frac{1}{2 \pi \sqrt{C_1 L_1}}$$

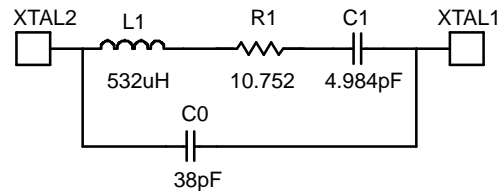
$$L1 = 0.532 \text{ mH}$$

$$C1 = 4.984 \text{ pF}$$

$$R1 = 10.752 \Omega$$

$$C0 = 38 \text{ pF}$$

$$Q = 896$$



**Figure 6. Crystal Equivalent Schematic**





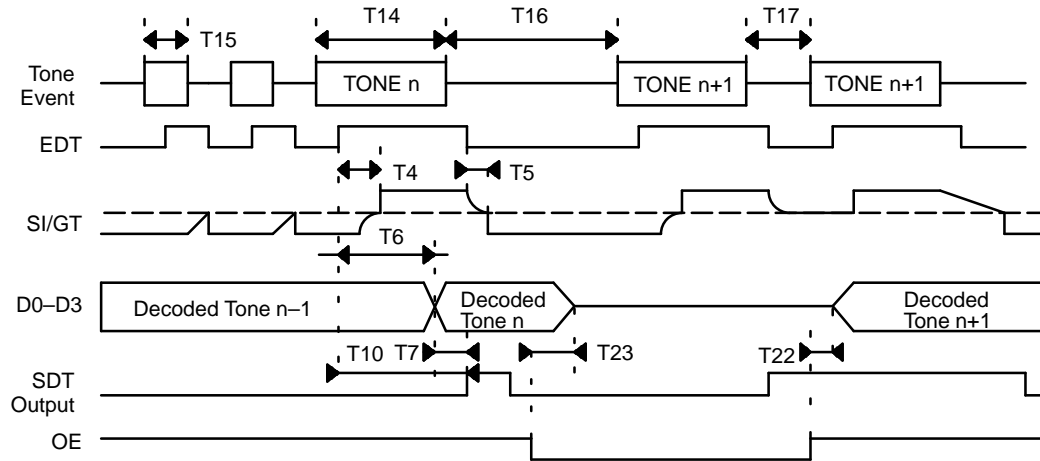
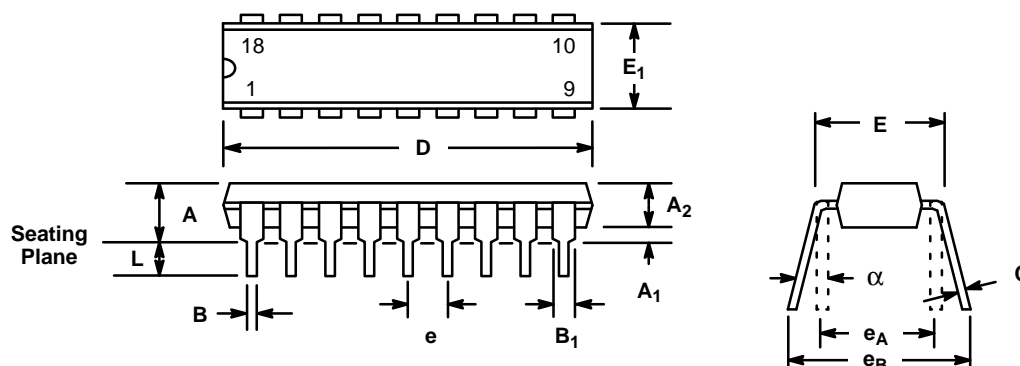


Figure 9. Timing Diagram

## 18 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

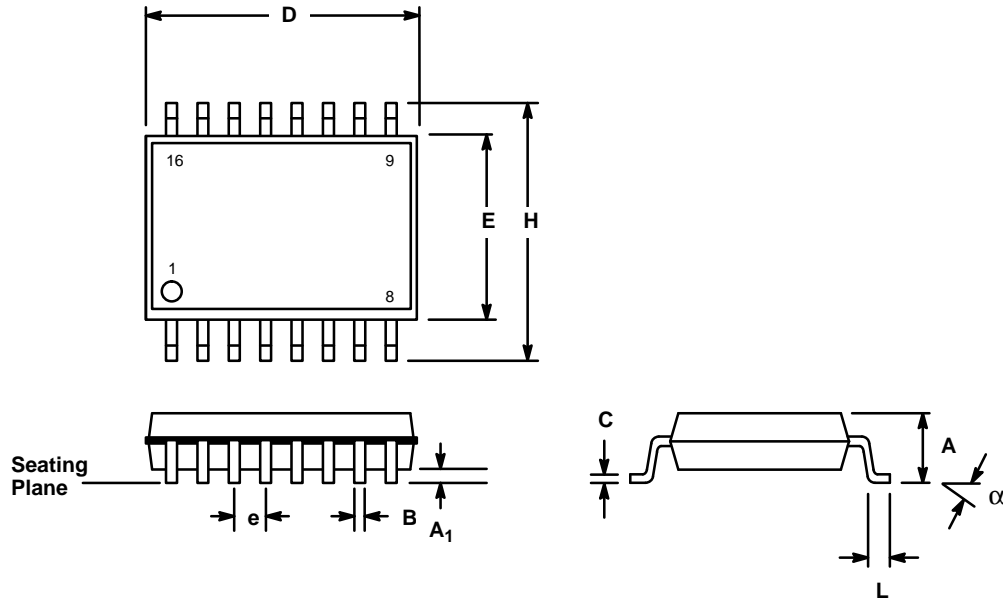


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A <sub>1</sub>	0.015	0.070	0.38	1.78
A <sub>2</sub>	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B <sub>1</sub>	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.845	0.925	21.46	23.50
E	0.300	0.325	7.62	8.26
E <sub>1</sub>	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e <sub>A</sub>	0.300 BSC		7.62 BSC	
e <sub>B</sub>	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

**16 LEAD SMALL OUTLINE  
(300 MIL JEDEC SOIC)**

*Rev. 1.00*



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A <sub>1</sub>	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.398	0.413	10.10	10.50
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

*Note: The control dimension is the millimeter column*

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