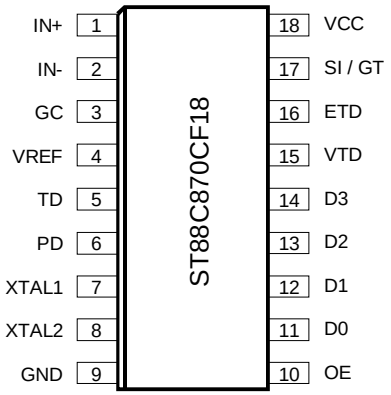
INTEGRATED DTMF RECEIVER

DESCRIPTION

The ST88C870 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three state bus interface.

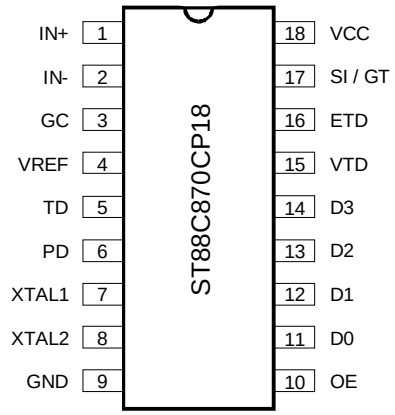
SOIC Package



FEATURES

- complete DTMF Receiver
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power-down mode
- Inhibit mode
- Pin-To-Pin and functional compatible with Mitel MT8870

Plastic Dip Package



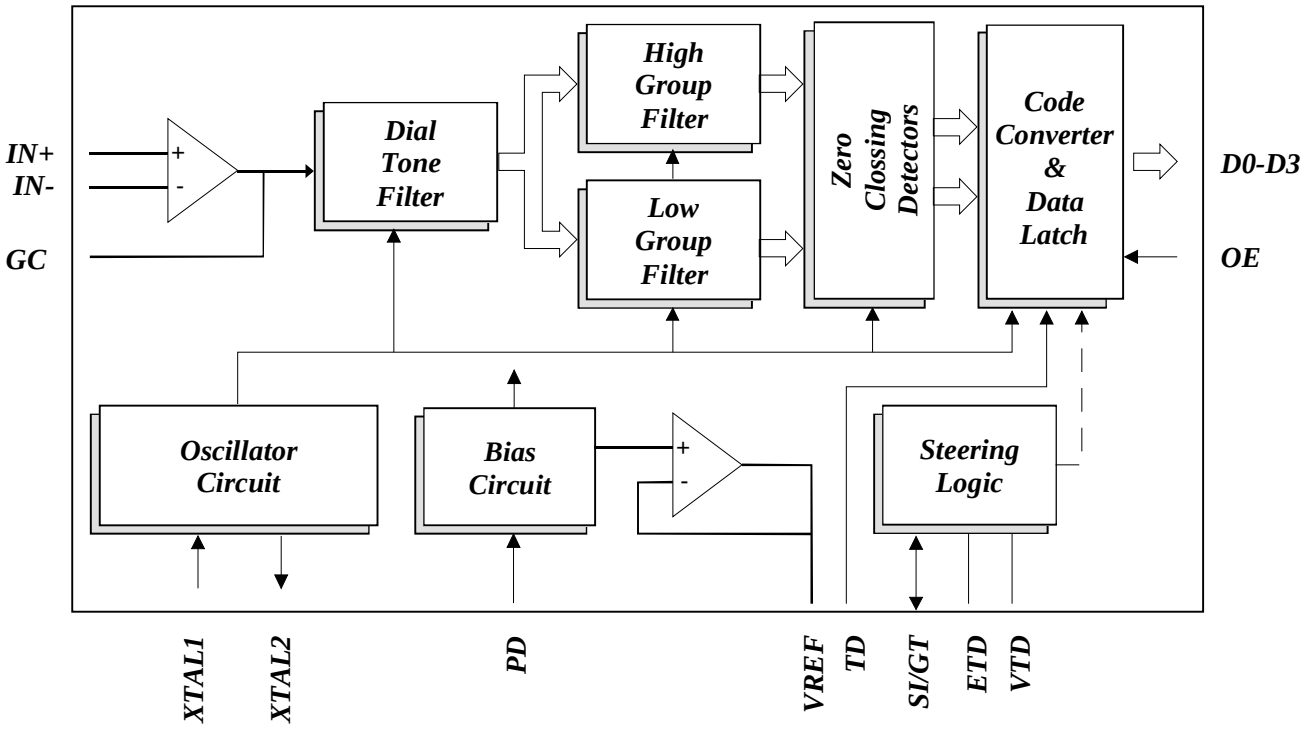
ORDERING INFORMATION

Part number	Package	Operating temperature
ST88C870CP18	Plastic-DIP	0° C to + 70° C
ST88C870CF18	SOIC	0° C to + 70° C

***Industrial operating range are available.**

ST88C870

BLOCK DIAGRAM



ST88C870

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
IN+	1	I	Non-Inverting Op-Amp input.
IN-	2	I	Inverting Op-Amp input.
GC	3	I	Gain adjustment. Op-Amp output of front end differential amplifier for connection of feedback resistor.
Vref	4	O	Reference Voltage Output, Nominally set to half supply voltage, is used to bias inputs at mid-rail
TD	5**	I	Tone disable. Logic high inhibits the detection of tones representing characters A, B, C and D.
PD	6**	I	Power Down (active high). Powers down the device and inhibits the oscillator.
XTAL1	7	I	Crystal oscillator, or External clock input pin. A 3.579545 MHz crystal connected between XTAL1 and XTAL2 completes the internal oscillator circuit.
XTAL2	8	O	Crystal oscillator output pin.
GND	9	O	Supply ground pin.
OE	10*	I	Output Enable (active high). To enable / disable the D0-D3 outputs.
D0-D3	11-14	O	Data outputs. When enabled by OE, provide the code corresponding to the last valid tone pair received. When OE is low, the data outputs are three stated.
VTD	15	O	Valid Tone detection signal. Presents a logic high when a received tone pair has been registered and the output latch updated, returns to Logic low when the voltage on SI/GT falls below Vtst.
ETD	16	O	Early Tone detection. Presents a logic high once the digital algorithm has detected a valid tone pair. Any momentary loss of signal condition will cause ETD to return to a logic low.

ST88C870

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
SI/GT	17	I/O	Steering Input / Guard time (Output) Bidirectional. A voltage greater than Vtst detected at SI causes the device to register the detected tone pair and update the output latch. A voltage less than Vtst frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant; its state is a function of ETD and the voltage on SI.
VCC	18	I	Most positive power supply. Typically 5 Volts.

* = Internal pull-up resistor
** = Internal pull-down resistor

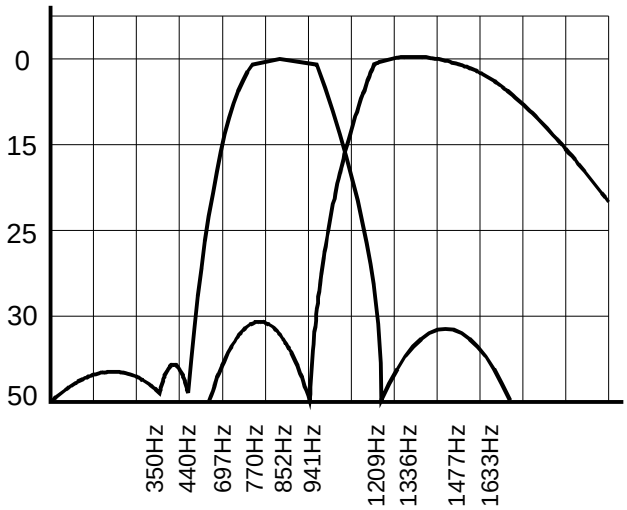
FILTER SECTION

Separation of the low group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection. Each filter output is followed by a single order RC smoothing filter section which smoothes the signals prior to limiting. Limiting is performed by high gain compactors which are provided with hysteresis to prevent detection of unwanted low level signals. The outputs of the compactors provide full rail logic swings at the frequencies of the incoming DTMF signals.

DECODER SECTION

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies and noise.

When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the ETD output will go to an active state. Any subsequent loss of signal condition will cause ETD to assume an inactive state.



ST88C870

FUNCTIONAL DECODING TABLE:

KEY	OE	CE	ETD	D3	D2	D1	D0	FL	FH
ANY	L	X	H	Z	Z	Z	Z		
1	H	X	H	0	0	0	1	697	1209
2	H	X	H	0	0	1	0	697	1336
3	H	X	H	0	0	1	1	697	1477
4	H	X	H	0	1	0	0	770	1209
5	H	X	H	0	1	0	1	770	1336
6	H	X	H	0	1	1	0	770	1477
7	H	X	H	0	1	1	1	852	1209
8	H	X	H	1	0	0	0	852	1336
9	H	X	H	1	0	0	1	852	1477
0	H	X	H	1	0	1	0	941	1209
*	H	X	H	1	0	1	1	941	1336
#	H	X	H	1	1	0	0	941	1477
A	H	X	H	1	1	0	1	697	1633
B	H	X	H	1	1	1	0	770	1633
C	H	X	H	1	1	1	1	852	1633
D	H	X	H	0	0	0	0	941	1633
A	H	H	L	***The output code will remain the same as the previous detected code.***					
B	H	H	L						
C	H	H	L						
D	H	H	L						

STEERING CIRCUIT

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ETD. A logic high on ETD causes **Vcx** (Fig. 1,2) to rise as the capacitor discharges. Provided signal condition is maintained (ETD remains high) for the validation period (T12) **Vcx** reaches the threshold (ETD) of the steering logic to register the tone pair, latching its corresponding 4-bit code into the output latch. At this point the GT output is activated and drives **Vcx** to Vcc. GT continues to drive high as long as ETD remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag STD goes high, signaling that a received tone pair has been registered.

The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (OE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

GUARD TIME ADJUSTMENTS

In many situations not requiring selection of tone duration and interdigit pause, the simple steering circuit shown in is applicable.

Component values are chosen according to the formula:

T14 = T12 + T4
T16 = T13 + T5

T4 = (RpCx) Ln [VCC / (VCC-Vcx)]
T5 = (R1Cx) Ln (VCC / Vcx)
Rp = (R1R2) / (R1+R2)

- Decreasing T4 (T4 < T5) Fig. 2
- Decreasing T5 (T4 > T5) Fig. 1

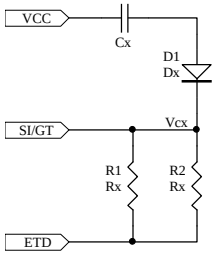


Figure 1.

ST88C870

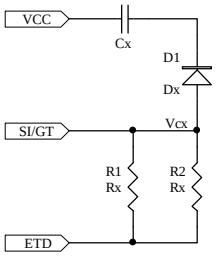


Figure 2.

The value of T12 is a device parameter and T14 is the minimum signal duration to be recognized by the receiver (see timing diagram). A value for C of 0.1µF is recommended for most applications, leaving R to be selected by the designer.

Different steering arrangements may be used to select independently the guard times for tone present (T4) and tone absent (T5). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing T14 improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, relatively short T14 with a long T17 would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required.

POWER DOWN MODE

A logic high applied to PD will power down the device to minimize the power consumption in a standby mode. It stops the oscillator and the functions of the filters.

Inhibit mode is enabled by a logic high input to the TD. It inhibits the detection of tones representing characters A, B, C, and D. The output code will remain the same as the previous detected code.

DIFFERENTIAL INPUT CONFIGURATION

The input arrangement of the ST88C870 provides a differential input operational amplifier as well as a bias source (Vref) which is used to bias the inputs at mid rail. Provision is made for connection of a feedback resistor to the op-amp output (GC) for adjustment of gain. In a single ended configuration, the input pins are connected as shown in Figure 4 with the op-amp connected for unity gain and Vref biasing the input at VCC/2.

Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R3.

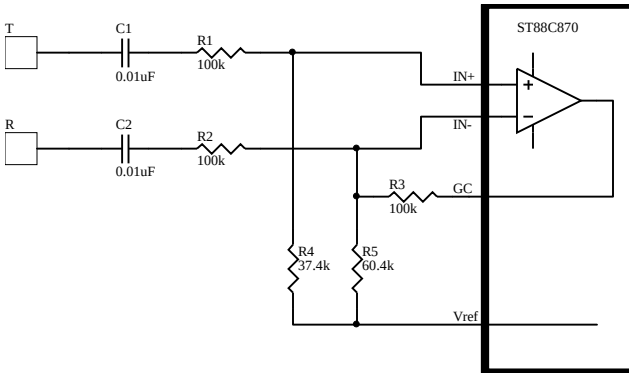


Figure 3.

R4 = (R3R5) / (R3+R5)
Voltage gain = R3 / R2

$Z\,in = 2\sqrt{R2^2 + (1 / WC)^2}$

CRYSTAL OSCILLATOR CIRCUIT

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal and is normally connected as shown in Figure 4 (Single-Ended Input Configuration). However it is possible to configure several ST88C870 devices employing only

a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30pF capacitor to the oscillator input (XTAL1) of the next device Figure 5. Subsequent devices are connected in a similar fashion. The problems associated with unbalanced loading are not a concern with the arrangement shown, i.e., precision balancing capacitors are not required.

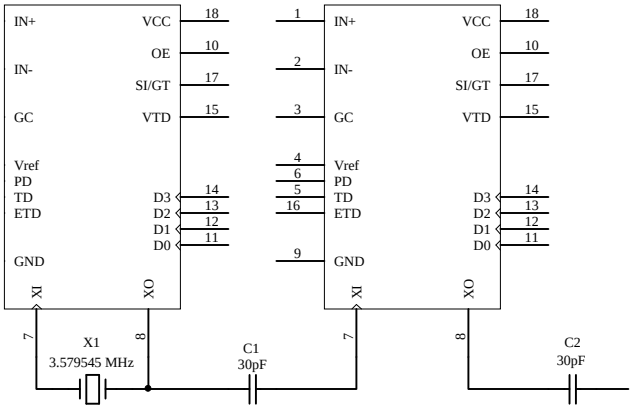


Figure 5.

CRYSTAL OSCILLATOR SPECIFICATIONS

F = 1 / (2π √ (L1 C1)
L1 ≈ 0.532 mH
C1 ≈ 4.984 pF
R1 ≈ 10.752 Ω
C0 = 38 pF
Q = 896

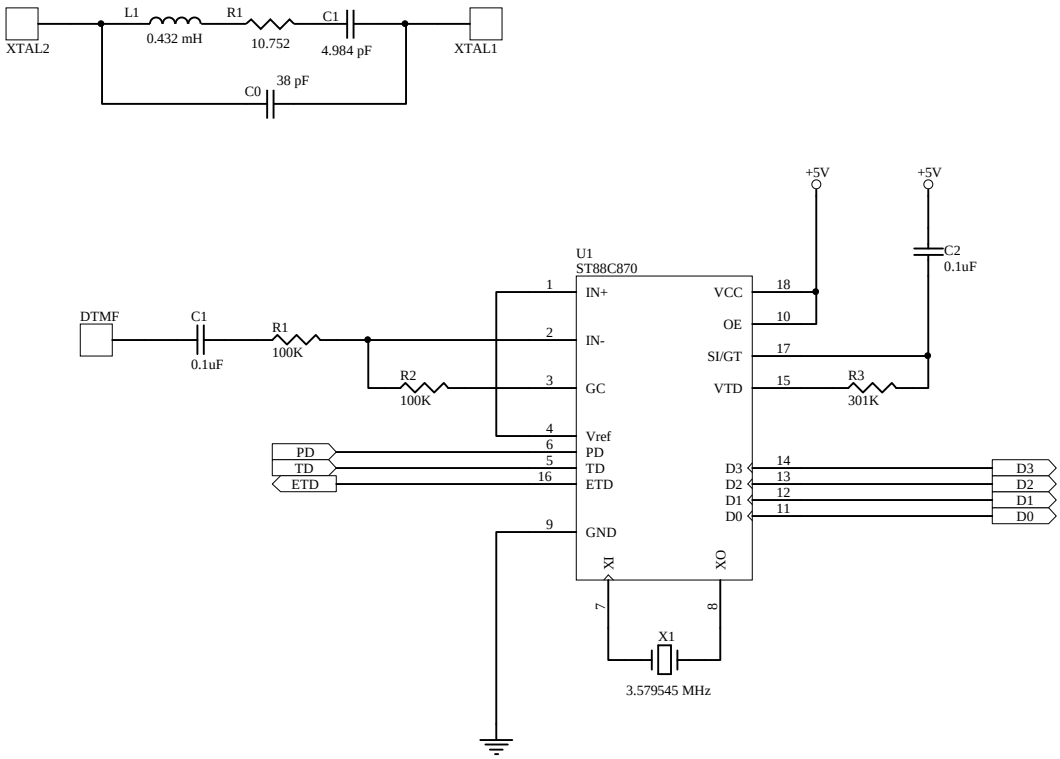


Figure 4.

ST88C870

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current		5	10	mA	
I_{STD}	Standby current		10	25	µA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	
R_{IIL}	Input leakage current		0.1		µA	
I_{UP}	Input pull-up current		10	20	µA	
I_{DN}	Input pull-down current		15	40	µA	
R_{IN}	Input impedance		10		MΩ	
V_{VT}	Threshold voltage	2.2	2.4	2.5	V	
V_{REF}	Vref output voltage	2.3	2.5	2.7	V	
V_R	Vref output resistance		1		kΩ	

ST88C870

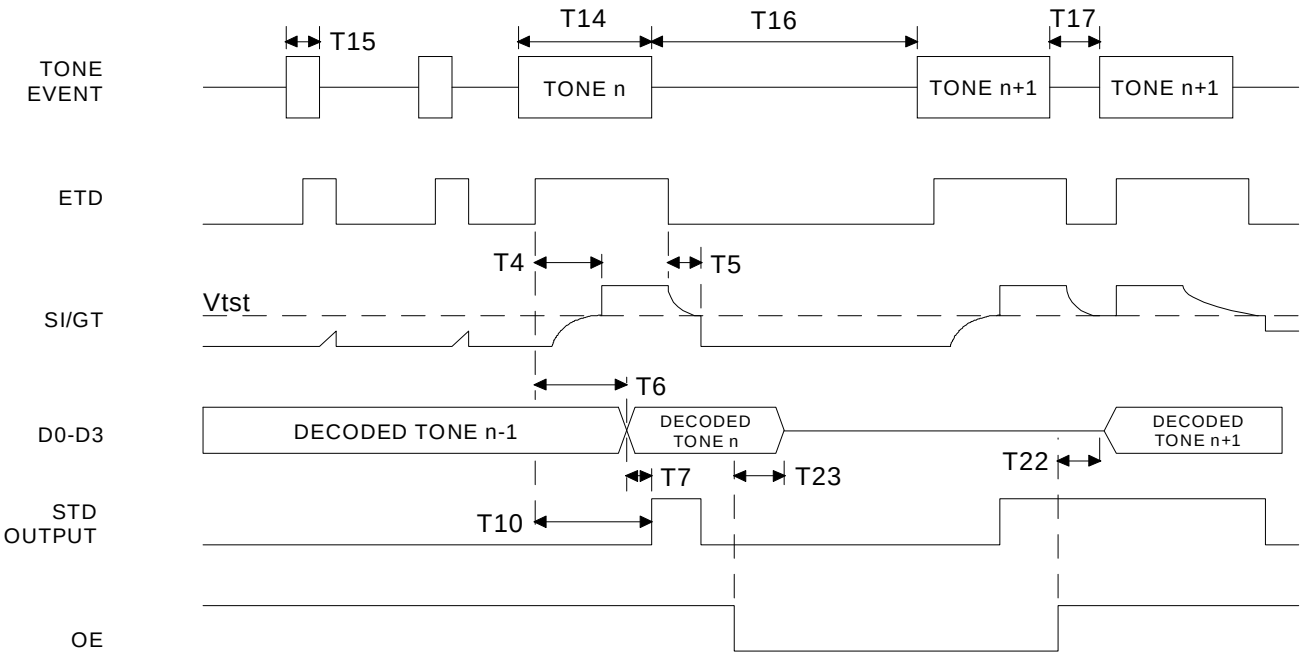
AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
T_1	Input clock frequency		3.5795		MHz	
T_2	Input clock duty cycle	40	50	60	%	
T_3	Clock rise/fall time			110	ns	
T_6	Propagation delay SI to D0-D3		8	16	µs	
T_7	Propagation delay D0-D3 to STD		8	16	µs	
T_8	Power down time		20		ms	
T_9	Power up time		30		ms	
T_{10}	Propagation delay SI to STD		12	16	µs	
T_{12}	Tone present detect time	5	11	14	ms	
T_{13}	Tone absent detect time	0.5	4	8.5	ms	
T_{14}	Tone duration accept			40	ms	
T_{15}	Tone duration reject	20			ms	
T_{16}	Interdigit pause accept			40	ms	
T_{17}	Interdigit pause reject	20			ms	
T_{19}	Propagation delay		8	16	µs	
T_{21}	Output data setup time		3.4		µs	
T_{22}	Propagation delay OE to D0-D3 disable		50		ns	
T_{23}	Propagation delay OE to D0-D3 enable		300		ns	

*NOTES
1. dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3.Tone duration=40 ms,tone pause=40ms.
6.Signal condition consists of nominal DTMF frequencies.
S.Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5% ±2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 400 Hz) ±2 %.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Guaranteed by design and characterization.

ST88C870


T15
T14
T16
T17
TONE EVENT
TONE n
TONE n+1
TONE n+1
ETD
T4
T5
Vtst
SI/GT
T6
D0-D3
DECODED TONE n-1
DECODED TONE n
DECODED TONE n+1
T22
T7
T23
STD OUTPUT
T10
OE