STARTECH

An EXAR Company

ST84C72

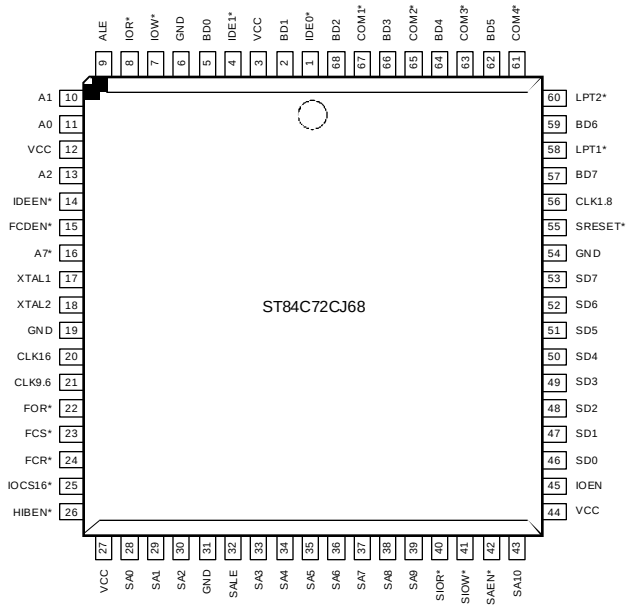
Printed June 19, 1996

IDE INTERFACE WITH I/O DECODE

DESCRIPTION

The ST84C72 is designed to replace all necessary TTL logics for 16 bit IDE interface and decode logic for floppy controller and serial / parallel I/O ports. A select pin is provided to select primary or secondary address for hard and floppy decodes. On board crystal oscillator circuit provides 16, 9, and 1.8461 MHz clock outputs for some floppy controllers and uart from 48 MHz external crystal connected to ST84C72.

PLCC package



FEATURES

- Low power CMOS design
- Direct bus connect
- Replacement for more than 7 TTL parts
- High speed for new design
- Selectable I/O decode ports. (COM1-COM4, LPT1-LPT2)
- Floppy address decode
- Pin selectable primary and secondary address decodes

ORDERING INFORMATION

Part number	Package	Operating temperature
ST84C72CJ68	PLCC	0 ° C to +70 ° C

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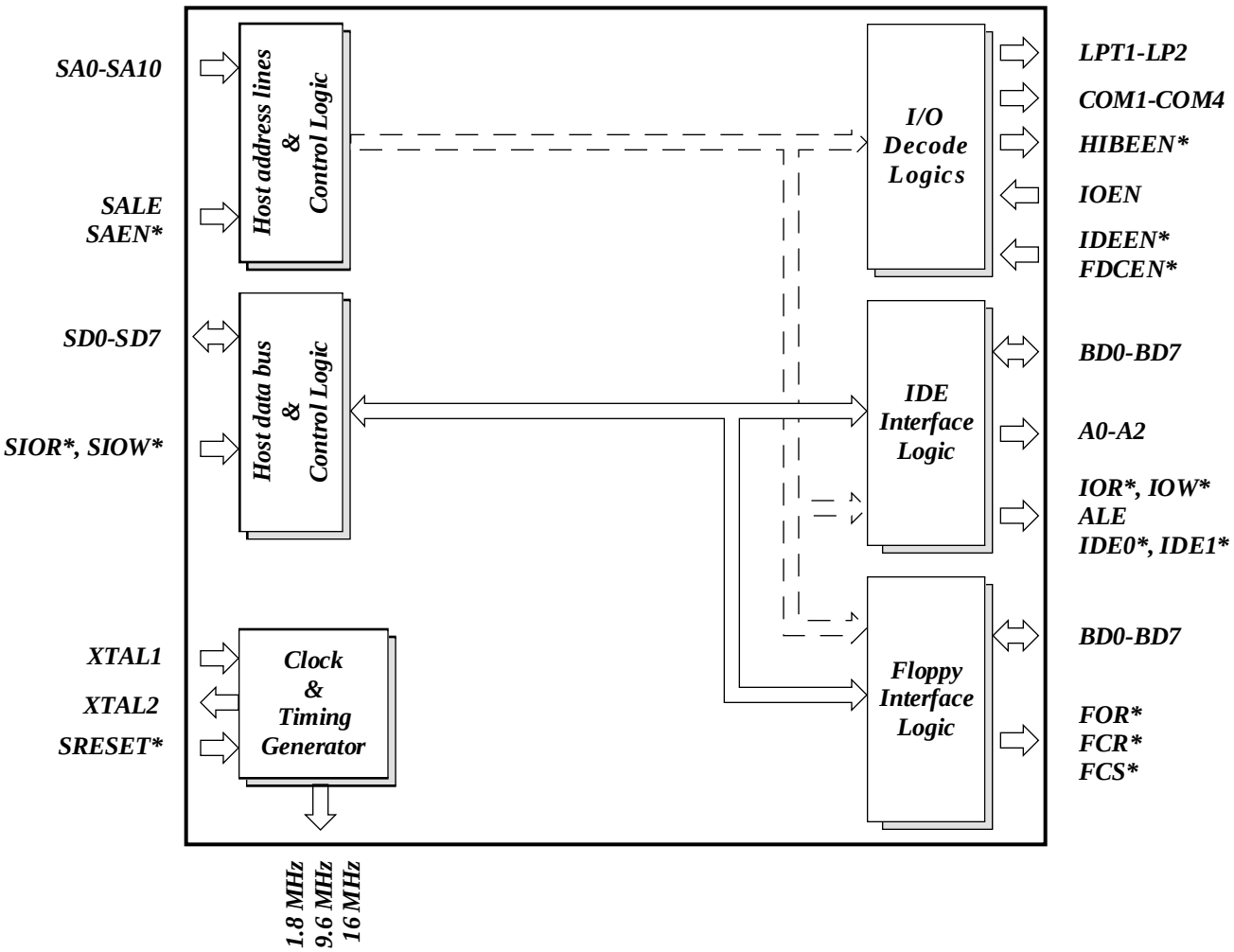
BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
SA0-SA2	28-30	I	Host address lines A0-A2.
SA3-SA9	33-40	I	Host address lines A3-A9.
SA10	43	I	Host address line A10.
SALE	32	I	Host address latch enable (active high).
SAEN*	42	I	Host address enable (active low). All decoded addresses are valid when SAEN* is low.
SIOW*	41	I	Host I/O write signal input (active low). Buffered data bus (BD7-BD0) are gated with SIOW*, SIOR* and I/O decoded addresses to insure proper valid data time slots.
SIOR*	40	I	Host I/O read signal input (active low).Buffered data bus (B07-BD7) are gated with SIOR*, SIOW* and I/O decoded addresses to insure proper valid data time slots.
SD0-SD7	46-53	I/O	Host data bus.
SRESET*	55	I	Host system reset (internally pulled up, active low). This pin is used to set internal clock dividers to known state. For normal operation this pin should be left open or connected to VCC.
XTAL1	17	I	Crystal or external clock input. A crystal can be connected between XTAL1 and XTAL2 with some additional filters to generate 48 Mhz clock frequency for floppy controller and UART clock . This pin can be connected to VCC or GND if CLK16, CLK9.6 and CLK1.8 are not used.
XTAL2	18	O	Crystal output. This pin should be left open if external clock is used to connect to XTAL1 or clock is not used.
LPT1*	58	O	Line printer enable (active low). Primary printer enable signal. Decoded for address 378 Hex (LPT1).
LPT2*	60	O	Line printer enable (active low). Secondary printer enable signal. Decoded for address 278 Hex (LPT2).

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
COM1*	67	O	Serial communication select pin (active low). Decoded for 3F8 Hex (COM-1).
COM2*	65	O	Serial communication select pin (active low). Decoded for 2F8 Hex (COM-2).
COM3*	63	O	Serial communication select pin (active low). Decoded for 3E8 Hex (COM-3).
COM4*	61	O	Serial communication select pin (active low). Decoded for 2E8 Hex (COM-4).
CLK1.8	56	O	1.8461 Mhz clock output generated from 48 Mhz crystal (crystal frequency or external clock divide by 26). This clock can substitute the standard 1.8432 Mhz serial communication clock.
IOEN	45	I	Serial and parallel port access. Connecting this pin to pin 44 (RDOUT) of the ST16C452, ST16C552, or ST16C553 enables the BD0-BD7 to access the serial and parallel ports. This pin should be tied to GND if external serial/ parallel ports are not used.
FDCEN*	15	I	Floppy controller enable/disable (internally pulled up). Floppy controller select is disabled when this pin is left open or connected to VCC. Floppy controller can be selected when this pin is connected to host SA7 pin (primary selection address 3F7, 3F5, 3F4 and 3F2 Hex) or A7* output pin of the ST84C72 (secondary selection address 377, 375, 374 and 372 Hex).
FOR*	22	O	Floppy controller address decode (372/3F2 Hex).
FCS*	23	O	Floppy controller address decode (377/3F7 Hex).
FCR*	24	O	Floppy controller address decode (374-5/3F4-5 Hex).
CLK16	20	O	16 Mhz clock output generated from 48 Mhz crystal (crystal frequency or external clock divided by 3).

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CLK9.6	21	O	9.6 Mhz clock output generated from 48 Mhz crystal (crystal frequency or external clock divide by 5).
IOCS16*	25	I	IDE 16 bit data transfer enable (internally pulled up, active low). This pin enables the external 74LS245 bus driver (HIBEN*) when IDE port is selected and 16 bit data transfer is required.
IDEEN*	14	I	IDE Enable/Disable (internally pulled up). IDE select is disabled when this pin is left open or connected to VCC. IDE controller can be selected when this pin is connected to A7* output pin of the ST84C72 (primary selection address 3F0-3F7 and 1F0-1F7 Hex) or host address line SA7 (secondary selection address 370-377 and 170-177Hex).
IDE1*	4	O	IDE drive/register select-1 (active low). When IDEEN* is enabled via SA7, this pin is enabled when I/O port address 3F6 or 3F7 Hex is accessed. When IDEEN* is enabled via A7* pin, IDE1* is enabled when I/O port address 376 or 377 Hex is accessed.
IDE0*	1	O	IDE drive/register select-0 (active low). When IDEEN* is enabled via SA7, this pin is enabled when I/O port address 1F0-1F7 Hex is accessed. When IDEEN* is enabled via A7* pin, IDE0* is enabled when I/O port address 170-177 Hex is accessed.
HIBEN*	26	O	High order data bus enable. This pin enables the external 74LS245 data buffer (host SD8-SD15) when IOCS16* is active and IDE port is selected.
A0-A1	11-10	O	Buffered host addresses A0 and A1.
A2	13	O	Buffered host address A2.
A7*	16	O	Inverted host address line SA7. This pin is used to primary IDE and floppy controller.
BD3-BD0	5,2,68,66	I/O	Buffered LSB of low order host data bus (SD0-SD3). These bits are set to input mode when SIOW* is low.

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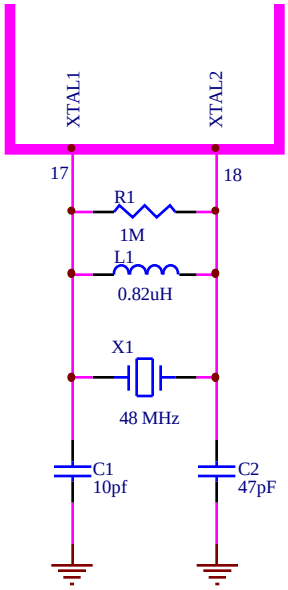
SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
BD4-BD6	64,62,59	I/O	Buffered MSB of low order host data bus (SD4-SD6). These bits are set to input mode when SIOW* is low.
BD7	57	I/O	Buffered host data bit -7 (SD7). This bit goes to high impedance when address 3F7 or 1F7 Hex is accessed during I/O read operation. BD7 is set to input mode when SIOW* is low.
ALE	9	O	Buffered host address latch (SALE).
IOR*	8	O	Buffered host I/O read signal (HIOR*).
IOW*	7	O	Buffered host I/O write signal (HIOW*).
GND	6,19,31,54	O	Signal and power ground.
VCC	3,12,27,44	I	Power supply input.

Optional external filter.



ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 16 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -16 mA
I_{CC}	Avg power supply current			15	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

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