STARTECH
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☎ Preliminary Information

ST78C36
ST78C36A

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ECP/EPP PARALLEL PRINTER PORT WITH 16 BYTE FIFO

DESCRIPTION

The ST78C36/36A is a monolithic Parallel Port Interface for use with IBM PC compatible platforms.

Operation as a standard Centronics printer port is the default, but software may re-configure the device to support bi-directional IBM PS/2 parallel port, Enhanced Parallel Port (EPP), or the Extended Capabilities Port (ECP, as defined by Hewlett Packard and Microsoft) modes.

The ECP modes are supported by a 16 byte FIFO that may be accessed by programmed I/O or DMA cycles.
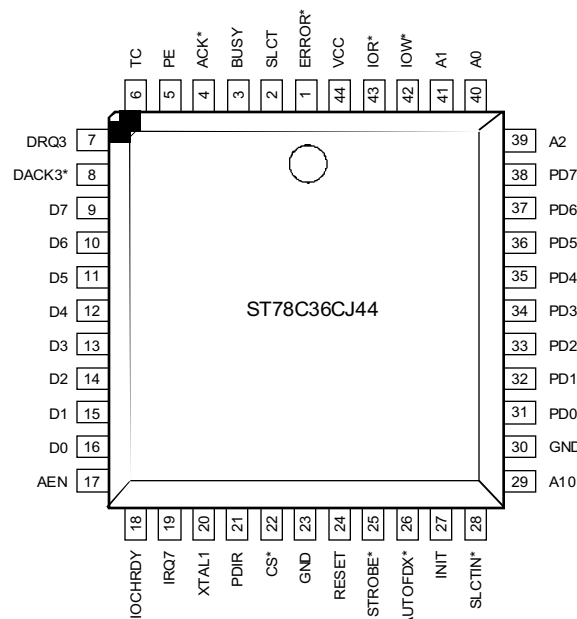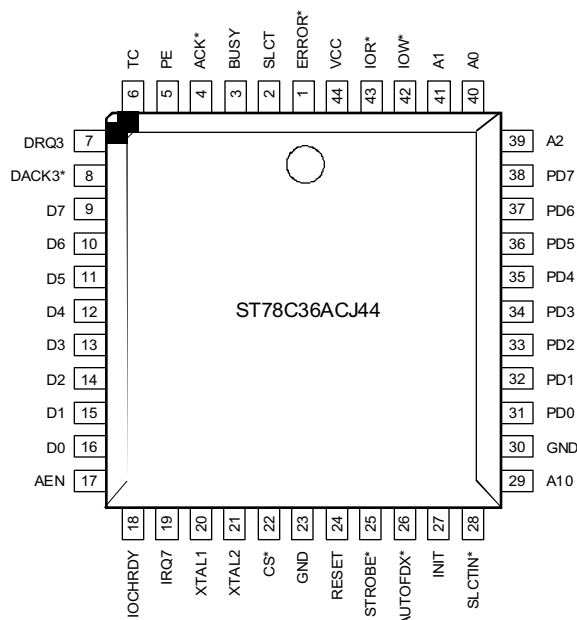
PLCC Package

ST78C36ACJ44

FEATURES

• IBM AT bus compatible
• Bi-directional port capability
• 16 byte FIFO for ECP modes
• On-chip oscillator (ST78C36A, ST78C36CQ64)
• Software selectable Interrupt (5, 7, or 9) and 8-bit DMA channel (ST78C36CQ64)

ST78C36CJ44

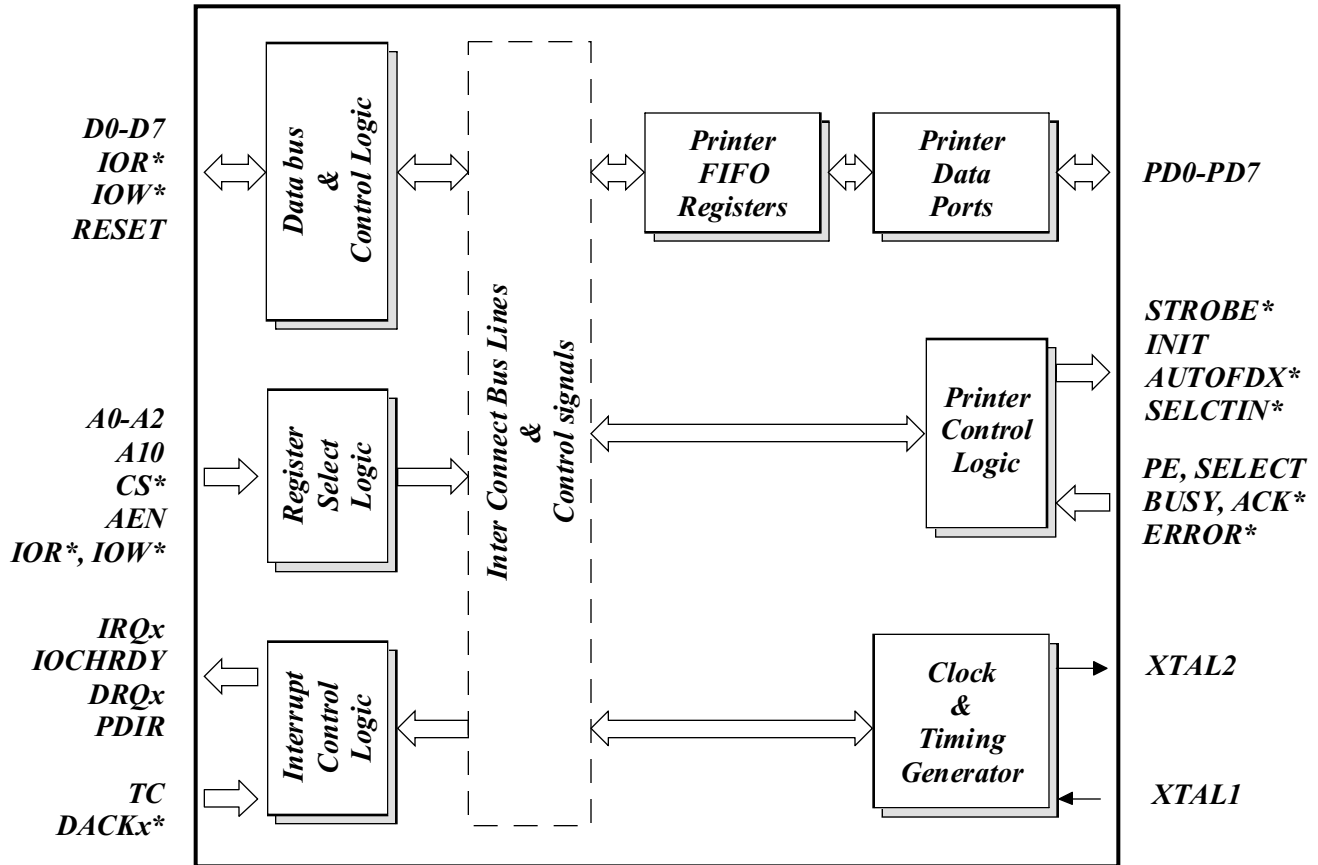## ORDERING INFORMATION

Part number	Package	Operating temperature
ST78C36CJ44	PLCC	0° C to + 70° C
ST78C36ACJ44	PLCC	0° C to + 70° C
ST78C36CQ64	QFP	0° C to + 70° C

Rev. 3.0

4-23

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BLOCK DIAGRAM

D0-D7 **IOR*** **IOW*** **RESET**	*Data bus & Control Logic*
A0-A2 **A10** **CS*** **AEN** **IOR*, IOW***	*Register Select Logic*
IRQx **IOCHRDY** **DRQx** **PDIR** **TC** **DACKx***	*Interrupt Control Logic*

Inter Connect Bus Lines & Control signals

Printer FIFO Registers

Printer Data Ports — **PD0-PD7**

Printer Control Logic

STROBE* **INIT** **AUTOFDX*** **SELCTIN***

PE, SELECT **BUSY, ACK*** **ERROR***

Clock & Timing Generator

XTAL2

XTAL1

SYMBOL DESCRIPTION

Symbol	Pin 44	Pin 64	Signal Type	Pin Description
DACK2*	-	2®	I	DMA Acknowledge for channel 2 (internal pull-up / three stated active low).
DRQ3	7	3®	O	DMA Request for channel 3 (internal pull-down three stated active high). see DRQ1
DACK3*	8	4®	I	DMA Acknowledge for channel 3 (internal pull-up / three stated active low).
D7 - D0	9-16	5-12	I/O	Data bus. Bi-directional data port.
AEN	17	13	I	DMA address enable (active high). When this line is high, the DMA controller has controll of the address bus.
IRQ9*	-	14	O	Interrupt Request channel 9 (three stated active low).
IRQ5*	-	18	O	Interrupt Request channel 5 (three stated active low).
IOCHRDY	18	19®	O	I/O Channel ready (internal pull-up / three stated active high). This pin goes low when ST78C36 requires addition clock cycles for read and write.
IRQ7*	19	20	O	Interrupt Request channel 7 (three stated active low).
XTAL1	20	21	I	Crystal oscillator input (ST78C36A, ST78C36CQ64) or External clock input (ST78C36), nominal 24 MHz.
XTAL2	21	22	O	Crystal oscillator output, nominal 24 MHz. ST78C36A, ST78C36CQ64 only.
PDIR	21	23®	O	Printer port direction indicator. High indicates ST78C36 is in input mode, low indicates output mode ST78C36, ST78C36CQ64
CS*	22	24	I	Chip select (active low). A low at this pin enables the parallel port / CPU data transfer operation.
RESET	24	26	I	System RESET (active high).
STROBE*	25	27®	I/O	Data strobe output (internal pull-up / three stated active

SYMBOL DESCRIPTION

Symbol	Pin		Signal Type	Pin Description
	44	64		
				low). This output indicates to the printer that valid data is available at the printer port (PD0-PD7).
AUTOFD*	26	28®	I/O	Automatic line feed (internal pull-up / three stated active low). When this signal is low the printer should automatically line feed after each line is printed.
INIT*	27	29®	I/O	Initialize line printer (internal pull-up / three stated active low). When this signal is low, it causes the printer to be initialized.
SLCTIN*	28	30®	I/O	Line printer select (internal pull-up / three stated active low). When this signal is low, it selects the printer.
A10	29	36	I	Address select line 10, places the ECP control/status/data ports at 400 hex offset from CS* decoded address.
PD0 - PD7	31-38	38-45	I/O	Bi-directional parallel ports (three state). To transfer data in or out of the ST78C36 parallel port. PD7-PD0 are latched during output mode. Output only for SPP and PPF modes, bi-directional for all other modes.
A2	39	46	I	Address select line 2.
DACK1*	-	47®	I	Active low AT bus DMA ACKnowledge for channel 1 (internal pull-up / three stated active low).
DRQ1	-	51®	O	Active high AT bus DMA ReQuest for channel 1 (internal pull-down three stated active high). A request is generated by bringing a DRQx line to a high level. A DRQx line is held high until the corresponding DMA acknowledge "DACKx*" line goes low.
A0-A1	40,41	52,53	I	Address select line 0 - 1, used for register (port) selection.
IOW*	42	54	I	Active low AT bus I/O Write strobe.
IOR*	43	55	I	Active low AT bus I/O Read strobe.
ERROR*	1	57®	I	Line printer error (internal pull-up / active low). This is an

SYMBOL DESCRIPTION

Symbol	Pin 44	64	Signal Type	Pin Description
				output from the printer to indicate an error by holding it low during error condition.
SLCT	2	58®	I	Line printer selected (internal pull-up / active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	3	59®	I	Line printer busy (internal pull-up / active high). An output from the printer to indicate printer is not ready to accept data.
ACK*	4	60®	I	Line printer acknowledge (internal pull-up / active low). This input is pulsed low by the printer to indicate that data has been accepted successfully.
PE	5	61®	I	Line printer paper empty (internal pull-up / active high). An output from the printer to indicate out of paper.
TC	6	62	I	Terminal Count (active high). The ST78C36 terminates the DMA channel when a high pulse is detected.
DRQ2	-	63®	O	DMA Request for channel 2 (internal pull-down / three stated active high). See DRQ1
VCC	44	16,56	I	Supply power (+5 Vdc).
GND	23,30	15,25, 37,48 , 64	O	Supply ground.

® Indicates internal pull up / down resistor

ST78C36/36A

OVERVIEW

This device is designed around the Hewlett Packard/ Microsoft specification for Extended Capabilities Port Protocol with "ECR mode 100" defined as Enhanced Parallel Port (EPP) mode. The internal timing engines were designed around a 24 MHz reference, which can be supplied from an external source or by the built-in oscillator circuit (ST78C36CQ64 only) with an appropriate crystal.

At system RESET, the device defaults to standard IBM PC compatible Centronics printer mode (output only). The bi-directional PS/2, EPP, and ECP modes can only be activated by programming the ECR mode field (this requires address bit A10 = 1, which is outside the normal a three state state/ISA I/O space).

Optional capabilities of the ECP specification are set as follows:

- ECP defined interrupts are pulsed, low true (Centronics ACK* is non-pulsed, low true).
- PWord size is forced to 1 byte.
- There is 1 byte in the transmitter that does not affect the FIFO full bit (ECP modes).
- RLE compression is not supported in hardware.
- IRQ channel is selectable as 5, 7, or 9 (ST78C36CQ64 only).
- DMA channel is selectable as 1, 2, or 3 (ST78C36CQ64 only).
- FIFO THRESHOLD is set at 8 (used only for non-DMA access to the FIFO).

PORT	ADDRESS	R/W	MODE	FUNCTION
DATA	000	R/W	000-001	Data Register
ECP-AFIFO	000	W	011	ECP FIFO (Address)
DSR	001	R	All	Status Register
DCR	002	R/W	All	Control Register
EPP-APort	003	R/W	100	EPP Port (Address)
EPP-DPort	004-007	R/W	100	EPP Port (Data)
C-FIFO	400	W	010	Parallel Port Data FIFO
ECP-DFIFO	400	R/W	011	ECP FIFO (Data)
T-FIFO	400	R/W	110	Test FIFO
Cnfg-A	400	R	111	Configuration Register A
Cnfg-B	401	R-R/W	111	Configuration Register B
ECR	402	R/W	All	Extended Control Register

STANDARD DEFINITIONS

• **Forward direction only.**
Compatible Mode, "Centronics" or standard mode.

• **Reverse direction only.**
Nibble mode:
4 bits at a time using status lines for data "Hewlett Packard Bi-tronics".

• **Bi-directional.**
EPP:
Enhanced Parallel port-used primarily by non-printer peripherals.

ECP:
Extended Capability Port-used primarily bt new generation of printers and scanners.

DATA REGISTER (DATA)

DATA Bit 0-7:
For host output cycles in SPP mode (ECR mode 000) or PS/2 mode (ECR mode 001), data from the host is registered at the trailing edge of IOW*. On host input cycles, data at the peripheral port is passed through to the host data bus.

ECP FIFO ADDRESS (ECP-AFIFO)

ECP-AFIFO Bit 0-7:
This port is only available for programmed I/O (non-DMA), and only has significance for host write. Data written to this port is stored in the FIFO if FIFO-F = 0 and will be lost if FIFO-F = 1. A 9th FIFO bit (tag) is set low on write.

A read from this port is the same as a read at 400.

STATUS REGISTER (DSR)
This status register is read-only except for bit-0, and all bits are latched for the duration of IOR*.

DSR Bit-0:
If EPP mode is not selected, this bit returns logic one.

During EPP mode, bit-0 will return a high if the EPP 10 µsecond TimeOut elapsed during the last EPP read or write cycle (this TimeOut also aborts the EPP cycle). This status bit is cleared by exiting EPP mode or by the host writing a high to bit-0 of this register.

DSR Bit 1-2:
Reserved, logic one.

DSR Bit-3:
The true state of the ERROR* pad.

DSR Bit-4:
The true state of the SLCT pad.

DSR Bit-5:
The true state of the PE(mpty) pad.

DSR Bit-6:
The true state of the ACK* pad.

DSR Bit-7:
The complement of the BUSY pad.

CONTROL REGISTER (DCR)

DCR Bit-0:
The complement of this bit drives STROBE*, and the complement of the pad state is returned for read.

DCR Bit-1:
The complement of this bit drives AUTOFD*, and the complement of the pad state is returned for read.

DCR Bit-2:
This bit drives INIT, and the pad state is returned for read.

DCR Bit-3:
The complement of this bit drives SLCTIN*, and the complement of the pad state is returned for read.

DCR Bit-4:
Ack Interrupt Enable set to a high will generate an interrupt when ACK* is low. When either returns to a high state, this interrupt source will go in-active. This interrupt is not pulsed.

DCR Bit-5:
Peripheral port direction, OUT = 0 and IN = 1.
This bit is forced to logic zero by ECR modes 000 or 010. It can be written only in ECR mode 001, and will maintain that state if the ECR mode is changed to 011, 100, or 110. This bit must be set low for EPP mode, which allows the host to control direction with IOR* and IOW*. The final port direction also drives PDIR.

DCR Bits 6-7:
Reserved, logic zero.

EPP ADDRESS PORT (EPP-APort)
When EPP mode is enabled, a host read or write with this port will result in a data transfer directly to/from the peripheral with SLCTIN* active. Direction is set by host read/write and will drive STROBE* low during a write if DCR bit 5 (DIR) is not set high.

EPP DATA PORT (EPP-DPort)
When EPP mode is enabled, a host read or write with this port will result in a data transfer directly to/from the peripheral with AUTOFD* active. Direction is set by host read/write and will drive STROBE* low during a write if DCR bit 5 (DIR) is not set high.

PARALLEL PORT DATA (C-FIFO)
This port is available for programmed I/O and DMA access. Data written to this port is stored in the FIFO if FIFO-F = 0 and will be lost if FIFO-F = 1.
Data written to this port will be automatically transferred to the peripheral with STROBE* handshaking with BUSY. This port is only defined for write, host reads will interfere with FIFO read sequencing.

ECP DATA FIFO (ECP-DFIFO)

This port is available for programmed I/O and DMA access. Data written to this port is stored in the FIFO if FIFO-F = 0 and will be lost if FIFO-F = 1. A 9th FIFO bit (tag) is set high on write.
Data read from this port will undergo de-compression if the FIFO tag bit and data bit-7 are both low. The byte containing the RLE count is loaded into the RLE counter and the succeeding byte in the FIFO will be returned to the host RLE count + 1 times before the

FIFO read address is incremented. If a FIFO under-run is incurred during host read, the last data byte is returned and FIFO-E remains coherent.

TEST FIFO (T-FIFO)
This port is available for programmed I/O and DMA access. Data written to this port is stored in the FIFO if FIFO-F = 0 and will be lost if FIFO-F = 1. During a read cycle from this port a FIFO under-run will return last data read and FIFO-E remains coherent.

CONFIGURATION REGISTER A (Cnfg-A)
This read-only register is available in ECR mode 111 only.

Cnfg-A Bit 0-1:
Forced to logic zero, this field is don't care for PWord = 1 byte.

Cnfg-A Bit-2:
When transmitting, there is 1 byte waiting to be transmitted that does not affect FIFO-F.

Cnfg-A Bit-3:
Reserved, logic zero.

Cnfg-A Bit 4-6:
Indicates PWord = 1 byte (8-bit implementation).

Cnfg-A Bit-7:
Indicates ECP interrupts are pulsed.

CONFIGURATION REGISTER B (Cnfg-B)
This register is available in ECR mode 111 only, and returns bits 0-5 as logic zero for the ST78C36CJ44. The ST78C36CQ64 will allow programmed selection of the Interrupt and DMA channels after a system RESET state of 001011 (bits 0-5).

Cnfg-B Bit 0-2:
With bit 2 forced low, select an 8-bit DMA channel per the following table:

IOW*	IOR*	DMA
X00	000	3
X01	001	1
X10	010	2
X11	011	3 (default)

Cnfg-B Bit 3-5:
Select an IRQ channel per the following table:

IOW*	IOR*	IRQ
000	001	7
001	001	7 (default)
010	010	9
011	001	7
100	001	7
101	001	7
110	001	7
111	111	5

Cnfg-B Bit-6:
Returns the true value of the selected IRQ pad.

Cnfg-B Bit-7:
Indicates RLE compression is not supported.

EXTENDED CONTROL REGISTER (ECR)
The Extended Control Register has a system RESET state of 00010101. The significance of the bits is defined by the ECP specification as:

ECR Bit-0:
This read-only bit returns FIFO empty status (FIFO-E) and is forced high unless PPF, ECP, or TST mode is selected.

0 = At least one byte of data contains in the FIFO.
1 = FIFO is empty.

ECR Bit-1:
This read-only bit returns FIFO full status (FIFO-F) and is forced low unless PPF, ECP, or TST mode is selected.

0 = At least one empty location is available in the FIFO.
1 = FIFO is full.

ECR Bit-2:
When low, this bit (ServiceIntr) enables a pulsed interrupt and enables DMA requests (if bit-3 is set). If the enabled interrupt occurs, this bit is automatically returned to a high. The interrupt conditions are:

ECR Bit-3 = **DMA**
DCR Bit-5 = **DIR**ection

DMA	DIR	CONDITION
0	0	8 empty bytes in the FIFO.
0	1	8 filled bytes in the FIFO.
1	X	DMA Terminal Count (TC).

ECR BIT-3:
This bit disables DMA when set low. When set high, a low on ServiceIntr will enable DMA requests.

0 = DMA disabled, DRQx pin is three-stated.
1 = DMA enabled

ECR Bit-4:
When low, this bit (ErrIntrEn*) enables a pulsed interrupt if ERROR* (Fault*) is low. The interrupt is only enabled in ECP mode.

ECR Bit 5-7:
This field can be set to any value if the current value is 000 or 001. If the current value is not 000 or 001, then the field can only be written to 000 or 001. The modes are defined as:

MODE	NAME	DESCRIPTION
000	SPP	Standard, output only. DCR Bit-5 is forced to "0".
001	PS2	Bi-directional PS/2 parallel port. FIFO is disabled
010	PPF	FIFOed, output only. DCR Bit-5 is forced to "0".
011	ECP	ECP FIFOed port with RLE de-compression. FIFO direction is controlled by DCR Bit-5.
100	EPP	EPP mode.
101	-	reserved
110	TST	FIFO test mode. FIFO is accessible via TFIFO register.
111	CFG	Configuration A/B register enable.

OPERATION

SPP MODE

This is ECR mode 000 (system RESET mode).
In this output-only mode the host data is registered to PD[7:0] at the trailing edge of IOW*; PDIR is driven low; STROBE*, AUTOFD*, INIT, and SLCTIN* are open-drain; and all timing is managed by the host through DSR and DCR registers.

PS2 MODE

This is ECR mode 001.
In this bi-directional mode the host output data is registered to PD[7:0] at the trailing edge of IOW*, PDIR is driven by DIR to allow peripheral data input, AUTOFD*, INIT, and SLCTIN* are totem-pole, and all timing is managed by the host through DSR and DCR registers.

PPF MODE

This is ECR mode 010.
In this output-only mode the host data is written to the FIFO with I/O writes to address 400 or by DMA writes; PDIR is driven low*; AUTOFD*, INIT, and SLCTIN* are totem-pole.
FIFO data is automatically registered to PD[7:0]

whenever the FIFO-E bit is low (data available), and timing is generated by controller logic that handshakes STROBE* (controller) with BUSY (peripheral).

ECP MODE

This is ECR mode 011.
In this bi-directional mode the host data is written to the FIFO with I/O writes to address 000, 400 or DMA; PDIR is driven by DIR (can only be set in ECR mode 001); AUTOFD*, INIT, and SLCTIN* are totem-pole. I/O writes to address 000 will write a low into the FIFO tag bit, while I/O writes to address 400 or DMA will insert a high.

ECP FORWARD MODE (PDIR = 0)

FIFO data is automatically registered to PD[7:0] whenever the FIFO-E bit is low (data available), and timing is generated by controller logic that handshakes STROBE* (controller) with BUSY (peripheral). Data from the FIFO tag bit is output on AUTOFD* after being registered simultaneous with FIFO data.

ECP REVERSE MODE (PDIR = 1)

PD[7:0] data and BUSY are latched into the FIFO and tag bit respectively at the trailing edge of AUTOFD* if FIFO-F = 0. Timing is generated by controller logic that handshakes ACK* (peripheral) with AUTOFD* (controller).

EPP MODE

This is ECR mode 100.
In this bi-directional mode, I/O writes will latch host output data at the trailing edge of IOW*, and peripheral input data will be latched at the trailing edge of SLCTIN* or AUTOFD*. PDIR, and STROBE* are driven by the state of IOW* (DCR bits 5 and 0 must be set low); AUTOFD*, INIT, and SLCTIN* are totem-pole.

EPP mode allows buffered access between the PC bus and the peripheral with timing provided by the peripheral via BUSY handshake into IOCHRDY. I/O cycles with address 003 - 007 will immediately drive IOCHRDY low. STROBE* will go low and PD[7:0] is allowed to change (write cycles) after BUSY has been low for at least 60n second. (this delay may have elapsed prior to cycle initiation), immediately followed by a low driven on SLCTIN* for address 003 or

AUTOFD* (DATASTB*) for address 004 - 007 (read and write cycles). When BUSY returns high for a minimum of 60n second, IOCHRDY and the active strobe will be driven high - allowing the host to complete the I/O transaction.

To prevent a system stall, a 10 μsecond TimeOut aborts the cycle if it expires before BUSY returns high. This TimeOut also sets bit 0 of DCR, which is cleared by disabling EPP mode or writing a high to DCR bit 0.

TST MODE
This is ECR mode 110.
This mode allows data to be transferred (read or write in any direction) between the FIFO and host at address 400 or DMA without activating the control interface (no data is transferred to/from the peripheral). PDIR is driven by DIR (can only be set in ECR mode 001); AUTOFD*, INIT, and SLCTIN* are totem-pole.

Performing I/O cycles in this mode allows software to test for the value of FIFOThreshold (FT) for both output and input directions.

CFG MODE
This is ECR mode 111.
This mode enables I/O access to the configuration registers cnfgA and cnfgB and disables I/O access to the FIFO.

IRQ
The module has four sources of interrupt which may be directed to IRQ5*, IRQ7*, IRQ9* (see cnfgB) or externally jumpered.

1) When DCR bit 4 (AIE) is high and ACK* is low the interrupt is active.

2) When ECP mode is active, if ECR bit 4 is low when ERROR transitions low or ECR bit 4 transitions low when Fault* is low an interrupt pulse of at least 200n seconds will be generated.

3) In FIFO modes (PPF, ECP, or TST) with ECR bit 3 (DMA) low, an interrupt pulse of at least 200n seconds will be generated when ECR bit 2 (SI) is set low if there are at least 8 empty bytes in the FIFO and PDIR = 0 or there are at least 8 filled bytes in the FIFO and PDIR

= 1. This interrupt will automatically disable itself by setting ECR bit 2 high.

4) In FIFO modes (PPF, ECP, or TST) with (DMA request enabled), an interrupt pulse of at least 200n seconds will be generated when TC is received if PDACK* is low.
This interrupt will automatically disable itself and the DMA request by setting ECR bit 2 high.

DMA
DMA cycles occur only between the host and the FIFO data port (address 400) for PPF, ECP, or TST modes. The selected DRQ(1, 2, or 3) will be driven high if ECR bit 3 (DMA) is high and ECR bit 2 (SI) is low when {PDIR = 0 and FIFO-F = 0} or {PDIR = 1 and FIFO-E = 0} or TST mode is active.

When the selected DACK*(1, 2, or 3) is low, IOW* will transfer host data to the FIFO and IOR* will transfer FIFO data to the host.
The selected DRQ will be driven low to terminate the DMA channel when {PDIR = 0 and FIFO-F = 1} or {PDIR = 1 and FIFO-E = 1} or ECR bit 2 (SI) goes high (interrupt condition 4 above) or more than 32 consecutive DMA data cycles (read or write) have occurred.

FIFO-F and FIFO-E terminated cycles will automatically restart when their state returns low. Consecutive cycle termination will automatically restart because the counter is reset when the selected DACK* goes high. TC terminated cycles can only be restarted by the host setting ECR bit 2 (SI) low again.

RLE
The module does not support RLE compression (indicated by the "0" in cnfgB bit 7) but is required to support RLE de-compression.

The host may send compressed data to the peripheral by writing the RLE length byte (bit 7 = 0) to address 000 (NOTE: DMA cannot be used for this byte) which will place a zero into the FIFO tag bit. This must be followed immediately by the data byte being written to the FIFO at address 400. These bytes will be transferred to the peripheral in the normal manner.

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De-compression takes place if PDIR = 1 when data is read from the FIFO at address 000, 400 or DMA. When a byte is read from the FIFO, bits 0-6 (length) are placed in a counter if data bit-7 and the FIFO tag bit are both low. The subsequent byte in the FIFO (data) is presented to the host count + 1 times before the FIFO read pointer is advanced.

"CENTRONICS, SPP" SIGNAL DESCRIPTIONS

Signal name	Signal Type	Description
STROBE*	O	Active low. Indicates valid data is on the data lines.
AUTOFD*	O	Active low. Instructs the printer to automatically insert a line feed for each carriage return.
SLCTIN*	O	Active low. Used to indicate to the printer that it is selected.
INIT*	O	Active low. Used to reset the printer
ACK*	I	A low asserted pulse used to indicate that the last character was received.
BUSY	I	A high signal asserted by the printer to indicate that it is busy and cannot take data.
PE	I	A high signal indicated that printer Paper is empty.
SLCT	I	A high signal indicates that printer is online.
ERROR*	I	Asserted low to indicate that some error condition exists.
PD0-PD7	O	Data.

"NIBBLE MODE" SIGNAL DESCRIPTIONS

Signal name	Signal Type	Nibble mode Name	Description
STROBE*	O	STROBE*	Not used for reverse data transfer.
AUTOFD*	O	HostBusy	Host nibble mode handshake signal. Set low to indicate host is ready for nibble. Set high to indicate nibble has been received.
SLCTIN*	O	1284Active	Set high when host is in a 1284 transfer mode.
INIT*	O	INIT*	Not used for reverse data transfer.
ACK*	I	PtrClk	Set low to indicate valid nibble data, set high in response to "HostBusy" going high.
BUSY	I	PtrBusy	Used for Data Bit-3, then Bit-7.
PE	I	AckDataReq	Used for Data Bit-2, then Bit-6.
SLCT	I	Xflag	Used for Data Bit-1, then Bit-5.
ERROR*	I	DataAvail*	Used for Data Bit-0, then Bit-4.
PD0-PD7	O		Not used.

NIBBLE Mode Data Transfer Cycle

1. Host signals ability to take data by asserting HostBusy low.
2. Peripheral responds by placing first nibble on status lines.
3. Peripheral signals valid nibble by asserting PtrClk low.
4. Host sets HostBusy high to indicate that it has received the nibble and is not ready for another nibble.
5. Peripheral sets PtrClk high to acknowledge host.

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"EPP MODE" SIGNAL DESCRIPTIONS

Signal name	Signal Type	EPP mode Name	Description
STROBE*	O	Write*	Active low. Indicates a write operation, high for a read cycle
AUTOFD*	O	DataStb*	Active low. Indicates a Data-Read or Data-Write operation is in process.
SLCTIN*	O	AddrStb*	Active low. Indicates an Address-Read or Address-Write operation is in process.
INIT*	O	Reset*	Active low. Peripheral reset.
ACK*	I	Intr*	Peripheral interrupt. Used to generate an interrupt to the host.
BUSY	I	Wait*	Handshake signal. When low it indicates that is okay to start a cycle, when high it indicates that it is okay to end the cycle.
PE	I	User defined	Not used.
SLCT	I	User defined	Not used.
ERROR*	I	User defined	Not used.
PD0-PD7	O	AD0-AD7	Bi-directional address / data lines.

EPP Mode Data Transfer Cycle

1. Program executes an I/O write cycle to EPP Data Port-4.
2. The Write* line is asserted and the data is output to the parallel port.
3. The DataStb* is asserted, since Write* is asserted low.
4. The port waits for the acknowledge from the peripheral, Write* deasserted.
5. The DataStr* is deasserted and EPP cycle ends.
6. Write* is asserted low to indicate that the next cycle may begin.

"ECP MODE" SIGNAL DESCRIPTIONS

Signal Name	Signal Type	ECP mode Name	Description
STROBE*	O	HostClk	Used with PeriphAck to transfer data or address information in the forward direction.
AUTOFD*	O	HostAck	Provides Command / Data status in the forward direction. Used with PeriphClk to transfer data in the reverse direction.
SLCTIN*	O	1284Active	Set high when host is in a 1284 transfer mode.
INIT*	O	ReverseReq*	Driven low to put the channel in reverse direction.
ACK*	I	PeriphClk	Used with HostAck to transfer data in the reverse direction.
BUSY	I	PeriphAck	Used with HostClk to transfer data or address information in the forward direction. Provides Command / Data status in the reverse direction.
PE	I	AckReverse*	Driven low to acknowledge ReverseRequest.
SLCT	I	Xflag	Extensibility flag.
ERROR*	I	PeriphReq*	Set low by peripheral to indicate that reverse dat is available.
PD0-PD7	I/O	D0-D7	Bi-directional data lines.

ECP Mode Forawrd Data and Command Transfer Cycle

1. Host places data on the data lines and indicates a data cycle by setting HostAck high.
2. Host asserts HostClk low to indicate valid data.
3. Peripheral acknowledge host by setting PeriphAck high.
4. Host sets HostClk high. This is the edge that should be used to clock the data in to the peripheral.
5. Peripheral sets PeriphAck low to indicate that it is ready for the next byte.
6. The cycle repeats, but this time it is command cycle because HostAck is low.

ECP Mode Reverse Data and Command Transfer Cycle

1. The Host requests a reverse channel transfer by setting ReverseReq* low.
2. The peripheral signals that it is okay to proceed by setting AckReverse* low.
3. The peripheral places data on the data lines and indicates a data cycle by setting PeriphAck high.
4. Peripheral asserts PeriphClk low to indicate valid data.
5. Host acknowledges by setting HostAck high.
6. Peripheral sets PeriphClk high. This is the edge that should be used to clock the data in to the host.
7. Host sets HostAck low to indicate that it is ready for the next byte.
8. The cycle repeats, but this time it is a Command cycle because PeriphAck is low.

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AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
TRRQ	DRQx inactive delay from DACK*x active			100	ns	
TASU	AEN setup to command active	40			ns	
TAH	AEN hold from command inactive	10			ns	
TCMD	Command width	150			ns	
TACC	Data access from IOR* active			100	ns	
TDSU	Data setup to IOW* inactive	40			ns	
TDH	Data hold from command inactive	10			ns	
HOST	DMA TIMING					
TPDD	PD7-0, STROBE*, AUTOFD*, INIT, SLCTIN* delay from IOW* inactive			100	ns	
TIRQ	Interrupt delay from ACK*			60	ns	
TPW	Interrupt pre-charge pulse at release			10	ns	
TDS	PD7-0 setup to STROBE* active		600		ns	
TWS	STROBE* width		600		ns	
TDH	PD7-0 hold from STROBE* inactive		450		ns	
THS	STROBE* active to BUSY active (handshake)			500	ns	
TDD	PD7-0 hold from BUSY inactive		80		ns	
TCD	BUSY inactive to STROBE* active (cycle delay)		680		ns	
TDS	PD7-0, AUTOFD* setup to STROBE* active		0	60	ns	
T1	STROBE* inactive to BUSY inactive		0		ns	
T2	BUSY inactive to STROBE* active		80	200	ns	
T3	STROBE* active to BUSY active		0		ns	
T4	BUSY active to STROBE* inactive		80	180	ns	
TDH	PD7-0, AUTOFD* hold from BUSY active		80	180	ns	
TDS	PD7-0, BUSY setup to ACK* active		0		ns	
T1	ACK* inactive to AUTOFD* active		80	200	ns	
T2	AUTOFD* active to ACK* active		0		ns	
T3	ACK* active to AUTOFD* inactive		80	200	ns	
T4	AUTOFD* inactive to ACK* inactive		0		ns	
TDH	PD7-0 data hold from AUTOFD*		0		ns	
TAS	Host address setup to IOW* active		40		ns	
TAH	Host address hold from IOW* active		10		ns	
TDS	Host data setup to IOW* active		0	20	ns	

AC ELECTRICAL CHARACTERISTICS

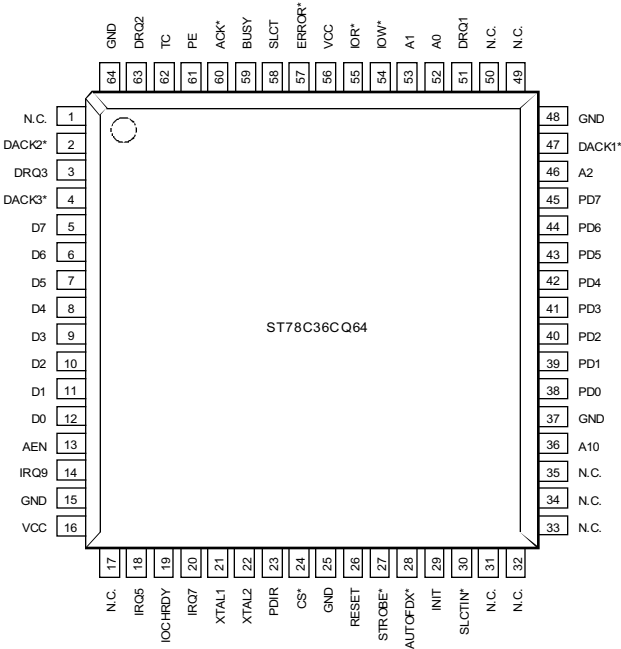T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
TDH	Host data hold from IOW* active		0		ns	
TBSY	IOW* active to IOCHRDY low		0	20	ns	
TDD	IOW* active to PD7-0 valid		0	50	ns	
TWPD	WAIT* active to PDIR change			10	ns	
THT	IOCHRDY high to Host terminate (IOW* inactive)		10		ns	
TCD	IOW* inactive to Host command active (IOW* or IOR*)		40		ns	
TPDW	PDIR low to WRITE* active		0		ns	
TPW	IOCHRDY pre-charge width at release			10	ns	
TDWS	WAIT* active to ADDRSTB*/ DATASTB* active		60	175	ns	
TWW	WAIT* active to WRITE* change		60	155	ns	
TWDH	WAIT* active to PD7-0 change		60	140	ns	
TRDY	WAIT* inactive to IOCHRDY high		60	155	ns	
TWS	WAIT* inactive to ADDRSTB*/ DATASTB* inactive		60	155	ns	
TSWD	ADDRSTB*/DATASTB* inactive to WAIT* active		0		ns	
TSW	ADDRSTB*/DATASTB* active to WAIT* inactive		0	10	μs	
TTO	IOW* active to WAIT* inactive (Time Out)		10	12	μs	
TAS	Host address setup to IOR* active		40		ns	
TAH	Host address hold from IOR* active		10		ns	
TDS	Host data setup to IOR* inactive		0	20	ns	
TDH	Host data hold from IOR* inactive		0		ns	
TBSY	IOR* active to IOCHRDY low		0	20	ns	
TACC	ADDRSTB*/DATASTB* active to PD7-0 valid to D7-0 valid		0		ns	
TDD	PD7-0 valid to D7-0 valid		0	75	ns	
TWPD	WAIT* active to PDIR change PD7-0 valid		60	150	ns	
THT	IOCHRDY high to Host terminate (IOR* inactive)		10		ns	
TCD	IOR* inactive to Host command active (IOW* or IOR*)		40		ns	
TPW	IOCHRDY pre-charge width at release			10	ns	

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AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
TDWS	WAIT* active to ADDRSTB*/ DATASTB* active		0	175	ns	
TWW	WAIT* active to WRITE* change		0	140	ns	
TWDH	WAIT* active to PD7-0 change		60	160	ns	
TRDY	WAIT* inactive to IOCHRDY high		60	160	ns	
TWS	WAIT* inactive to ADDRSTB*/ DATASTB* inactive		60	160	ns	
TSWD	ADDRSTB*/DATASTB* inactive to WAIT* active		0		ns	
TSW	ADDRSTB*/DATASTB* active to WAIT* inactive		0	10	μs	
TTO	IOR* active to WAIT* inactive (Time Out)		10	12	μs	

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Pinout (top, pins 49–64): GND, DRQ2, TC, PE, ACK*, BUSY, SLCT, ERROR*, VCC, IOR*, IOW*, A1, A0, DRQ1, N.C., N.C.

Left side (pins 1–16): N.C., DACK2*, DRQ3, DACK3*, D7, D6, D5, D4, D3, D2, D1, D0, AEN, IRQ9, GND, VCC

Right side (pins 48–33): GND, DACK1*, A2, PD7, PD6, PD5, PD4, PD3, PD2, PD1, PD0, GND, A10, N.C., N.C., N.C.

Bottom (pins 17–32): N.C., IRQ5, IOCHRDY, IRQ7, XTAL1, XTAL2, PDIR, CS*, GND, RESET, STROBE*, AUTOFDX*, INIT, SLCTIN*, N.C., N.C.

ABSOLUTE MAXIMUM RATINGS

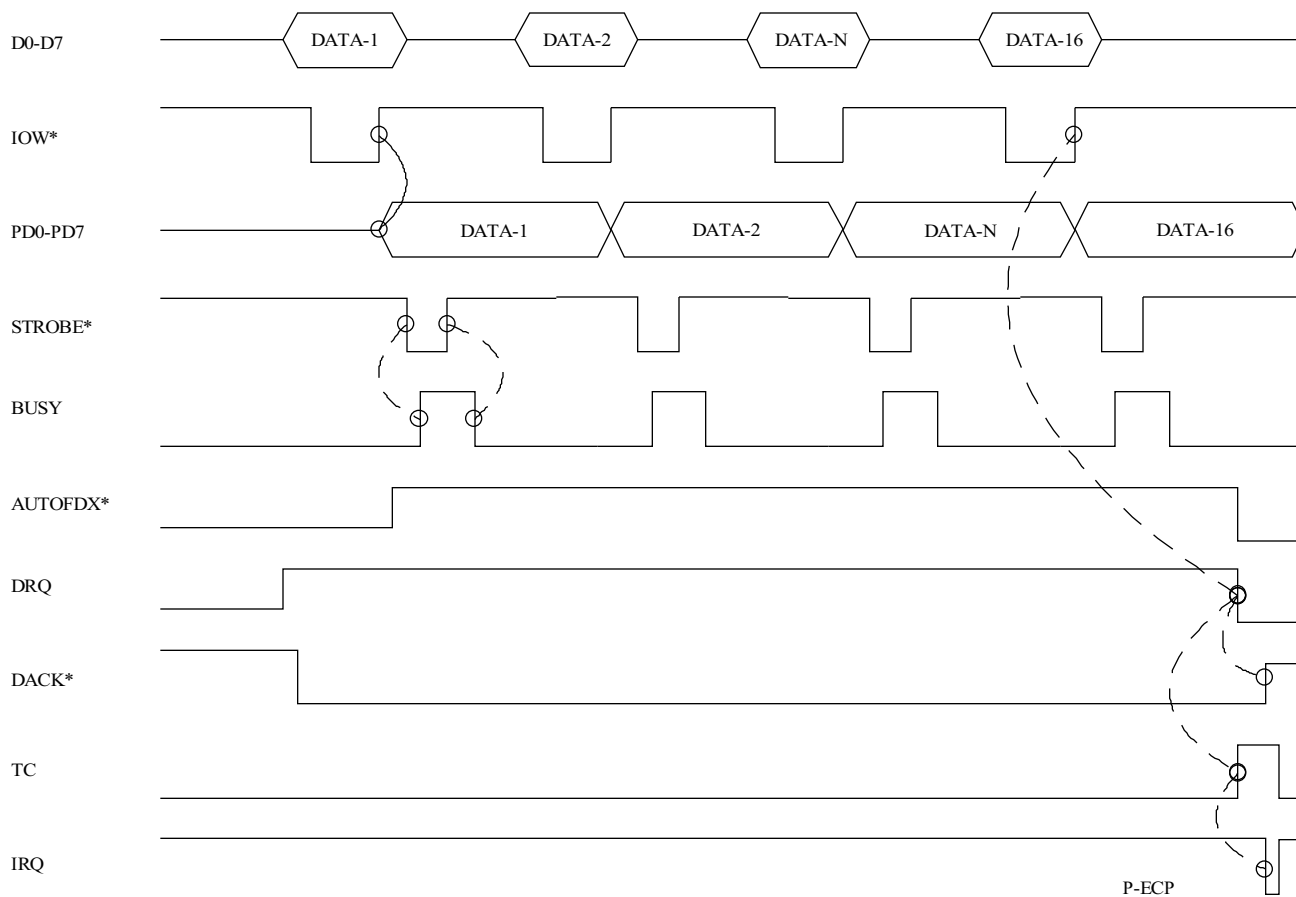|	
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

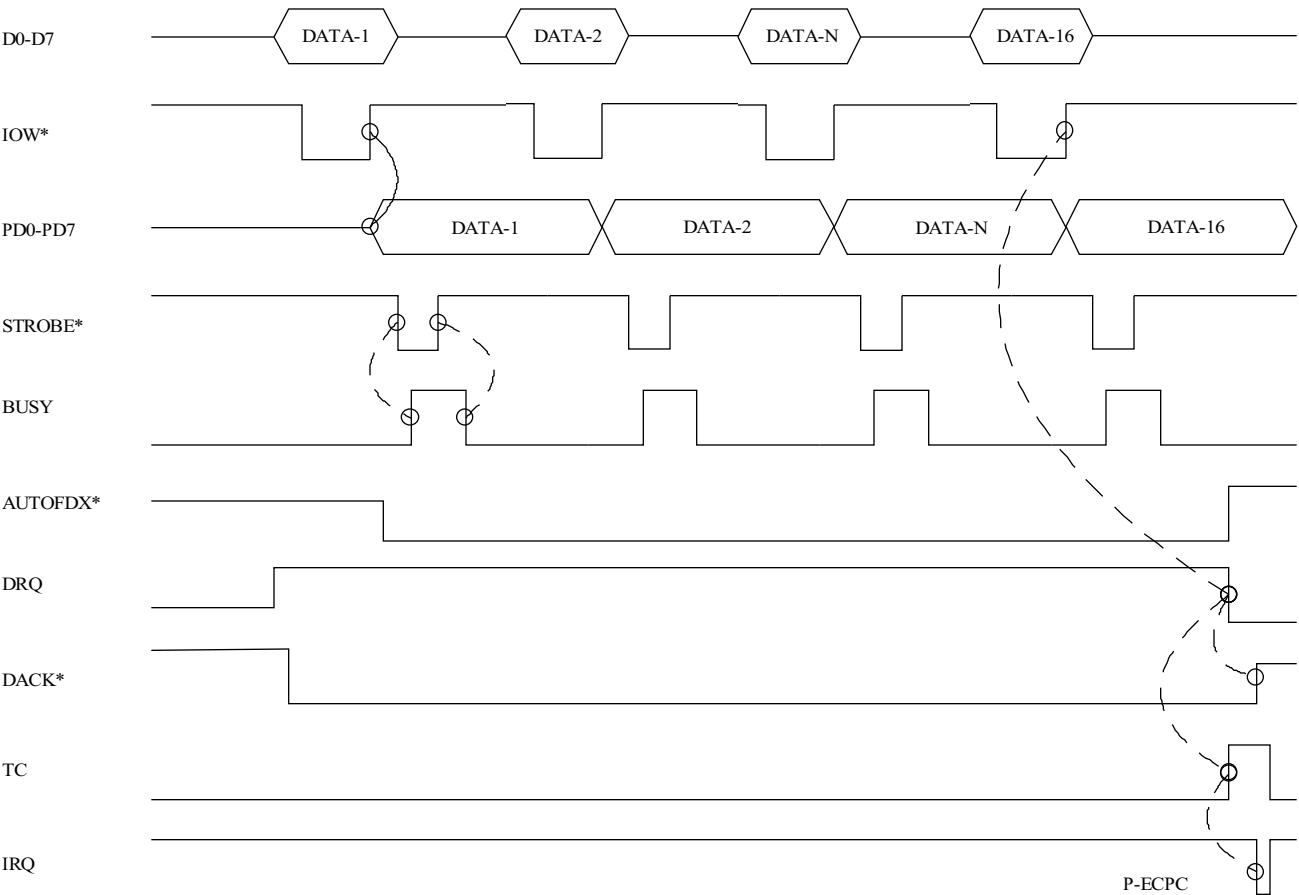| Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
VILCK	Clock Input Low level	-0.5		0.6	V	
VIHCK	Clock Input High level	3.0		VCC	V	
VIL	Input Low level	-0.5		0.8	V	
VIH	Input High level	2.0		VCC	V	
VOL	Output Low level			0.4	V	Except PDIR, D0-D7 IOL=20 mA
VOL PDIR	Output Low level IOL=4 mA			0.4	V	D0-D7, IOL=12 mA
VOH	Output High level	2.4			V	Except PDIR, D0-D7 IOH=-20 mA
VOH PDIR	Output High level IOH=-1 mA	2.4			V	D0-D7, IOL=-12mA
ICC	Avg. power supply current		5	7	mA	
IIL	Input leakage			10	μA	
ICL	Clock leakage			10	μA	
R$_{IN}$	Internal pull up/down resistance	25		50	kΩ	®Marked pins

NOTE: Hewlett Packard / Microsoft compliance testing requires all ECP mode drivers to be push-pull and that they have an impedance controlled series resistor of at least 20 Ohms and that the typical on resistance of the combination of the driver-resistor pair is in the 45-65 Ohm range.

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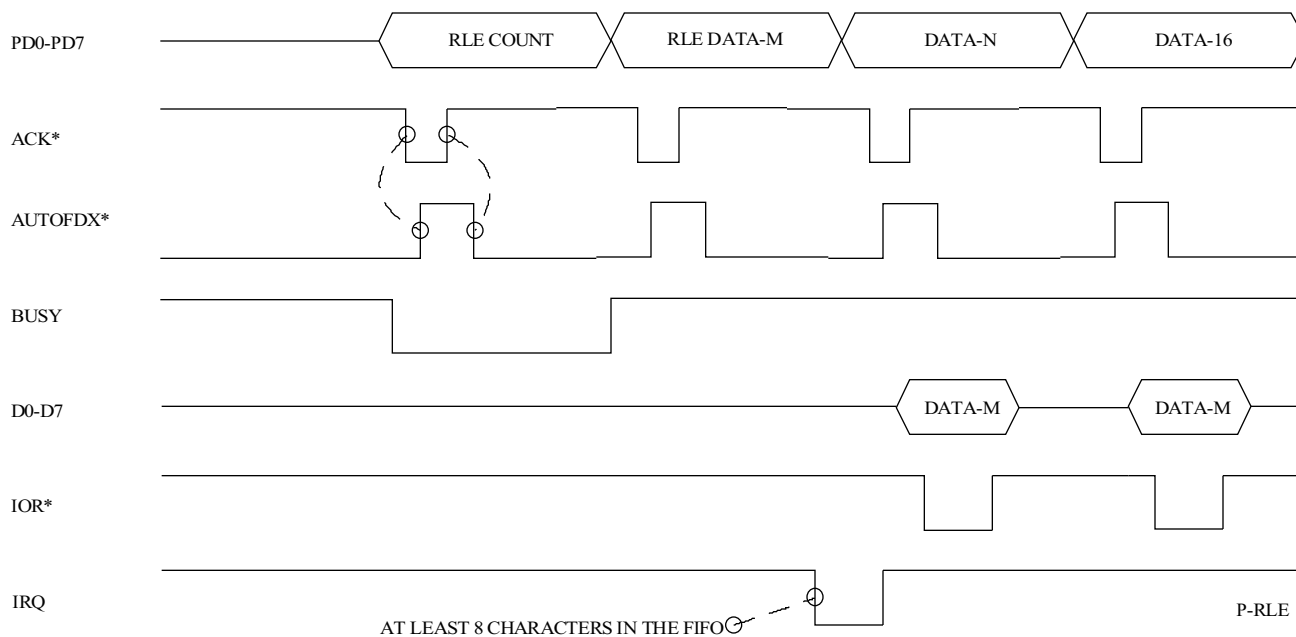ECP MODE (MODE 011, DATA MODE OPERATION, OUTPUT DIRECTION)

4-42

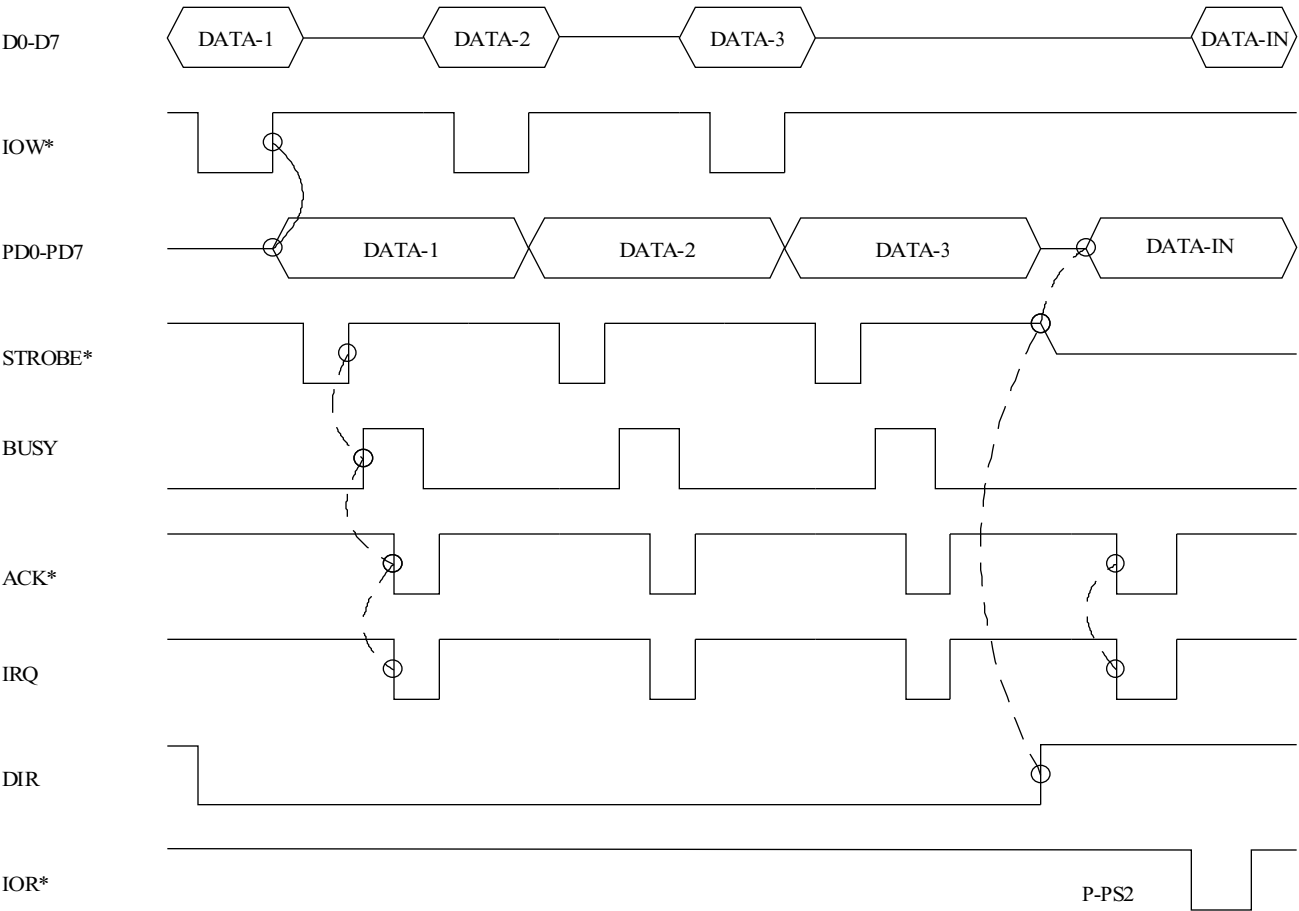ECP MODE (MODE 011, COMMAND MODE OPERATION OUTPUT DIRECTION)

| D0-D7 | DATA-1 | DATA-2 | DATA-N | DATA-16 |

IOW*

PD0-PD7 | DATA-1 | DATA-2 | DATA-N | DATA-16 |

STROBE*

BUSY

AUTOFDX*

DRQ

DACK*

TC

IRQ

P-ECPC

ECP MODE (MODE 011, DATA DECOMPRESSION, INPUT DIRECTION)

PD0-PD7	RLE COUNT	RLE DATA-M	DATA-N	DATA-16

ACK*

AUTOFDX*

BUSY

D0-D7	DATA-M	DATA-M

IOR*

IRQ

AT LEAST 8 CHARACTERS IN THE FIFO   P-RLE

PS2 MODE (MODE 001)

| D0-D7 | DATA-1 | DATA-2 | DATA-3 | DATA-IN |

IOW*

PD0-PD7   DATA-1   DATA-2   DATA-3   DATA-IN

STROBE*

BUSY

ACK*

IRQ

DIR

IOR*

P-PS2

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PPF MODE (MODE 000, FIFO'S ARE SET FOR OUTPUT DIRECTION ONLY)

EPP MODE (MODE 100 , WRITE ADDRESS , OUTMODE)

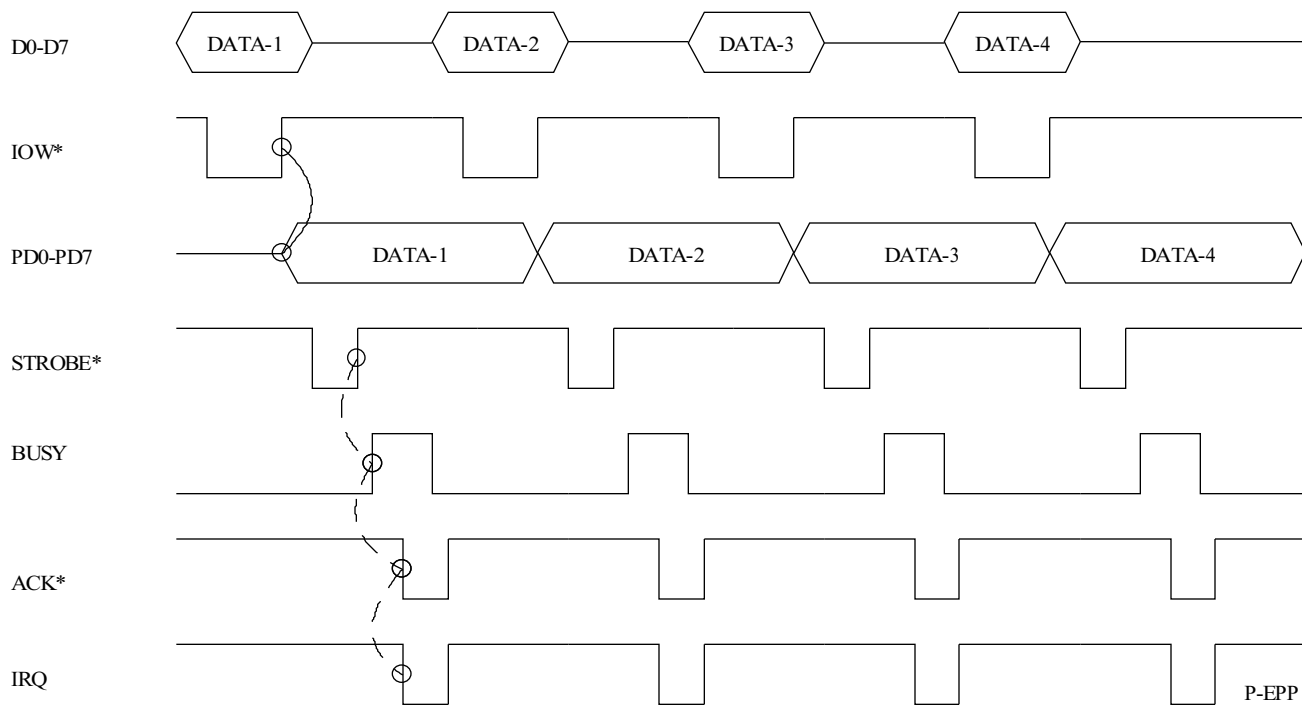
SLCTIN*

PD0-PD7 — DATA-1 — DATA-2

STROBE*

BUSY

D0-D7 — DATA-1 — DATA-2

IOW*
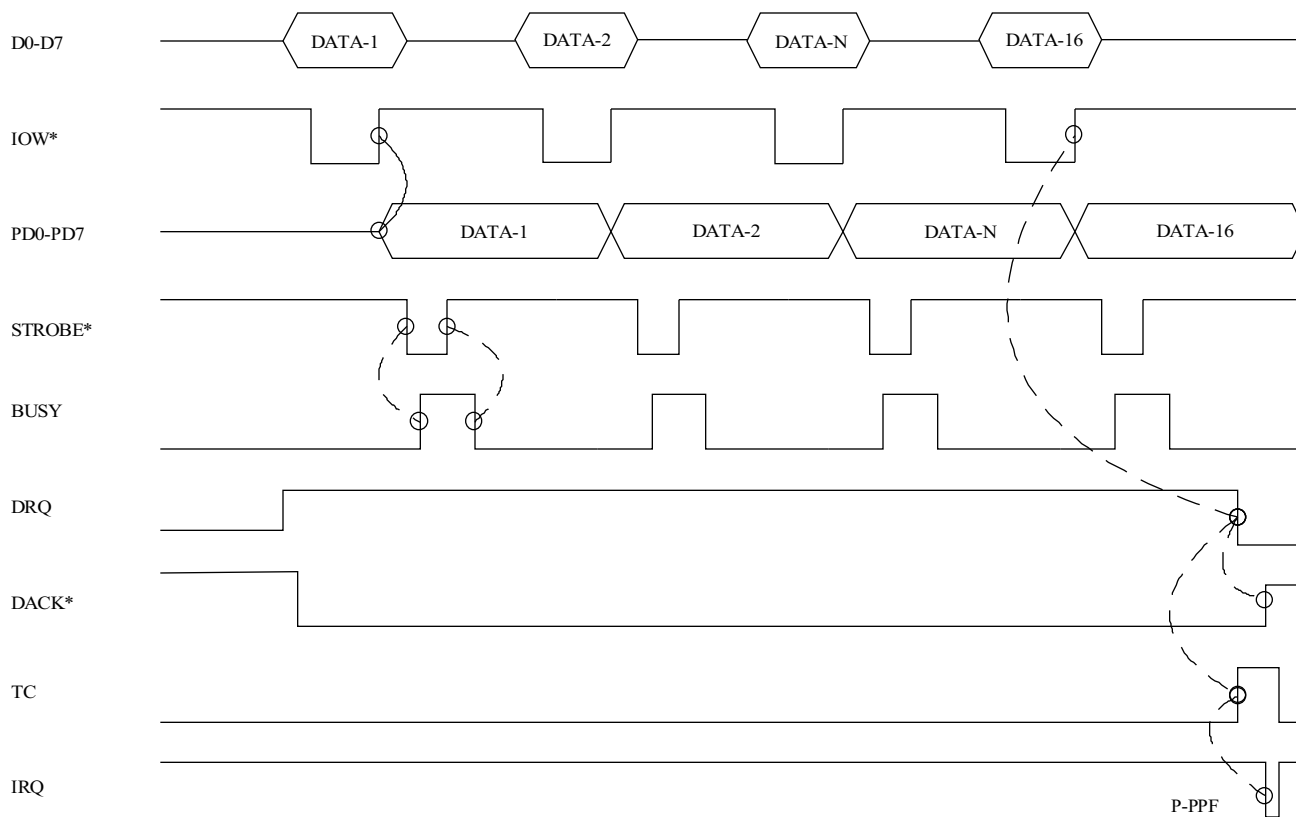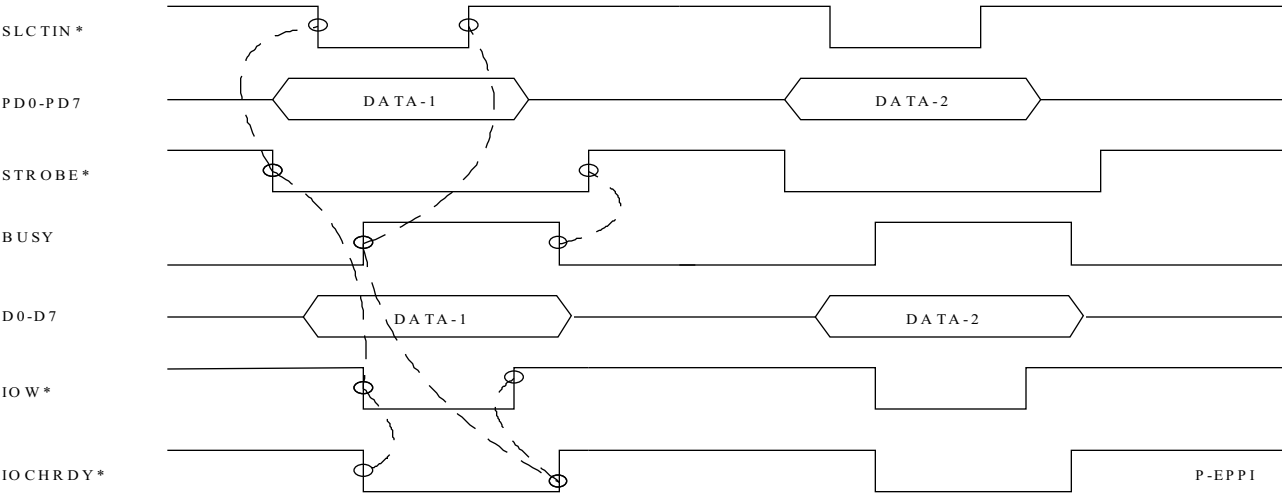
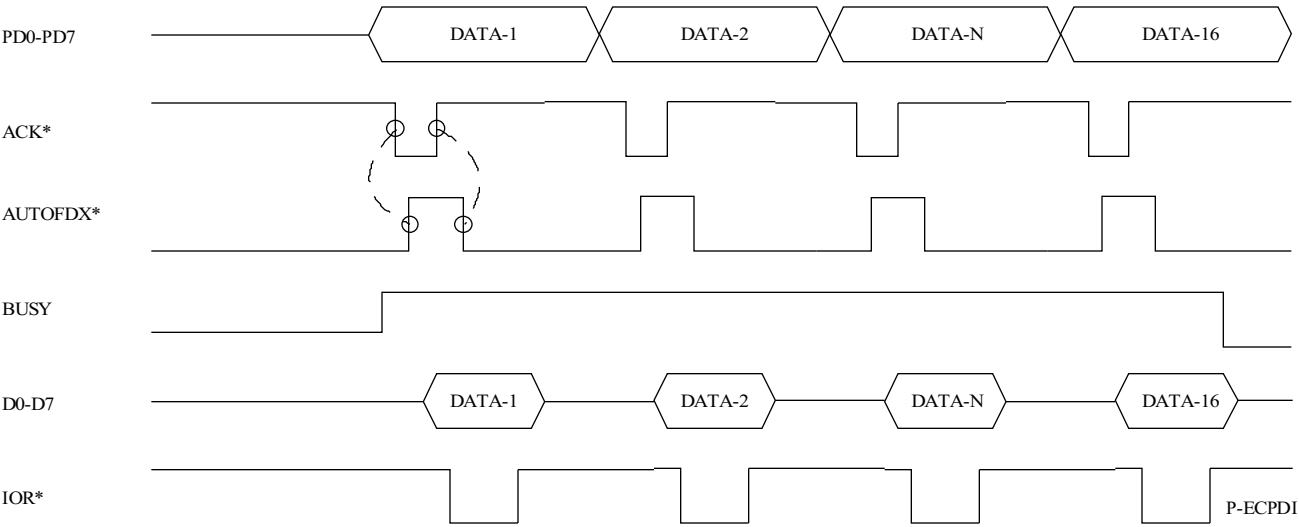IOCHRDY*   P-EPP1

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STANDARD CENTRONIC MODE (MODE 000)

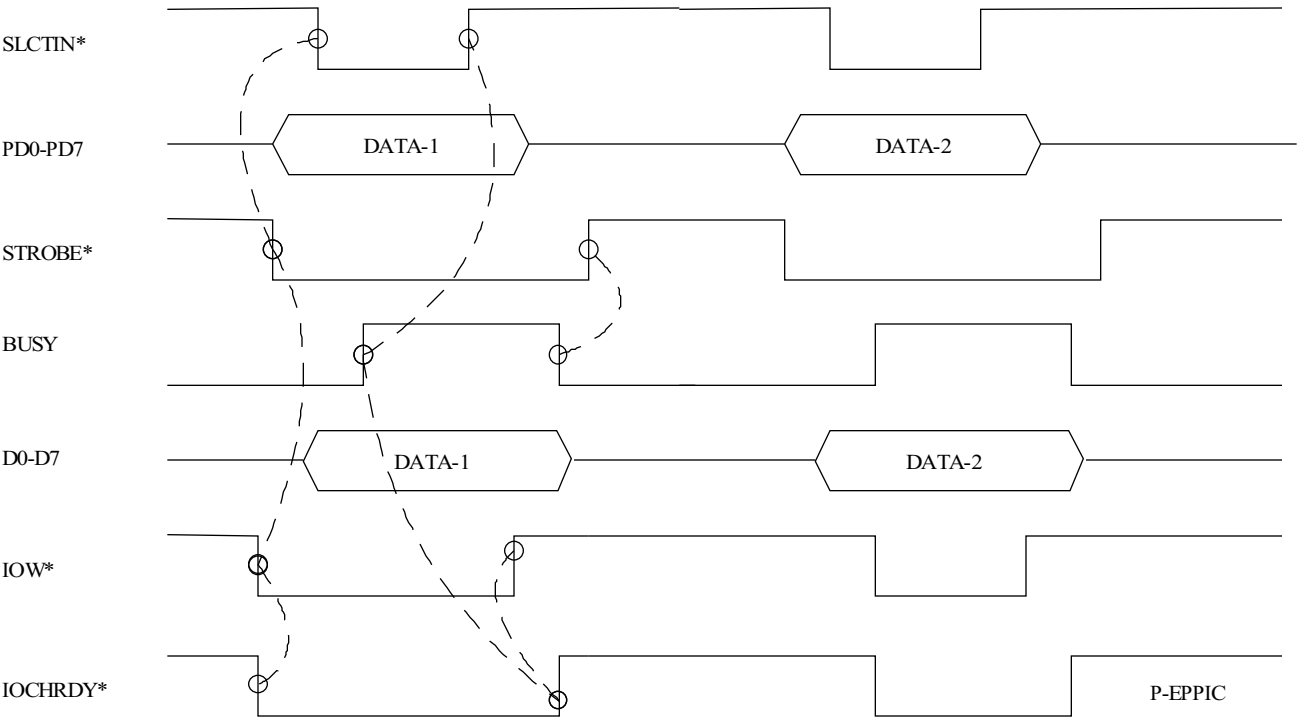ECP MODE (MODE 011, DATA MODE OPERATION INPUT DIRECTION)
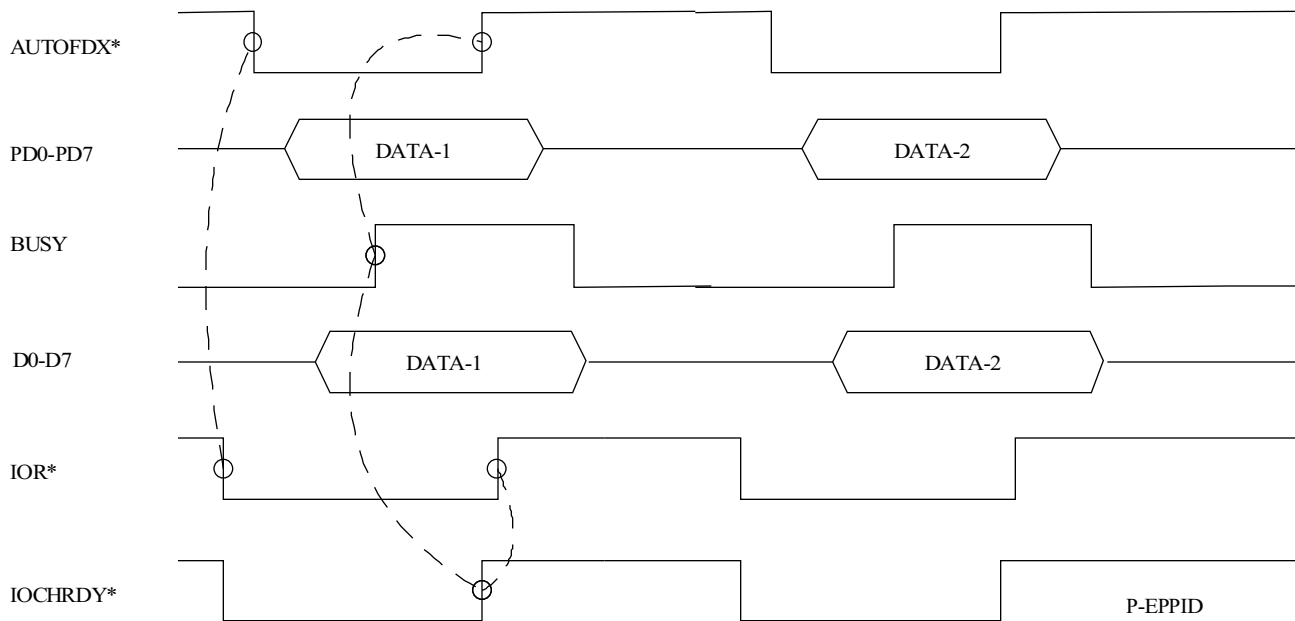

P-ECPDI

EPP MODE (MODE 100, WRITE DATA, OUTMODE)

AUTOFDX*

PD0-PD7   DATA-1   DATA-2

STROBE*

BUSY

D0-D7   DATA-1   DATA-2

IOW*
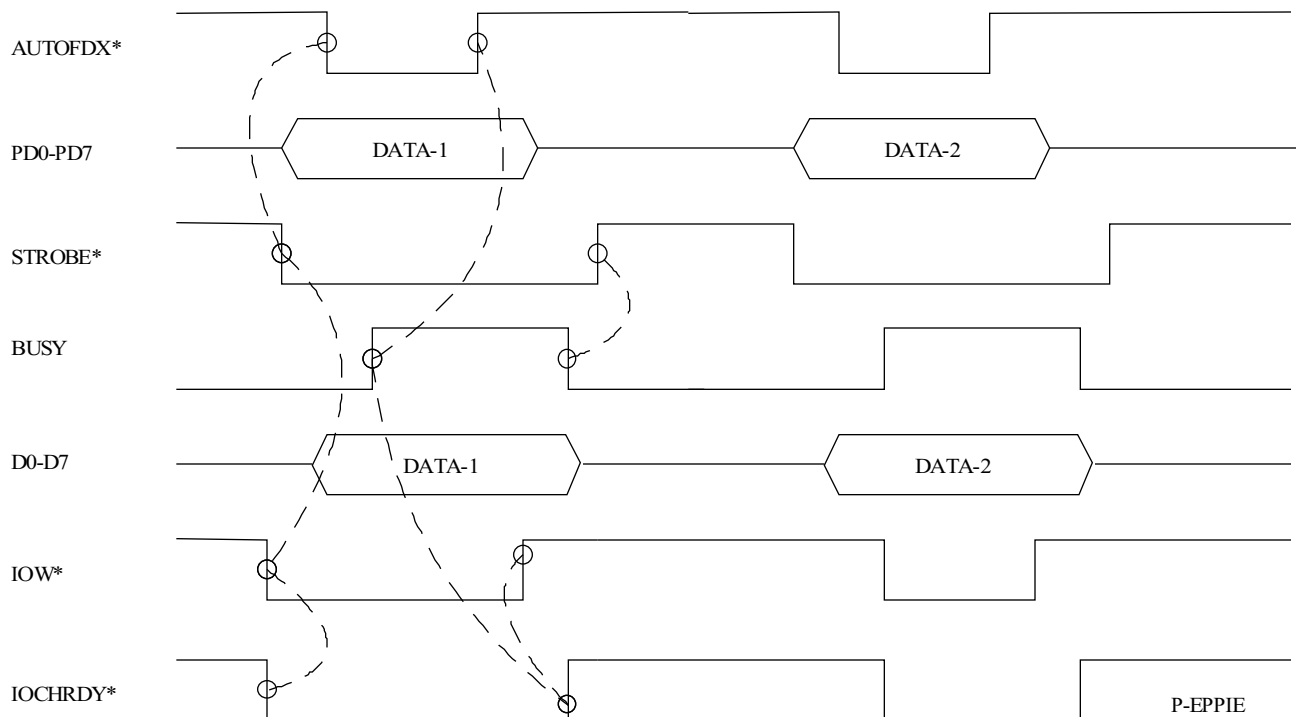
IOCHRDY*   P-EPPIE

EPP MODE (MODE 100, WRITE ADDRESS, OUTMODE)

P-EPPIC

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EPP MODE (MODE 100, DATA READ, INPUT MODE)

Signal	Waveform
AUTOFDX*	
PD0-PD7	DATA-1 DATA-2
BUSY	
D0-D7	DATA-1 DATA-2
IOR*	
IOCHRDY*	P-EPPID

EPP MODE (MODE 100, ADDRESS READ, INPUT MODE)

SLCTIN*

PD0-PD7

BUSY

D0-D7

IOR*

IOCHRDY*

DATA-1

DATA-2

P-EPPIA