ST49C159-14

Frequency Generator/Buffer for PC Motherboards

August 1996-4

FEATURES

- Four Copies of CPU Clock (Selectable 50, 55, 60 or 66 MHz)
- Six Copies of Bus Clock (Sync. CPU Clock/2)
- One Disk Controller Clock @ 24 MHz
- One USB Clock @ 48 MHz
- Two Copies of Reference Clock @ 14.31818 MHz
- Synchronous Clocks Skew Less Than ±250 ps
- Reference 14.31818 MHz Xtal Oscillator
- Glitch-free Clock Start/Stop
- 3V to 5.5V Power Supply Range
- 28 pin SOIC or SSOP Package

GENERAL DESCRIPTION

The ST49C159-14 is a frequency generator designed to satisfy the multiple frequency clock needs of Pentium™ based motherboards. The ST49C159-14 is optimized for use with the Intel Triton™ Pentium™ platforms with USB support. It also satisfies the clocking requirements of may popular RISC and CISC processor system configurations including 486, Pentium, and Power PC™. EXAR has designed the ST49C159-14 to be easily customized for other customer system configurations.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
ST49C159CT28-14	28 Lead 5.3 mm SSOP	0°C to +70°C
ST49C159CF28-14	28 Lead 300 Mil Jedec SOIC	0°C to +70°C

BLOCK DIAGRAM

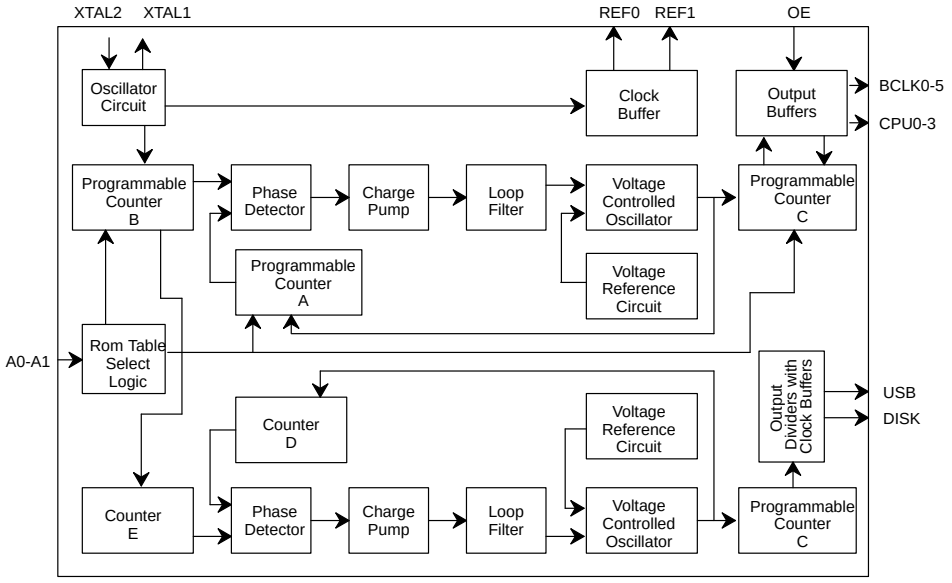

Figure 1. Block Diagram

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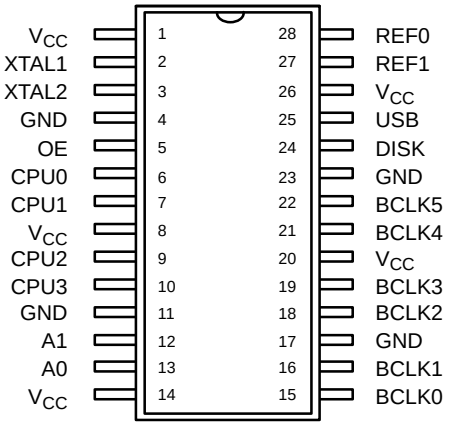
PIN CONFIGURATION



28 Lead SOIC, SSOP (Jedec, 0.300")

PIN DESCRIPTION

Symbol	Pin #	Type	Description
XTAL1	2	O	Crystal or external clock input.
XTAL2	3	I	Crystal output pin.
A0	13[1]	I	CPU clock frequency select address 0.
A1	12[1]	I	CPU clock frequency select address 1.
CPU0-3	6, 7, 9,10	O	Selectable CPU clock output.
BCLK0-5	15,16,18, 19,21,22	O	Selectable Bus clock output.
DISK	24	O	Disk controller clock, 24 MHz clock output.
USB	25	O	USB clock, 48 MHz clock output.
REF0	28	O	14.318 MHz reference clock output.
REF1	27	O	14.318 MHz reference clock output.
OE	5[1]	I	Output enable (active high). Three states outputs when low.
V_{CC}	8,20,26	I	Supply voltage. Single +3 to +5.5 volts.
V_{CC}	1, 14	I	Supply voltage. Single +3 to +5.5 volts.
GND	17, 23	O	Signal ground.
GND	4,11	O	Signal ground.

Notes
[1]Has internal pull-up resistor.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 0 to 70°C, V_{CC} = 3.3 - 5.0V ± 10% Unless Otherwise Specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IL}	Input Low Level			0.8	V	
V_{IH}	Input High Level	2.0			V	
V_{OL}	Output Low Level[1]			0.4	V	I_{OL} = 15 mA, CPU & BCLK
V_{OH}	Output High Level[1]	2.4			V	I_{OH} = -30 mA, CPU & BCLK
V_{OL2}	Output Low Level[1]			0.4	V	I_{OL} = 12.5 mA, Fix Clocks
V_{OH2}	Output High Level[1]	2.4			V	I_{OH} = -20 mA, Fix Clocks
I_{IL}	Input Low Current	-40			µA	Except Pin 2, V_{IN} = 0
I_{IH}	Input High Current			40	µA	Except Pin 2, V_{IN} = V_{CC}
I_{CC}	Operating Current		50	130	mA	No Load @ 66 MHz
R_{IN}	Internal Pull-up Resistance[1]	150	300	600	kΩ	

Notes

[1]Parameters is guaranteed by design and characterization, Not 100% tested in production.

AC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 0 to 70°C, V_{CC} = 3.3V ± 10% Unless Otherwise Specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
	Output Rise Time[1]		0.8	1.7	ns	0.8V - 2.0V, 20pF, PCLK & BCLK
	Output Fall Time[1]		0.7	1.6	ns	2.0V - 0.8V, 20pF, PCLK & BCLK
	Output Rise Time		1.2	2.1	ns	PCLK & BCLK, 20 pF load, 20% to 80%
	Output Fall Time		1.1	2.0	ns	PCLK & BCLK, 20 pF load, 20% to 80%
	Duty Cycle[1, 2]	45	48/52	55	%	1.4V switch point
	Jitter 1 Sigma[1]		±1	±3	%	REF0,1, DISK, USB, load=20 pF
	Jitter Absolute[1]		±2	±5	%	REF0,1, DISK, USB, load=20 pF
	Input Frequency[1]		14.318		MHz	
	Input Clock Rise Time[1]			20	ns	
	Jitter 1 Sigma[1]		50	150	ps	CPU, BCLK, load=20 pF F_{OUT}>20 MHz
	Jitter Absolute[1]	-250		+250	ps	CPU, BCLK, load= 20 pF F_{OUT}>20 MHz
	Clock Skew Between CPU Outputs[1]		100	±250	ps	1.4V switch point, load=20 pF
	Clock Skew Between BCLK Outputs[1]	-500		+500	ps	1.4V switch point, load=20 pF
	Clock Skew Between CPU and BCLK (CPU Ahead)[1]	1	2.5	5	ns	1.4V switch point, load=20 pF

Notes

[1] Parameters is guaranteed by design and characterization, Not 100% tested in production.

[2] Except buffer clock which is 40%–60%.

AC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 0 to 70°C, V_{CC} = 5.0V ± 10% Unless Otherwise Specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
	Output Rise Time[1]		0.55	1.1	ns	0.8V - 2.0V, 20pF, PCLK & BCLK
	Output Fall Time[1]		0.5	1.0	ns	2.0V - 0.8V, 20pF, PCLK & BCLK
	Output Rise Time		1.2	2.1	ns	PCLK & BCLK, 20 pF load, 20% to 80%
	Output Fall Time		1.1	2.0	ns	PCLK & BCLK, 20 pF load, 20% to 80%
	Duty Cycle[1, 2]	45	48/52	55	%	1.4V switch point
	Jitter 1 Sigma[1]		±1	±3	%	REF0,1, DISK, USB, load=20 pF
	Jitter Absolute[1]		±2	±5	%	REF0,1, DISK, USB, load=20 pF
	Input Frequency[1]		14.318		MHz	
	Input Clock Rise Time[1]			20	ns	
	Jitter 1 Sigma[1]		50	150	ps	CPU, BCLK, load=20 pF F_{OUT}>20 MHz
	Jitter Absolute[1]	-250		+250	ps	CPU, BCLK, load= 20 pF F_{OUT}>20 MHz
	Clock Skew Between CPU Outputs[1]		100	±250	ps	1.4V switch point, load=20 pF
	Clock Skew Between BCLK Outputs[1]	-500		+500	ps	1.4V switch point, load=20 pF
	Clock Skew Between CPU and BCLK (CPU Ahead)[1]	1	2.5	5	ns	1.4V switch point, load=20 pF

Notes

[1] Parameters is guaranteed by design and characterization, Not 100% tested in production.

[2] Except reference clock which is 40%–60%.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . 7 Volts
Voltage at Any Pin . . . . . GND-0.3V to V_{CC} +0.3V
Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -40°C to +150°C
Package Dissipation . . . . . 500 mW

ST49C159-14 ACTUAL OUTPUT FREQUENCIES (Using 14.318 MHz Input. All Frequencies in MHz).

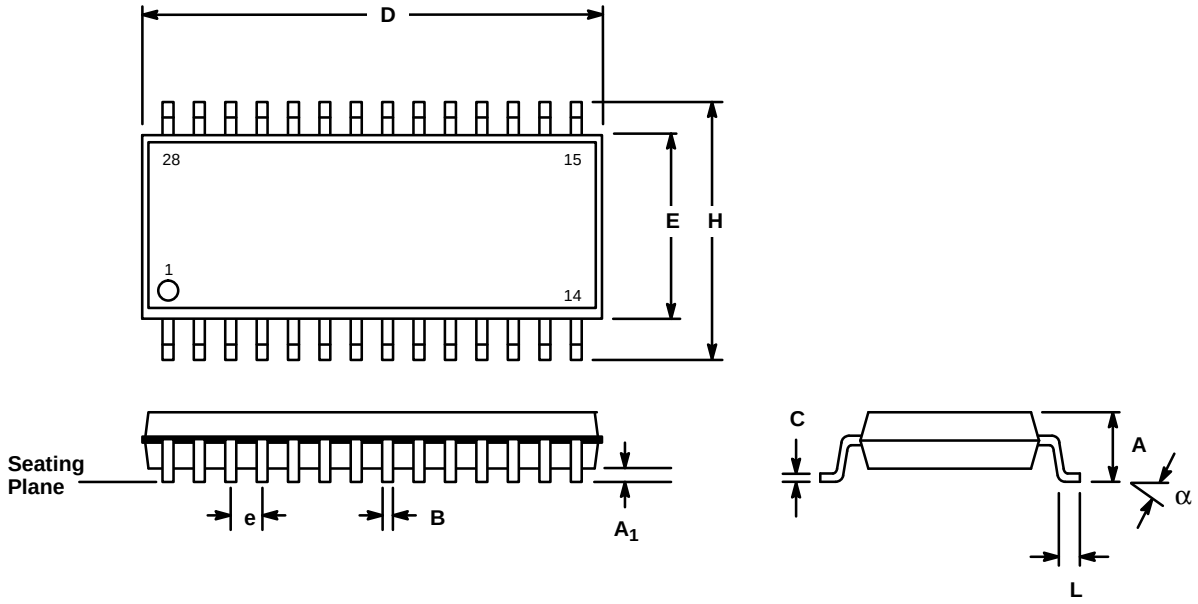
A1	A0	CPU 0-3	BCLK 0-5	REF 0-1	USB	DISK
0	0	50	25	14.3	48	24
0	1	66	33	14.3	48	24
1	0	60	30	14.3	48	24
1	1	55	27.5	14.3	48	24

FREQUENCY TRANSITIONS

The ST49C159-14 is designed to provide smooth, glitch-free frequency transitions on the CPU and BCLK clocks when the frequency select pins are changed.

28 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)

Rev. 1.00

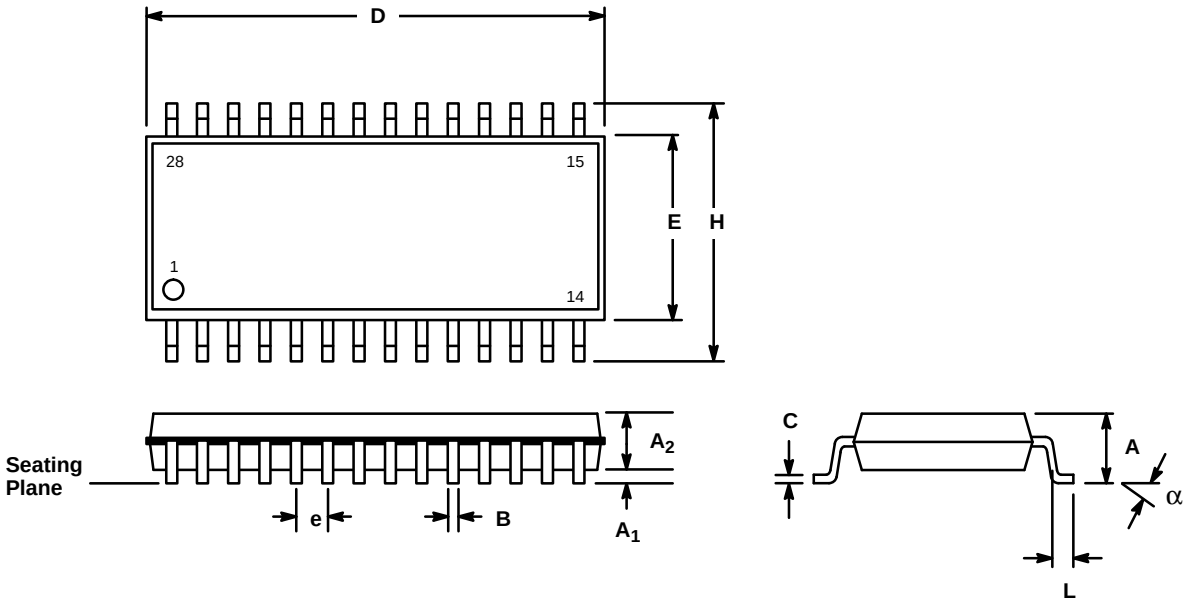


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.697	0.713	17.70	18.10
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

28 LEAD SHRINK SMALL OUTLINE PACKAGE (5.3 mm SSOP)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.066	0.084	1.67	2.13
A_1	0.002	0.010	0.05	0.25
A_2	0.064	0.074	1.62	1.88
B	0.009	0.015	0.22	0.38
C	0.004	0.008	0.09	0.20
D	0.390	0.414	9.90	10.50
E	0.197	0.221	5.00	5.60
e	0.0256 BSC		0.65 BSC	
H	0.292	0.323	7.40	8.20
L	0.025	0.041	0.63	1.03
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

NOTICE

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