ST49C101

Preprogrammed High Speed Frequency Multiplier

July 1996-4

FEATURES

- Can replace expensive high frequency oscillator
- Mask programmable analog phase locked loop
- Low power single 5V CMOS technology
- 8 pin DIP or SOIC package
- Crystal oscillator circuit on board

GENERAL DESCRIPTION

The ST49C101 is a mask programmable monolithic analog CMOS device, designed to replace existing high frequency crystal/oscillator with single low frequency crystal. The ST49C101 provides high speed and low jitter clock output.

ST49C101 is designed in a CMOS state-of-the-art process to achieve 110 MHz speed for high end frequencies.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
ST49C101CP8	8 Lead 300 Mil PDIP	0°C to 70°C
ST49C101CF8	8 Lead 150 Mil Jedec SOIC	0°C to 70°C

BLOCK DIAGRAM

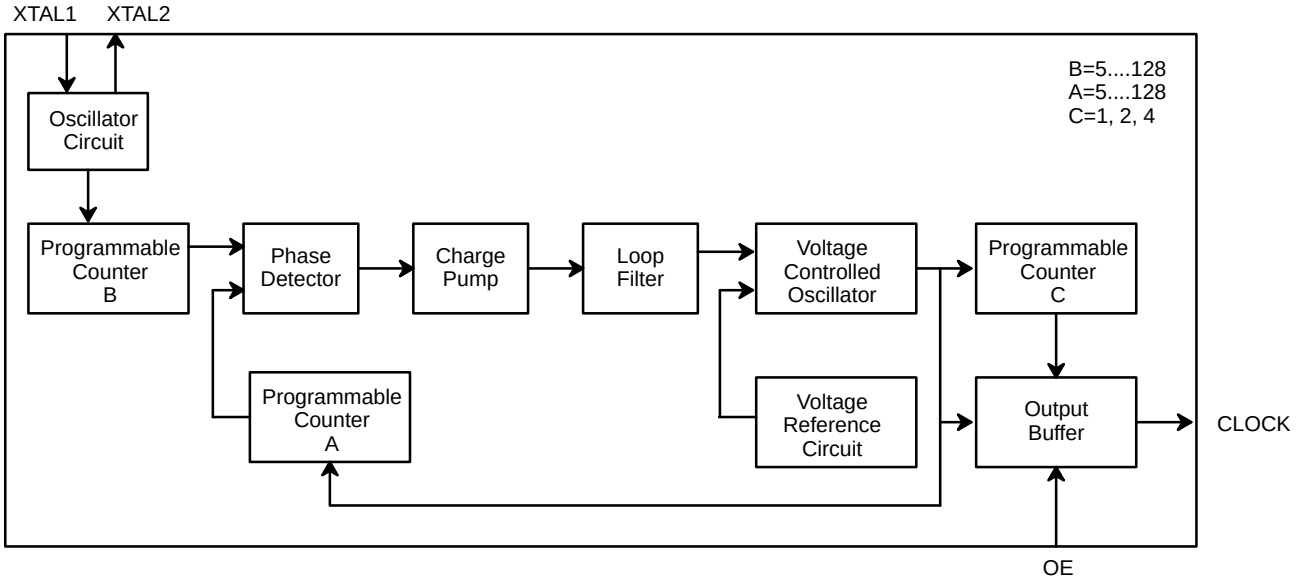
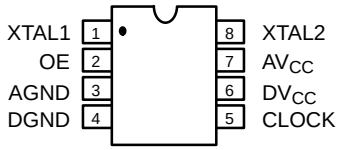


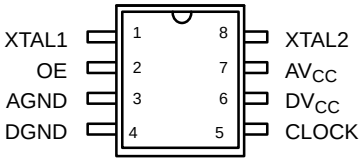
Figure 1. Block Diagram

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017

PIN CONFIGURATION



8 Lead PDIP (0.300”)



8 Pin SOIC (Jedec, 0.150”)

PIN DESCRIPTION (ST49C101)

Pin #	Symbol	Type	Description
1	XTAL1	I	Crystal or External Clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external clock, XTAL2 is left open or used as buffered clock output.
2*	OE	I	Clock Output Enable (Active high). CLOCK output is three stated when this pin is low.
3	AGND	O	Analog ground.
4	DGND	O	Digital ground.
5	CLOCK	O	Programmed output clock.
6	DV_{CC}	I	Positive supply voltage. Single +5 volts.
7	AV_{CC}	I	Analog supply voltage. Single +5 volts.
8	XTAL2	O	Crystal output.

** Has internal pull-up resistor*

DC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 0 to 70°C, V_{CC} = 5.0V ± 10% Unless Otherwise Specified

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.5	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.8			V	I_{OH} = 8.0 mA
I_{IL}	Input low current			-100	µA	Pin 2 only
I_{IH}	Input high current			1	µA	V_{IN}=V_{CC} Pin 2
I_{CC}	Operating current		55	65	mA	No load. CLOCK=100MHz
R_{IN}	Input pull-up resistance	50	75	100	kΩ	

AC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 0 to 70°C, V_{CC} = 5.0V ± 10% Unless Otherwise Specified

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
$T_{1,2}$	CLOCK rise/fall time		1.5	3	ns	Load=30 pF, 0.6V - 2.2V
T_4	Duty cycle	40	48/52	60	%	1.4V switch point
T_5	Duty cycle	45	48/52	55	%	V_{CC}/2 switch point
T_3	Jitter 1 sigma		±0.5	±2	%	
T_3	Jitter absolute		±2	±5	%	
T_{IN}	Input reference frequency	7	10	25	MHz	
T_{OUT}	Output frequency			110	MHz	

DC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 0 to 70°C, V_{CC} = 3.0V ± 10% Unless Otherwise Specified

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.5	V	I_{OL} = 4.0 mA
V_{OH}	Output high level	2.0			V	I_{OH} = 4.0 mA
I_{IL}	Input low current			-100	µA	Pin 2 only
II_H	Input high current			1	µA	V_{IN}=V_{CC} Pin 2
I_{CC}	Operating current		40	60	mA	No load. CLOCK=80 MHz
R_{IN}	Input pull-up resistance	50	75	100	kΩ	

AC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 0 to 70°C, V_{CC} = 3.0V ± 10% Unless Otherwise Specified

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
$T_{1,2}$	CLOCK rise/fall time		2	3	ns	Load 30pF, 0.6V - 2.2V
T_5	Duty cycle	45	48/52	55	%	V_{CC}/2 switch point
T_3	Jitter 1 sigma		±0.5	±2	%	
T_3	Jitter absolute		±2	±5	%	
T_{IN}	Input reference frequency	7	10	20	MHz	
T_{OUT}	Output frequency			80	MHz	

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Supply Range . . . . . 7 Volts
Voltage at Any Pin . . . . . GND-0.3V to V_{CC} +0.3V

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -40°C to +150°C
Package Dissipation . . . . . 500 mW

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup, it is recommended to connect 0.047µF capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C101 contains an analog phase locked loop circuit with digital closed loop dividers and a final output divider to achieve the desired dividing ratios for the clock output.

The accuracy of the frequencies produced by the ST49C101 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

$$CLOCK = 2 \cdot \frac{(Reference\ Clock) \cdot A}{B \cdot C}$$

where A=5, 6, 7,.....128
B=5, 6, 7,.....128
C=1,2,4

Preprogrammed Options:

ST49C101-XX	Factor	Max. Output Frequency
ST49C101-01	12	100 MHz
ST49C101-02	6	100 MHz
ST49C101-03	8	110 MHz
ST49C101-04	4	100 MHz

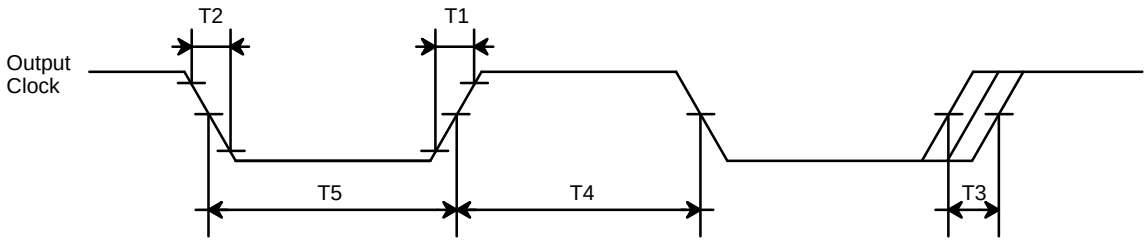
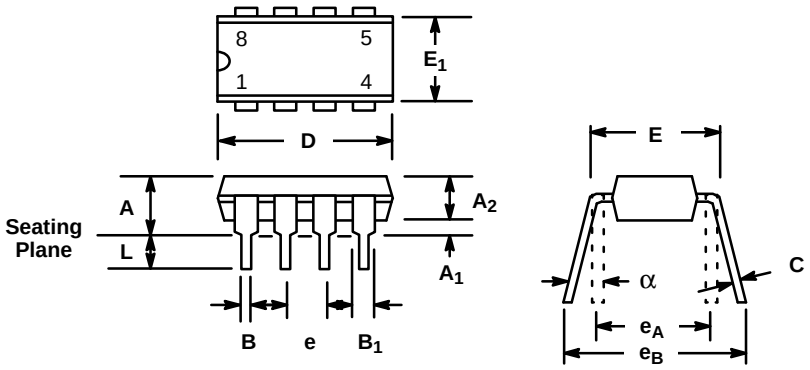


Figure 2. Timing Diagram

8 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

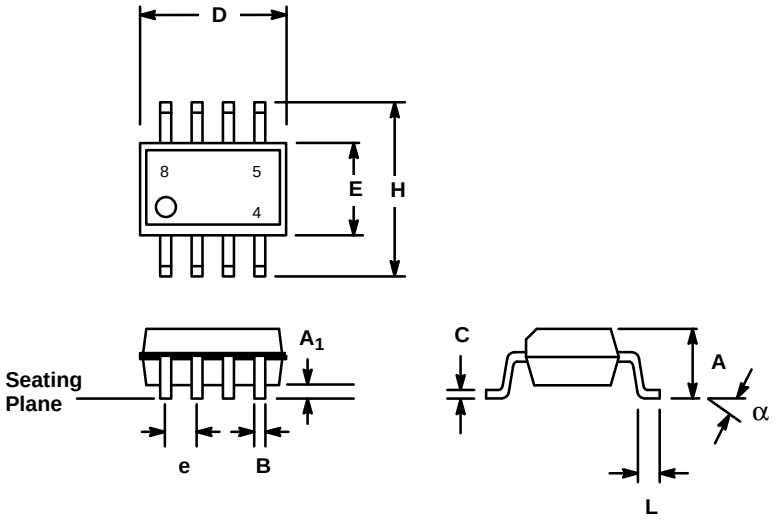


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A_2	0.015	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.348	0.430	8.84	10.92
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

8 LEAD SMALL OUTLINE
(150 MIL JEDEC SOIC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A_1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

NOTICE

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