EXAR ...the analog plus company™

ST49C148-02

Frequency Generator/Buffer for Pentium And Pentium Pro Systems

November 1996-4

FEATURES

- Three Copies of CPU Clock
- Six Copies of Bus Clock
- Four Pin Selectable CPU/BUS Clocks
- Three Copies of Reference Clock
- Metal Mask Adjustable Skew for CPU and BUS Clock (0 ,1 ,2ns)
- 3.3V Power Supply
- Output Disable and PLL Power Down
- Glitch-free Clock Start and Stop
- 28 Pin SSOP

GENERAL DESCRIPTION

The ST49C148-02 is a frequency generator chip designed to address the multiple frequency needs of the Pentium™ and PCI based systems. It offers several copies of CPU and BUS clocks. Using a metal mask change, each of these outputs can be delayed by 0, 1 or 2ns. This feature is very suitable in laptop and notebook applications, where board space and EMI may be reduced by eliminating the need for extending clock traces to match the delays. The ST49C148-02, also, provides three buffered copies of the reference clock. Various output disable and power down features of the chip provide different energy saving options.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
ST49C148CT28-02	28 Lead 5.3 mm SSOP	0°C to +70°C
ST49C148CF28-02	28 Lead 300 Mil JEDEC SOIC	0°C to +70°C

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017

BLOCK DIAGRAM

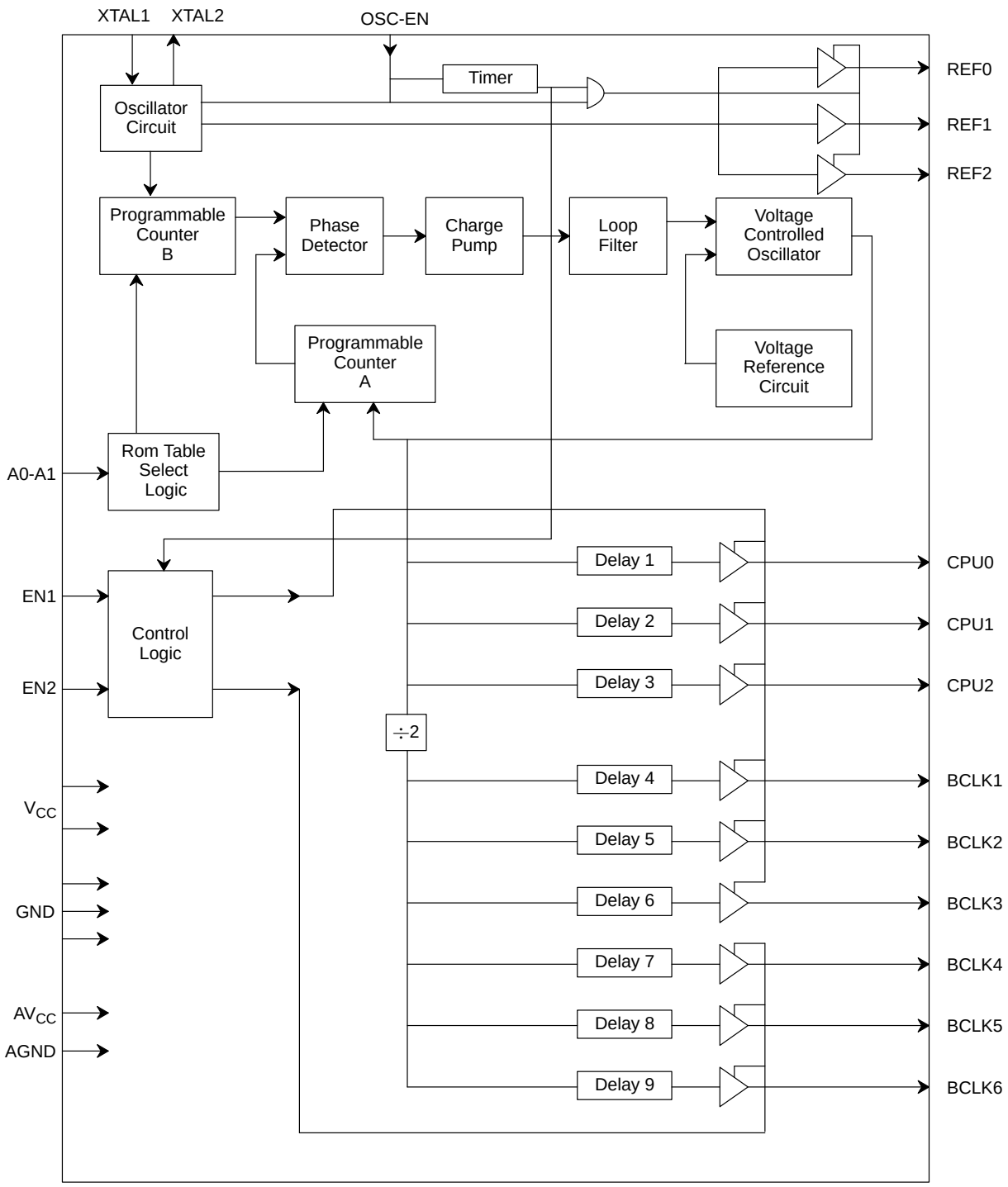
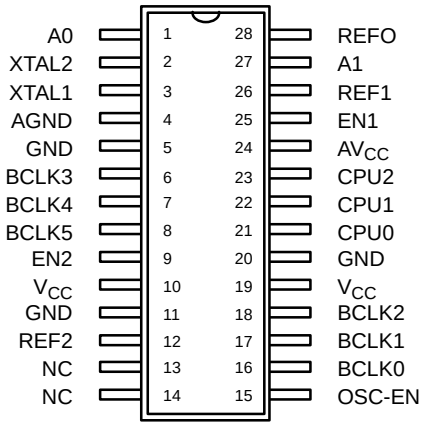


Figure 1. Block Diagram

PIN CONFIGURATION



28 Lead SOIC (Jedec, 0.300")
28 Lead SSOP (5.3 mm)

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	A0	I	CPU and BCLK frequency select address 0.
2	XTAL2	O	Crystal output.
3	XTAL1	I	Crystal input.
4	AGND	O	Ground (analog).
5	GND	O	Ground.
6	BCLK3	O	Selectable bus clock output.
7	BCLK4	O	Selectable bus clock output.
8	BCLK5	O	Selectable bus clock output.
9	EN2	I	BCLK3-5 output enable; active high.
10	V_{CC}	I	Positive supply.
11	GND	O	Ground.
12	REF2	O	14.318MHz reference clock.
13	NC		No connects.
14	NC		No connects.
15	OSC-EN	I	Crystal oscillator enable; active high.
16	BCLK0	O	Selectable bus clock output.
17	BCLK1	O	Selectable bus clock output.
18	BCLK2	O	Selectable bus clock output.
19	V_{CC}	I	Positive supply.

PIN DESCRIPTION (CONT'D)

Pin #	Symbol	Type	Description
20	GND	O	Ground.
21	CPU0	O	Selectable CPU clock output.
22	CPU1	O	Selectable CPU clock output.
23	CPU2	O	Selectable CPU clock output.
24	AV_{CC}	I	Positive supply (analog).
25	EN1	I	Enables CPU0-2 and BCLK0-2 outputs; active high.
26	REF1	O	14.318MHz reference clock.
27	A1	I	CPU and BCLK frequency select address 1
28	REF0	O	14.318MHz reference clock.

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 0° to 70°C, V_{CC} = 3.3V ±10% Unless Otherwise Specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
DC Electrical Characteristics						
V_{IL}	Input Low Level			0.8	V	
V_{IH}	Input High Level	2.0			V	
I_{IL}	Input Low Current	-40			µA	Except Pin 3, V_{IN}=0
I_{IH}	Input High Current			40	µA	Except Pin 3, V_{IN} = V_{CC}
I_{CC}	Operating Current		35	60	mA	No Load
R_{IN}	Internal Pull-up Resistance[1]	150	300	600	kΩ	
AC Electrical Characteristics						
	Output Rise Time[1]		1.0	2	ns	0.8V - 2.0V, CPU, BCLK, Load=20pF
	Output Fall Time[1]		1	2	ns	2.0V - 0.8V, CPU, BCLK, Load=20pF
	Duty Cycle[1]	45	50	55	%	1.4V Switch Point
	Jitter 1 Sigma[1]		±1	±3	%	REF0-2
	Jitter Absolute[1]		±2	±5	%	REF0-2
	Input Frequency[1]		14.318		MHz	
	Input Clock Rise Time[1]			20	ns	
	Jitter 1 Sigma[1]		50	150	ps	CPU, BCLK, Load=20pF F_{OUT}>20MHz
	Jitter Absolute[1]	-400		+400	ps	CPU, BCLK, Load=20pF
	Clock Skew Between CPU and BCLK Outputs (when all delays are set to “0”)			250	ps	1.4V Switch Point, Load=20pF
	CPU or BCLK Delay Step[1]	0.7	1	1.3	ns	1.4V Switch Point, Load=20pF
T_{PLL}	Delay from PLL Active to Output Enable		1.2	1.4	ms	XTAL Oscillator is Active and Stable
T_{OSC}	Delay from OSC-EN Active to REF0,2 Active		2.3	2.5	ms	Power Supply Stable

Note

[1] Parameters is guaranteed by design and characterization, not 100% tested in production.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 7V
Voltage at any Pin . . . . . GND -0.3V to V_{CC} +0.3V
Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -40°C to +150°C
Package Dissipation 500mW

OUTPUT AND PLL CONTROL PINS

Two pins, EN1 and EN2 , control the output drivers and the PLL per following table:

EN1	EN2	Function
0	0	Disable all of the output buffers, except REF1.
0	1	Tri-state all the outputs.
1	0	Enable the PLL and CPU0-2 and BCLK0-2 drivers, BCLK3-5 disabled.
1	1	All outputs enabled.

Table 1. Output Buffer Control

Every time that PLL is activated, from a power down state, an internal timer will generate a delay of T_{PLL} for PLL to stabilize and then enables the outputs (see *AC Electrical Characteristics Table*). This delay can be adjusted by metal mask. When outputs are disabled or enabled, they make a glitch free transition to their low state or normal clock.

OSCILLATOR CONTROL PIN

To allow further power saving, the crystal oscillator and PLL are controlled by the OSC-EN pin. When crystal oscillator is activated, after being disabled, a metal mask programmable timer on the chip will delay activation of some of the reference clock buffers by T_{OSC} until oscillator is stabilized (see *AC Electrical Characteristics Table*). Other reference clock buffers are activated instantaneously.

The following table summarizes the function of this pin.

OSC-EN	Function
0	Crystal oscillator is disabled and PLL is shut down.
1	Crystal oscillator is enabled and its output buffers are activated simultaneously or after a delay. PLL is powered up.

Table 2. Oscillator and PLL Control

POWER DOWN MODE

Using combinations of EN1, EN2 and OSC-EN pins, different levels of power reductions can be achieved by disabling some of the output drivers, PLL and output drivers, oscillator plus PLL and output drivers.

CPU AND BCLK SKEW

Each CPU and BCLK driver is preceded by a metal mask programmable delay line which allows its individual output to be delayed by 0, 1 or 2nsec. These delays can be used to compensate for the propagation delay mismatches on the board due to trace length variations. This may reduce or eliminate the need for extending the traces on the PC board, for skew adjustment, and consequently saves space and lowers EMI problems.

Clock	Nominal Delay (ns)
CPU0	2
CPU1	2
CPU2	2
BCLK0	2
BCLK1	1
BCLK2	2
BCLK3	0
BCLK4	0
BCLK5	1

Table 3. ST49C148-02 CPU and BCLK Delays

A1	A0	CPU0-2 (Nominal)	BCLK0-5 (Nominal)
0	0	40	20
0	1	50	25
1	0	60	30
1	1	66.66	33.33

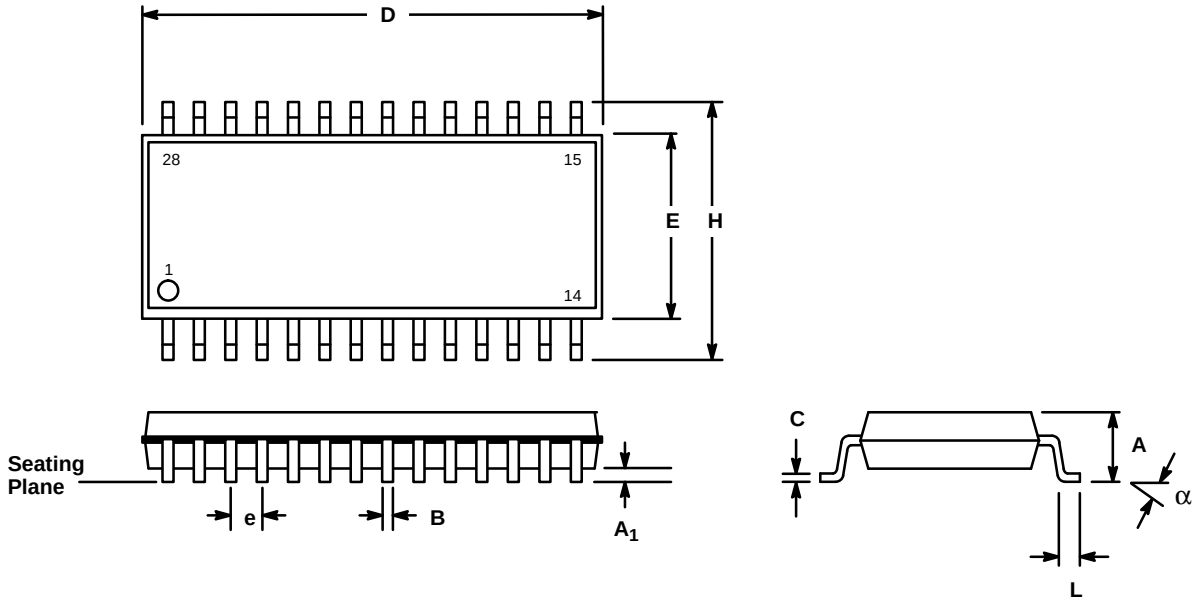
Table 4. ST49C148-02 Output Frequencies Nominal using 14.318MHz input (all frequencies in MHz).

A1	A0	CPU0-2 (Actual)	BCLK0-5 (Actual)
0	0	40.091	20.045
0	1	50.114	25.057
1	0	60.136	30.068
1	1	66.818	33.414

Table 5. ST49C148-02 Output Frequencies Actual using 14.318MHz input (all frequencies in MHz).

28 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)

Rev. 1.00

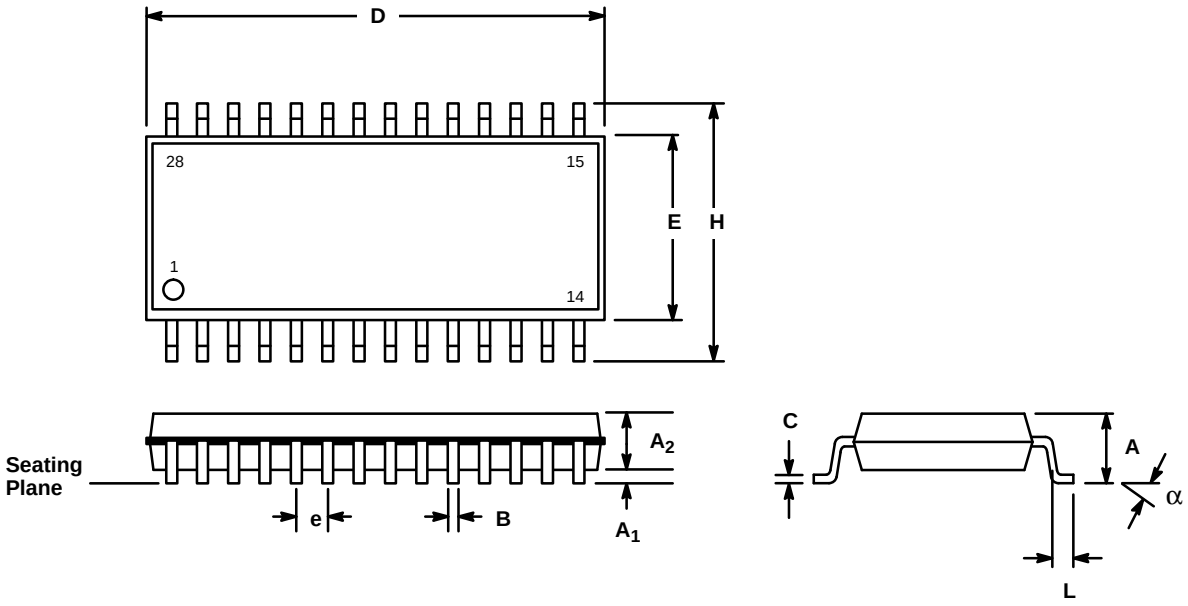


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.697	0.713	17.70	18.10
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

28 LEAD SHRINK SMALL OUTLINE PACKAGE (5.3 mm SSOP)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.066	0.084	1.67	2.13
A_1	0.002	0.010	0.05	0.25
A_2	0.064	0.074	1.62	1.88
B	0.009	0.015	0.22	0.38
C	0.004	0.008	0.09	0.20
D	0.390	0.414	9.90	10.50
E	0.197	0.221	5.00	5.60
e	0.0256 BSC		0.65 BSC	
H	0.292	0.323	7.40	8.20
L	0.025	0.041	0.63	1.03
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

Notes

Notes

Notes

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained herein are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Datasheet November 1996