ST16C452AT
ST16C452PS

STARTECH
An EXAR Company

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DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH PARALLEL PRINTER PORT

DESCRIPTION

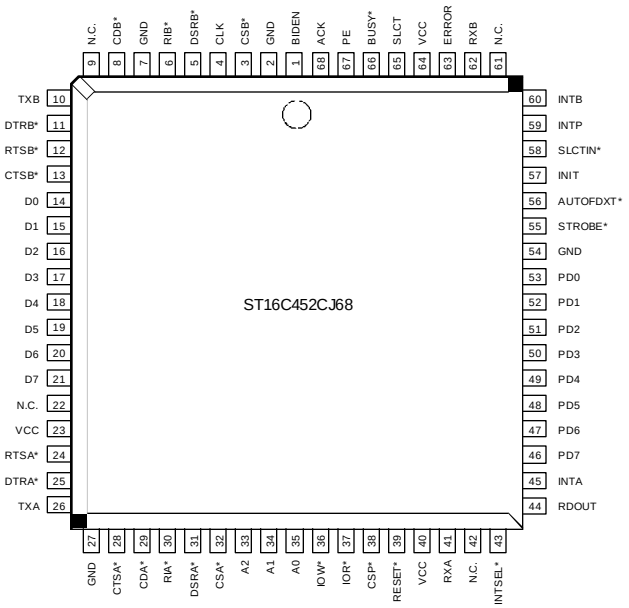
The ST16C452 is a dual universal asynchronous receiver and transmitter with a bi-directional CENTRONICS type parallel printer port. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 1.5 MHz.

STARTECH ST16C452PS provides additional features to control the printer port direction without any additional external logic.

The ST16C452 is an improved version of the VL16C452 UART with higher operating speed and lower access time. The ST16C452 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C452 provides internal loop-back capability for on board diagnostic testing.

The ST16C452 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



FEATURES

- Pin to pin and functional compatible to VL16C452, WD16C452
- Fully compatible with all new bi-directional PS/2 printer port registers.
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Independent transmit and receive control
- Software compatible with INS8250, NS16C450
- 460.8 kHz transmit/receive operation with 7.372 MHz crystal or external clock source.
- Bi-directional hardware/software parallel port
- Bi-directional I/O ports

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C452CJ68	PLCC	0° C to + 70° C
ST16C452IJ68	PLCC	-40° C to + 85° C

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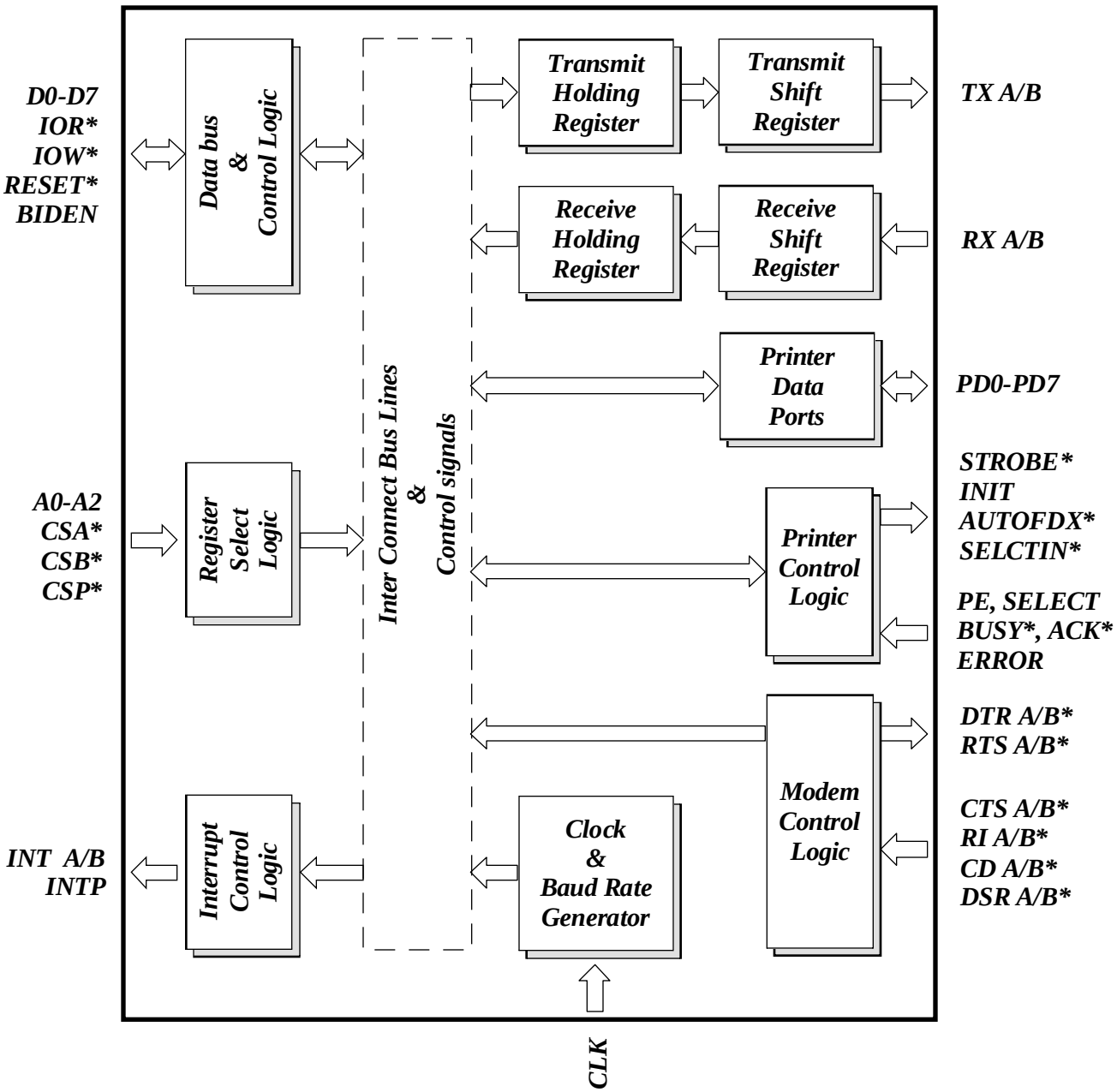
BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	14-21	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
A0-A2	35-33	I	Address select lines. To select internal registers.
CLK	4	I	Clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
BIDEN	1	I	Printer direction select. A high puts the parallel port in the input mode for ST16C452AT and software controlled mode (input/output) to ST16C452PS. Allow sets the ST16C452 to output mode.
IOW*	36	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	37	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C452 data bus to the CPU.
RDOUT	44	O	Read select out (active high). This pin goes high when the CPU is reading data from the ST16C452 to en/disable the external transceiver or logic's.
RESET*	39	I	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CS* A/B	32,3	I	Chip select A/B (active low). A low at this pin enables the serial port-A/B / CPU data transfer operation.
DSR* A/B	31,5	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
RI* A/B	30,6	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			telephone line.
CD* A/B	29,8	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
TX A/B	26,10	O	Serial data output A/B. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
DTR* A/B	25,11	O	Data terminal ready A/B (active low). To indicate that ST16C452 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RTS* A/B	24,12	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
RX A/B	41,62	I	Serial data input A/B. The serial information (data) received from serial port to ST16C452 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
CTS* A/B	28,13	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
INT A/B	45,60	O	Interrupt output A/B (three state active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CSP*	38	I	Parallel printer port chip select (active low). A low at this pin enables the parallel port / CPU data transfer operation.
PD7-PD0	46-53	I/O	Bi-directional parallel ports (three state). To transfer data in or out of the ST16C452 parallel port. PD7-PD0 are latched during output mode.
STROBE*	55®	I/O	General purpose I/O or data strobe output (open drain active low). This output indicates to the printer that valid data is available at the printer port (PD0-PD7).
AUTOFDXT*	56®	I/O	General purpose I/O or automatic line feed (open drain active low). When this signal is low the printer should automatically line feed after each line is printed.
INIT	57®	I/O	General purpose I/O or initialize line printer (open drain active low). When this signal is low it causes the printer to be initializes.
SLCTIN*	58®	I/O	General purpose I/O or line printer select (open drain active low). When this signal is low it selects the printer.
ERROR*	63®	I	General purpose input or line printer error (active low) This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	65®	I	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	66®	I	General purpose input or line printer busy (active high). An output from the printer to indicate printer is not ready to accept data.
PE	67®	I	General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.
ACK*	68®	I	General purpose input or line printer acknowledge (active low). This input is pulsed low by the printer to indicate that data has been accepted successfully.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INTP*	59	O	Printer interrupt output (active low). To signal the state of the printer port. This pin tracks the ACK* input pin, When ACK* is low INTP is low and when ACK* is high INTP is high
INTSEL*	43	I	Interrupt select mode. The external ACK* can be selected as an interrupt source by connecting this pin to the GND. Connecting this pin to VCC will set the interrupt to latched mode, reading the status register of the printer section resets the INTP output.
GND	2,7,22 42,54,61	O	Signal and power ground. All ground pins are connected internally.
VCC	23,40,64	I	Power supply input. All power pins are connected internally.

® Has internal pull-up resistor.

PROGRAMMING TABLE FOR SERIAL PORTS A/B

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C452 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	INT priority bit-1	INT priority bit-0	INT status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to “1”.

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REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C452 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2^{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C452 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C452 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to "0".

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

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MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
This bit is used for internal loop-back mode, and is not used for regular operation.

MCR BIT-3:
0= sets the INT output pin to three state mode.
1= enables the INT output pin.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2,3are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. ST16C452 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used. Set to “0”.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to “1” whenever a control input from the MODEM changes state. They are set to “0” whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C452 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C452 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C452 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C452 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to MCR bit-3 during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic “1”, a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C452 provides a temporary data register to store 8 bits of information for variable use.

SIGNAL	RESET STATE
TX A/B	High
RTS* A/B	High
DTR* A/B	High
INT A/B,P	Three state mode

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C452 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	BITS 0-7=0
ISR	BIT-0=1, ISR BITS 1-7=0
LCR	BITS 0-7=0
MCR	BITS 0-7=0
LSR	BITS 0-4=0,
LSR	BITS 5-6=1 LSR, BIT 7=0
MSR	BITS 0-3=0,
MSR	BITS 4-7=input signals

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PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW*	IOR*
0	0	PORT REGISTER	PORT REGISTER
0	1	I/O SELECT REGISTER	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER

* Reading the status register will reset the INTP output.

PARALLEL PORT DIRECTION SELECT REGISTER (WRITE ONLY)

ST16C452XX	CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER	PORT DIRECTION
ST16C452AT	X	0	X	Output mode
ST16C452PS	X	0	AA Hex	Input mode
ST16C452PS	X	0	55 Hex	Output mode
ST16C452AT	X	1	X	Input mode
ST16C452PS	0	1	X	Output mode
ST16C452PS	1	1	X	Input mode

PRINTER PORTREGISTER DESCRIPTIONS

PORT REGISTER

Bi-directional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports. Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:
PD7-PD0 bi-directional I/O ports.

STATUS REGISTER

This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to “1” permanently.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to “0” at the falling edge of the ACK* input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to “1”.

SR BIT-3:
ERROR* input state.
0= ERROR* input is in low state
1= ERROR* input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK* input state.
0= ACK* input is in low state
1= ACK* input is in high state

SR BIT-7:
BUSY input state.
0= BUSY input is in high state
1= BUSY input is in low state

COMMAND REGISTER

The state of the STROBE*, AUTOFDXT*, INIT, SLCTIN* pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE* input pin.
0= STROBE* pin is in high state
1= STROBE* pin is in low state

COM BIT-1:
AUTOFDXT* input pin.
0= AUTOFDXT* pin is in high state
1= AUTOFDXT* pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN* input pin.
0= SLCTIN* pin is in high state
1= SLCTIN* pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt (INTP output) is disabled
1= Interrupt (INTP output) is enabled

COM BIT 7-5:
Not used. Are set to “1” permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE*, AUTOFDXT*, INIT, SLCTIN pins, and interrupt mask register.

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CON BIT-0:
STROBE* output control bit.
0= STROBE* output is set to high state
1= STROBE* output is set to low state

CON BIT-1:
AUTOFDXT* output control bit.
0= AUTOFDXT* output is set to high state
1= AUTOFDXT* output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:
SLCTIN* output control bit.
0= SLCTIN* output is set to high state
1= SLCTIN* output is set to low state

CON BIT-4:
Interrupt output control bit.
0= INTP output is disabled
1= INTP output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

I/O SELECT REGISTER

Software controlled I/O select.
Bi-directional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one"
Hardware/software I/O select.
Bi-directional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or "55" Hex for output. I/O select register and control register bit-5 are only available for ST16C452PS parts.

ST16C452 EXTERNAL RESET CONDITION

SIGNALS	RESET STATE
PD0-PD7	low, output mode
STROBE*	High, output mode
AUTOFDXT*	High, output mode
INIT	Low, output mode
SLCTIN*	High, output mode

ST16C452 PRINTER PORT REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY*	ACK	PE	SLCT	ERROR	IRQ STATE	1	1
					1= No interrupt 0= Interrupt (PS only)		

COMMAND REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
			0= IRQ disabled 1= IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	I/O SELECT	IRQ MASK	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
	0=Output (PS only) 1=Input (PS only) X= AT only		0=INTP output disabled 1=INTP output enabled				

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AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	0			ns	
T_9	Chip select hold time	0			ns	
T_{11}	IOR* to DDIS* delay			25	ns	100 pF load
T_{12}	Data set up time	15			ns	
T_{13}	IOW* delay from chip select	10			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{CLK}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{39}	ACK* pulse width	75			ns	
T_{40}	PD7-PD0 setup time	10			ns	
T_{41}	PD7-PD0 hold time	25			ns	
T_{42}	Delay from ACK* low to interrupt low	5			ns	
T_{43}	Delay from IOR* to reset interrupt	5			ns	
T_R	Reset pulse width	10			ns	
N	Baud rate devisor	1		2^{16}-1		

Note 1 * = Baudout* cycle

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ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

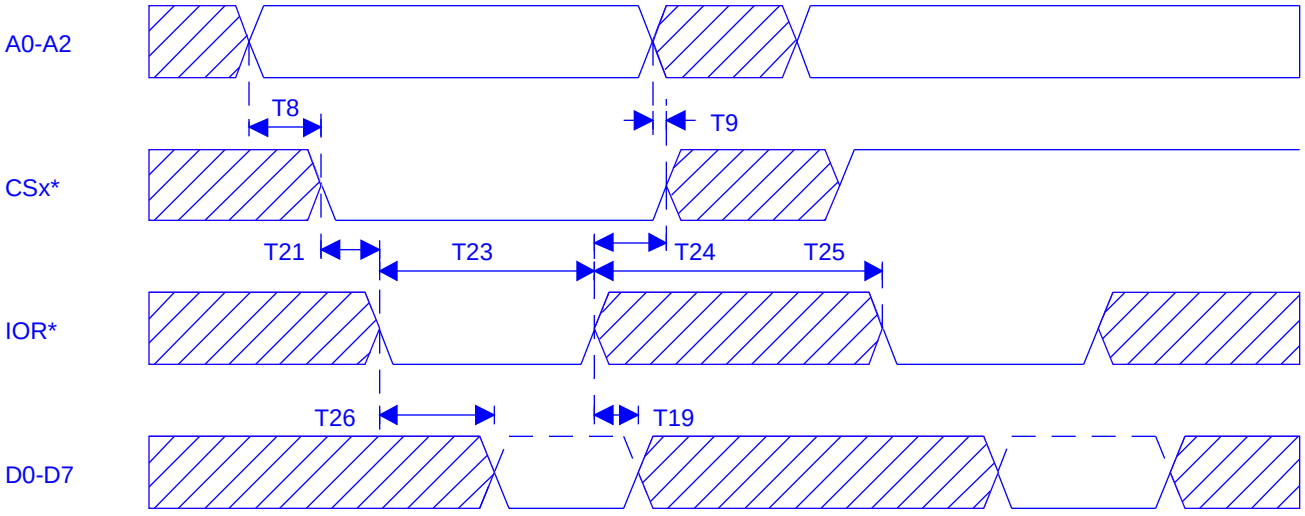
DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 20.0 mA PD7-PD0 I_{OL}= 10 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -0.2 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OH}= -6.0 mA on all the outputs
I_{CC}	Avg. power supply current		12		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	
R_{IN}	Internal pull-up resistance	4		15	kΩ	* Marked pins

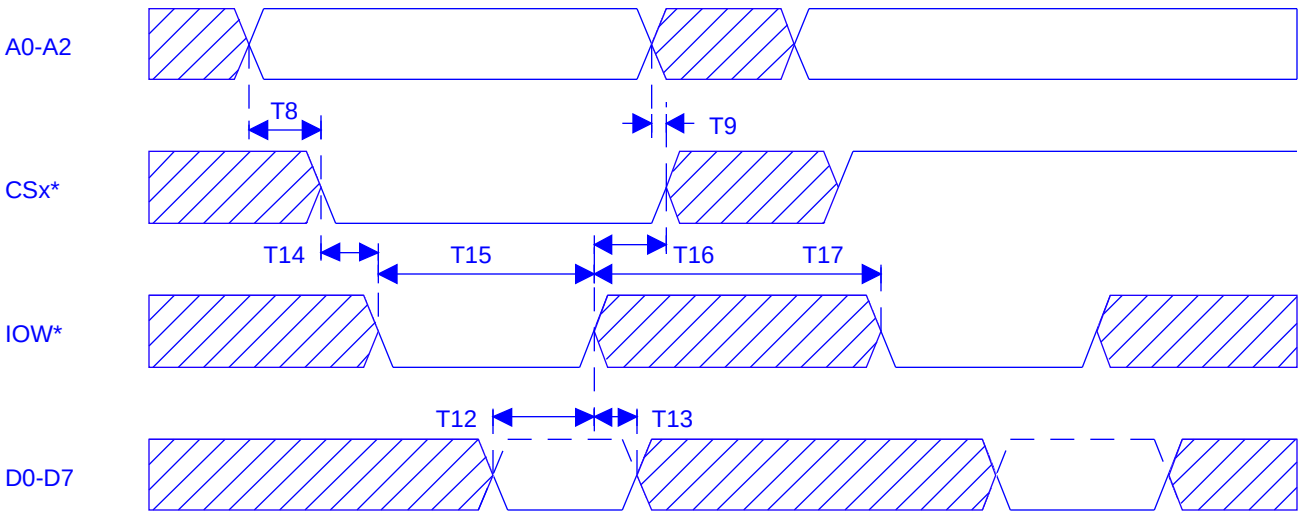
This product can operate in 3.0 Volts environment. Please consult with factory for additional information.

GENERAL READ TIMING



162450-RD-1

GENERAL WRITE TIMING



162450-WD-1

ST16C452AT
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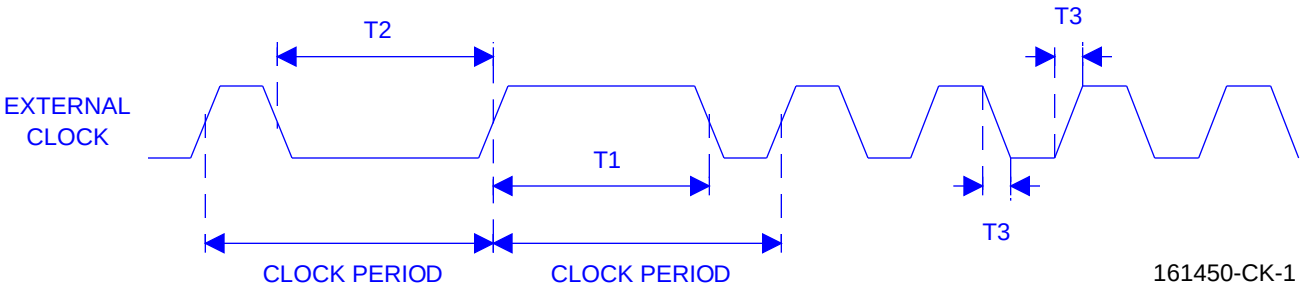
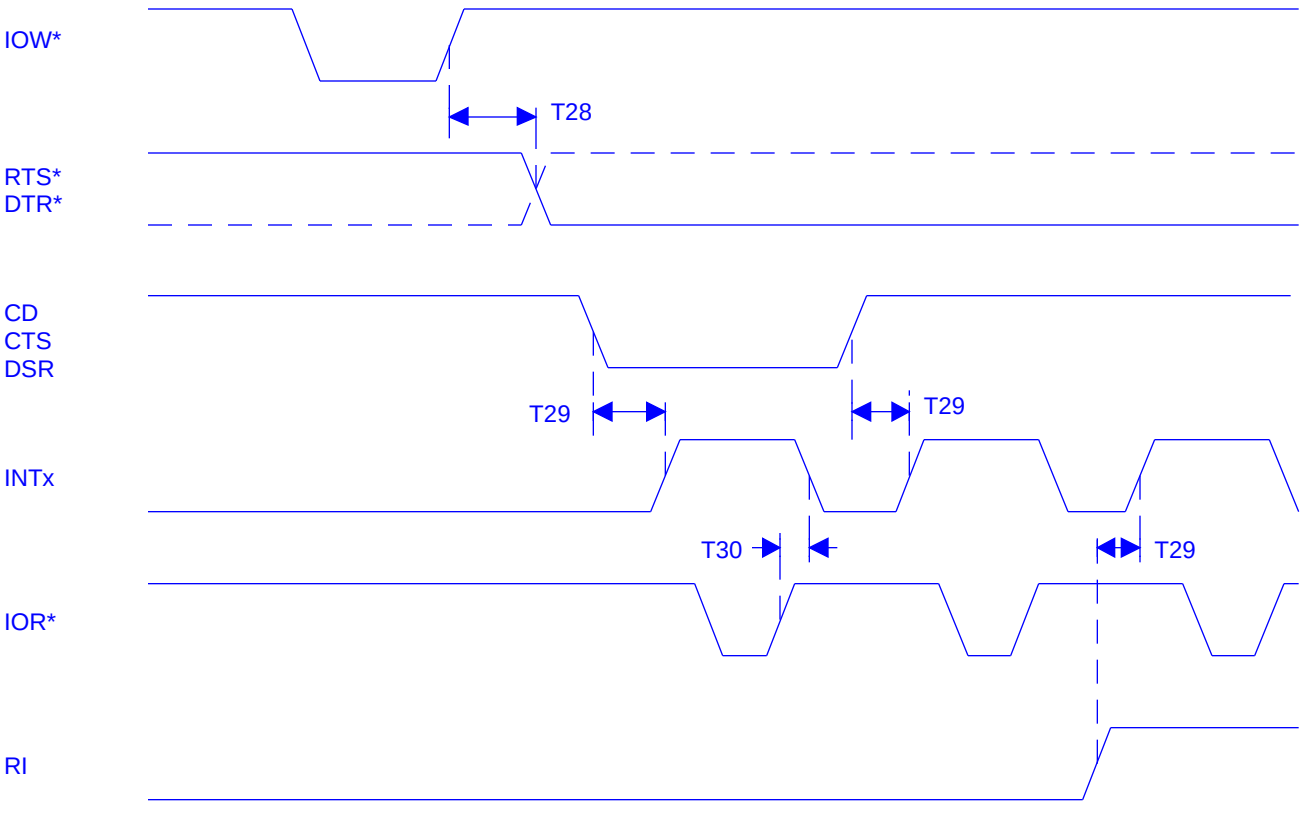
CLOCK TIMING



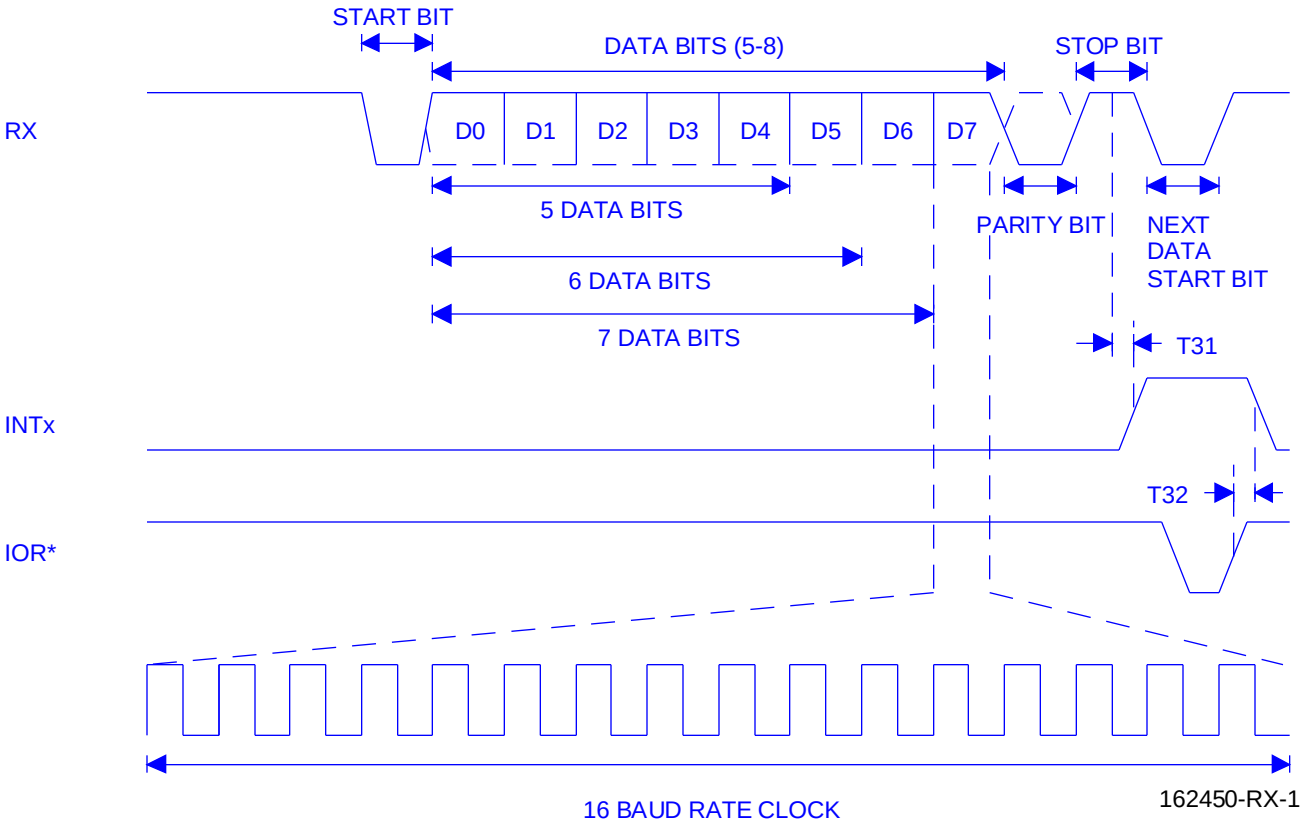
161450-CK-1

MODEM TIMING



162450-MD-1

RECEIVE TIMING



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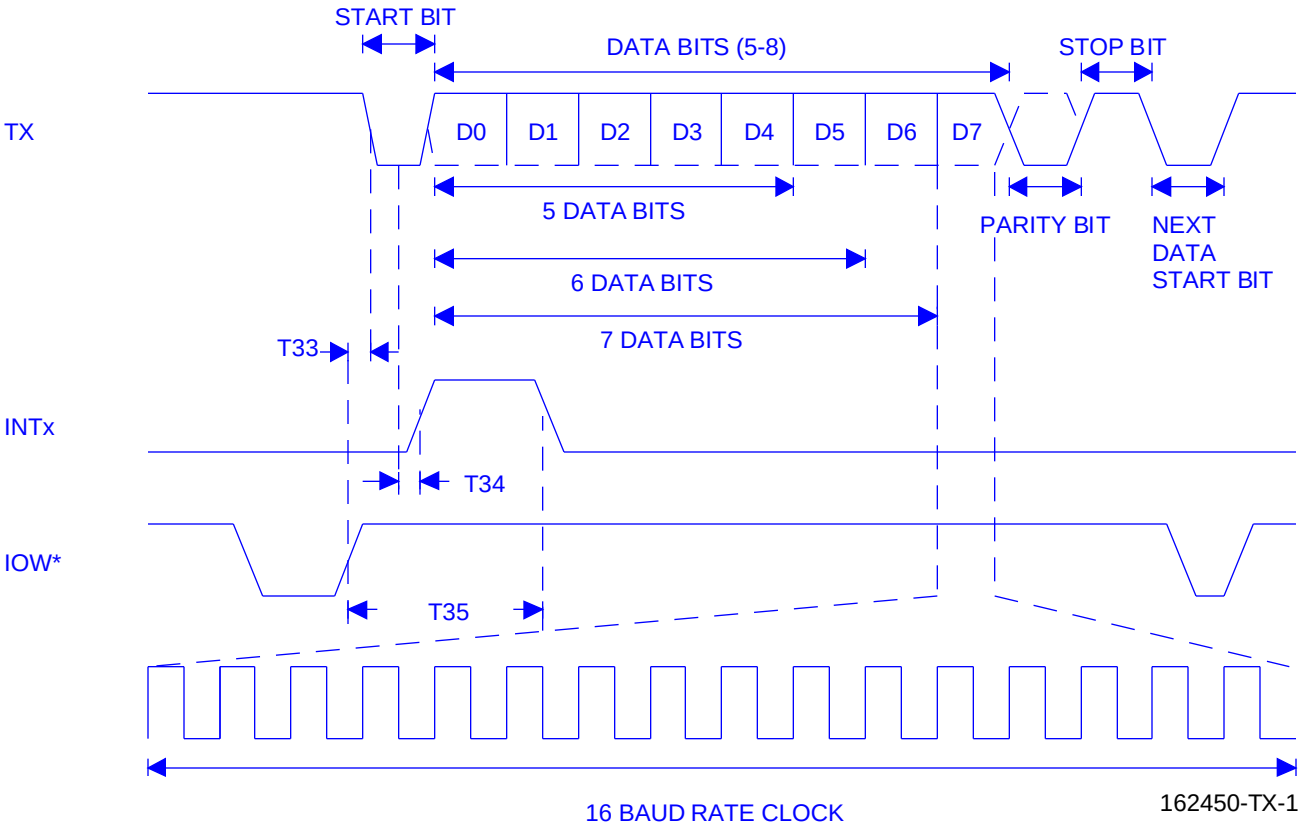
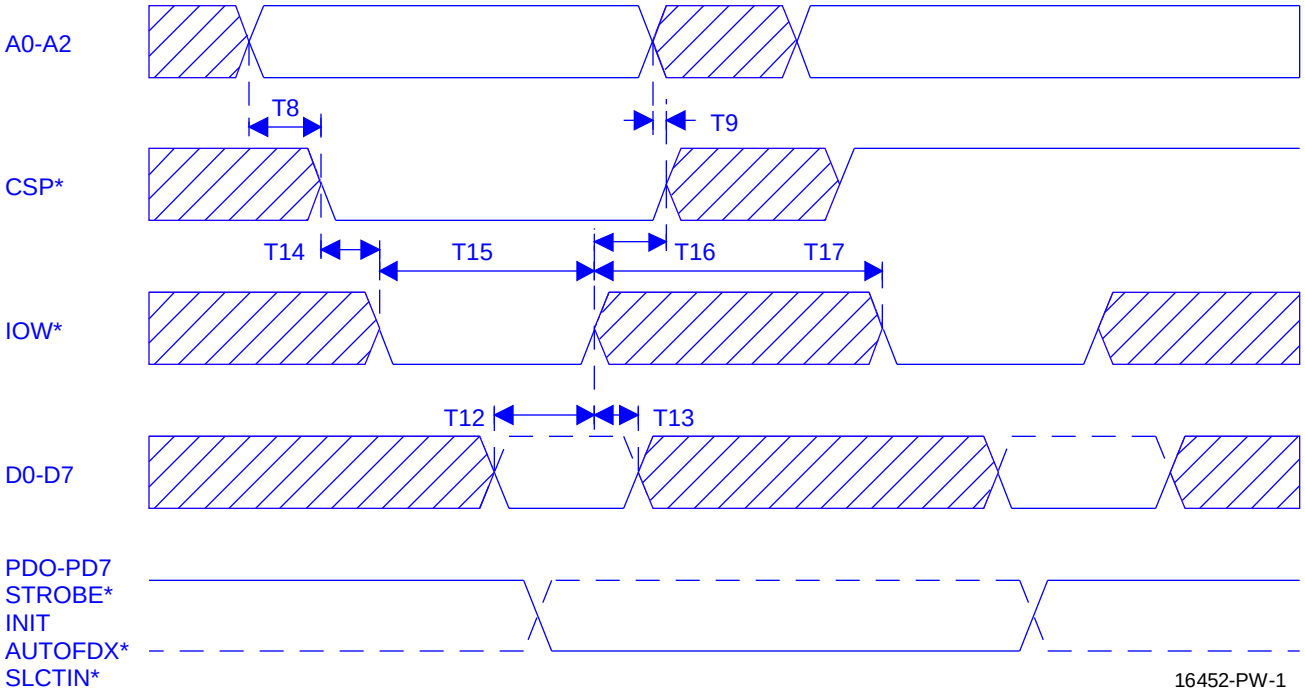
ST16C452PS

TRANSMIT TIMING



PARALLEL PORT GENERAL WRITE TIMING



ST16C452AT
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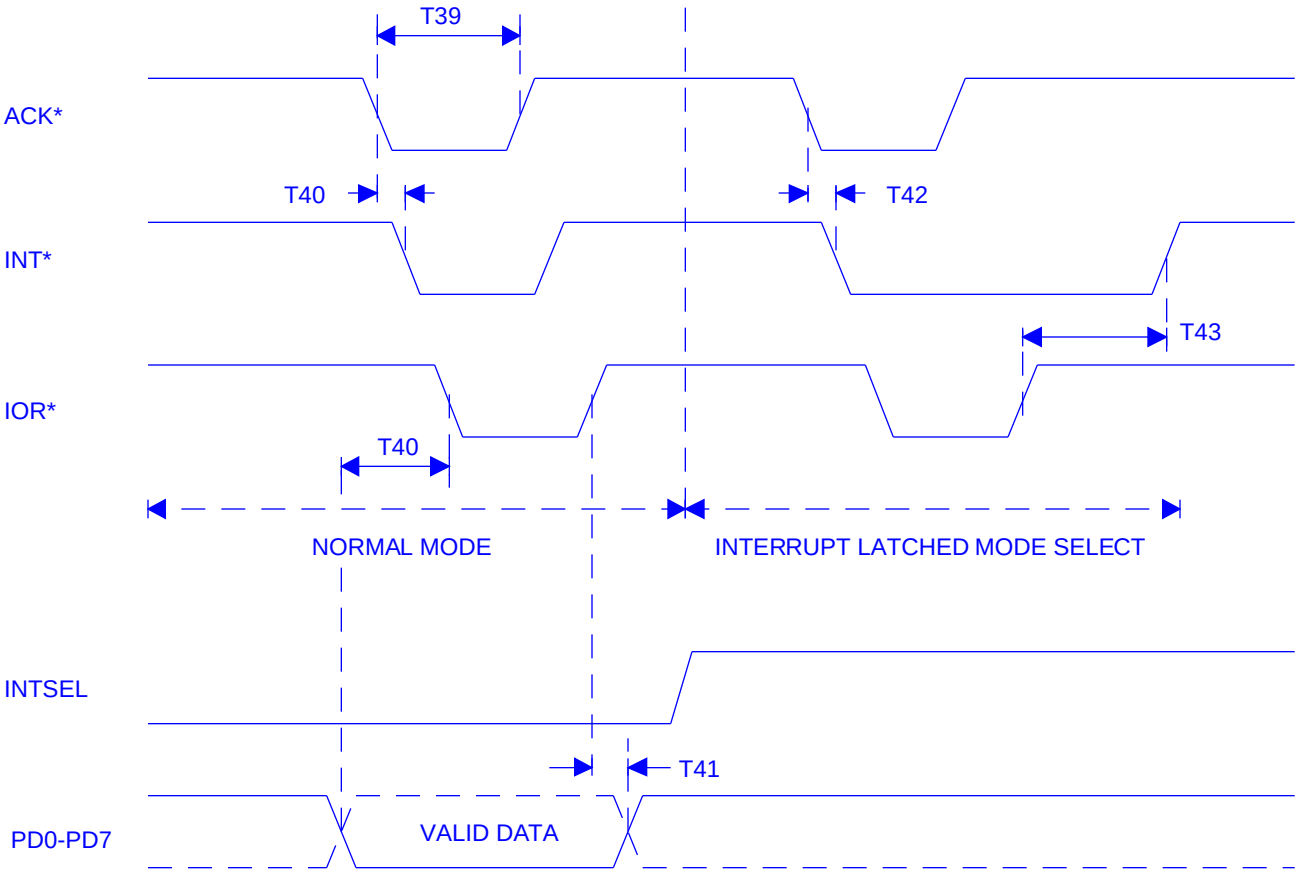
GENERAL READ TIMING



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