SGS-THOMSON MICROELECTRONICS

ST10R262

16-BIT MCU WITH ON-CHIP MAC

- **High Performance CPU**
  - Multiply-Accumulate unit (MAC)
  - 16-bit CPU with 4-stage pipeline and 40ns instruction cycle time at 50-MHz CPU clock
  - Register-based architecture
  - 1024 bytes on-Chip special function register area
  - Enhanced boolean bit manipulation facilities
  - Additional instructions to support HLL and operating systems
  - Single-cycle context switching
- **Memory Organization**
  - 1Kbytes on-chip RAM
  - Up to 16 MBytes linear address space for code and data
- **External Memory Interface**
  - Programmable external bus characteristics for different address ranges
  - 8-Bit or 16-bit external data bus
  - Hold-acknowledge bus arbitration support
  - Multiplexed or demultiplexed external address/data buses
  - Five programmable chip-select signals
- **One channel PWM Unit**
- **Fail-safe Protection**
  - Programmable watchdog timer
  - Oscillator Watchdog
- **Interrupt**
  - 16-priority-level interrupt system with 17 sources, sample-rate down to 40 ns
  - 8-channel interrupt-driven single-cycle data transfer facilities via peripheral event controller
- **Timers**
  - Two multi-functional general purpose timer units with 5 timers
  - Clock Generation via on-chip PLL or via direct or prescaled clock input
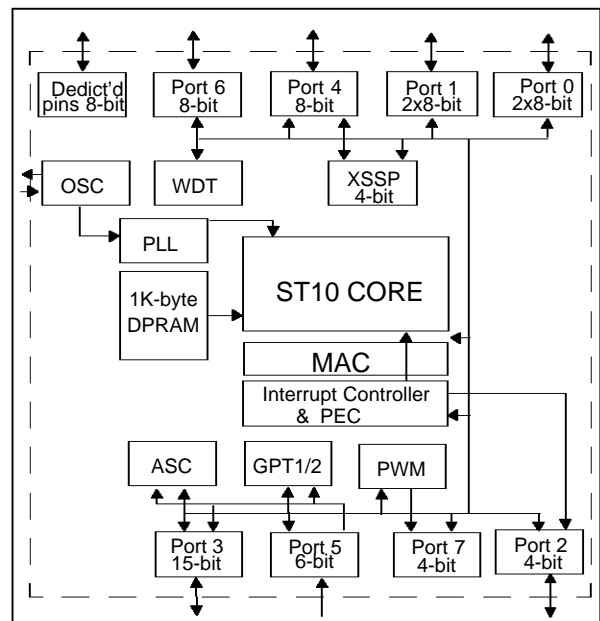
- **Serial channels**
  - Synchronous/Asynchronous
  - High speed Synchronous Serial Port
- **Up to 77 general purpose I/O lines**
- **Electrical Characteristics**
  - Power 5volt +/-10%,
  - Idle Current <5 mA
  - Power down supply current <50 A
- **Support**
  - C-compilers, macro-assembler packages, emulators, evaluation boards, HLL-debuggers, simulators, logic analyzer disassemblers, programming boards
- **Package Option**
  - 100-Pin Thin Quad Flat Pack

Table of Contents

Table of Contents

1 Pin Data

Figure 1.1 TQFP-100 pin configuration (top view)
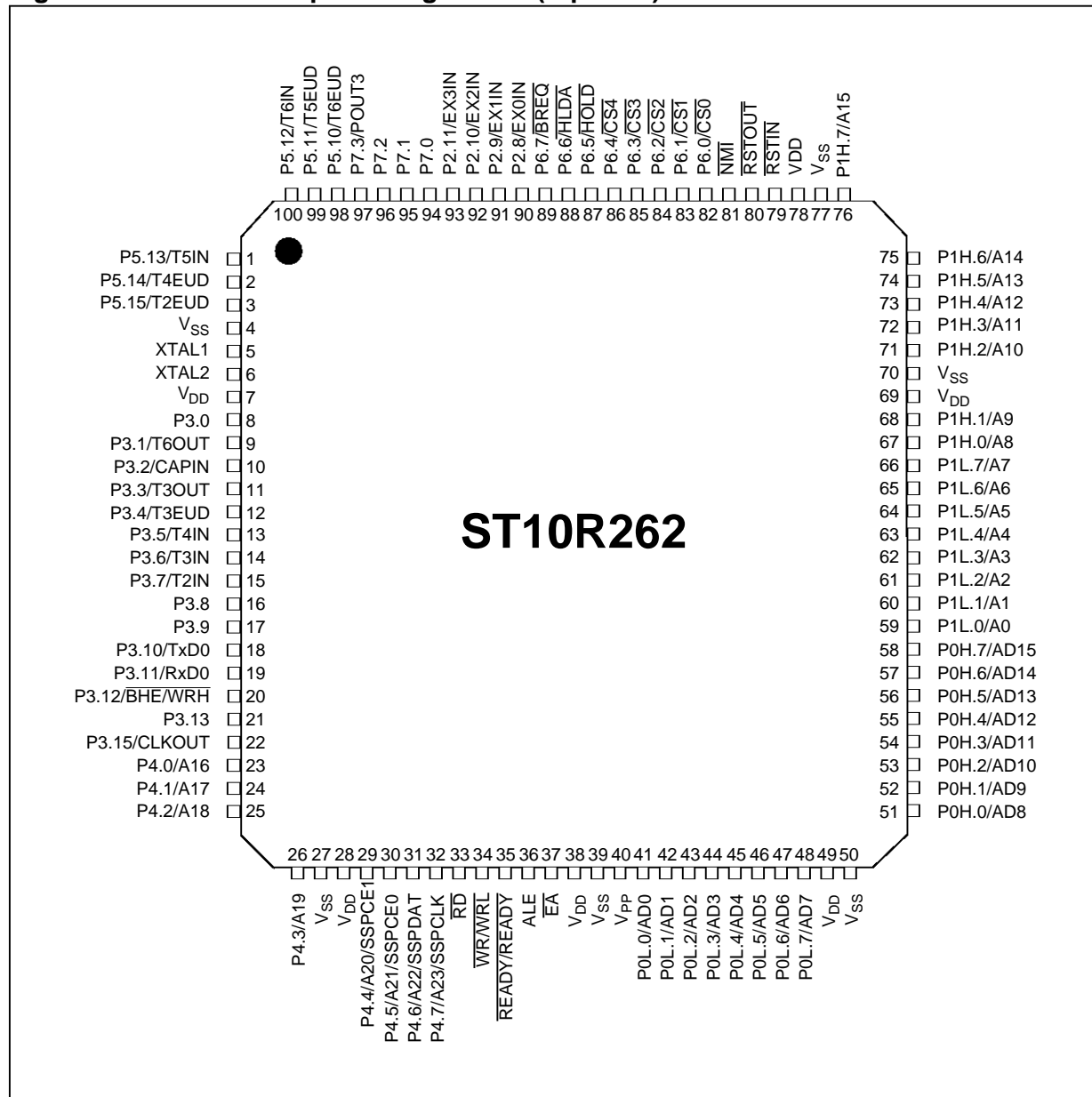
Table 1.1   Pin description

Symbol	Pin Number (TQFP)	Input (I) Output (O)	Function
P5.10 – P5.15	98-100 1- 3	I I	Port 5 is a 6-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 also serve as timer inputs:
	98	I	P5.10 T6EUD GPT2 Timer T6 Ext.Up/Down Ctrl.Input
	99	I	P5.11 T5EUD GPT2 Timer T5 Ext.Up/Down Ctrl.Input
	100	I	P5.12 T6IN GPT2 Timer T6 Count Input
	1	I	P5.13 T5IN GPT2 Timer T5 Count Input
	2	I	P5.14 T4EUD GPT1 Timer T4 Ext.Up/Down Ctrl.Input
	3	I	P5.15 T2EUD GPT1 Timer T2 Ext.Up/Down Ctrl.Input
XTAL1	5	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator
XTAL2	6	O	XTAL2: Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.
P3.0 – P3.13, P3.15	8 21 22	I/O I/O I/O	Port 3 is a 15-bit (P3.14 is missing) bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The following Port 3 pins also serve for alternate functions:
	9	O	P3.1 T6OUT GPT2 Timer T6 Toggle Latch Output
	10	I	P3.2 CAPIN GPT2 Register CAPREL Capture Input
	11	O	P3.3 T3OUT GPT1 Timer T3 Toggle Latch Output
	12	I	P3.4 T3EUD GPT1 Timer T3 Ext.Up/Down Ctrl.Input
	13	I	P3.5 T4IN GPT1 Timer T4 Input for Count/Gate/Reload/Capture
	14	I	P3.6 T3IN GPT1 Timer T3 Count/Gate Input
	15	I	P3.7 T2IN GPT1 Timer T2 Input for Count/Gate/Reload/Capture
	18	O	P3.10 T×D0 ASC0 Clock/Data Output (Asyn./Syn.)
	19	I/O	P3.11 R×D0 ASC0 Data Input (Asyn.) or I/O (Syn.)
	20	O	P3.12 BHE Ext. Memory High Byte Enable Signal,
		O	WRH Ext. Memory High Byte Write Strobe
	22	O	P3.15 CLKOUT System Clock Output (=CPU Clock)

Table 1.1   Pin description (cont'd)

Symbol	Pin Number (TQFP)	Input (I) Output (O)	Function
P4.0 – P4.7	23-26 29-32-	I/O	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, Port 4 can be used to output the segment address lines:
	23	O	P4.0 A16 Least Significant Segment Addr. Line
	...	...	... ...
	26	O	P4.3 A19 Segment Address Line
	29	O	P4.4 A20 Segment Address Line,
		O	SSPCE1 SSP Chip Enable Line 1
	30	O	P4.5 A21 Segment Address Line,
		O	SSPCE0 SSP Chip Enable Line 0
	31	O	P4.6 A22 Segment Address Line,
		I/O	SSPDAT SSP Data Input/Output Line
	32	O	P4.7 A23 Most Significant Segment Addr. Line
		O	SSPCLK SSP Clock Output Line
$\overline{RD}$	33	O	External Memory Read Strobe. RD is activated for every external instruction or data read access.
$\overline{WR}/\overline{WRL}$	34	O	External Memory Write Strobe. In WR-mode this pin is activated for every external data write access. In WRL-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
$\overline{READY}/$ $\overline{READY}$	35	I	Ready Input. The active level is programmable. When the Ready function is enabled, the selected inactive level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to the selected active level.
ALE	36	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes. Polarity is programmable.
$\overline{EA}$	37	I	External Access Enable pin. Low level during and after reset forces the ST10R262 to begin instruction execution out of external memory.

Table 1.1 Pin description (cont'd)

Symbol	Pin Number (TQFP)	Input (I) Output (O)	Function
PORT0: P0L.0 – P0L.7, P0H.0 - P0H.7	41 48 51 58	I/O	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** Data Path Width:8-bit16-bit P0L.0 – P0L.7:D0 – D7D0 - D7 P0H.0 – P0H.7:I/O D8 - D15 **Multiplexed bus modes:** Data Path Width:8-bit16-bit P0L.0 – P0L.7:AD0 – AD7AD0 - AD7 P0H.0 – P0H.7:A8 - A15AD8 - AD15
PORT1: P1L.0 – P1L.7, P1H.0 - P1H.7	59 66 67 - 68 71 - 76	I/O	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also in multiplexed bus mode if any BUSCON register selects a demultiplexed mode.
$\overline{\text{RSTIN}}$	79	I/O	Reset Input with Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running resets the ST10R262. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}. The RSTIN pin is pulled-down during 512 internal clock cycles for hardware, software or watchdog timer triggered resets
$\overline{\text{RSTOUT}}$	80	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{NMI}}$	81	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.

Table 1.1   Pin description (cont'd)

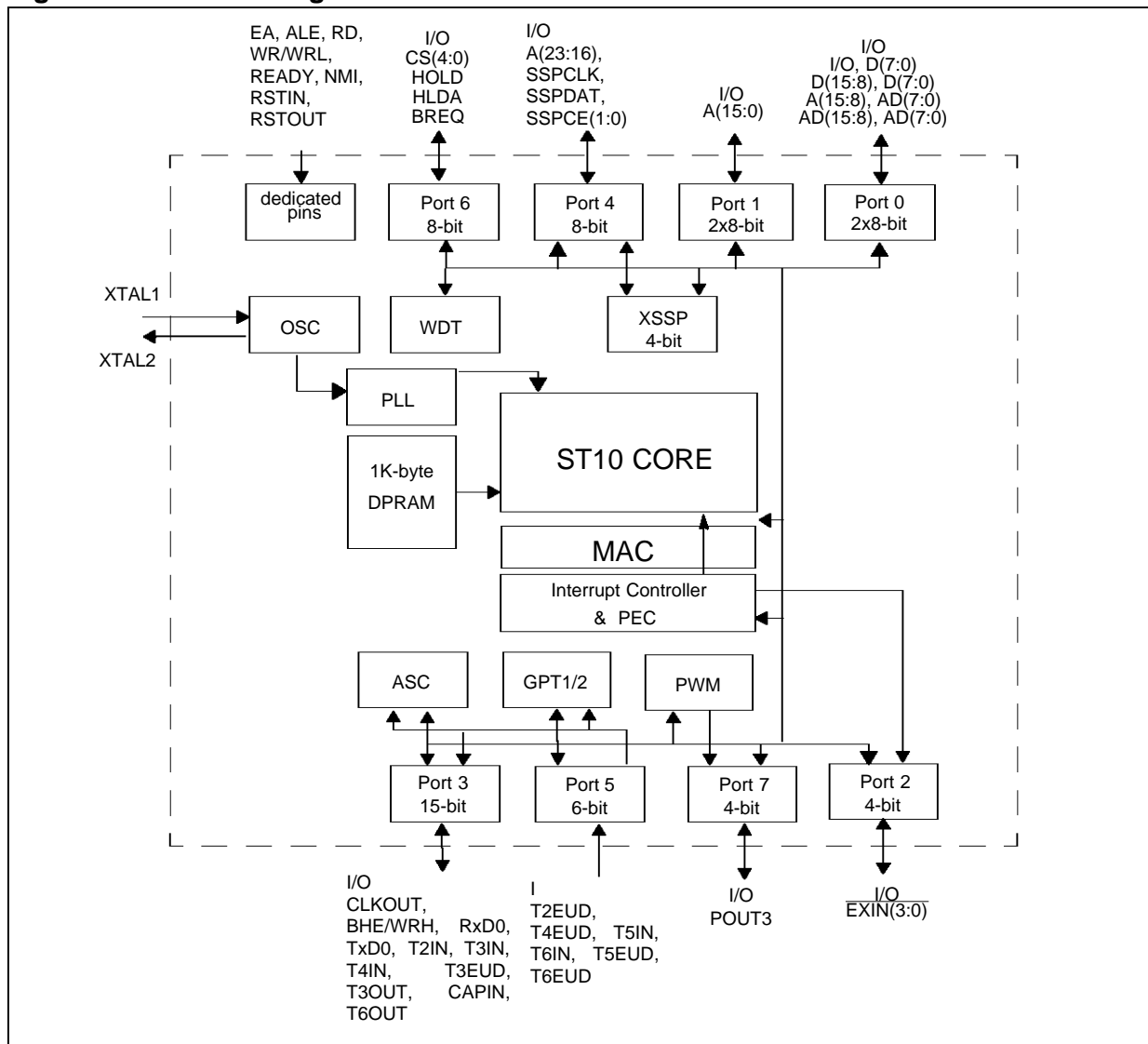| Symbol	Pin Number (TQFP)	Input (I) Output (O)	Function
P6.0 – P6.7	82 - 89	I/O	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The following Port 6 pins also serve for alternate functions:
	82	O	P6.0 $\overline{CS0}$ Chip Select 0 Output
	...	...	... ...
	86	O	P6.4 $\overline{CS4}$ Chip Select 4 Output
	87	I	P6.5 $\overline{HOLD}$ External Master Hold Request Input (Master mode: O, Slave mode: I)
	88	I/O	P6.6 $\overline{HLDA}$ Hold Acknowledge Output
	89	O	P6.7 $\overline{BREQ}$ Bus Request Output
P2.8 – P2.11	90 - 93	I/O	Port 2 is an 4-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The following Port 2 pins also serve for alternate functions:
	90	I	P2.8 EX0IN Fast External Interrupt 0 Input
	...	...	... ...
	93	I	P2.11 EX3IN Fast External Interrupt 3 Input
P7.0 – P7.3	94 - 97	I/O	Port 7 is an 4-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7outputs can be configured as push/pull or open drain drivers. The following Port 7 pins also serve for alternate functions:
	97	O	P7.3 POUT3 PWM (Channel 3) Output
V_{PP}	40	-	Timing pin for "exit from power-down" circuit and power-up asynchronous reset. If a Fast External Interrupt pin (EX3IN..EX0IN) is used to exit from Power Down mode, an external RC circuit should be connected to the Vpp pin. The discharging of the external capacitor causes a delay that allows the oscillator and PLL circuits to stabilize before the clock signal is delivered to the CPU and peripherals.

Table 1.1   Pin description (cont'd)

Symbol	Pin Number (TQFP)	Input (I) Output (O)	Function
V_{DD}	7, 28, 38, 49, 69, 78	-	Digital Supply Voltage.
V_{SS}	4, 27, 39, 50, 70, 77	-	Digital Ground.

2 Functional Description

The architecture of the ST10R262 combines the advantages of both RISC and CISC processors and an advanced peripheral subsystem. The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the ST10R262.

Figure 2.1 Block diagram

3 Central Processing Unit (CPU)

Figure 3.1   CPU block diagram
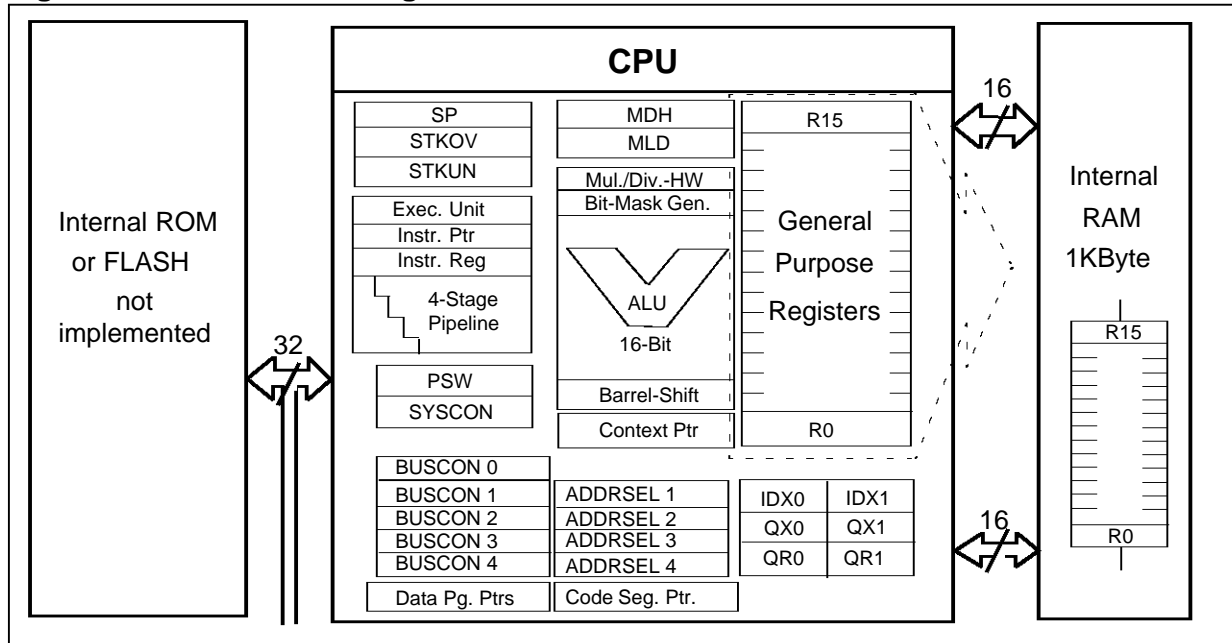
The main core of the CPU consists of a 4-stage instruction pipeline and a Multiply-Accumulation Unit. The MAC performs multiply-accumulate operations with enhanced instruction set for 32-bit arithmetic computation and data moves. The CPU also contains a separate multiply and divide unit and a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the ST10R262's instructions can be executed in one machine cycle which requires 40ns at 50MHz CPU clock.

The CPU includes an actual register context. This consists of 16 wordwide GPRs which are physically located within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at a time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, one register bank may overlap others.

A system stack of up to 1024 bytes is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are compared against the stack pointer value during each stack access to detect stack overflow or underflow.

4 Memory Mapping

The internal RAM space of the ST10R262 is 1 KByte. The RAM address range is 00'FA00h - 00'FDFFh. It is used for variables, the register banks, and the system stack. It also contains the PEC pointers (address range 00'FCE0h - 00'FCFFh) and the bit-addressable space (00'FD00h - 00'FDFFh).

Figure 4.1   Internal RAM area and SFR areas
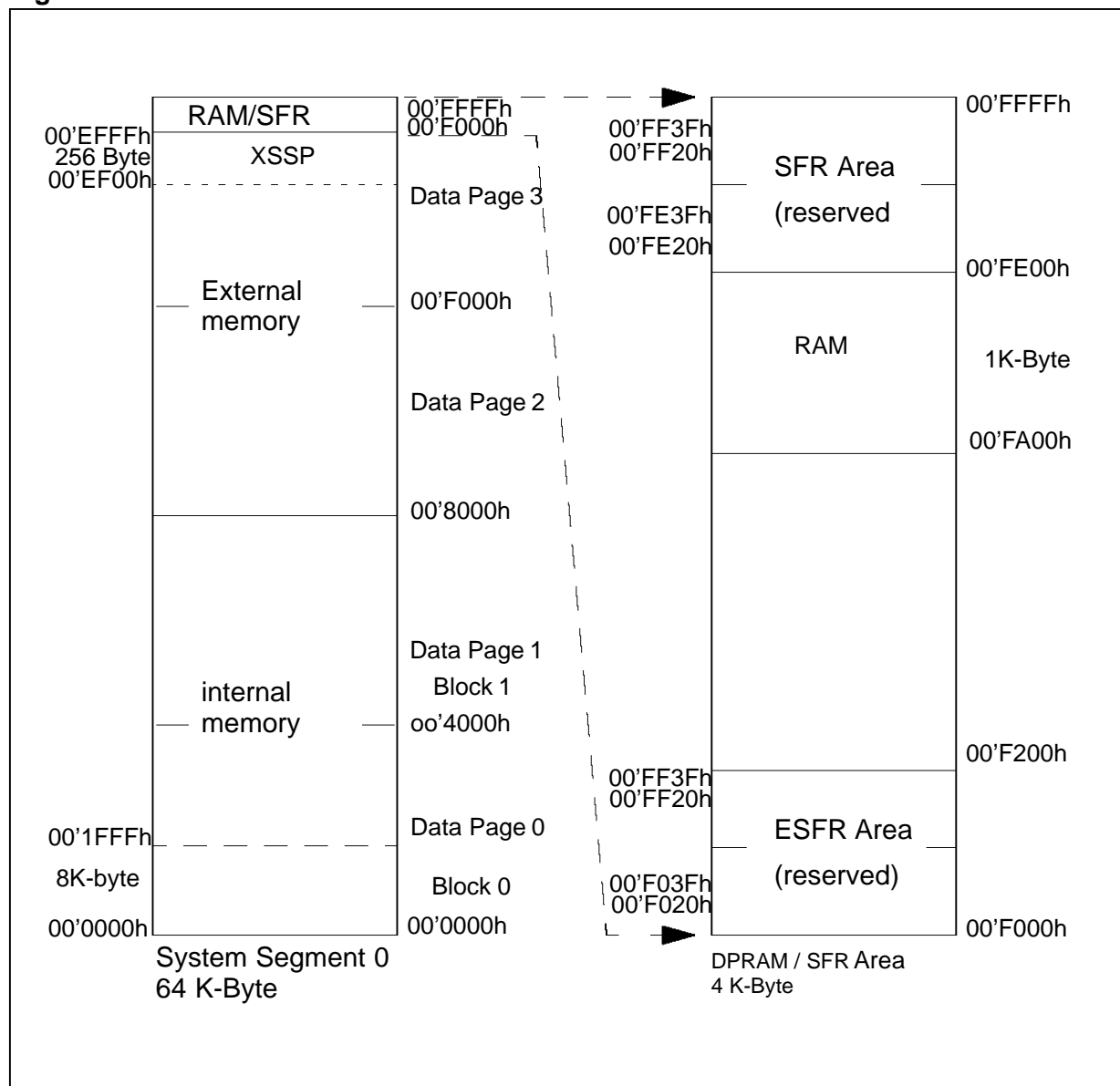
Note: The upper 256 bytes of SFR area, ESFR area and internal RAM are bit-addressable.

5   Multiply-Accumulate Unit (MAC)

The MAC is a specialized co-processor added to the ST10R262 CPU core to improve the performance of signal processing algorithms. It includes:

- a multiply-accumulate unit
- an address generation unit, able to feed the mac unit with 2 operands per cycle
- a repeat unit, to execute a series of multiply-accumulate instructions

Figure 5.1   MAC Architecture
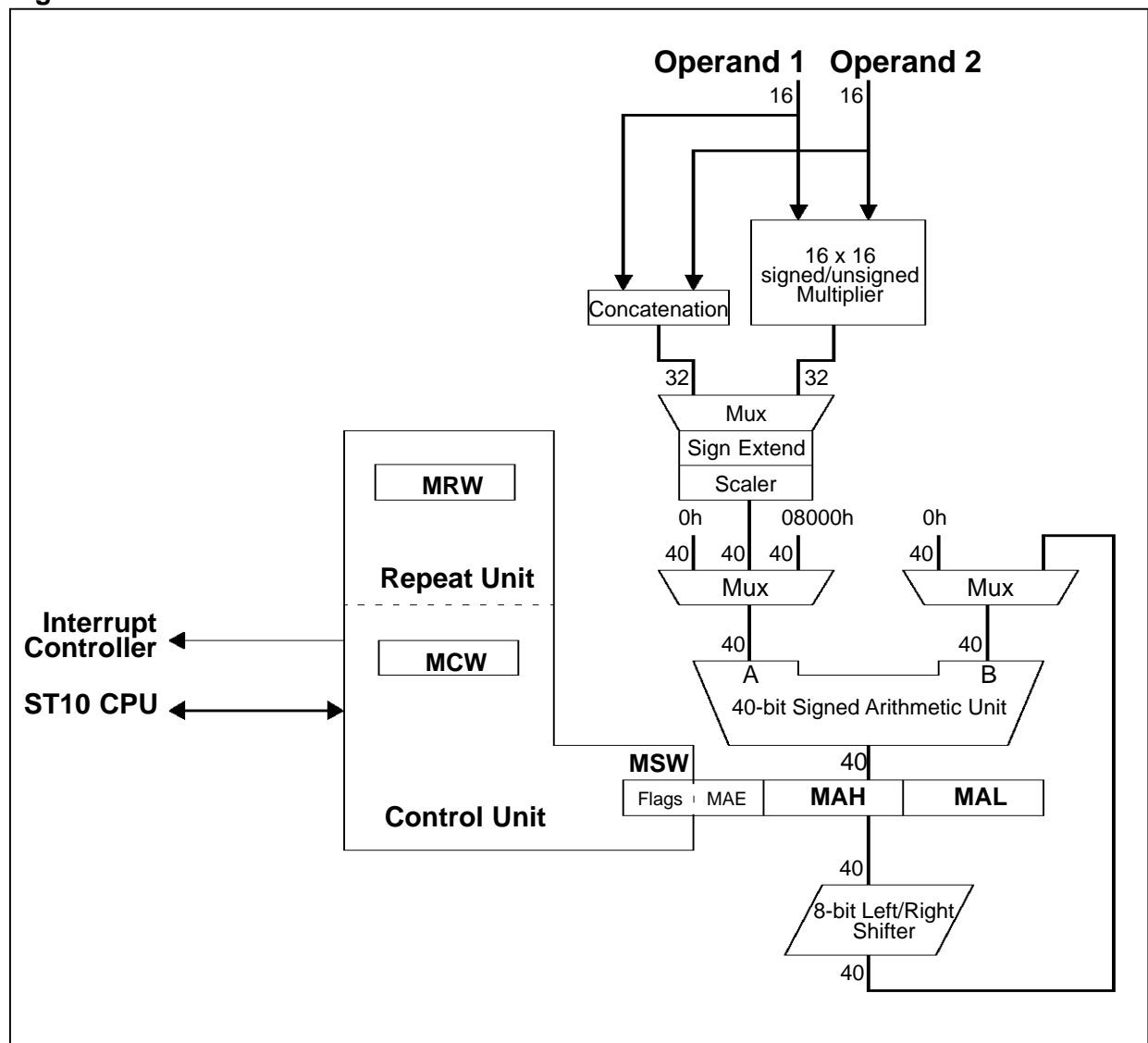
5.1 MAC Features

Enhanced addressing capabilities

- New addressing modes including a double indirect addressing mode with pointer post-modification.

- Parallel Data Move allows one operand move during Multiply-Accumulate instructions without penalty.

- New transfer instructions CoSTORE (for fast access to the MAC SFRs) and CoMOV (for fast memory to memory table transfer).

Multiply-accumulate unit

- One-cycle execution for all MAC operations.

- 16 x 16 signed/unsigned parallel multiplier.

- 40-bit signed arithmetic unit with automatic saturation mode.

- 40-bit accumulator.

- 8-bit left/right shifter.

- Scaler (one-bit left shifter)

- Data limiter

- Full instruction set with multiply and multiply-accumulate, 32-bit signed arithmetic and compare instructions.

- Three 16-bit status and control registers:
  MSW: MAC Status Word
  MCW: MAC Control Word
  MRW: MAC Repeat Word.

Program control

- Repeat Unit allows some MAC co-processor instructions to be repeated up to 8192 times. Repeated instructions may be interrupted.

- MAC interrupt (Class B Trap) on MAC condition flags.

5.2 MAC Operation

5.2.1 Instruction pipelining

All MAC instructions use the 4-stage pipeline. During each stage the following tasks are performed:

- FETCH: All new instructions are double-word instructions.

- DECODE: If required, operand addresses are calculated and the resulting operands are fetched. IDX and GPR pointers are post-modified if necessary.

- EXECUTE: Performs the MAC operation. At the end of the cycle, the Accumulator and the MAC condition flags are updated if required. Modified GPR pointers are written-back during this stage, if required.

- WRITEBACK: Operand write-back in the case of parallel data move.

Note:At least one instruction which does not use the MAC must be inserted between two instructions that read from a MAC register. This is because the Accumulator and the status of the MAC are modified during the Execute stage. The CoSTORE instruction has been added to allow access to the MAC registers immediately after a MAC operation.

5.2.2 Address generation

MAC instructions can use some standard ST10 addressing modes such as GPR direct or #data4 for immediate shift value.

New addressing modes have been added to supply the MAC with two new operands per instruction cycle. These allow indirect addressing with address pointer post-modification.

Double indirect addressing requires two pointers. Any GPR can be used for one pointer, the other pointer is provided by one of two specific SFRs IDX0 and IDX1. Two pairs of offset registers QR0/QR1 and QX0/QX1 are associated with each pointer (GPR or IDX_i). The GPR pointer allows access to the entire memory space, but IDX_i are limited to the internal Dual-Port RAM, except for the CoMOV instruction.

The following table shows the various combinations of pointer post-modification for each of these 2 new addressing modes. In this document the symbols "$[Rw_n \otimes]$" and "$[IDX_i \otimes]$" will be used to refer to these addressing modes.

Table 5.1   Pointer post-modification combinations for IDXi and Rwn

Symbol	Mnemonic	Address Pointer Operation
"$[IDX_i \otimes]$" stands for	$[IDX_i]$	$(IDX_i) \leftarrow (IDX_i)$ (no-op)
	$[IDX_i +]$	$(IDX_i) \leftarrow (IDX_i) +2$ (i=0,1)
	$[IDX_i -]$	$(IDX_i) \leftarrow (IDX_i) -2$ (i=0,1)
	$[IDX_i + QX_j]$	$(IDX_i) \leftarrow (IDX_i) + (QX_j)$ (i, j =0,1)
	$[IDX_i - QX_j]$	$(IDX_i) \leftarrow (IDX_i) - (QX_j)$ (i, j =0,1)
"$[Rw_n \otimes]$" stands for	$[Rwn]$	$(Rwn) \leftarrow (Rwn)$ (no-op)
	$[Rwn+]$	$(Rwn) \leftarrow (Rwn) +2$ (n=0-15)
	$[Rwn-]$	$(Rwn) \leftarrow (Rwn) -2$ (k=0-15)
	$[Rwn+QR_j]$	$(Rwn) \leftarrow (Rwn) + (QR_j)$ (n=0-15;j =0,1)
	$[Rwn - QR_j]$	$(Rwn) \leftarrow (Rwn) - (QR_j)$ (n=0-15; j =0,1)

For the CoMACM class of instruction, a mechanism called Parallel Data Move has been implemented. This class of instruction is only available with double indirect addressing mode. The Parallel Data Move allows the operand pointed by IDX_i to be moved to a new location in parallel with the MAC operation. The write-back address of the Parallel Data Move is calculated depending on the post-modification of IDX_i. It is obtained by the reverse operation than the one used to calculate the new value of IDX_i. The following table shows these rules.

**Table 5.2   Parallel data move addressing**

Instruction	Writeback Address
CoMACM $[IDX_i+]$,...	$<IDX_i-2>$
CoMACM $[IDX_i-]$,...	$<IDX_i+2>$
CoMACM $[IDX_i+QX_j]$,...	$<IDX_i-QX_j>$
CoMACM $[IDX_i-QX_j]$,...	$<IDX_i+QX_j>$

The Parallel Data Move shifts a table of operands in parallel with a computation on those operands. Its specific use is for signal processing algorithms like filter computation.

The following figure gives an example of Parallel Data Move with CoMACM instruction.

Figure 5.2   Example of parallel data move
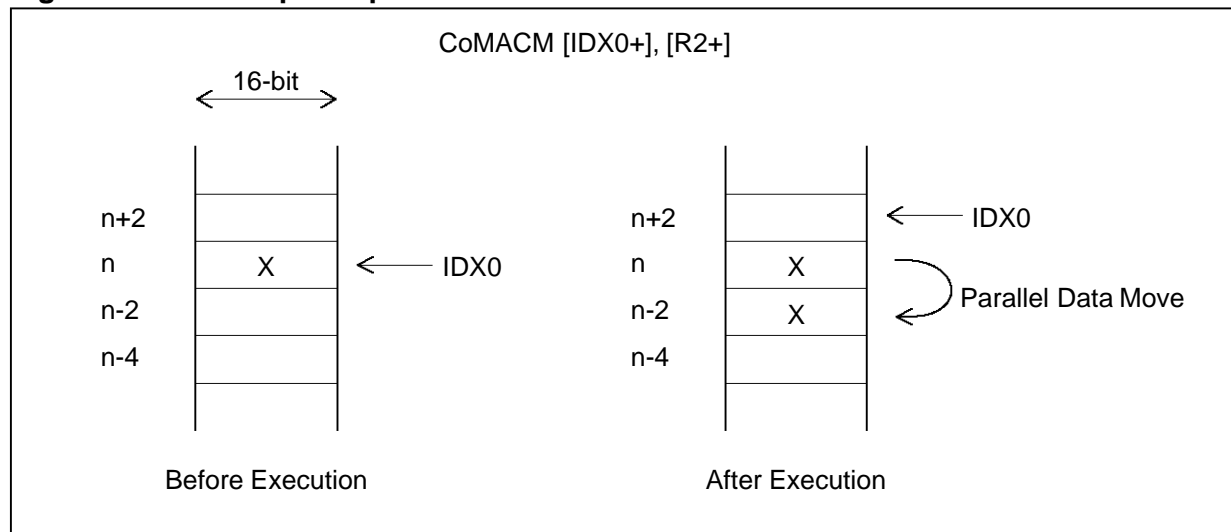
5.2.3   16 x 16 signed/unsigned parallel multiplier

The multiplier executes 16 x 16-bit parallel signed/unsigned fractional and integer multiplies. The multiplier has two 16-bit input ports, and a 32-bit product output port. The input ports can accept data from the MA-bus and from the MB-bus. The output is sign-extended and then feeds a scaler that shifts the multiplier output according to the shift mode bit MP specified in the co-processor Control Word (MCW). The product is shifted one bit left to compensate for the extra sign bit gained in multiplying two 16-bit signed (2's complement) fractional numbers.

5.2.4 40-bit signed arithmetic unit

The arithmetic unit over 32 bits wide to allow intermediate overflow in a series of multiply/accumulate operations. The extension flag E, contained in the most significant byte of MSW, is set when the Accumulator has overflowed beyond the 32-bit boundary, that is, when there are significant (non-sign) bits in the top eight (signed arithmetic) bits of the Accumulator.

The 40-bit arithmetic unit has two 40-bit input ports A and B. The A-input port accepts data from 4 possible sources: 00,0000,0000h, 00,0000,8000h (round), the sign-extended product, or the sign-extended data conveyed by the 32-bit bus resulting from the concatenation of MA- and MB-buses. Product and Concatenation can be shifted left by one according to MP for the multiplier or to the instruction for the concatenation. The B-input port is fed either by the 40-bit shifted/not shifted and inverted/not inverted accumulator or by 00,0000,0000h. A-input and B-input ports can receive 00,0000,0000h to allow direct transfers from the B-source and A-source, respectively, to the Accumulator (case of Multiplication, Shift..). The output of the arithmetic unit goes to the Accumulator.

It is also possible to saturate the Accumulator on a 32-bit value, automatically after every accumulation. Automatic saturation is enabled by setting the saturation bit MS in the MCW register. When the Accumulator is in the saturation mode and an 32-bit overflow occurs, the accumulator is loaded with either the most positive or the most negative value representable in a 32-bit value, depending on the direction of the overflow. The value of the Accumulator upon saturation is 00,7fff,ffffh (positive) or ff,8000,0000h (negative) in signed arithmetic. Automatic saturation sets the SL flag MSW. This flag is a sticky flag which means it stays set until it is explicitly reset by the user.

40-bit overflow of the Accumulator sets the SV flag in MSW. This flag is also a sticky flag.

5.2.5 40-bit accumulator register

The 40-bit Accumulator consists of three SFR registers MAH, MAL and MAE. MAH and MAL are 16-bit wide. MAE is 8-bit wide and is contained within the least significant byte of MSW. Most co-processor operations specify the 40-bit Accumulator register as source and/or destination operand.

5.2.6 Data limiter

Saturation arithmetic is also provided to selectively limit overflow, when reading the accumulator by means of a CoSTORE <destination> MAS instruction. Limiting is performed on the MAC Accumulator. If the contents of the Accumulator can be represented in the destination operand size without overflow, the data limiter is disabled and the operand is not modified. If the contents of the accumulator cannot be represented without overflow in the destination operand size, the limiter will substitute a 'limited' data as explained in the following table.

Table 5.3   Data Limit Values

Register	E bit	N bit	Output of the Limiter
x	0	x	unchanged
MAS	1	0	7fffh
MAS	1	1	8000h

Note: In this case, the accumulator and the status register are not affected. MAS readable from a CoS-TORE instruction.

5.2.7 Accumulator shifter

The Accumulator shifter is a parallel shifter with a 40-bit input and a 40-bit output. The source operand of the shifter is the Accumulator and the possible shifting operations are:

- No shift (Unmodified)

- Up to 8-bit Arithmetic Left Shift

- Up to 8-bit Arithmetic Right Shift

E, SV and SL bits from MSW are affected by Left shifts, therefore if the saturation mechanism is enabled (MS), the behavior is similar to the one of the arithmetic unit. The carry flag C is also affected by left shifts.

5.2.8 Repeat unit

The MAC includes a repeat unit allowing the repetition of some co-processor instructions up to 2^{13} (8192) times. The repeat count may be specified either by an immediate value (up to 31 times) or by the content of the Repeat Count (bits 12 to 0) in the MAC Repeat Word (MRW). If the Repeat Count equals "N" the instruction will be executed "N+1" times. At each iteration of a cumulative instruction the Repeat Count is tested for zero. If it is zero the instruction is terminated else the Repeat Count is decremented and the instruction is repeated. During such a repeat sequence, the Repeat Flag in MRW is set until the last execution of the repeated instruction.

The syntax of repeated instructions is shown in the following examples:

- Repeat 24 times
CoMAC[IDX0+],[R0+]; repeated 24 times

In this example, the instruction is repeated according to a 5-bit immediate value. The Repeat Count in MRW is automatically loaded with this value minus one.

- MOV MRW, #00FFh; load MRW
NOP; instruction latency
Repeat MRW times
CoMACM [IDX1-],[R2+]; repeated 256 times

In this example, the instruction is repeated according to the Repeat Count in MRW. Notice that due to the pipeline processing at least one instruction should be inserted between the write of MRW and the next repeated instruction.

Repeat sequences may be interrupted. When an interrupt occurs during a repeat sequence, the sequence is stopped and the interrupt routine is executed. The repeat sequence resumes at the end of the interrupt routine. During the interrupt, MR remains set, indicating that a repeated instruction has been interrupted and the Repeat Count holds the number (minus 1) of repetition that remains to complete the sequence. If the Repeat Unit is used in the interrupt routine, MRW must be saved by the user and restored before the end of the interrupt routine.
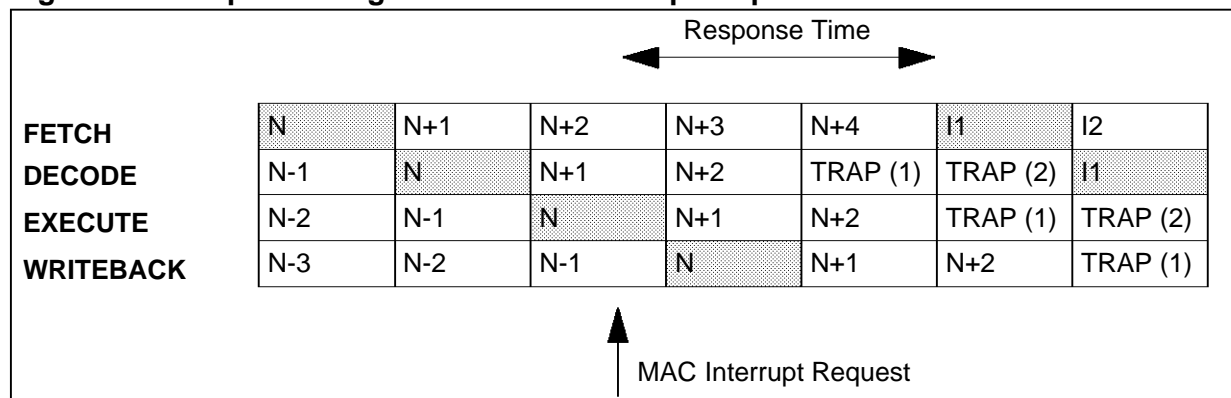
Note:The Repeat Count should be used with caution. In this case MR should be written as 0. In general MR should not be set by the user otherwise correct instruction processing can not be guaranteed.

5.2.9 MAC interrupt

The MAC can generate an interrupt according to the value of the status flags C (carry), SV (overflow), E (extension) or SL (limit) of the MSW. The MAC interrupt is globally enabled when the MIE flag in MCW is set. When it is enabled the flags C, SV, E or SL can triggered a MAC interrupt when they are set provided that the corresponding mask flag CM, VM, EM or LM in MCW is also set. A MAC interrupt request set the MIR flag in MSW, this flag must be reset by the user during the interrupt routine otherwise the interrupt processing restarts when returning from the interrupt routine.

The MAC interrupt is implemented as a Class B hardware trap (trap number Ah - trap priority I). The associated Trap Flag in the TFR register is MACTRP, bit #6 of the TFR (Remember that this flag must also be reset by the user in the case of an MAC interrupt request).

As the MAC status flags are updated (or eventually written by software) during the Execute stage of the pipeline, the response time of a MAC interrupt request is 3 instruction cycles (see Figure 3). It is the number of instruction cycles required between the time the request is sent and the time the first instruction located at the interrupt vector location enters the pipeline. Note that the IP value stacked after a MAC interrupt does not point to the instruction that triggers the interrupt.

Figure 5.3   Pipeline diagram for MAC interrupt response time

FETCH	N	N+1	N+2	N+3	N+4	I1	I2
DECODE	N-1	N	N+1	N+2	TRAP (1)	TRAP (2)	I1
EXECUTE	N-2	N-1	N	N+1	N+2	TRAP (1)	TRAP (2)
WRITEBACK	N-3	N-2	N-1	N	N+1	N+2	TRAP (1)

MAC Interrupt Request

Response Time

5.2.10   Number representation & rounding

The MAC supports the two's-complement representation of binary numbers. In this format, the sign bit is the MSB of the binary word. This is set to zero for positive numbers and set to one for negative numbers. Unsigned numbers are supported only by multiply/multiply-accumulate instructions which specifies whether each operand is signed or unsigned.

In two's complement fractional format, the N-bit operand is represented using the 1.[N-1] format (1 signed bit, N-1 fractional bits). Such a format can represent numbers between -1 and +1-$2^{-[N-1]}$. This format is supported when MP of MCW is set.

The MAC implements 'two's complement rounding'. With this rounding type, one is added to the bit to the right of the rounding point (bit 15 of MAL), before truncation (MAL is cleared).

6 Interrupt and Trap Functions

With an interrupt response time from 100 ns to 240 ns (in the case of internal program execution @ 50MHz CPU clock), the ST10R262 reacts quickly to the occurrence of non-deterministic events.

The architecture of the ST10R262 supports several mechanisms for fast and flexible response to the service requests that can be generated from various sources, internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced, either by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In a standard interrupt service, program execution is suspended and a branch to the interrupt service routine is performed. For a PEC service, just one cycle is 'stolen' from the current CPU activity. A PEC service is a single, byte or word data transfer between any two memory locations, with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is decremented for each PEC service, except in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are very well suited, for example, to the transmission or reception of blocks of data. The ST10R262 has 8 PEC channels, each of which offers fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield, exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher priority service request. For standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs, feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

6.1   Interrupt Sources

The follownig table shows all of the possible ST10R262 interrupt sources and the correspond-ing hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers:

Table 6.1   List of possible interrupt sources, flags, vector and trap numbers

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
External Interrupt 0	CC8IR	CC8IE	CC8INT	60h	18h
External Interrupt 1	CC9IR	CC9IE	CC9INT	64h	19h
External Interrupt 2	CC10IR	CC10IE	CC10INT	68h	1Ah
External Interrupt 3	CC11IR	CC11IE	CC11INT	6Ch	1Bh
GPT1 Timer 2	T2IR	T2IE	T2INT	88h	22h
GPT1 Timer 3	T3IR	T3IE	T3INT	8Ch	23h
GPT1 Timer 4	T4IR	T4IE	T4INT	90h	24h
GPT2 Timer 5	T5IR	T5IE	T5INT	94h	25h
GPT2 Timer 6	T6IR	T6IE	T6INT	98h	26h
GPT2 CAPREL Register	CRIR	CRIE	CRINT	9Ch	27h
ASC0 Transmit	S0TIR	S0TIE	S0TINT	A8h	2Ah
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	11Ch	47h
ASC0 Receive	S0RIR	S0RIE	S0RINT	ACh	2Bh
ASC0 Error	S0EIR	S0EIE	S0EINT	B0h	2Ch
PWM Channel 3	PWMIR	PWMIE	PWMINT	FCh	3Fh
SSP Interrupt	XP1IR	XP1IE	XP1INT	104h	41h
PLL Unlock	XP3IR	XP3IE	XP3INT	10Ch	43h

6.2 Hardware Traps

The ST10R262 provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called 'Hardware Traps'. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

The following table shows all of the possible exceptions or error conditions that can arise during run-time:

Table 6.2   List of possible exceptions or error conditions in run time

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions:					
•Hardware Reset		RESET	00'0000h	00h	III
•Software Reset		RESET	00'0000h	00h	III
•Watchdog Timer Overflow		RESET	00'0000h	00h	III
Class A Hardware Traps:					
•Non-Maskable Interrupt	NMI	NMITRAP	00'0008h	02h	II
•Stack Overflow	STKOF	STOTRAP	00'0010h	04h	II
•Stack Underflow	STKUF	STUTRAP	00'0018h	06h	II
Class B Hardware Traps:					
•Undefined Opcode	UNDOPC	BTRAP	00'0028h	0Ah	I
•Protected Instruction Fault	PRTFLT	BTRAP	00'0028h	0Ah	I
•Illegal Word Operand Access	ILLOPA	BTRAP	00'0028h	0Ah	I
•Illegal Instruction Access	ILLINA	BTRAP	00'0028h	0Ah	I
•Illegal External Bus Access	ILLBUS	BTRAP	00'0028h	0Ah	I
•MAC trap	MACTRP	BTRAP	00'0028h	0Ah	I
Reserved			[2Ch – 3Ch]	[0Bh – 0Fh]	
Software Traps					
•TRAP Instruction			Any [00'0000h – 00'01FCh] in steps of 4h	Any [00h – 7Fh]	Current CPU Priority

7 Parallel Ports

The ST10R262 provides up to 77 I/O lines which are organized into seven input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bi-directional ports which are switched to high impedance state when configured as inputs. The output drivers of three I/O ports can be configured (pin by pin) for push/pull operation, or via the control registers for open-drain operation. During the internal reset, all port pins are configured as inputs.

All port lines have associated, programmable, alternate, input or output functions. PORT0 and PORT1 may be used as address and data lines for external memory access. Port 4 outputs the additional segment address bits A23/19/17...A16 in systems where segmentation is enabled to access more than 64 KBytes of memory. Port 6 provides optional bus arbitration signals ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$) and chip select signals. Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal $\overline{\text{BHE}}$ and the system clock output (CLKOUT). Port 5 is used for timer control signals. All port lines that are not used for these alternate functions may be used as general purpose I/O lines.

8 Identification Registers

The ST10R262 has four Identification registers, mapped in ESFR space. These register contain:

- a manufacturer identifier,
- a chip identifier, with its revision,
- a internal memory and size identifier,
- programming voltage description

Refer to the user manual for the bit-field definition.

Table 8.1   Identification registers

Register	Physical Address	8-bit address	Description	Value
IDCHIP	F07Ch E	3Eh	Device identification register	1061h for step A 1062h for step B
IDMANUF	F07Eh E	3Fh	Manuafacturer identifier	0400h
IDMEM	F07Ah E	3Dh	Internal memory size & type	000h
IDPROG	F078h E	3Ch	Programming Vdd and Vpp voltage	000h

9   External Bus Controller

All external memory accesses are performed by an on-chip External Bus Controller (EBC). This can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes:

- 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
- 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses,   8-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses,   8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input or output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the choice of a wide range of different types of memories and external peripherals. In addition, up to 4 independent address windows may be defined (via register pairs AD-DRSELx / BUSCONx) which allow to access different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0. Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. Access to very slow memories is supported via a particular 'Ready' function.

A $\overline{HOLD}/\overline{HLDA}$ protocol is available for bus arbitration so that external resources can be shared with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register SYSCON. After setting HLDEN once, pins P6.7...P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{HLDA}$ pin is an output.

By setting bit DP6.7 to '1' the Slave Mode is selected where pin $\overline{HLDA}$ is switched to input. This directly connects the slave controller to another master controller without glue logic.

For applications which require less than 16 MBytes of external memory space, the address space can be restricted to 1 MByte, 256 KByte or to 64 KByte. In this case Port 4 outputs four, two or no address lines at all. If an address space of 16 MBytes is used, it outputs all 8 address lines.

Note: When the on-chip SSP Module is to be used the segment address output on Port 4 must be limited to 4 bits (i.e. A19...A16) in order to enable the alternate function of the SSP interface pins.

10 PWM Module

The Pulse Width Modulation Module generates an output signal using edge-aligned or centre-aligned PWM. The PWM module can also generate PWM burst signals and single shot outputs. The frequency range of this PWM signal for a 50 MHz CPU clock is from 9.54 Hz up to 20 MHz for edge aligned signal, and 4.77 Hz up to 10 MHz for center aligned signal. The minimum values depend on the width (16 bits) and the resolution (CLK/1 or CLK/64) of the PWM timer. The maximum values assume that the PWM output signal changes with every cycle of the timer. In a real application, the maximum PWM frequency will depend on the required resolution of the PWM output signal.

The Pulse Width Modulation Module operates on channel 3 of the PWM Module on the ST10R262. This channel has a 16-bit up/down counter PT3, a 16-bit period register PP3, a 16-bit pulse width register PW3 with a shadow latch, two comparators, and the necessary control logic. The operation of this channel is controlled by two control registers, PWMCON0 and PWMCON1, and the interrupt control and status is handled by one interrupt control register PWMIC.

The PWM module provides three different operating modes:

- Standard PWM generation (edge aligned PWM),
- Symmetrical PWM generation (center aligned PWM),
- Single shot mode.

The foolwing figure shows the PWM block diagram

Figure 10.1   PWM channel block diagram
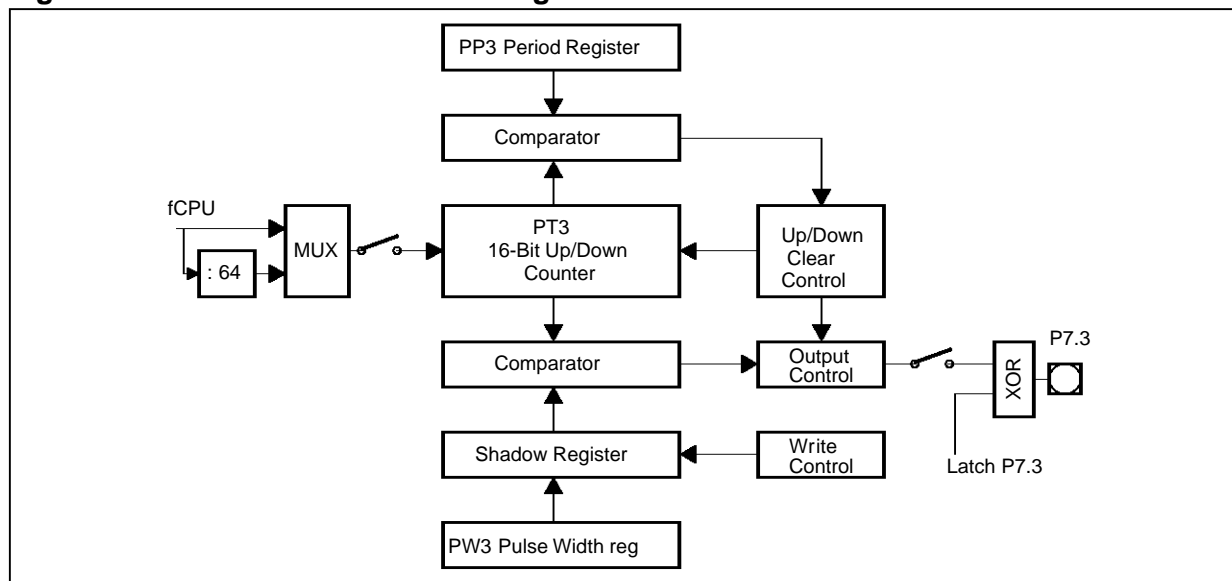
11 General Purpose Timer (GPT) Unit

The GPT unit is a flexible multifunctional timer/counter structure used for many different time-related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation or pulse multiplication.

The GPT unit incorporates five 16-bit timers, organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

GPT1

Each of the three timers T2, T3, T4 of module GPT1 can be configured individually for one of three basic modes of operation: Timer, Gated Timer, and Counter Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler. Counter Mode allows a timer to be clocked in reference to external events. Pulse width or duty cycle measurement is supported in Gated Timer Mode where the operation of a timer is controlled by the 'gate' level on an external input pin. Each timer has one associated port pin (Tx-IN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 200 ns (@ 50 MHz CPU clock).

The count direction (up/down) for each timer is programmable by software or can be altered dynamically by an external signal on a port pin (TxEUD). This would to facilitate, for example, position tracking applications.

Timers T3 and T4 have output toggle latches (TxOTL) which change their state on each timer over-flow/underflow. The state of these latches may be output on port pins (TxOUT) for applications such as time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4, triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

GPT2

With its maximum resolution of 100 ns (@ 50 MHz CPU clock), the GPT2 module provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported by the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, or may be output on a port pin (T6OUT). The overflows/underflows of timer T6 can also be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register. The CAPREL register captures the contents of T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.
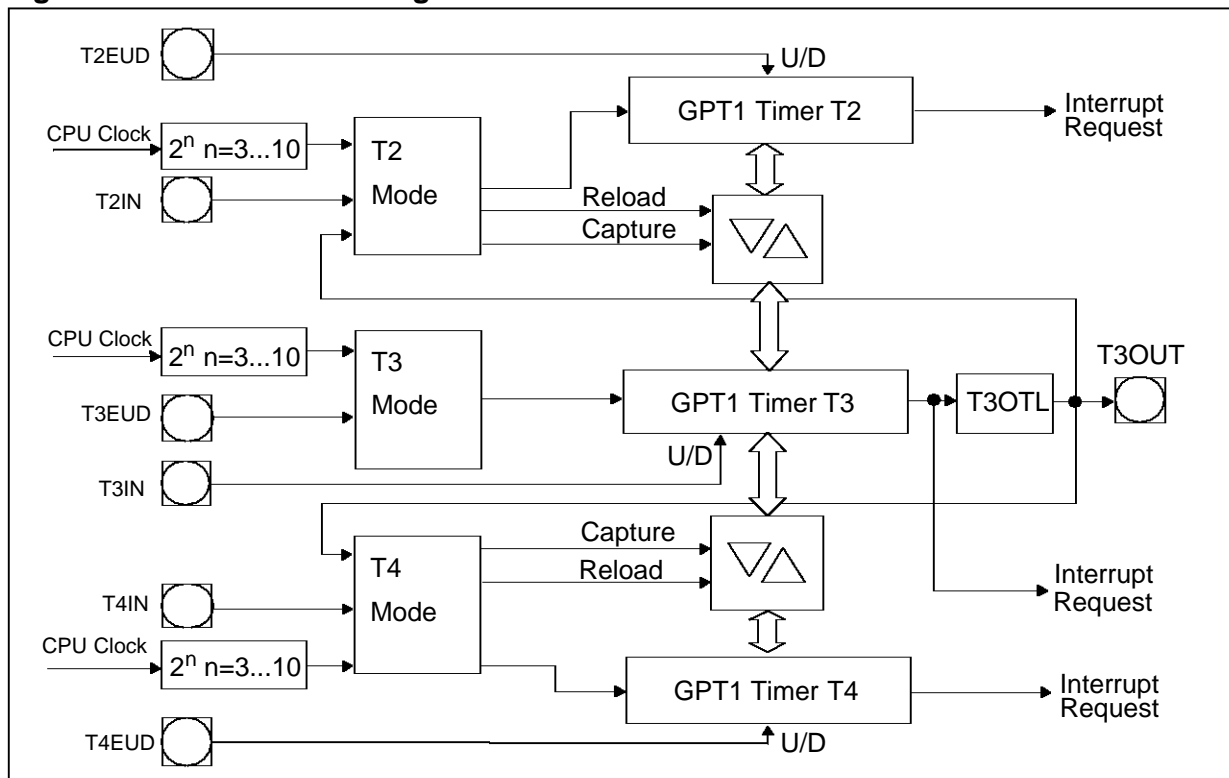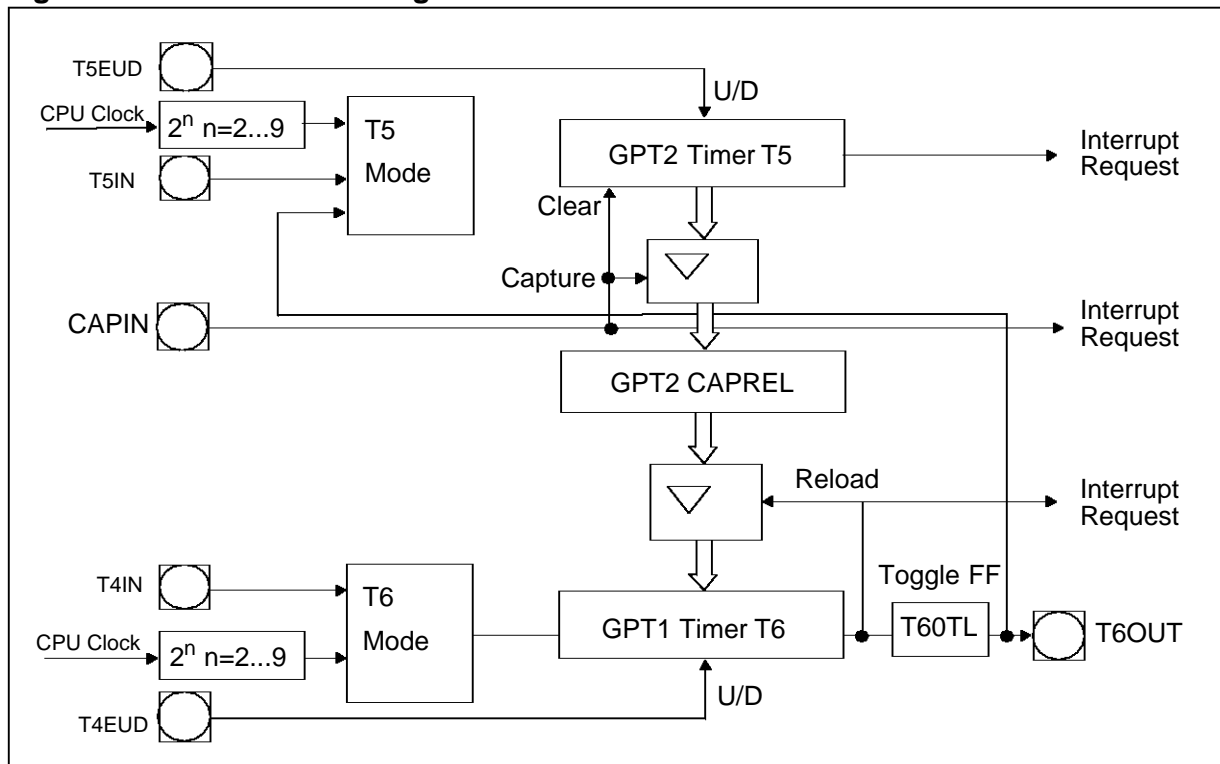
Figure 11.1   GPT1 block diagram

Figure 11.2   GPT2 block diagram

12 Serial Channels

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces, an Asynchronous/Synchronous Serial Channel (ASC0) and a Synchronous Serial Port (SSP).

ASC0 supports full-duplex asynchronous communication up to 625 KBaud and half-duplex synchronous communication up to 16 Mbaud (8 Mbaud on the ASC0) @ 50MHz system clock.

A dedicated baud rate generator makes it possible to set up all standard baud rates without oscillator tuning. For transmission, reception, and erroneous reception, 3 separate interrupt vectors are provided for ASC0. In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data + wake up bit mode).

In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The ASC0 always shifts the LSB first. A loop back option is available for testing purposes.

A number of optional hardware error detection capabilities have been included to increase the reliability of data transfers. A parity bit can be generated automatically on transmission, or checked on reception. Framing error detection recognizes data frames with missing stop bits. An overrun error is generated if the last character received was not read out of the receive buffer register at the time the reception of a new character is complete.

SSP transmits 1...3 bytes, or receives 1 byte, after synchronously sending 1...3 bytes to a shift clock which is generated by the SSP. The SSP can start shifting with the LSB or with the MSB, and selects shifting and latching clock edges as well as the clock polarity. To direct data transfers to one or both of two peripheral devices, up to two chip select lines may be activated.

One general interrupt vector is provided for the SSP.

The SSP is implemented as an Xperipheral onto the XBUS in the address range 00EF00h - 00EFFFh, a 256Byte range (10 byte addresses used). It is connected via a 16-bit demultiplexed bus, without waitstates, allowing word and byte accesses via the CPU or the PEC.

Bit 2 of control register SYSCON serves as an enable/disable control for the SSP module. This bit is named XSSPEN (Xperipheral SSP ENable Control). After reset, this bit is set to '0', so the SSP is disabled. The four upper pins of Port4 can then be used for segment address lines or general purpose IOs. In order to use the SSP, bit XSSPEN must be first set to '1'. Note that SYSCON registercan only be written to during the initialization phase after a reset, until the EINIT instruction is executed. After the EINIT instruction. The SYSCON register is locked against modifications until the next reset.

When the SSP is enabled, the four upper pins of Port4 can not be used as general purpose IO. The segment address selection done via the system start-up configuration during reset has priority and overrides the SSP functions on these pins.

13 Watchdog Timer

The Watchdog Timer is a fail-safe mechanism. It limits the maximum malfunction time of the controller

The Watchdog Timer is always enabled after device reset and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. In this way the chip's start-up procedure is always monitored. The software must be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to maintain the Watchdog Timer, it will overflow generating an internal hardware reset and pulling the $\overline{\text{RSTOUT}}$ pin low to reset external hardware components.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided either by 2 or by 128. The high byte of the Watchdog Timer register can be set to a pre-specified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Therefore, time intervals between 10.2μs and 168ms can be monitored (@ 50MHz CPU clock).

14 System Reset

The internal system reset function initializes the ST10R262 into a defined default state. System reset is invoked in the following ways:

- Hardware reset signal on pin $\overline{RSTIN}$ (Hardware Reset Input)

- Execution of the SRST instruction (Software Reset)

- Overflow of the watchdog timer

On system reset, the microcontroller is reset into its predefined default state through an internal reset procedure (Warm hardware reset, software and watchdog resets) or asynchronously with $\overline{RSTIN}$ (Asynchronous Reset).

The Asynchronous reset condition is defined by a low level on Vpp pin while $\overline{RSTIN}$ pin is asserted, while a Warm Hardware Reset (synchronized to the CPU clock) is defined by a high level on Vpp pin. As long as the $\overline{RSTIN}$ pin is asserted, a weak internal pull-down is turned on the Vpp pin.

When an asynchronous reset is initiated, the microcontroller is immediately (asynchronously) reset into its predefined default state, and does not require a stabilized clock signal on XTAL1 pin. When this asynchronous reset condition is removed, the microcontroller starts program execution from memory location 00'0000h in code segment zero.

When other than asynchronous reset is initiated, pending internal hold states are cancelled and the current internal access cycle (if any) is completed. An external bus cycle is aborted, except for a watchdog reset (see description). After that, the internal reset sequence starts, the bus pin drivers and the IO pin drivers are switched off (tristate), and the PORT0 pins are internally pulled high. The $\overline{RSTIN}$ pin is driven low for 512 CPU clock cycles.

The internal reset sequence duration is 512 CPU clock cycles. $\overline{RSTOUT}$ is activated and remains active until the execution of the EINIT instruction. The CPU and peripherals are set in their predefined default state.

The internal reset condition is active for the duration of the reset sequence and then until the $\overline{RSTIN}$ input is inactive. When this internal reset condition is removed (reset sequence complete and $\overline{RSTIN}$ inactive), the reset configuration is latched from PORT0, and pins ALE, $\overline{RD}$ and $\overline{WR}$ are driven to their inactive levels.

After the internal reset condition is removed, the microcontroller will start program execution from memory location 00'0000h in code segment zero. This start location will typically hold a branch instruction to the start of a software initialization routine for the application specific configuration of peripherals and CPU Special Function Registers.

15 Power Reduction Modes

Two different power reduction modes with different levels of power reduction have been implemented in the ST10R262, which may be entered under software control.

In **Idle mode** the CPU is stopped, while the peripherals continue their operation. Idle mode can be terminated by any reset or interrupt request.

In **Power Down mode** both the CPU and the peripherals are stopped. Power Down mode can now be configured by software in order to be terminated only by a hardware reset or by an external interrupt source on fast external interrupt pins.

All external bus actions are completed before Idle or Power Down mode is entered. However, Idle or Power Down mode is **not** entered if READY is enabled, but has not been activated (driven low for negative polarity, or driven high for positive polarity) during the last bus access.

16 Special Function Register Overview

The following table lists all of the ST10R262 SFRs in alphabetical order. Bit-addressable SFRs are marked with the letter "b" in column "Name". SFRs within the Extended SFR-Space (ESFRs) are marked with the letter "E" in column "Physical Address".

A SFR can be specified by its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or by its short 8-bit address (without using the Data Page Pointers).

Table 16.1   Special function register list

Name	Physical Address	8-Bit Address	Description	Reset Value
ADDRSEL1	FE18h	0Ch	Address Select Register 1	0000h
ADDRSEL2	FE1Ah	0Dh	Address Select Register 2	0000h
ADDRSEL3	FE1Ch	0Eh	Address Select Register 3	0000h
ADDRSEL4	FE1Eh	0Fh	Address Select Register 4	0000h
BUSCON0 b	FF0Ch	86h	Bus Configuration Register 0	0XX0h
BUSCON1 b	FF14h	8Ah	Bus Configuration Register 1	0000h
BUSCON2 b	FF16h	8Bh	Bus Configuration Register 2	0000h
BUSCON3 b	FF18h	8Ch	Bus Configuration Register 3	0000h
BUSCON4 b	FF1Ah	8Dh	Bus Configuration Register 4	0000h
CAPREL	FE4Ah	25h	GPT2 Capture/Reload Register	0000h
CC8IC b	FF88h	C4h	EX0IN Interrupt Control Register	0000h
CC9IC b	FF8Ah	C5h	EX1IN Interrupt Control Register	0000h
CC10IC b	FF8Ch	C6h	EX2IN Interrupt Control Register	0000h
CC11IC b	FF8Eh	C7h	EX3IN Interrupt Control Register	0000h
CP	FE10h	08h	CPU Context Pointer Register	FC00h
CRIC b	FF6Ah	B5h	GPT2 CAPREL Interrupt Control Register	0000h
CSP	FE08h	04h	CPU Code Segment Pointer Register (read only)	0000h
DP0L b	F100h E	80h	P0L Direction Control Register	00h
DP0H b	F102h E	81h	P0h Direction Control Register	00h
DP1L b	F104h E	82h	P1L Direction Control Register	00h
DP1H b	F106h E	83h	P1h Direction Control Register	00h
DP2 b	FFC2h	E1h	Port 2 Direction Control Register	-0--h
DP3 b	FFC6h	E3h	Port 3 Direction Control Register	0000h
DP4 b	FFCAh	E5h	Port 4 Direction Control Register	00h
DP6 b	FFCEh	E7h	Port 6 Direction Control Register	00h
DP7 b	FFD2h	E9h	Port 7 Direction Control Register	-0h
DPP0	FE00h	00h	CPU Data Page Pointer 0 Register (10 bits)	0000h
DPP1	FE02h	01h	CPU Data Page Pointer 1 Register (10 bits)	0001h
DPP2	FE04h	02h	CPU Data Page Pointer 2 Register (10 bits)	0002h

Table 16.1   Special function register list (cont'd)

Name		Physical Address	8-Bit Address	Description	Reset Value
DPP3		FE06h	03h	CPU Data Page Pointer 3 Register (10 bits)	0003h
EXICON	b	F1C0h E	E0h	External Interrupt Control Register	0000h
IDCHIP		F07Ch E	3Eh	Device Identifier Register	ref Table 8.1
IDMANUF		F07Eh E	3Fh	Manufacturer Identifier Register	0400h
IDMEM		F07Ah E	3Dh	On-chip Memory Identifier Register	0000h
IDPROG		F078h E	3Ch	Programming Voltage Identifier Register	0000h
IDX0	b	FF08h	84h	MAC Unit Address Pointer 0	0000h
IDX1	b	FF0Ah	85h	MAC Unit Address Pointer 1	0000h
MAH		FE5Eh	2Fh	MAC Unit Accumulator - High Word	0000h
MAL		FE5Ch	2Eh	MAC Unit Accumulator - Low Word	0000h
MCW		FFDCh	EEh	MAC Unit Control Word	0000h
MDC	b	FF0Eh	87h	CPU Multiply Divide Control Register	0000h
MDH		FE0Ch	06h	CPU Multiply Divide Register – High Word	0000h
MDL		FE0Eh	07h	CPU Multiply Divide Register – Low Word	0000h
MRW	b	FFDAh	EDh	MAC Unit Repeat Word	0000h
MSW	b	FFDEh	EFh	MAC Unit Status Word	0200h
ODP2	b	F1C2h E	E1h	Port 2 Open Drain Control Register	-0--h
ODP3	b	F1C6h E	E3h	Port 3 Open Drain Control Register	0000h
ODP6	b	F1CEh E	E7h	Port 6 Open Drain Control Register	00h
ODP7	b	F1D2h E	E9h	Port 7 Open Drain Control Register	-0h
ONES		FF1Eh	8Fh	Constant Value 1's Register (read only)	FFFFh
P0L	b	FF00h	80h	Port 0 Low Register (Lower half of PORT0)	00h
P0H	b	FF02h	81h	Port 0 High Register (Upper half of PORT0)	00h
P1L	b	FF04h	82h	Port 1 Low Register (Lower half of PORT1)	00h
P1H	b	FF06h	83h	Port 1 High Register (Upper half of PORT1)	00h
P2	b	FFC0h	E0h	Port 2 Register (4 bits)	-0--h
P3	b	FFC4h	E2h	Port 3 Register	0000h
P4	b	FFC8h	E4h	Port 4 Register (8 bits)	00h
P5	b	FFA2h	D1h	Port 5 Register (read only)	XXXXh
P6	b	FFCCh	E6h	Port 6 Register (8 bits)	00h
P7	b	FFD0h	E8h	Port 7Register (4 bits)	-0h
PECC0		FEC0h	60h	PEC Channel 0 Control Register	0000h
PECC1		FEC2h	61h	PEC Channel 1 Control Register	0000h
PECC2		FEC4h	62h	PEC Channel 2 Control Register	0000h
PECC3		FEC6h	63h	PEC Channel 3 Control Register	0000h
PECC4		FEC8h	64h	PEC Channel 4 Control Register	0000h
PECC5		FECAh	65h	PEC Channel 5 Control Register	0000h

Table 16.1   Special function register list (cont'd)

Name		Physical Address	8-Bit Address	Description	Reset Value
PECC6		FECCh	66h	PEC Channel 6 Control Register	0000h
PECC7		FECEh	67h	PEC Channel 7 Control Register	0000h
PP3		F03Eh E	1Fh	PWM Module Period Register 3	0000h
PSW	b	FF10h	88h	CPU Program Status Word	0000h
PT3		F036h E	1Bh	PWM ModuleUp/Down Count 3	0000h
PW3		FE36h	1Bh	PWM Module Pulse Width Register 3	0000h
PWMCON0	b	FF30h	98h	PWM Module Control Register 0	0000h
PWMCON1	b	FF32h	99h	PWM Module Control Register 1	0000h
PWMIC	b	F17Eh E	BFh	PWM Module Interrupt Control Register	0000h
QR0		F004h E	02h	MAC Unit Offset Register R0 (8 bits)	00h
QR1		F006h E	03h	MAC Unit Offset Register R1 (8 bits)	00h
QX0		F000h E	00h	MAC Unit Offset Register X0 (8 bits)	00h
QX1		F002h E	01h	MAC Unit Offset Register X1 (8 bits)	00h
RP0H	b	F108h E	84h	System Start-up Configuration Register (Rd. only)	XXh
S0BG		FEB4h	5Ah	Serial Channel 0 Baud Rate Generator Reload Reg	0000h
S0CON	b	FFB0h	D8h	Serial Channel 0 Control Register	0000h
S0EIC	b	FF70h	B8h	Serial Channel 0 Error Interrupt Control Register	0000h
S0RBUF		FEB2h	59h	Serial Channel 0 Receive Buffer Register (read only)	XXh
S0RIC	b	FF6Eh	B7h	Serial Channel 0 Receive Interrupt Control Register	0000h
S0TBIC	b	F19Ch E	CEh	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000h
S0TBUF		FEB0h	58h	Serial Channel 0 Transmit Buffer Register(write only)	00h
S0TIC	b	FF6Ch	B6h	Serial Channel 0 Transmit Interrupt Control Register	0000h
SP		FE12h	09h	CPU System Stack Pointer Register	FC00h
SSPCON0		EF00h X	---	SSP Control Register 0	0000h
SSPCON1		EF02h X	---	SSP Control Register 1	0000h
SSPRTB		EF04h X	---	SSP Receive/Transmit Buffer	XXXXh
SSPTBH		EF06h X	---	SSP Transmit Buffer High	XXXXh
STKOV		FE14h	0Ah	CPU Stack Overflow Pointer Register	FA00h
STKUN		FE16h	0Bh	CPU Stack Underflow Pointer Register	FC00h
SYSCON	b	FF12h	89h	CPU System Configuration Register	0xx0h[1]
T2		FE40h	20h	GPT1 Timer 2 Register	0000h
T2CON	b	FF40h	A0h	GPT1 Timer 2 Control Register	0000h
T2IC	b	FF60h	B0h	GPT1 Timer 2 Interrupt Control Register	0000h
T3		FE42h	21h	GPT1 Timer 3 Register	0000h
T3CON	b	FF42h	A1h	GPT1 Timer 3 Control Register	0000h
T3IC	b	FF62h	B1h	GPT1 Timer 3 Interrupt Control Register	0000h
T4		FE44h	22h	GPT1 Timer 4 Register	0000h

Table 16.1   Special function register list (cont'd)

Name		Physical Address	8-Bit Address	Description	Reset Value
T4CON	**b**	FF44h	A2h	GPT1 Timer 4 Control Register	0000h
T4IC	**b**	FF64h	B2h	GPT1 Timer 4 Interrupt Control Register	0000h
T5		FE46h	23h	GPT2 Timer 5 Register	0000h
T5CON	**b**	FF46h	A3h	GPT2 Timer 5 Control Register	0000h
T5IC	**b**	FF66h	B3h	GPT2 Timer 5 Interrupt Control Register	0000h
T6		FE48h	24h	GPT2 Timer 6 Register	0000h
T6CON	**b**	FF48h	A4h	GPT2 Timer 6 Control Register	0000h
T6IC	**b**	FF68h	B4h	GPT2 Timer 6 Interrupt Control Register	0000h
TFR	**b**	FFACh	D6h	Trap Flag Register	0000h
WDT		FEAEh	57h	Watchdog Timer Register (read only)	0000h
WDTCON		FFAEh	D7h	Watchdog Timer Control Register	000xh[2]
XP1IC	**b**	F18Eh $_E$	C7h	SSP Interrupt Control Register	0000h
XP3IC	**b**	F19Eh $_E$	CFh	PLL unlock Interrupt Control Register	0000h
ZEROS	**b**	FF1Ch	8Eh	Constant Value 0's Register (read only)	0000h

Notes   1:   The system configuration is selected during reset.

2:   Bit WDTR indicates a watchdog timer triggered reset.

17 Electrical Characteristics

17.1 Absolute Maximum Ratings

- Ambient temperature under bias (T_A): . . . . 0 to +70 °C
- Storage temperature (T_{ST}): . . . . − 65 to +150 °C
- Voltage on V_{DD} pins with respect to ground (V_{SS}): . . . . 0.5 to +6.5 V
- Voltage on any pin with respect to ground (V_{SS}): . . . . −0.5 to V_{DD} +0.5 V
- Input current on any pin during overload condition: . . . . −10 to +10 mA
- Absolute sum of all input currents during overload condition: . . . . |100 mA|
- Power dissipation: . . . . 2.5 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions (V_{IN}>V_{DD} or V_{IN}<V_{SS}) the voltage on pins with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.

17.2 Parameter Interpretation

The parameters listed in the Electrical Characteristics tables 17.1 to 17.10 represent the characteristics of the ST10X262 and its demands on the system.

Where the ST10X262 logic provides signals with their respective timing characteristics, the symbol "CC" for Controller Characteristics, is included in the "Symbol" column.

Where the external system must provide signals with their respective timing characteristics to the ST10X262, the symbol "SR" for System Requirement, is included in the "Symbol" column.

17.3 DC Characteristics

V_{DD} = 5 V 10%,V_{SS} = 0 V, f_{CPU} = 50 MHz, Reset active, T_A = 0 to +70 °C

Table 17.1   DC characteristircs

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage	$V_{IL}SR$	− 0.5	$0.2\,V_{DD}$ − 0.1	V	–
Input high voltage (all except $\overline{RSTIN}$ and XTAL1)	$V_{IH}SR$	$0.2\,V_{DD}$ + 0.9	V_{DD} + 0.5	V	–
Input high voltage $\overline{RSTIN}$	$V_{IH}1SR$	$0.6\,V_{DD}$	V_{DD} + 0.5	V	–
Input high voltage XTAL1	$V_{IH}2SR$	$0.7\,V_{DD}$	V_{DD} + 0.5	V	–
Output low voltage (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	$V_{OL}CC$	–	0.45	V	I_{OL} = 2.4 mA
Output low voltage (all other outputs)	$V_{OL1}CC$	–	0.45	V	I_{OL1} = 1.6 mA
Output high voltage (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	$V_{OH}CC$	$0.9\,V_{DD}$ 2.4	–	V	I_{OH} = − 500 A I_{OH} = −2.4 mA
Output high voltage [1] (all other outputs)	$V_{OH1}CC$	$0.9\,V_{DD}$ 2.4	–	V V	I_{OH} = − 250 A I_{OH} = − 1.6 mA
Input leakage current	$I_{OZ}CC$	–	10	A	0 V < V_{IN} < V_{DD}
$\overline{RSTIN}$ pull-up resistor [5]	$R_{RST}CC$	50	150	kohm	–
Read/Write inactive current [4]	I_{RWH} [2]	–	-40	A	V_{OUT} = 2.4 V
Read/Write active current [4]	I_{RWL} [3]	-500	–	A	V_{OUT} = V_{OLmax}
ALE inactive current [4]	I_{ALEL} [2]	–	40	A	V_{OUT} = V_{OLmax}
ALE active current [4]	I_{ALEH} [3]	500	–	A	V_{OUT} = 2.4 V
Port 6 inactive current [4]	I_{P6H} [2]	–	-40	A	V_{OUT} = 2.4 V
Port 6 active current [4]	I_{P6L} [3]	-500	–	A	V_{OUT} = V_{OL1max}
PORT0 configuration current [4]	I_{P0H} [2]	–	-10	A	V_{IN} = V_{IHmin}
	I_{P0L} [3]	-100	–	A	V_{IN} = V_{ILmax}
XTAL1 input current	$I_{IL}CC$	–	20	A	0 V < V_{IN} < V_{DD}
Pin capacitance [5] (digital inputs/outputs)	$C_{IO}CC$	–	10	pF	f = 1 MHz T_A = 25 °C
Power supply current	I_{CC}	–	20 + 4 * f_{CPU}	mA	f_{CPU} in [MHz] [6]
Idle mode supply current	I_{ID}	–	5 + 1.5 * f_{CPU}	mA	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz] [6]
Power-down mode supply current	I_{PD}	–	50	A	V_{DD} = 5.5 V [7]

Notes 1: Notes:This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

2: The maximum current may be drawn while the respective signal line remains inactive.

3: The minimum current must be drawn in order to drive the respective signal line active.

4: This specification is only valid during Reset, or during Hold- or Adapt-mode. Port 6 pins are only affected, if they are used for $\overline{CS}$ output and the open drain function is not enabled.

5: Not 100% tested, guaranteed by design characterization.

6: The supply current is a function of the operating frequency. This dependency is illustrated in the figure below.
These parameters are tested at V_{DDmax} and 50 MHz CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH} with a infinite execution of NOP instruction fetched from external memory.

7: This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at $V_{DD} - 0.1$ V to V_{DD}, $V_{REF} = 0$ V, all outputs (including pins configured as outputs) disconnected.

Figure 17.1   Supply/idle current as a function of operating frequency
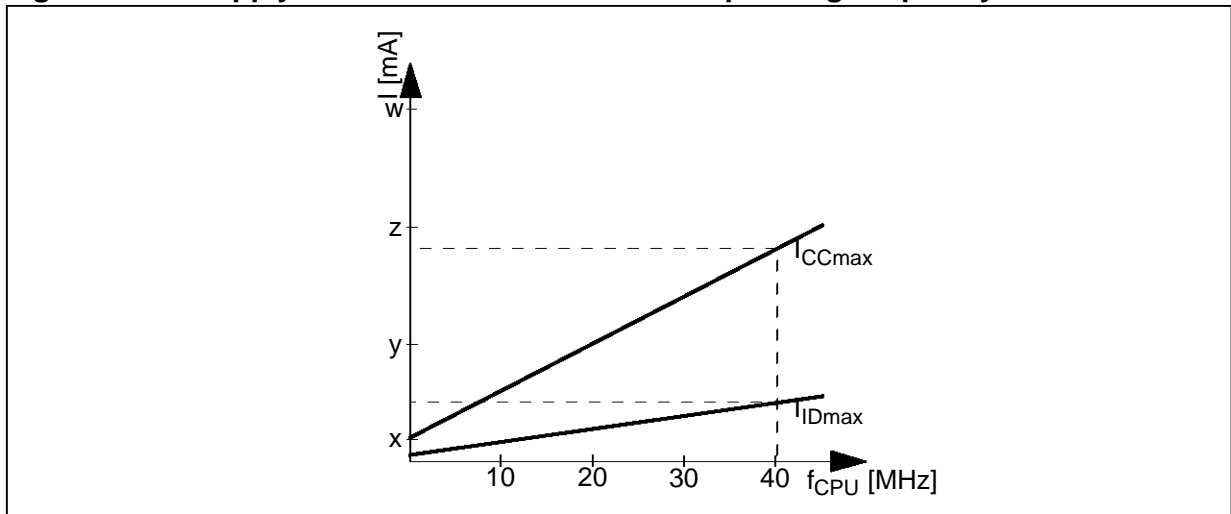
17.4 AC Characteristics

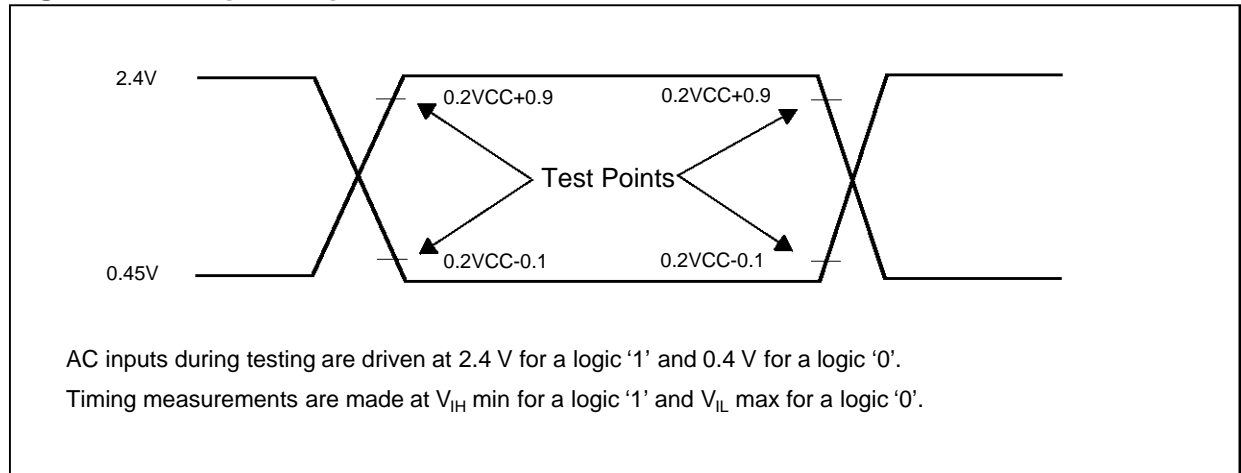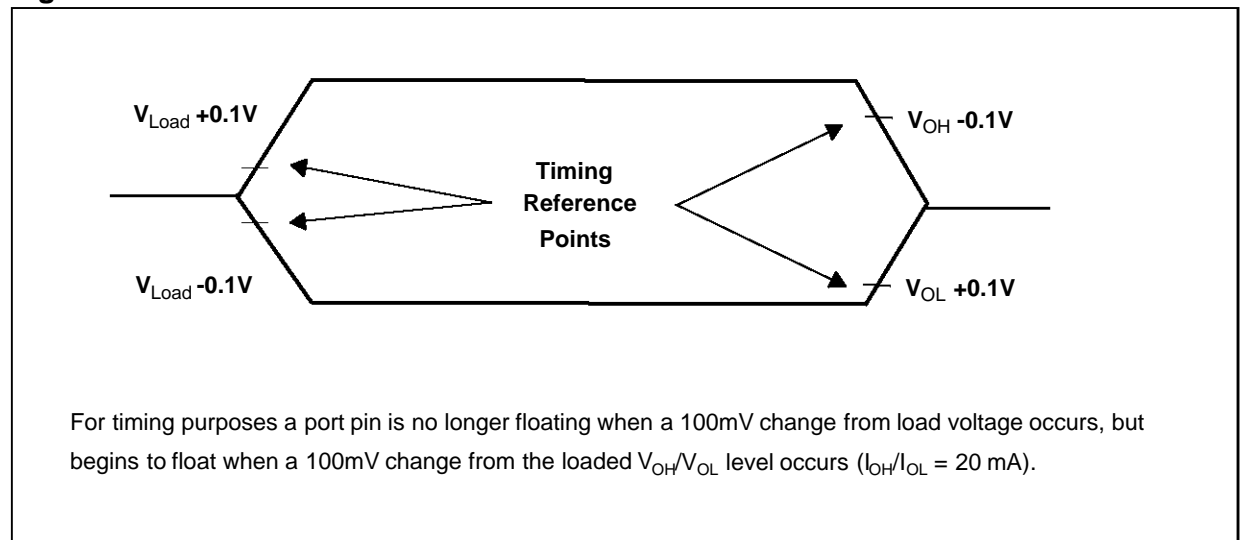## 17.4.1 Test waveforms

Figure 17.2 Input output waveforms

AC inputs during testing are driven at 2.4 V for a logic '1' and 0.4 V for a logic '0'.

Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

Figure 17.3 Float waveforms

For timing purposes a port pin is no longer floating when a 100mV change from load voltage occurs, but begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

17.4.2 Definition of internal timing

The internal operation of the ST10X262 is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (eg. pipeline) or external (eg. bus cycles) operations.

The external timing (AC Characteristics) depend on the time (TCL) between two consecutive edges of the CPU clock. The CPU clock f_{CPU} can be generated by different mechanisms. The duration of TCL and its variation (and hence the derived external timing) depends on the mechanism used to generate f_{CPU}. Figure 17.4 shows the CPU clock for direct drive, prescaler or PLL operations. This must be taken into account when calculating the timings for the ST10X262.

Figure 17.4   Generation mechanisms for the cpu clock
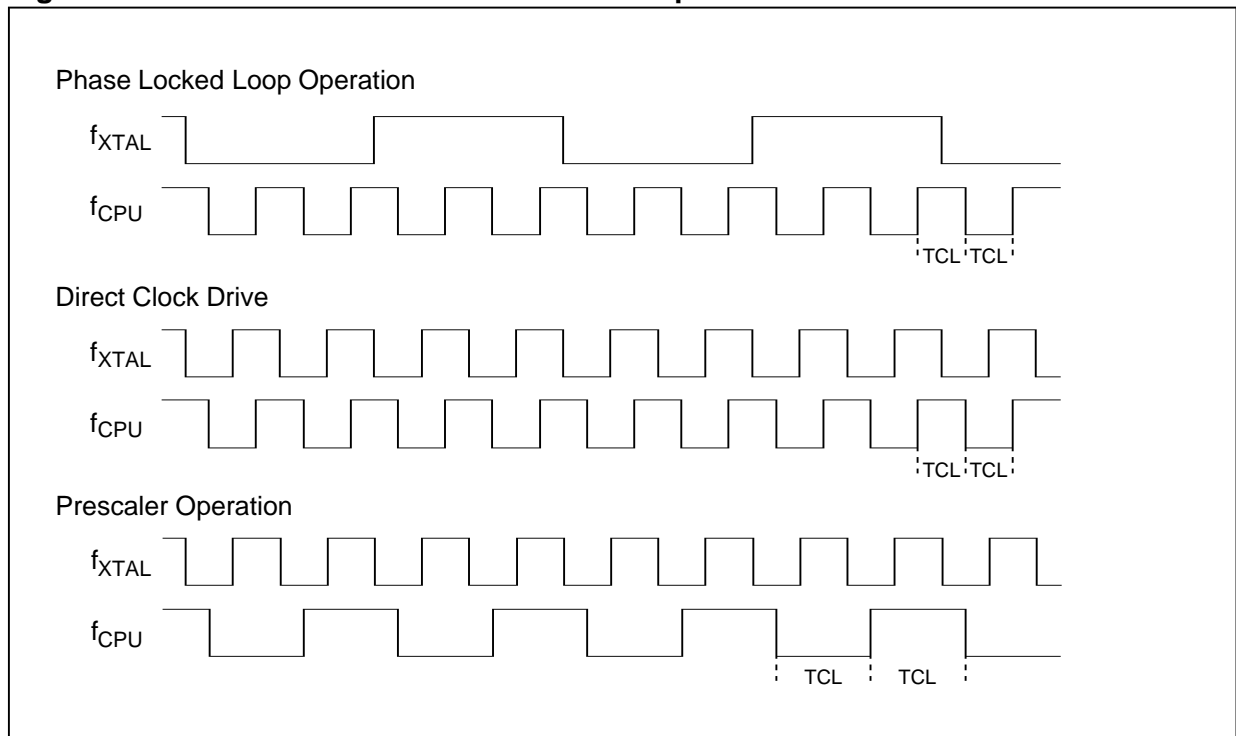
Note: The example for PLL operation shown in Figure 17.4 refers to a PLL factor of 4.

17.4.3 Clock generation modes

The mechanism used to generate the CPU clock is selected during reset by the logic levels on Port 0 pins P0.15-13 (P0H.7-5). The following table relates the combinations of these three bits to the respective clock generation mode: prescaler operation, direct drive and phase locked loop.

Table 17.2   Clock generation modes

P0.15-13 (P0H.7-5)			CPU Frequency $f_{CPU} = f_{XTAL} * F$	External Clock Input Range [1]	Notes
1	1	1	$F_{XTAL} * 4$	2.5 to 10 MHz	Default configuration
1	1	0	$F_{XTAL} * 3$	3.33 to 13.33 MHz	
1	0	1	$F_{XTAL} * 2$	5 to 20 MHz	
1	0	0	$F_{XTAL} * 5$	2 to 8 MHz	
0	1	1	$F_{XTAL} * 1$	1 to 50 MHz	Direct drive [2]
0	1	0	$F_{XTAL} * 1.5$	6.66 to 26.6 MHz	
0	0	1	$F_{XTAL} / 2$	2 to 80 MHz	CPU clock via prescaler
0	0	0	$F_{XTAL} * 2.5$	4 to 16 MHz	

Notes 1: The external clock input range refers to a CPU clock range of 10...50 MHz.

2: The maximum depends on the duty cycle of the external clock signal.

17.4.4 Prescaler operation

When pins P0.15-13 (P0H.7-5) equal '001' during reset the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.

The frequency of f_{CPU} is half the frequency of f_{XTAL} and the high and low time of f_{CPU} (ie. the duration of an individual TCL) is defined by the period of the input clock f_{XTAL}.

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of f_{XTAL} for any TCL.

Note that if the the bit OWDDIS in SYSCON register is cleared, the PLL is running on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

17.4.5 Direct drive

When pins P0.15-13 (P0H.7-5) equal '011' during reset, the on-chip phase locked loop is disabled and the CPU clock is driven from the internal oscillator with the input clock signal. The frequency of f_{CPU} directly follows the frequency of f_{XTAL} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{XTAL}.

The TCL timings listed below must, therefore, be calculated using the minimum possible TCL. This minimum value can be calculated via the following formula:

$$TCL_{min} = 1/f_{XTAL} \times DC_{min}$$
$$DC = dutycycle$$

For two consecutive TCLs, the deviation caused by the duty cycle of f_{XTAL} is compensated so that the duration of 2TCL is always $1/f_{XTAL}$. The minimum value TCL_{min}, therefore has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula:

$$2TCL = 1/f_{XTAL}$$

The address float timings in Multiplexed bus mode (t_{11} and t_{45}) use the maximum duration of TCL ($TCL_{max} = 1/f_{XTAL} * DC_{max}$) instead of TCL_{min}.

If the the bit OWDDIS in SYSCON register is cleared, the PLL is running on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

17.4.6 Oscillator watchdog (OWD)

When the direct drive or direct drive with prescaler, clock option is selected, an oscillator watchdog is implemented. This provides a fail safe mechanism in case of a loss of the external clock. The oscillator watchdog operates as follows:

After a reset, the Oscillator Watchdog is enabled by default. To disable the OWD, the bit OWDDIS (bit 4 of SYSCON register) must be set.

When the OWD is enabled, the PLL runs on its free-running frequency, and increments the Oscillator Watchdog counter. On each transition of XTAL1 pin, the Oscillator Watchdog is cleared. If an external clock failure occurs, then the Oscillator Watchdog counter overflows (after 16 PLL clock cycles). The CPU clock signal will be switched to the PLL free-running clock signal, and the Oscillator Watchdog Interrupt Request (XP3INT) is flagged. The CPU clock will not switch back to the external clock even if a valid external clock exits on XTAL1 pin. Only a hardware reset can switch the CPU clock source back to direct clock input.

When the OWD is disabled, the CPU clock is always fed from the oscillator input and the PLL is switched off to decrease power supply current.

17.4.7 Phase locked loop

For all other combinations of pins P0.15-13 (P0H.7-5), during reset the on-chip phase locked loop is enabled and provides the CPU clock (Figure 17.4). The PLL multiplies the input frequency by the factor F which is selected via the combination of pins P0.15-13 (ie. $f_{CPU} = f_{XTAL} * F$). With every F'th transition of f_{XTAL} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothely, i.e. the CPU clock frequency does not change abruptly.

Due to this adaptation of the input clock, the frequency of fcpu is constantly adjusted so it is locked to f_{XTAL}. The variation causes a jitter of fcpu, which in turn affects the duration of individual TCLs.

The timings listed in the AC Characteristics that refer to TCL must, therefore, be calculated using the minimum TCL that is possible with regard to jitter.

The actual minimum value for TCL depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so that it remains locked to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCL is lower than for one single TCL (see formula and figure below).

For a period of $N * TCL$ the minimum value is computed using the corresponding deviation D_N:

$$TCL_{min} = TCL_{nom} \times (1 - |D_N| / 100)$$

$$D_N = \pm(4 - N / 15)[\%]$$

where N = number of consecutive TCLs and 1 < N < 40. So for a period of 3 TCLs (ie. N = 3):

$$D_3 = 4 - 3 / 15$$

$$= 3.8\%$$

$$3TCL_{min} = 3TCL_{nom} \times 1 - 3.8 / 100$$

$$= 3TCL_{nom} \times 0.962$$

$$36.07 n \sec(f_{cpu} = 50MHz)$$

This is important for bus cycles using waitstates and for example, the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

Figure 17.5 shows the approximated maximumPLL jitter.

Figure 17.5   Approximated maximum PLL jitter
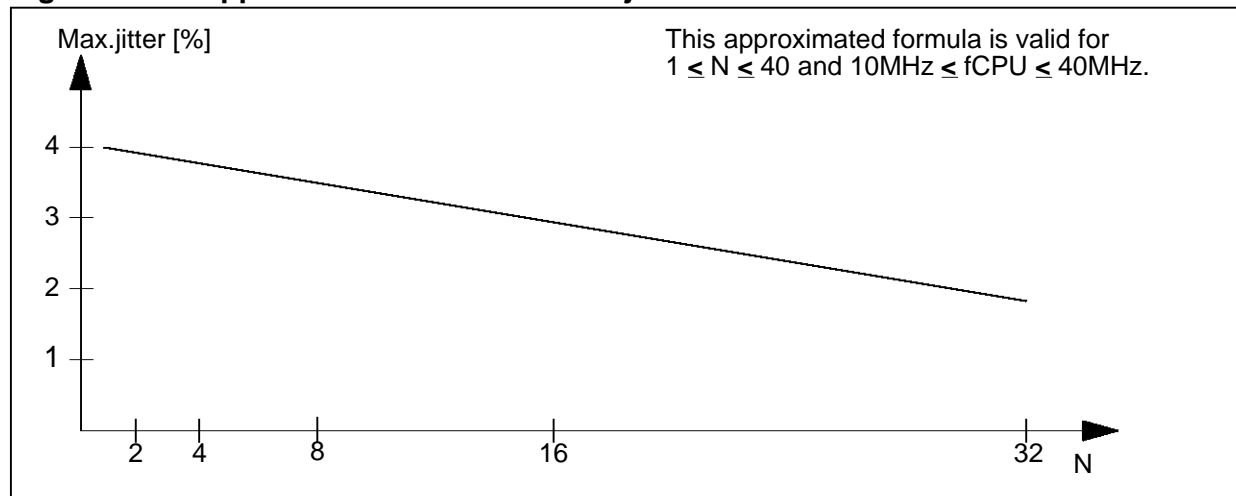
17.4.8   Memory cycle variables

The timing tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Table 17.3   Memory cycle variables

Description	Symbol	Values
ALE Extension	t_A	TCL * <ALECTL>
Memory Cycle Time Waitstates	t_C	2TCL * (15 - <MCTC>)
Memory Tristate Time	t_F	2TCL * (1 - <MTTC>)

17.4.9 External clock drive XTAL1

$V_{DD} = 5$ V   10%, $V_{SS} = 0$ V, $T_A = 0$ to +70 °C

Table 17.4   External clock drive

Parameter	Symbol	$f_{CPU} = f_{XTAL}$		$f_{CPU} = f_{XTAL} / 2$		$f_{CPU} = f_{XTAL} * N$ N = 1.5,/2,/2.5/3/4/5		Unit
		min.	max.	min.	max.	min.	max.	
Oscillator period	$T_{OSC}SR$	$20^{1)2)}$	-	$10^{2)}$	-	$20 * N^{2)}$	$100 * N$	ns
High time	t_1SR	$9^{3)}$	–	$5^{3)}$	–	$9^{3)}$	–	ns
Low time	t_2SR	$9^{3)}$	–	$5^{3)}$	–	$9^{3)}$	–	ns
Rise time	t_3SR	–	$3^{2)}$	–	$5^{3)}$	–	$5^{3)}$	ns
Fall time	t_4SR	–	$3^{2)}$	–	$5^{3)}$	–	$5^{3)}$	ns

Notes 1: Theoretical minimum. The real minimum value depends on the duty cycle of the input clock signal.

2: 25MHz is the maximum input frequency when using an external crystal oscillator (T_{osc} min=40ns), however, 50MHz can be applied with an external clock source (T_{osc} min=10ns)

3: The input clock signal must reach the defined levels V_{IL} and V_{IH2}

Figure 17.6   External clock drive XTAL1
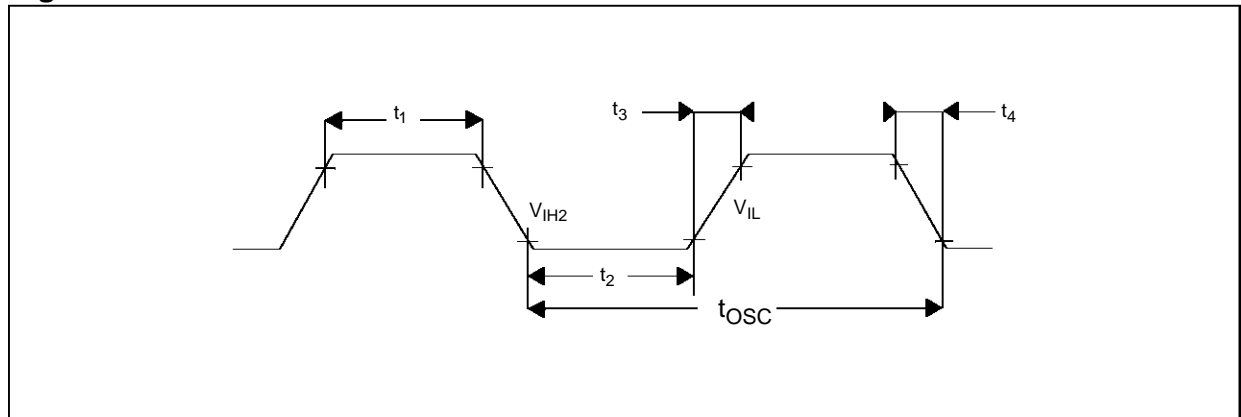
17.4.10 Multiplexed bus

$V_{DD} = 5$ V $\pm$ 10%, $V_{SS} = 0$, $T_A = 0$ to +70 °C
CL (for PORT0, PORT1, Port 4, ALE, RD, WR, BHE, CLKOUT) = 50 pF, CL (for Port 6, CS) = 50 pF
ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (60 ns at 50-MHz CPU clock without waitstates)

Table 17.5   Multiplexed bus

Parameter	Symbol	Max. CPU Clock = 50 MHz		Variable CPU Clock 1/2TCL = 1 to 50 MHz		Unit
		min.	max.	min.	max.	
ALE high time	t_5CC	$5 + t_A$	–	TCL - $5 + t_A$	–	ns
Address setup to ALE	t_6CC	$3 + t_A$	–	TCL - $7 + t_A$	–	ns
Address hold after ALE	t_7CC	$33 + t_A$	–	TCL - $7 + t_A$	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8CC	$5 + t_A$	–	TCL - $5 + t_A$	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9CC	$-5 + t_A$	–	$-5 + t_A$	–	ns
Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	$t_{10}CC$	–	5	–	5	ns
Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	$t_{11}CC$	–	15	–	TCL + 5	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	$t_{12}CC$	$13 + t_C$	–	2TCL - $7 + t_C$	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	$t_{13}CC$	$23 + t_C$	–	3TCL - $7 + t_C$	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	$t_{14}SR$	–	$5 + t_C$	–	2TCL - 15 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	$t_{15}SR$	–	$15 + t_C$	–	3TCL - 15 + t_C	ns
ALE low to valid data in	$t_{16}SR$	–	15 + t_A + t_C	–	3TCL - 15 + t_A + t_C	ns
Address/Unlatched $\overline{CS}$ to valid data in	$t_{17}SR$	–	20 + $2t_A$ + t_C	–	4TCL - 20 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	$t_{18}SR$	0	–	0	–	ns
Data float after $\overline{RD}$	$t_{19}SR$	–	15 + t_F	–	2TCL - 5 + t_F	ns
Data valid to $\overline{WR}$	$t_{22}CC$	$10 + t_C$	–	2TCL - 10 + t_C	–	ns
Data hold after $\overline{WR}$	$t_{23}CC$	$13 + t_F$	–	2TCL - $7 + t_F$	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	$t_{25}CC$	$10 + t_F$	–	2TCL - 10 + t_F	–	ns

Table 17.5 Multiplexed bus (cont'd)

Parameter	Symbol	Max. CPU Clock = 50 MHz		Variable CPU Clock 1/2TCL = 1 to 50 MHz		Unit
		min.	max.	min.	max.	
Address/Unlatched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	$t_{27}CC$	$10 + t_F$	–	$2TCL - 10 + t_F$	–	ns
ALE falling edge to Latched $\overline{CS}$	$t_{38}CC$	$-3 - t_A$	$5 - t_A$	$-3 - t_A$	$3 - t_A$	ns
Latched $\overline{CS}$ low to Valid Data In	$t_{39}SR$	–	$15 + t_C + 2t_A$	–	$3TCL - 15 + t_C + 2t_A$	ns
Latched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	$t_{40}CC$	$20 + t_F$	–	$3TCL - 10 + t_F$	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	$t_{42}CC$	$7 + t_A$	–	$TCL - 3 + t_A$	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	$t_{43}CC$	$-3 + t_A$	–	$-3 + t_A$	–	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	$t_{44}CC$	–	0	–	0	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	$t_{45}CC$	–	10	–	$TCL + 0$	ns
$\overline{RdCS}$ to Valid Data In (with RW delay)	$t_{46}SR$	–	$3 + t_C$	–	$2TCL - 17 + t_C$	ns
$\overline{RdCS}$ to Valid Data In (no RW delay)	$t_{47}SR$	–	$13 + t_C$	–	$3TCL - 17 + t_C$	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW delay)	$t_{48}CC$	$11 + t_C$	–	$2TCL - 9 + t_C$	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW delay)	$t_{49}CC$	$21 + t_C$	–	$3TCL - 9 + t_C$	–	ns
Data valid to $\overline{WrCS}$	$t_{50}CC$	$10 + t_C$	–	$2TCL - 10 + t_C$	–	ns
Data hold after $\overline{RdCS}$	$t_{51}SR$	0	–	0	–	ns
Data float after $\overline{RdCS}$	$t_{52}SR$	–	$12.5 + t_F$	–	$2TCL - 12.5 + t_F$	ns
Address hold after $\overline{RdCS}$, $\overline{WrCS}$	$t_{54}CC$	$10 + t_F$	–	$2TCL - 10 + t_F$	–	ns
Data hold after $\overline{WrCS}$	$t_{56}CC$	$10 + t_F$	–	$2TCL - 10 + t_F$	–	ns

Figure 17.7   External memory cycle:multiplexed bus, with read/write delay, normal ALE
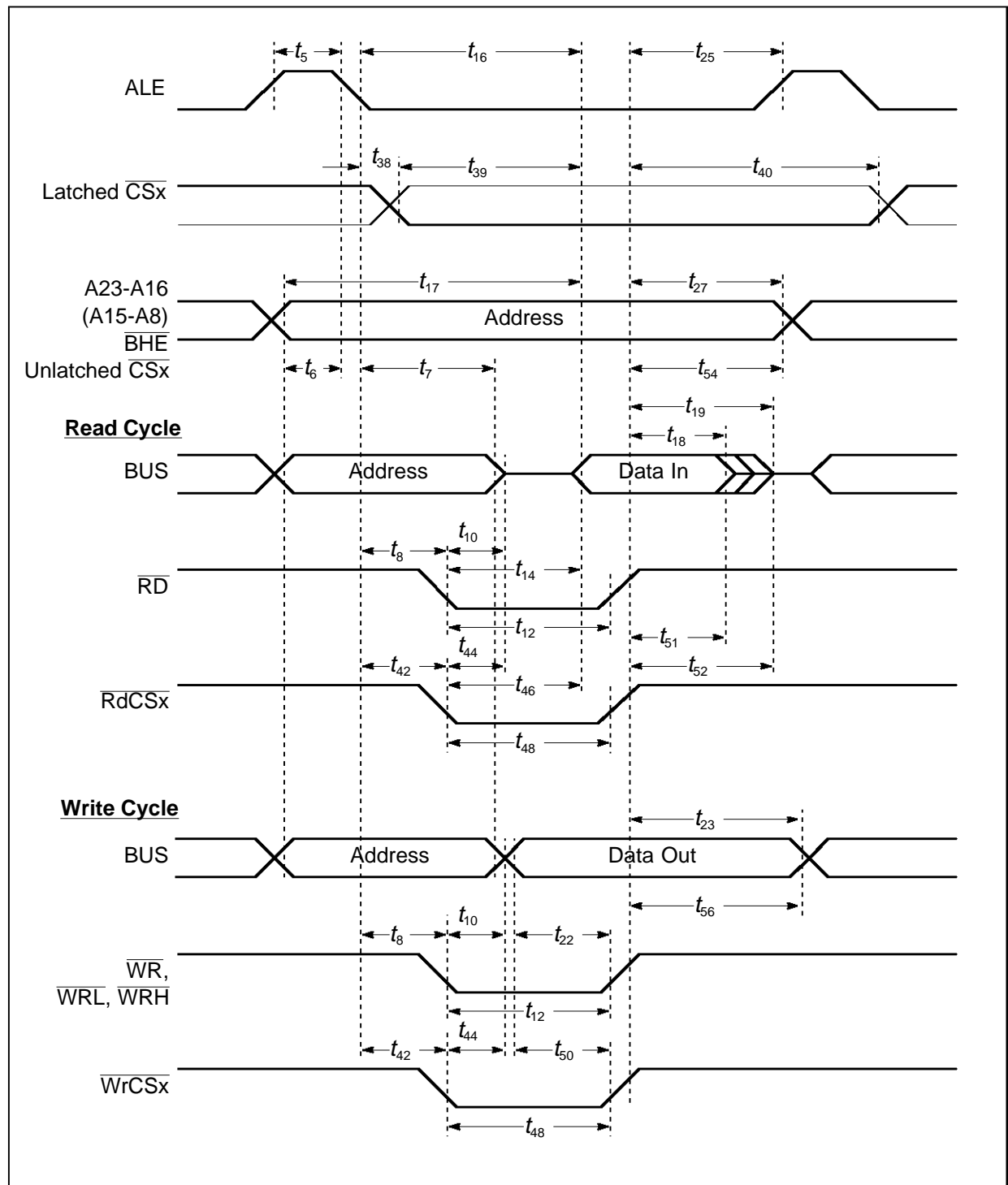
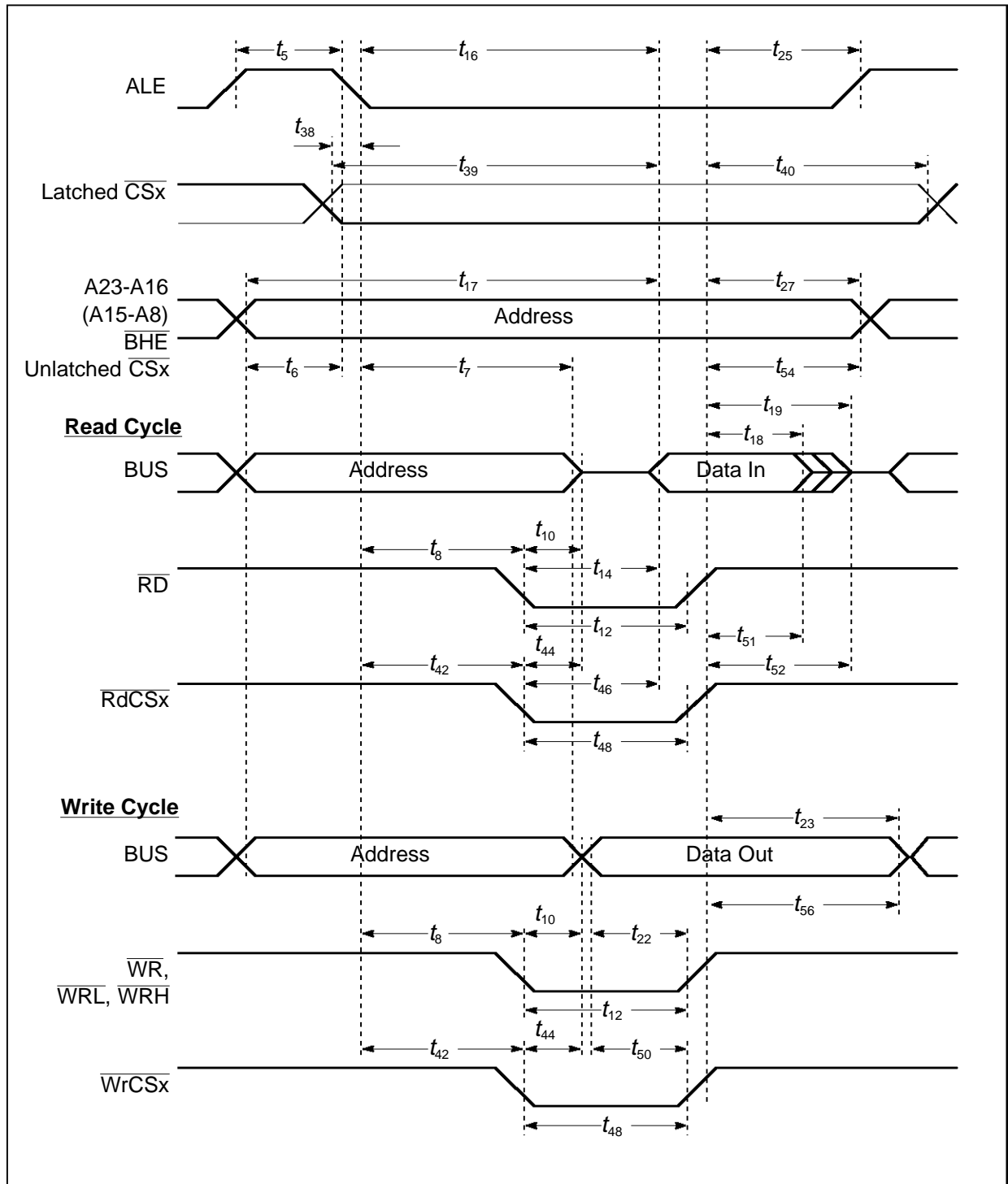**Figure 17.8   External memory cycle:multiplexed bus, with read/write delay, extended ALE**

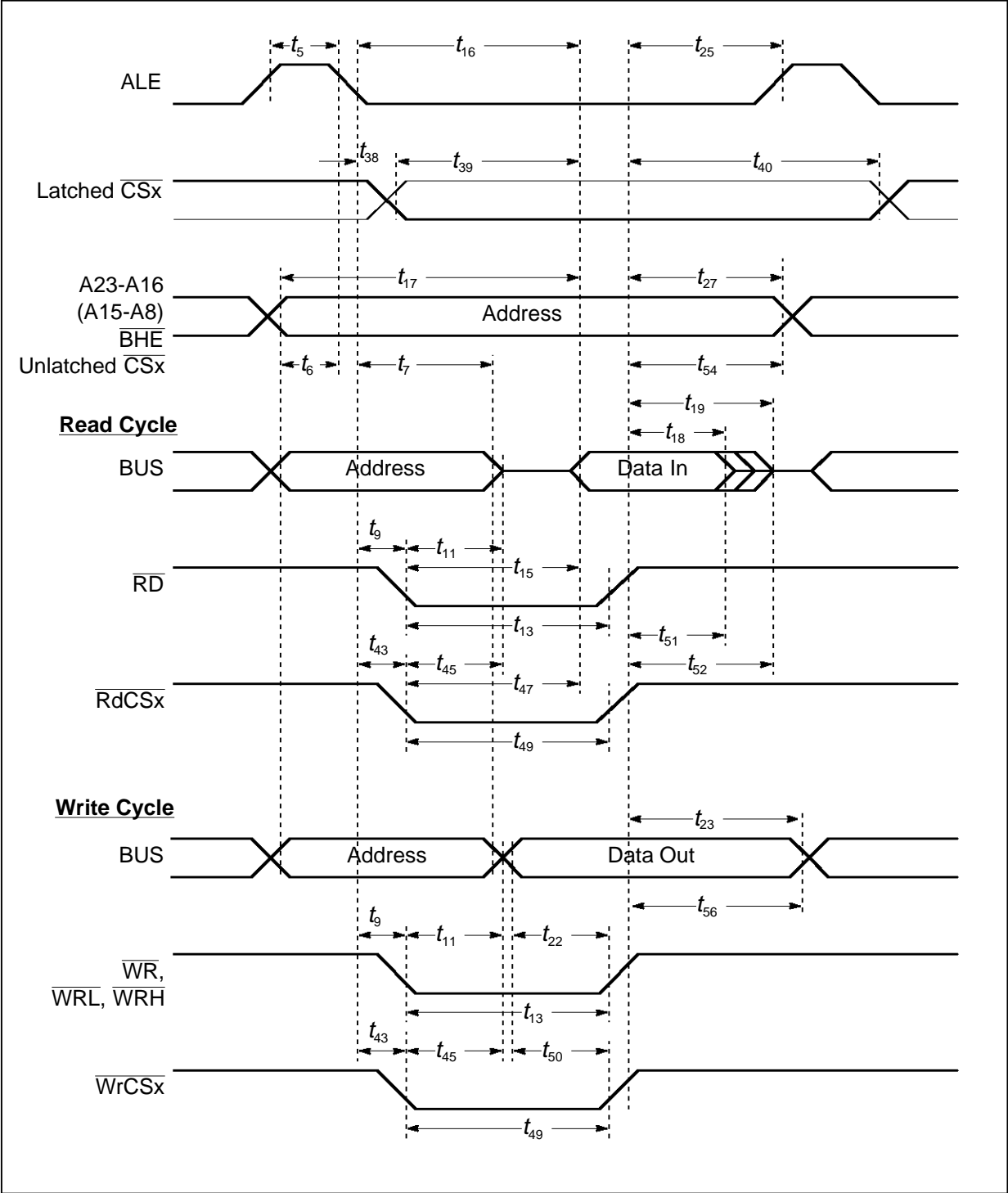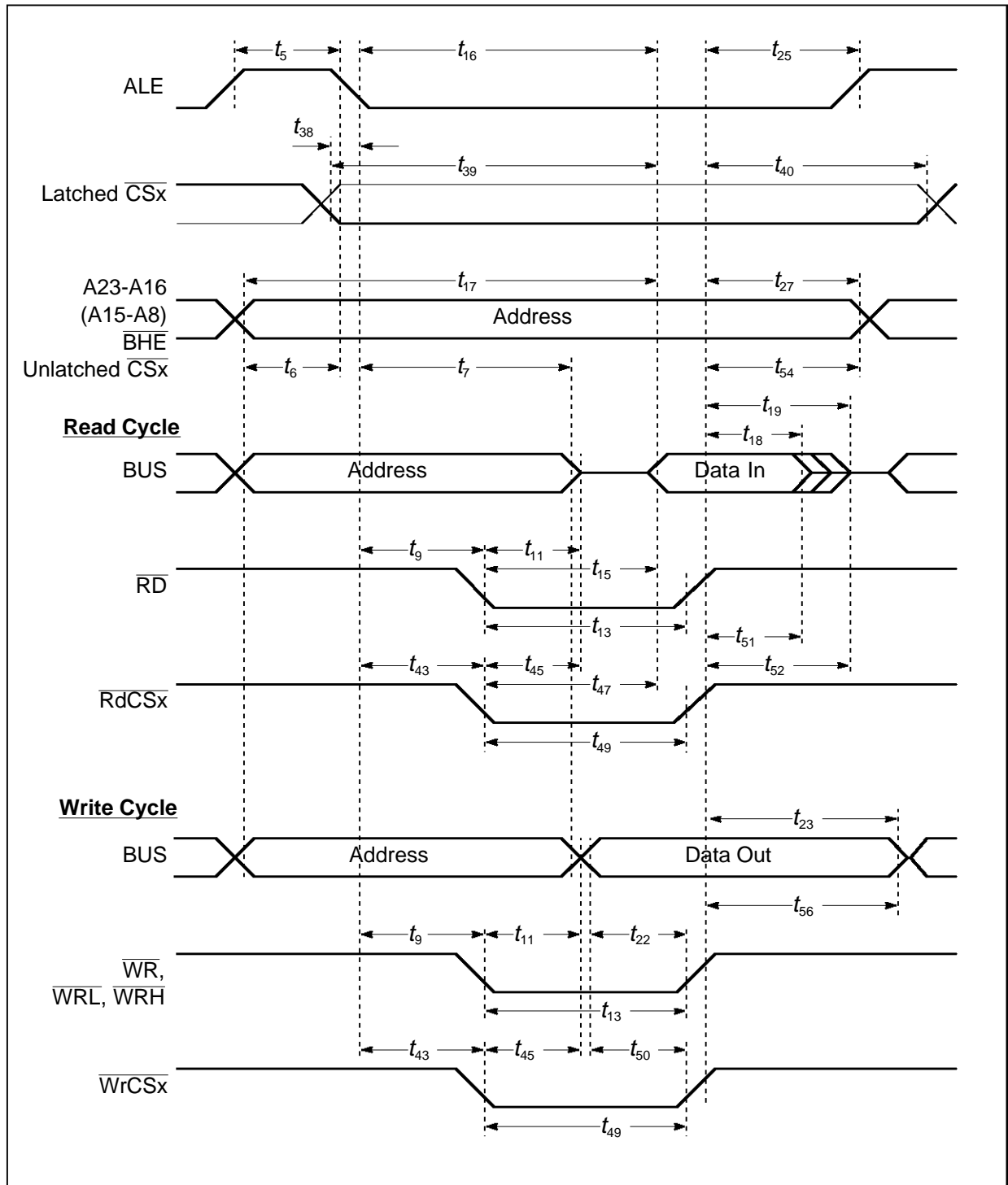**Figure 17.9   External memory cycle:multiplexed bus, no read/write delay, normal ALE**

Figure 17.10 External memory cycle:multiplexed bus, no read/write delay, extended ALE

17.4.11 Demultiplexed bus

V_{DD} = 5 V 10%, V_{SS} = 0 V, T_A = 0 to +70 °C
C_L (for PORT0, PORT1, Port 4, ALE, RD, WR, BHE, CLKOUT) = 50 pF,
C_L (for Port 6, CS) = 50 pF
ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (40 ns at 50 MHz CPU clock without waitstates)

Table 17.6 Demultiplexed bus

Parameter	Symbol	Max. CPU Clock = 50 MHz		Variable CPU Clock 1/2TCL = 1 to 50 MHz		Unit
		min.	max.	min.	max.	
ALE high time	t_5CC	$5 + t_A$	–	$TCL - 5 + t_A$	–	ns
Address setup to ALE	t_6CC	$3 + t_A$	–	$TCL - 7 + t_A$	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8CC	$5 + t_A$	–	$TCL - 5 + t_A$	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9CC	$-5 + t_A$	–	$-5 + t_A$	–	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}CC	$13 + t_C$	–	$2TCL - 7 + t_C$	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}CC	$23 + t_C$	–	$3TCL - 7 + t_C$	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}SR	–	$5 + t_C$	–	$2TCL - 15 + t_C$	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}SR	–	$15 + t_C$	–	$3TCL - 15 + t_C$	ns
ALE low to valid data in	t_{16}SR	–	$15 + t_A + t_C$	–	$3TCL - 15 + t_A + t_C$	ns
Address/Unlatched $\overline{CS}$ to valid data in	t_{17}SR	–	$20 + 2t_A + t_C$	–	$4TCL - 20 + 2t_A + t_C$	ns
Data hold after $\overline{RD}$ rising edge	t_{18}SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge (with RW-delay[1])	t_{20}SR	–	$15 + t_F$	–	$2TCL - 5 + t_F + 2t_A$[1]	ns
Data float after $\overline{RD}$ rising edge (no RW-delay[1])	t_{21}SR	–	$5 + t_F$	–	$TCL - 5 + t_F + 2t_A$[1]	ns
Data valid to $\overline{WR}$	t_{22}CC	$10 + t_C$	–	$2TCL - 10 + t_C$	–	ns
Data hold after $\overline{WR}$	t_{24}CC	$5 + t_F$	–	$TCL - 5 + t_F$	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{26}CC	$-5 + t_F$	–	$-5 + t_F$	–	ns
Address/Unlatched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$, $\overline{WRH}$	t_{28}CC	–3 (no t_F) -7 + t_F (t_F>0)	–	–3 (no t_F) -7 + t_F (t_F>0)	–	ns

Table 17.6   Demultiplexed bus (cont'd)

Parameter	Symbol	Max. CPU Clock = 50 MHz		Variable CPU Clock 1/2TCL = 1 to 50 MHz		Unit
		min.	max.	min.	max.	
ALE falling edge to Latched $\overline{CS}$	$t_{38}CC$	-3 - t_A	5 - t_A	-3 - t_A	3 - t_A	ns
Latched $\overline{CS}$ low to Valid Data In	$t_{39}SR$	–	15 + t_C + 2t_A	–	3TCL - 15 + t_C + 2t_A	ns
Latched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	$t_{41}CC$	3 + t_F	–	TCL - 7 + t_F	–	ns
ALE falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	$t_{42}CC$	7 + t_A	–	TCL - 3 + t_A	–	ns
ALE falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	$t_{43}CC$	-3 + t_A	–	-3 + t_A	–	ns
$\overline{RdCS}$ to Valid Data In (with RW-delay)	$t_{46}SR$	–	3 + t_C	–	2TCL - 17 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW-delay)	$t_{47}SR$	–	13 + t_C	–	3TCL - 17 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW-delay)	$t_{48}CC$	11 + t_C	–	2TCL - 9 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW-delay)	$t_{49}CC$	21 + t_C	–	3TCL - 9 + t_C	–	ns
Data valid to $\overline{WrCS}$	$t_{50}CC$	10 + t_C	–	2TCL - 10 + t_C	–	ns
Data hold after $\overline{RdCS}$	$t_{51}SR$	0	–	0	–	ns
Data float after $\overline{RdCS}$ (with RW-delay)	$t_{53}SR$	–	15 + t_F	–	2TCL - 5 + t_F	ns
Data float after $\overline{RdCS}$ (no RW-delay)	$t_{68}SR$	–	5 + t_F	–	TCL - 5 + t_F	ns
Address hold after $\overline{RdCS}$, $\overline{WrCS}$	$t_{55}CC$	-5 + t_F	–	-5 + t_F	–	ns
Data hold after $\overline{WrCS}$	$t_{57}CC$	3 + t_F	–	TCL - 7 + t_F	–	ns

Notes   1:   RW-delay and t_A refer to the next following bus cycle

2:   Read data are latched with the same clock edge that triggers the address change and the rising $\overline{RD}$ edge. Therefore address changes before the end of $\overline{RD}$ have no impact on read cycles.

Figure 17.11 External memory cycle:demultiplexed bus, with read/write delay, normal ALE
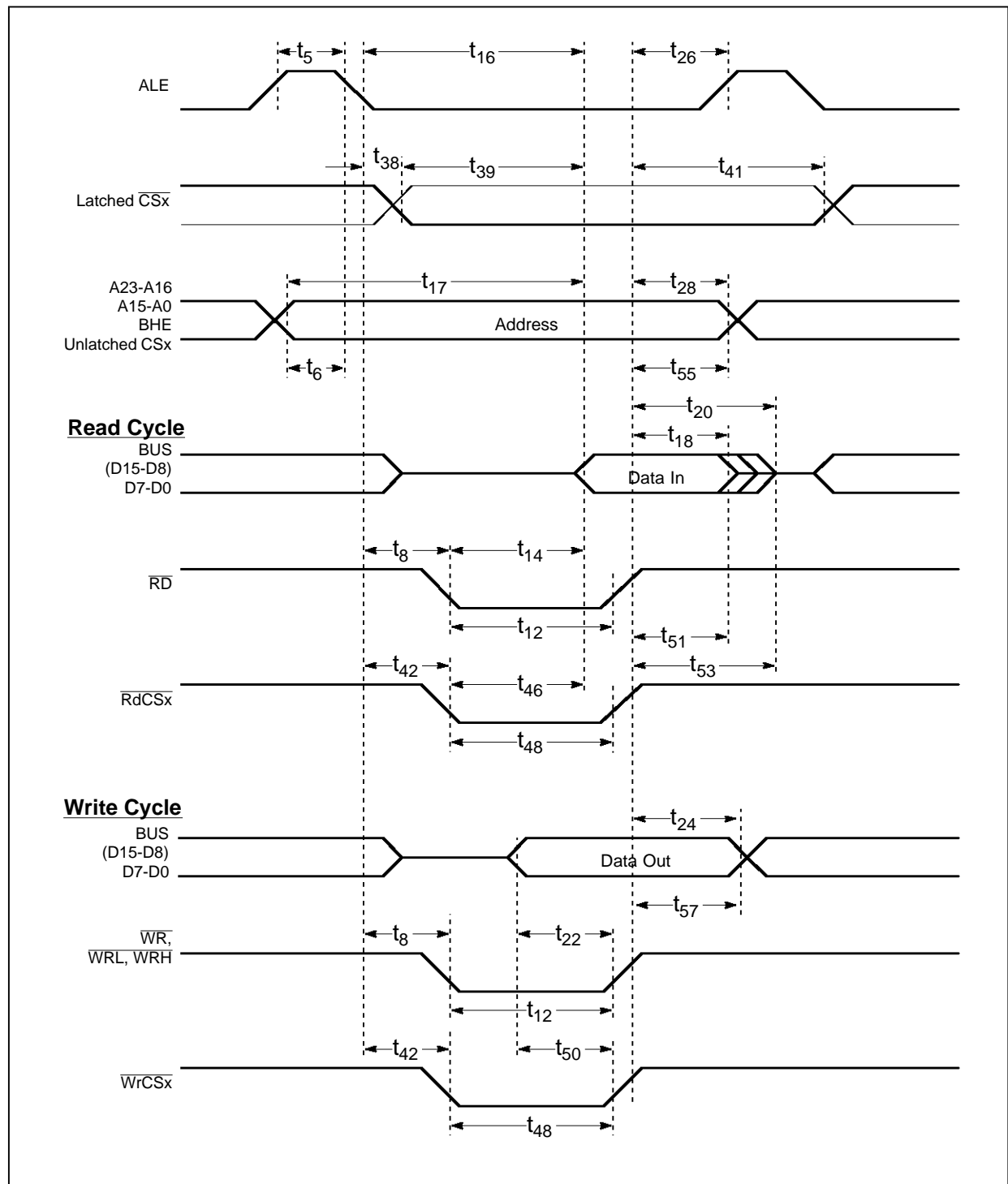
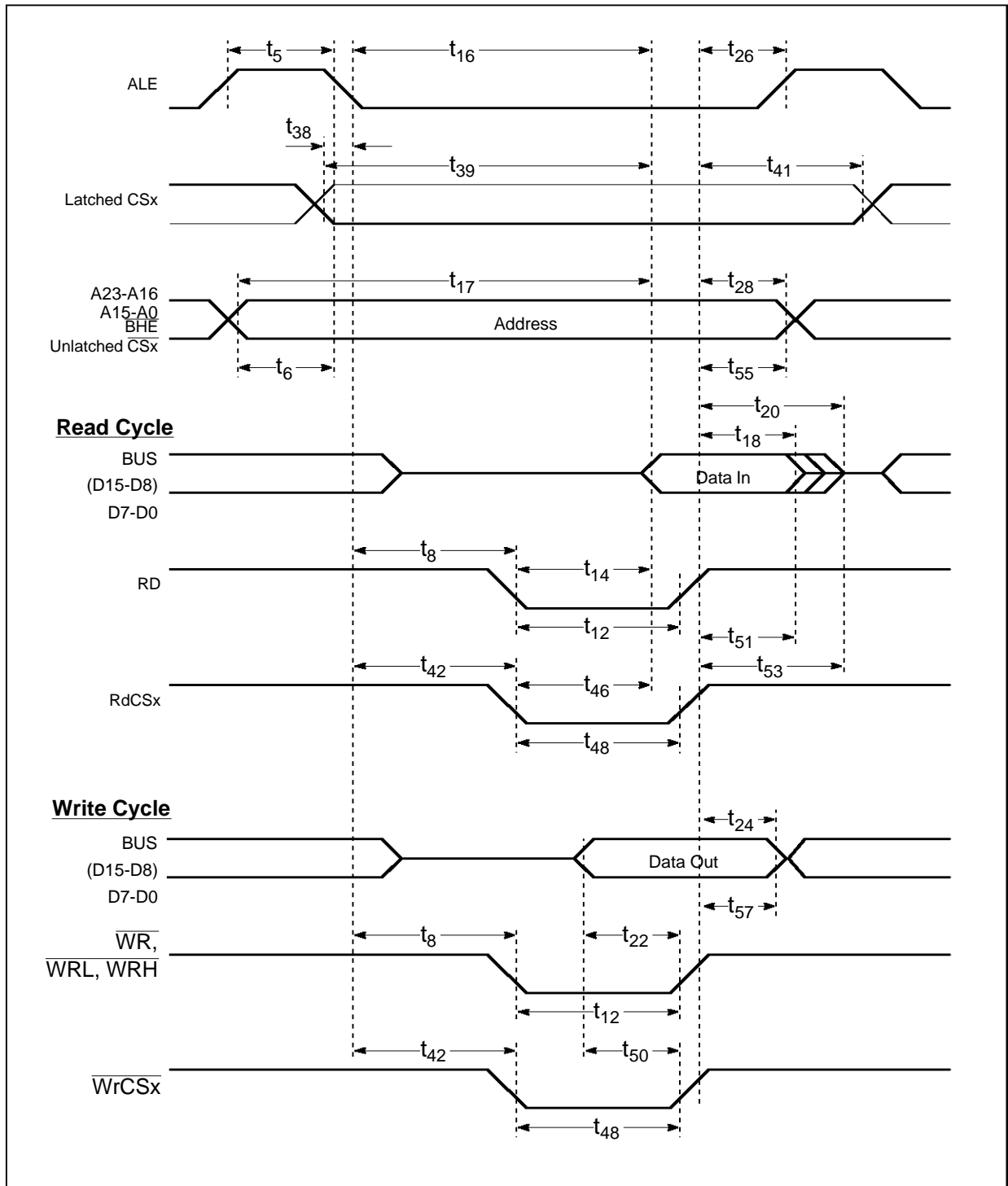**Figure 17.12 External memory cycle:demultiplexed   bus,   with   read/write   delay, extended ALE**

Figure 17.13 External memory cycle:demultiplexed bus, no read/write delay, normal ALE
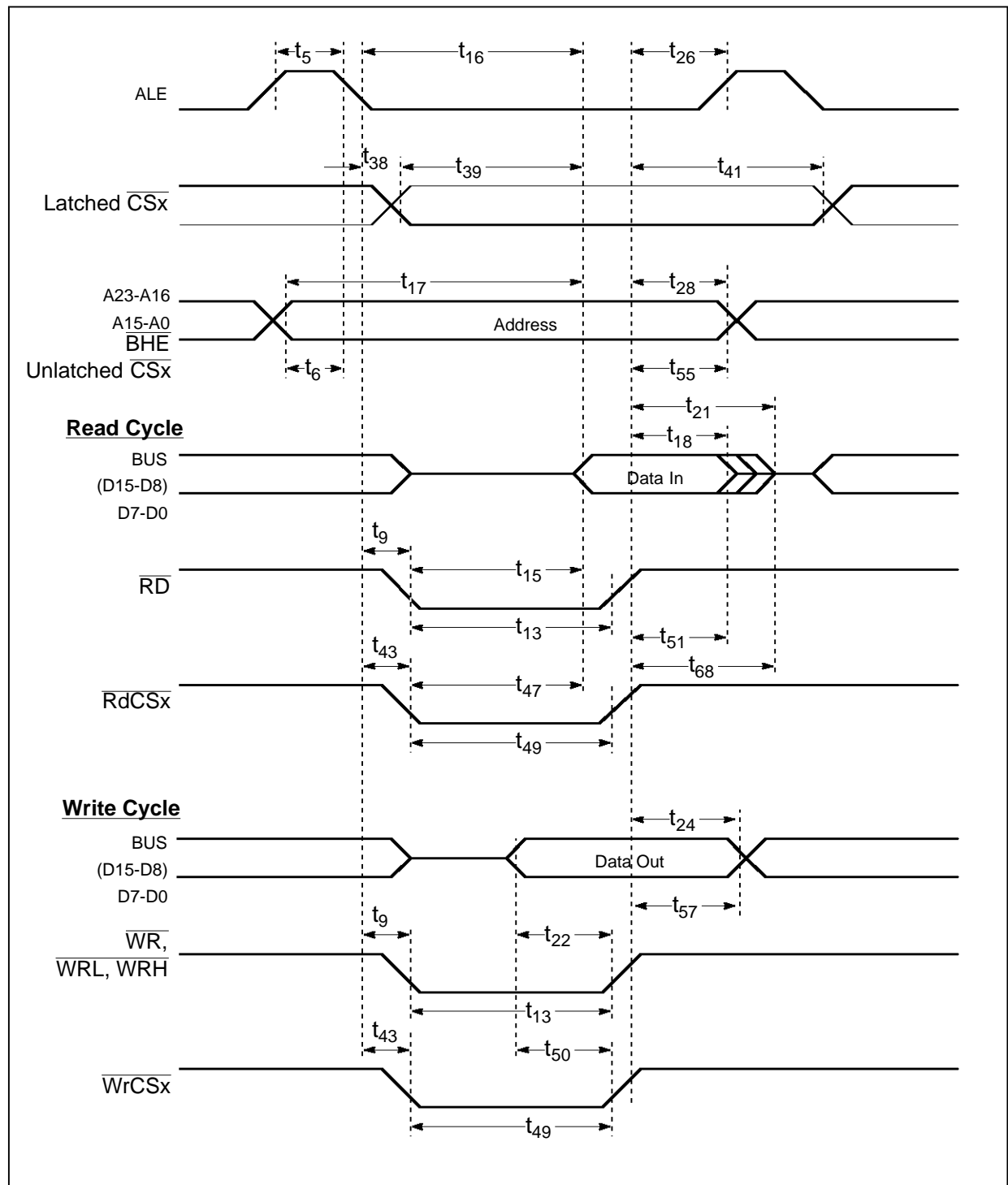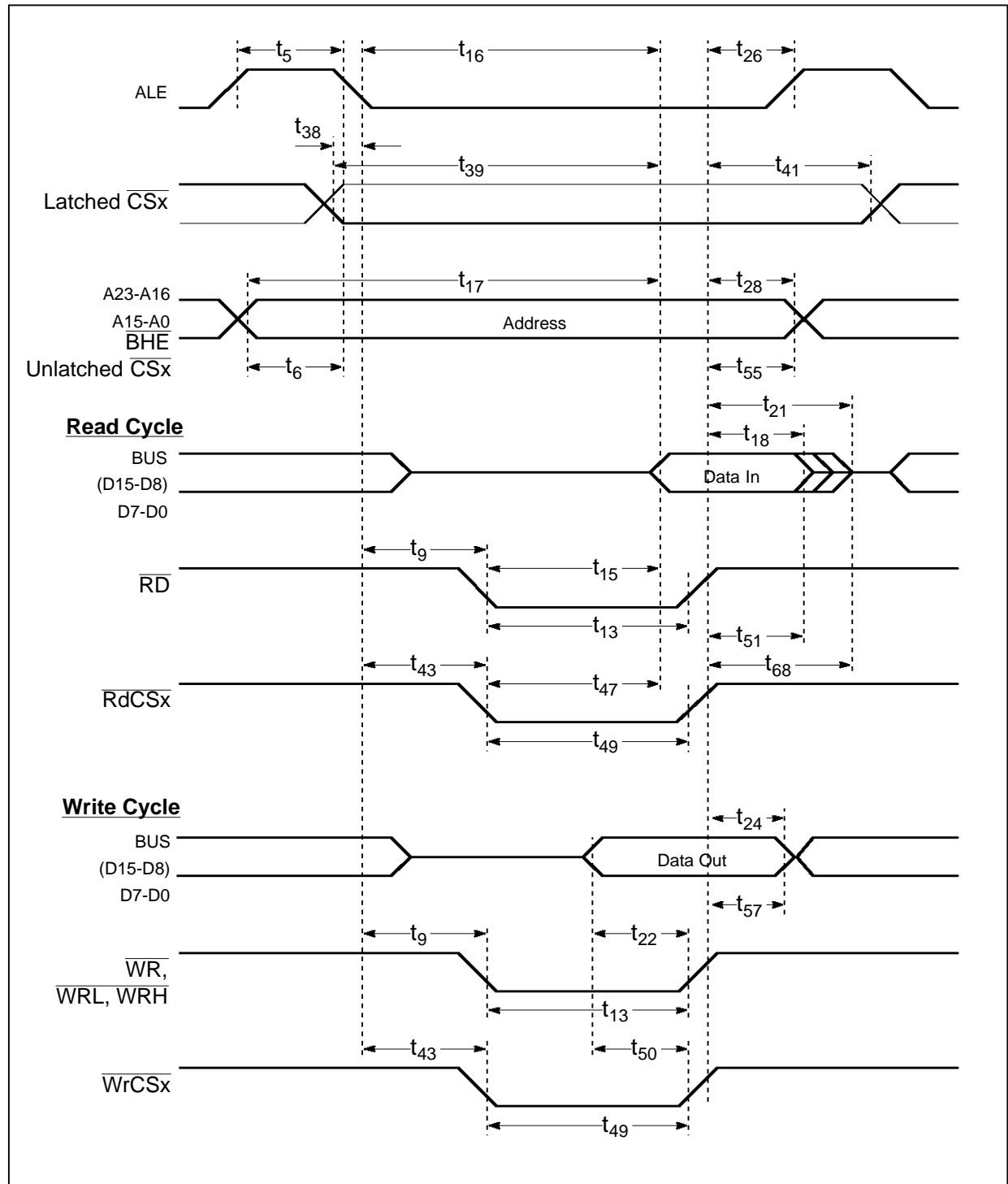
Figure 17.14 External memory cycle:demultiplexed bus, no read/write delay, extended ALE

17.4.12 CLKOUT and $\overline{\text{READY}}$

VDD = 5 V   10%, VSS = 0 V, TA = 0 to +70 °C, CL = 50 pF

Table 17.7   CLKOUT and READY

Parameter	Symbol	Max. CPU Clock = 50 MHz		Variable CPU Clock 1/2TCL = 1 to 50 MHz		Unit
		min.	max.	min.	max.	
CLKOUT cycle time	$t_{29}CC$	20	20	2TCL	2TCL	ns
CLKOUT high time	$t_{30}CC$	5	–	TCL – 5	–	ns
CLKOUT low time	$t_{31}CC$	5	–	TCL – 5	–	ns
CLKOUT rise time	$t_{32}CC$	–	3	–	3	ns
CLKOUT fall time	$t_{33}CC$	–	3	–	3	ns
CLKOUT rising edge to ALE falling edge	$t_{34}CC$	$-3 + t_A$	$5 + t_A$	$-3 + t_A$	$3 + t_A$	ns
Synchronous READY setup time to CLKOUT	$t_{35}SR$	9	–	9	–	ns
Synchronous READY hold time after CLKOUT	$t_{36}SR$	0	–	0	–	ns
Asynchronous READY low time	$t_{37}SR$	27	–	2TCL + 7	–	ns
Asynchronous READY setup time [1]	$t_{58}SR$	9	–	9	–	ns
Asynchronous READY hold time [1]	$t_{59}SR$	0	–	0	–	ns
Async. READY hold time after $\overline{\text{RD}}$, $\overline{\text{WR}}$ high (Demultiplexed Bus) [2]	$t_{60}SR$	0	$0 + 2t_A + t_c + t_F$ [2]	0	$TCL - 10 + 2t_A + t_c + t_F$ [2]	ns

Notes   1: These timings are given for test purposes only, in order to assure recognition at a specific clock edge.

2: Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating READY.
The $2t_A$ and t_C refer to the next following bus cycle, t_F refers to the current bus cycle.

**Figure 17.15 CLKOUT and $\overline{\text{READY}}$ (or READY)**
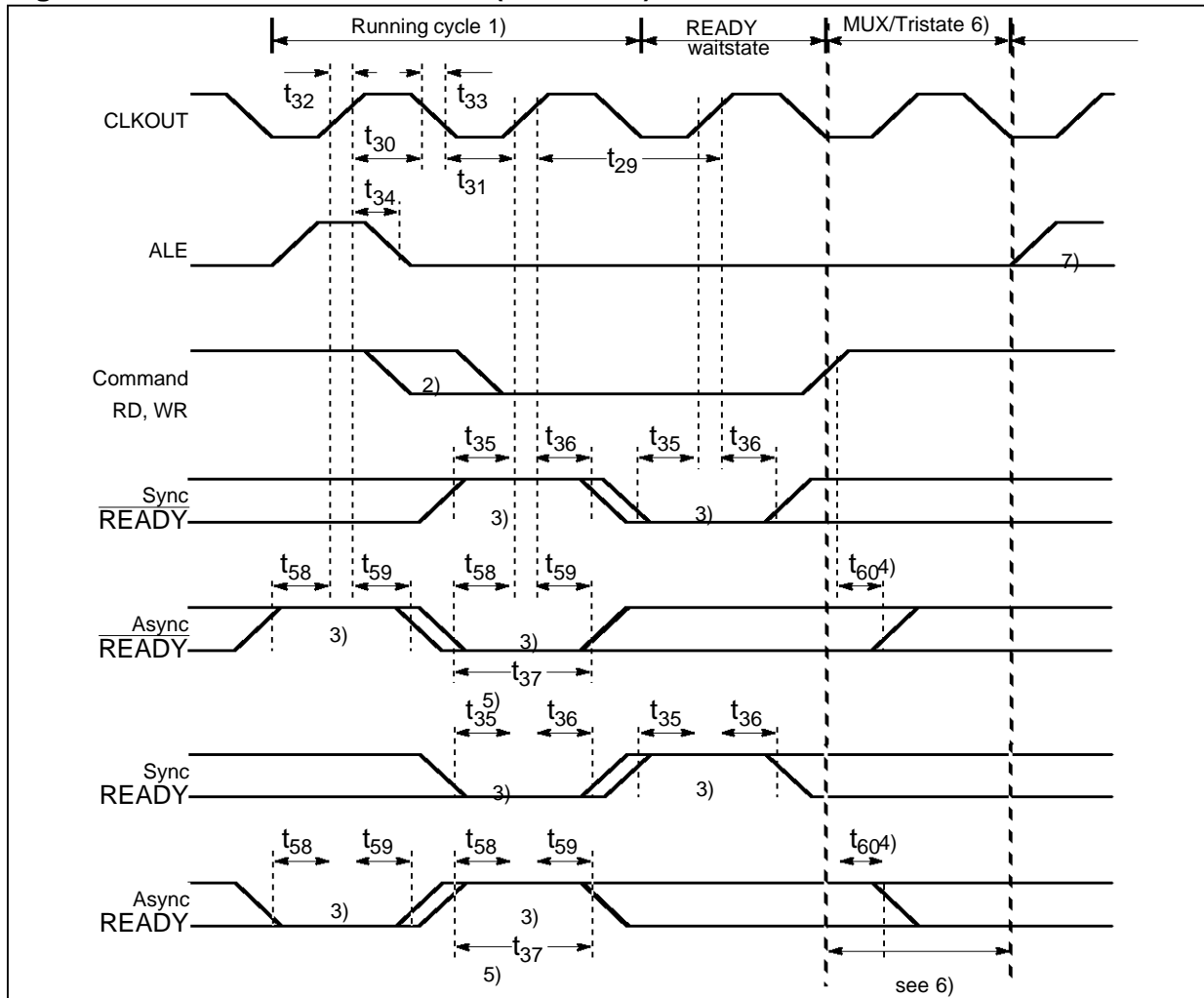
Notes 1: Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).

2: The leading edge of the respective command depends on RW-delay.

3: $\overline{\text{READY}}$ (or READY) sampled HIGH (resp. LOW) at this sampling point generates a READY controlled waitstate, $\overline{\text{READY}}$ (resp. READY) sampled LOW (resp. HIGH) at this sampling point terminates the currently running bus cycle.

4: $\overline{\text{READY}}$ (resp. READY) may be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).

5: If the Asynchronous $\overline{\text{READY}}$ (or READY) signal does not fulfill the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfill t 37 in order to be safely synchronized. This is guaranteed, if READY is removed in response to the command (see Note 4).

6: Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here. For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC waitstate this delay is zero.

7: The next external bus cycle may start here.

17.4.13 External bus arbitration

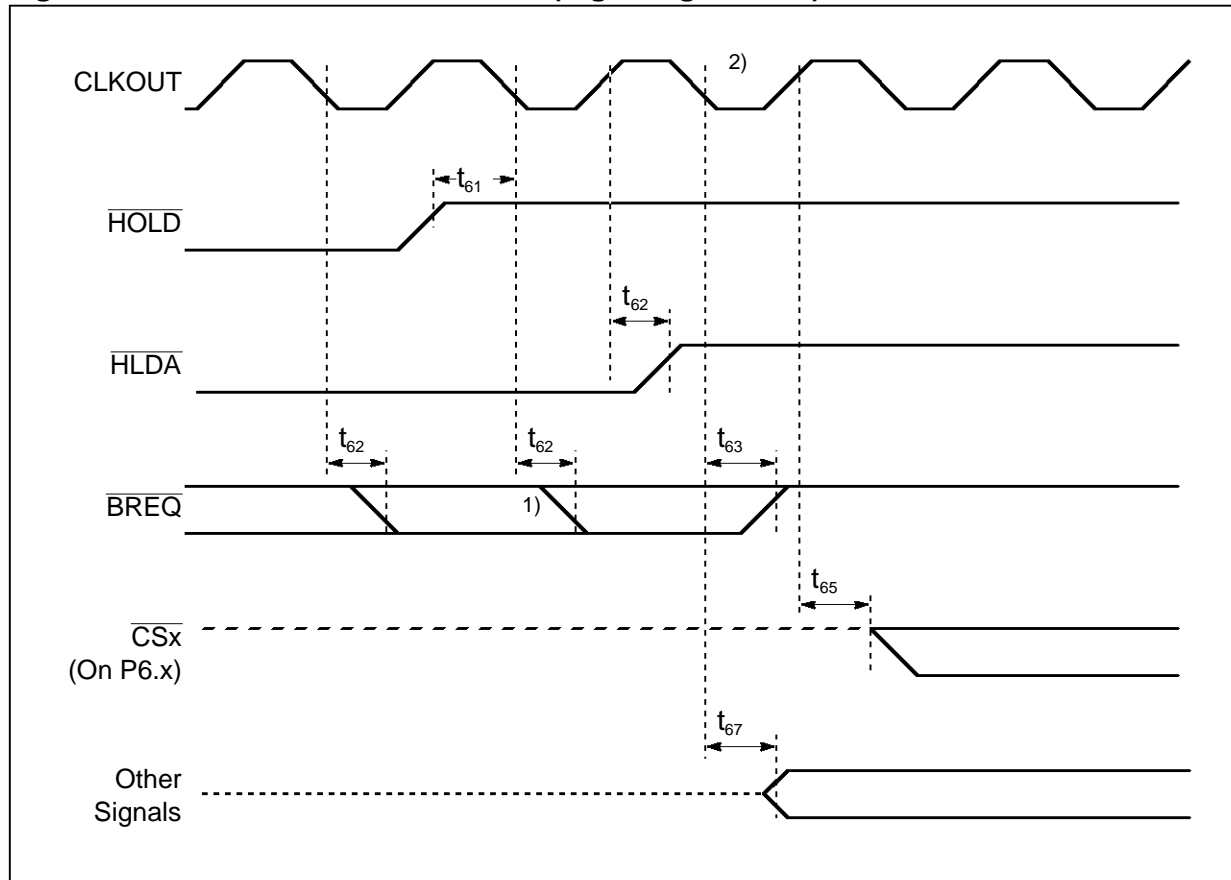$V_{DD} = 5 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, $T_A = 0$ to $+70 \,^{\circ}\text{C}$, $C_L = 50 \text{ pF}$

Table 17.8   External bus arbitration

Parameter	Symbol	Max. CPU Clock = 50 MHz		Variable CPU Clock 1/2TCL = 1 to 50 MHz		Unit
		min.	max.	min.	max.	
$\overline{\text{HOLD}}$ input setup time to CLKOUT	t_{61SR}	15	–	15	–	ns
CLKOUT to $\overline{\text{HLDA}}$ high or $\overline{\text{BREQ}}$ low delay	t_{62CC}	–	10	–	10	ns
CLKOUT to $\overline{\text{HLDA}}$ low or $\overline{\text{BREQ}}$ high delay	t_{63CC}	–	10	–	10	ns
$\overline{\text{CSx}}$ release	t_{64CC}	–	10	–	10	ns
$\overline{\text{CSx}}$ drive	t_{65CC}	-3	15	-3	15	ns
Other signals release	t_{66CC}	–	10	–	10	ns
Other signals drive	t_{67CC}	-3	15	-3	15	ns

Figure 17.16 External bus arbitration - releasing the bus
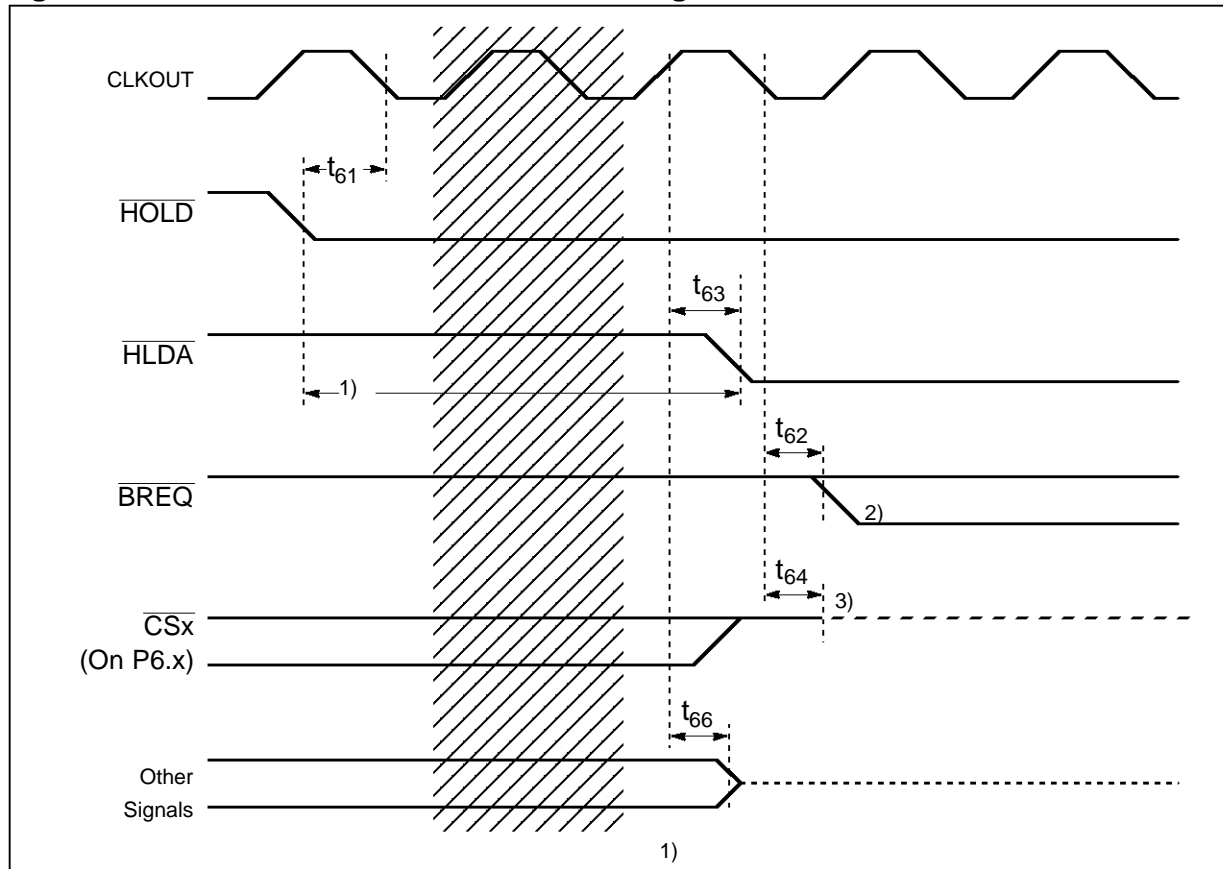
Notes   1:   The ST10X262 will complete the currently running bus cycle before granting bus access.

2:   This is the first possibility for $\overline{BREQ}$ to get active.

3:   The $\overline{CS}$ outputs will be resistive high (pullup) after t_{64}.

Figure 17.17 External bus arbitration, (regaining the bus)

Notes   1:   This is the last chance for $\overline{\text{BREQ}}$ to trigger the indicated regain-sequence.
Even if $\overline{\text{BREQ}}$ is activated earlier, the regain-sequence is initiated by $\overline{\text{HOLD}}$ going high.
$\overline{\text{HOLD}}$ may also be desactivated without the ST10X262 requesting the bus.

Notes   1:   The next ST10X262 driven bus cycle may start here.

17.4.14 External hardware reset

$V_{DD} = 5\ V\ \pm 10\%$, $V_{SS} = 0\ V$, $T_A = 0$ to $+70\ ^\circ C$, $C_L = 50\ pF$

Table 17.9 External hardware reset

Parameter	Symbol	Max. CPU Clock = 50 MHz		Variable CPU Clock 1/2TCL = 1 to 50 MHz		Unit
		min.	max.	min.	max.	
Sync. $\overline{RSTIN}$ low time1)	t_{70} SR	50	–	4 TCL + 10	–	ns
$\overline{RSTIN}$ low to internal reset sequence start	t_{71} CC	4	16	4	16	TCL
internal reset sequence, ($\overline{RSTIN}$ internaly pulled low)	t_{72} CC	1024	1024	1024	1024	TCL
$\overline{RSTIN}$ rising edge to internal reset condition end	t_{73} CC	4	6	4	6	TCL
PORT0 system startup configuration setup to $\overline{RSTIN}$ rising edge 2)	t_{74} SR	100	–	100	–	ns
PORT0 system startup configuration hold after $\overline{RSTIN}$ rising edge	t_{75} SR	1	6	1	6	TCL
Bus signals drive from internal reset end	t_{76} CC	0	20	0	20	ns
$\overline{RSTIN}$ low to signals release	t_{77} CC	–	50	–	50	ns
ALE rising edge from internal reset condition end	t_{78} CC	8	8	8	8	TCL
Async. $\overline{RSTIN}$ low time1)	t_{79} SR	1500	–	1500	–	ns

Notes 1: On power-up reset, the $\overline{RSTIN}$ pin must asserted until a stable clock signal is available (about 10...50 ms to allow the on-chip oscillator to stabilize) and until System Startup Configuration is correct on PORT0 (about 15 ms for internal pullup devices to load 50 pF from V_{IL}min to V_{IH}min.

2: The value of bits 0 (EMU), 1 (ADAPT), 13 to 15 (Clock Configuration) are loaded during hardware reset as long as internal reset signal is active, and have an immediat effect on the system.

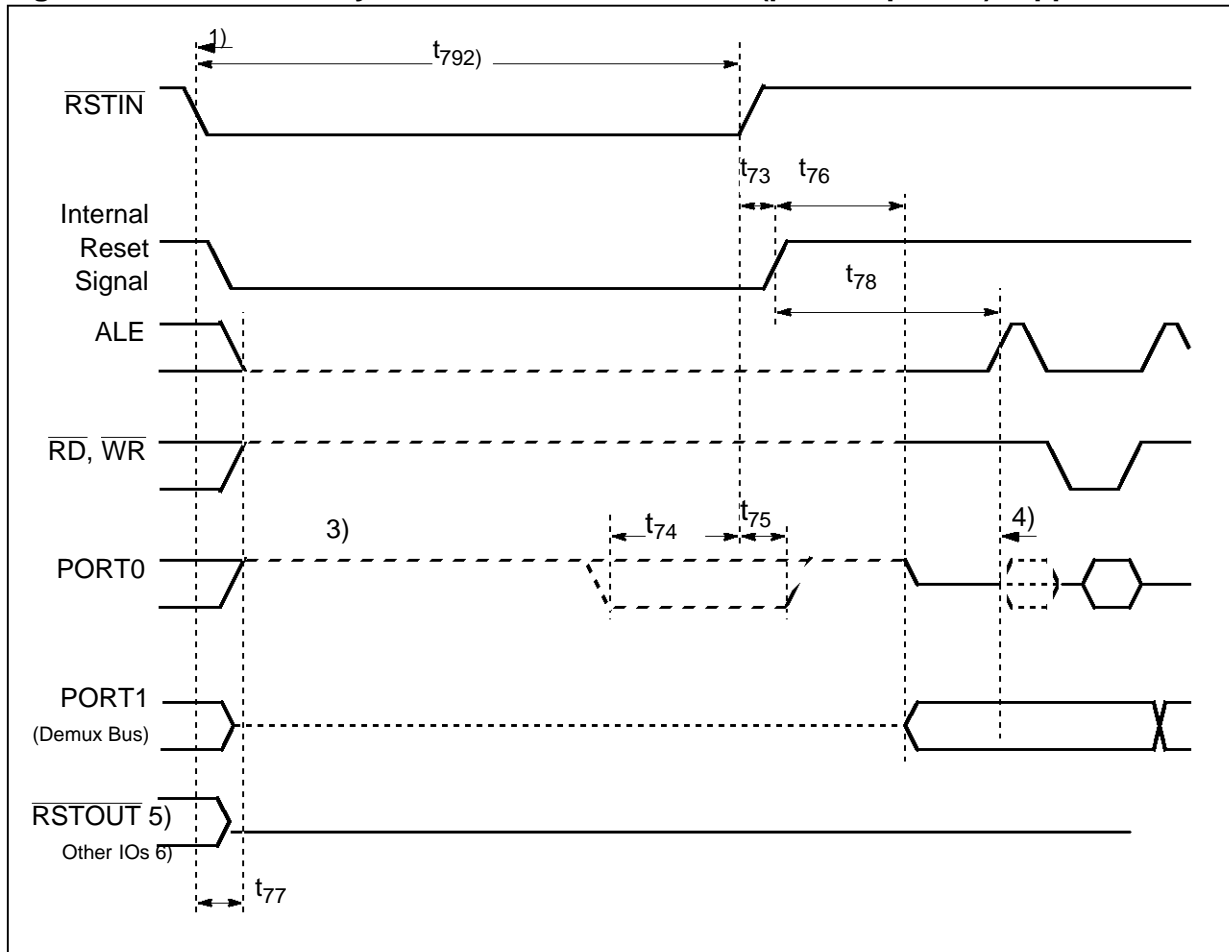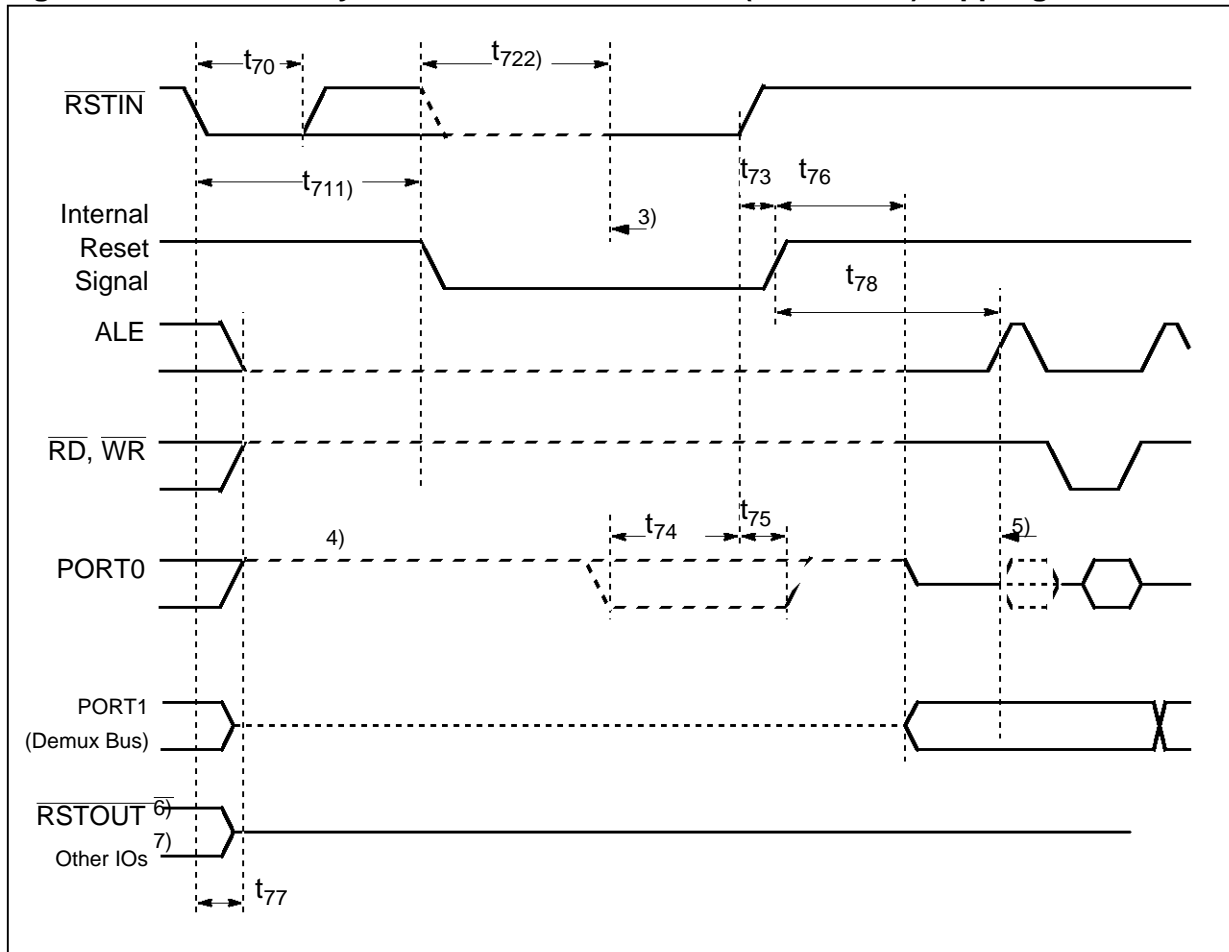**Figure 17.18 External asynchronous hardware reset (power-up reset): Vpp low**

Notes   1:   The ST10X262 is reset in its default state asynchronously with $\overline{RSTIN}$. Internal RAM content may be altered if an internal write access was in progress.

2:   On power-up, $\overline{RSTIN}$ must be asserted t_{79} after a stabilized CPU clock signal is available.

3:   Internal pullup devices are active on the PORT0 lines, so their input level is high, if the respective pin is left open, or is low, if the respective pin is connected to an external pulldown device.

4:   The ST10X262 starts execution here at address 00'0000h.

5:   $\overline{RSTOUT}$ stays active until execution of the EINIT (End of Initialization) instruction.

6:   Activation of the IO pins is controlled by software.

Figure 17.19 External synchronous hardware reset (warm reset): Vpp high

Notes 1: The pending internal hold states are cancelled and the current internal acces cycle (if any) is completed. .

2: $\overline{RSTIN}$ pulled low by internal device during internal reset sequence.

3: The reset condition may ends here if $\overline{RSTIN}$ pin is sampled high after t_{72}.

4: Internal pullup devices are active on the PORT0 lines, so their input level is high, if the respective pin is left open, or is low, if the respective pin is connected to an external pulldown devicebe resistive high (pullup) after t_{64}.

5: The ST10X262 starts execution here at address 00'0000h.

6: $\overline{RSTOUT}$ stays active until execution of the EINIT (End of Initialization) instruction.

7: Activation of the IO pins is controlled by software.

17.4.15 Synchronous serial port timing

VCC = 5 V   10 %, VSS = 0 V, TA = 0 to +70 °C, CL = 50 pF

Table 17.10   SSP port timing

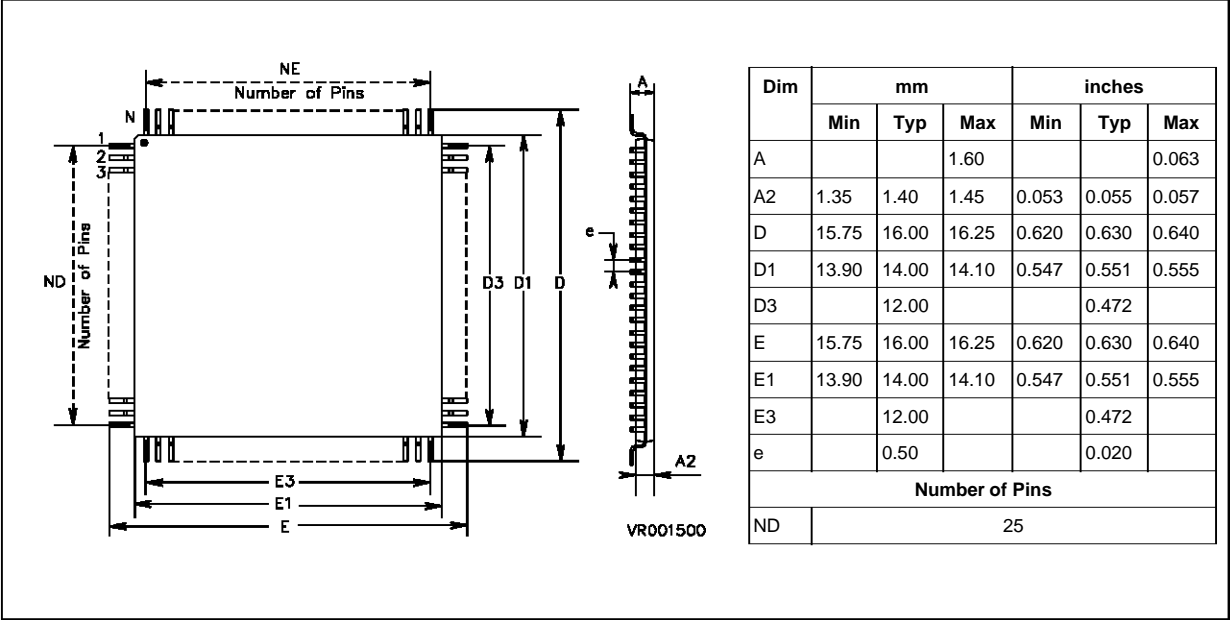| Parameter	Symbol	Max. Baudrate = 20 MBd		Variable Baudrate = 0.5 to 20 MBd		Unit
		min.	max.	min.	max.	
SSP clock cycle time	t_{200}CC	40	40	4 TCL	512 TCL	ns
SSP clock high time	t_{201}CC	13	–	$t_{200}/2 - 7$	–	ns
SSP clock low time	t_{202}CC	13	–	$t_{200}/2 - 7$	–	ns
SSP clock rise time	t_{203}CC	–	3	–	3	ns
SSP clock fall time	t_{204}CC	–	3	–	3	ns
CE active before shift edge	t_{205}CC	13	–	$t_{200}/2 - 7$	–	ns
CE inactive after latch edge	t_{206}CC	33	47	$t_{200} - 7$	$t_{200} + 7$	ns
Write data valid after shift edge	t_{207}CC	–	7	–	7	ns
Write data hold after shift edge	t_{208}CC	-3	–	-3	–	ns
Write data hold after latch edge	t_{209}CC	15	25	$t_{200}/2 - 5$	$t_{200}/2 + 5$	ns
Read data active after latch edge	t_{210}SR	27	–	$t_{200}/2 + 7$	–	ns
Read data setup time before latch edge	t_{211}SR	15	–	15	–	ns
Read data hold time after latch edge	t_{212}SR	0	–	0	–	ns

Figure 17.20 SSP write timing
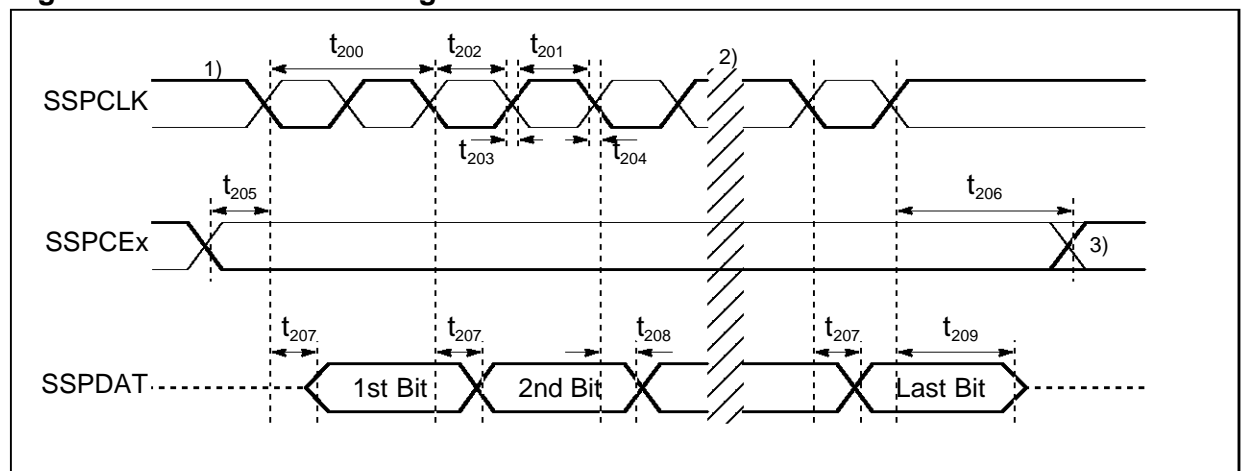
Figure 17.21 SSP read timing
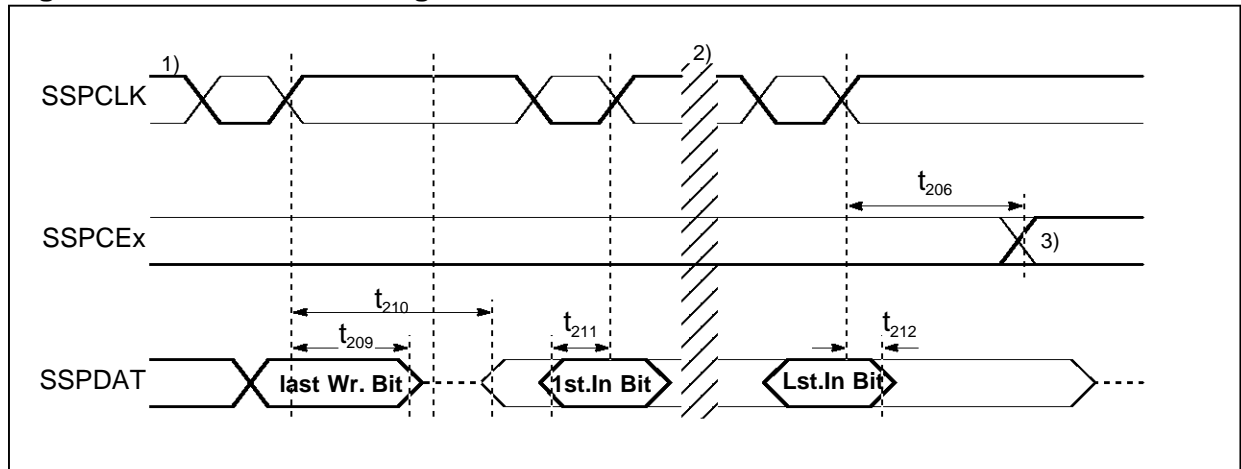
Notes 1: The transition of shift and latch edge of SSPCLK is programmable. This figure uses the falling
edge as shift edge (drawn bold).

2: The bit timing is repeated for all bits to be transmitted or received.

3: The active level of the chip enable lines is programmable. This figure uses an active low CE
(drawn bold).
At the end of a transmission or reception the CE signal is disabled in single transfer mode. In
continuous transfer mode it remains active.

18   Package Mechanical Data

Figure 18.1   Package outline TQFP100 (14 x 14 mm)

Dim	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	15.75	16.00	16.25	0.620	0.630	0.640
D1	13.90	14.00	14.10	0.547	0.551	0.555
D3		12.00			0.472	
E	15.75	16.00	16.25	0.620	0.630	0.640
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.00			0.472	
e		0.50			0.020	
Number of Pins						
ND	25					

VR001500

19   Ordering Information

Salestype	Temperature range	Package
ST10R262-T1	0°C to 70°C	TQFP100 (14x 14)