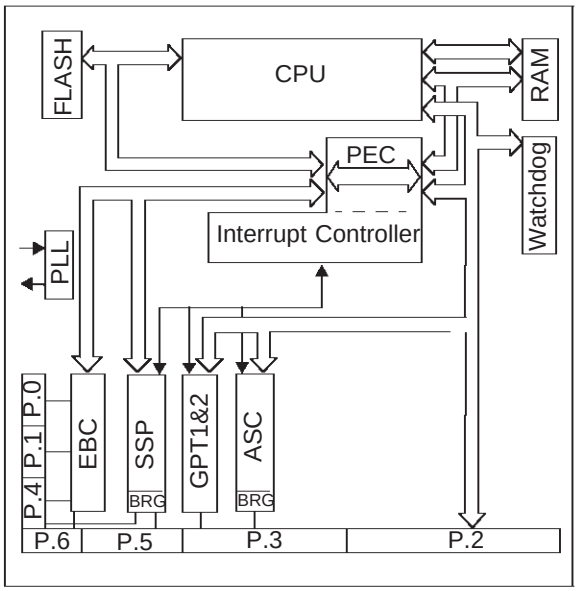
ST10F163

16-bit MCU with 128KByte Flash Memory

DATA SHEET

- High performance CPU
  - High performance 16-bit CPU with 4-stage pipeline
  - 80ns instruction cycle time @ 25MHz CPU clock
  - 400 ns multiplication (16 × 16 bits)
  - 800 ns division (32 / 16 bit)
  - Enhanced boolean bit manipulation facilities
  - Additional instructions to support HLL and operating systems
  - Single-cycle context switching support
- Memory organization
  - Up to 16 MBytes linear address space for code and data (1MByte with SSP used)
  - 1 KBytes on-chip RAM
  - **128 KBytes on-chip Flash memory**
  - 4 independently erasable banks of Flash
- Fast and flexible bus
  - Programmable EBC
  - 8-Bit or 16-bit external data bus
  - Multiplexed or demultiplexed external address/data buses
  - Five programmable chip-select signals
  - Hold and hold-acknowledge bus arbitration support
- On-chip bootstrap loader
- Fail-safe protection
  - Programmable watchdog timer
  - Oscillator Watchdog
- Interrupt
  - 8-channel interrupt-driven single-cycle data transfer facilities via peripheral event controller (PEC)
  - 16-priority-level interrupt system with 20 sources, sample-rate down to 40 ns
- Timers
  - Two general purpose timer units with 5 timers



- Clock generation
  - On-chip PLL
  - Direct or prescaled clock input
- Up to 77 general purpose I/O lines
- Idle and power down modes
- Serial channels
  - Synchronous/asynchronous
  - High-speed synchronous serial port SSP
- Development support
  - C-compilers, macro-assembler packages, emulators, evaluation boards, HLL-debuggers, simulators, logic analyzer disassemblers, programming boards
- Package
  - 100-Pin Thin Quad Flat Pack (TQFP)

Table of Contents

1 Introduction

The ST10F163 is a Flash derivative of the STMicroelectronics ST10 family of 16-bit microcontrollers. It combines high CPU performance (up to 12.5 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. 128KBytes of an electrically erasable and re-programmable Flash EPROM is provided on-chip.

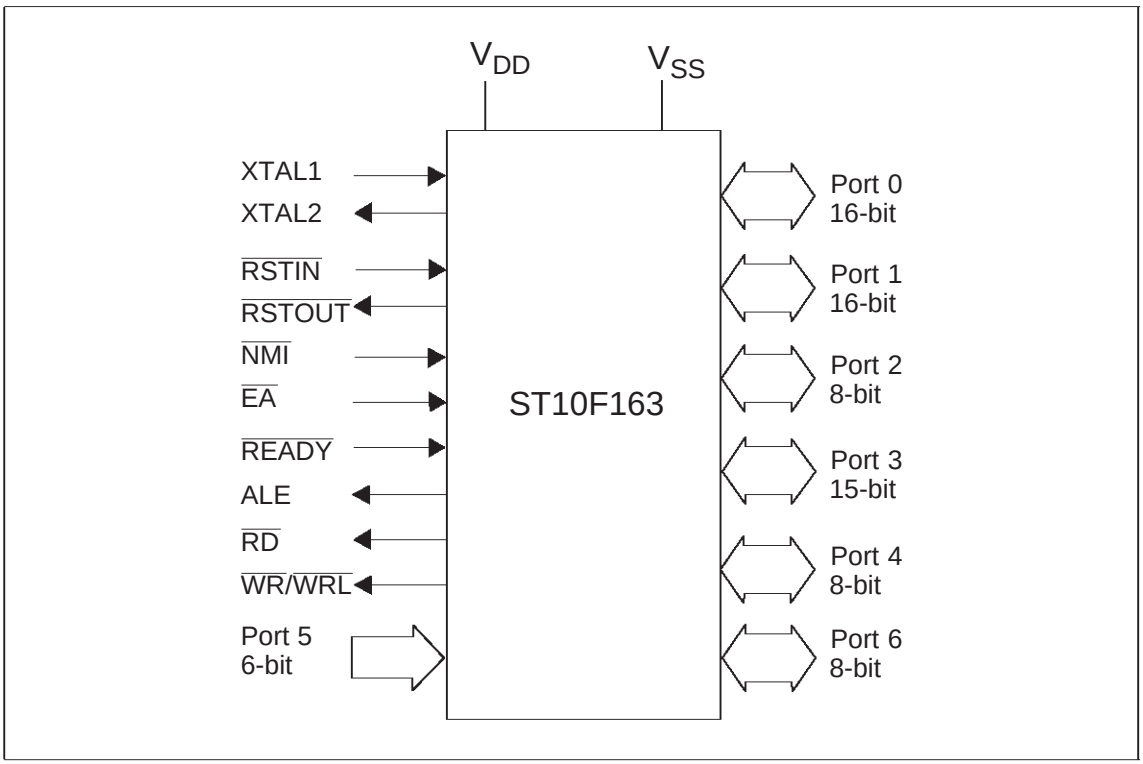


Figure 1 Logic symbol

2 Pin Data

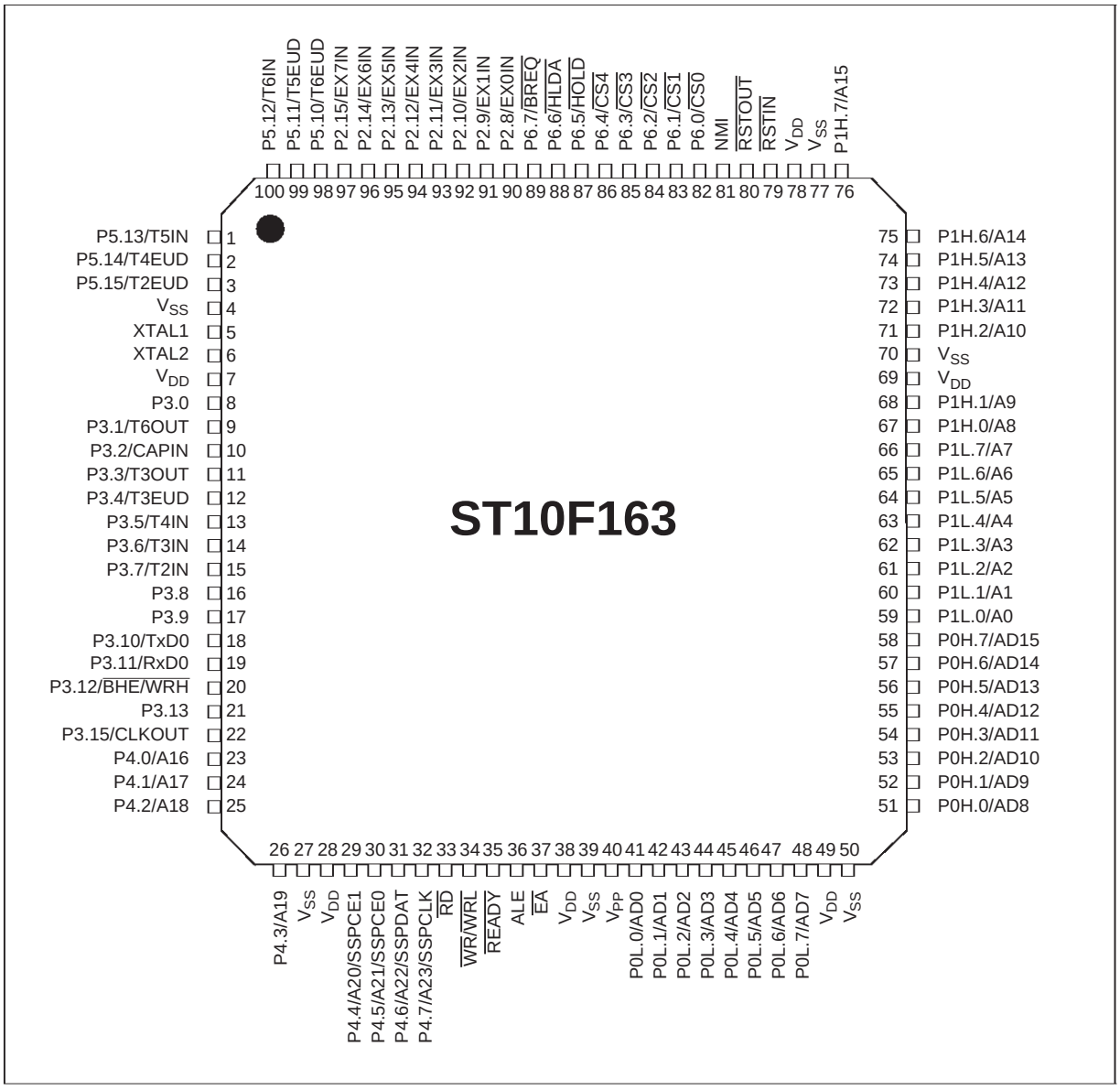


Figure 2 TQFP pin configuration (top view)

Symbol	Pin Number (TQFP)	Input (I) Output (O)	Function		
P5.10 – P5.15	98-100 1- 3	I I	6-bit input-only port with Schmitt-Trigger characteristics. Port 5 pins also serve as timer inputs:		
	98	I	P5.10	T6EUD	GPT2 Timer T6 Ext.Up/Down Ctrl.Input
	99	I	P5.11	T5EUD	GPT2 Timer T5 Ext.Up/Down Ctrl.Input
	100	I	P5.12	T6IN	GPT2 Timer T6 Count Input
	1	I	P5.13	T5IN	GPT2 Timer T5 Count Input
	2	I	P5.14	T4EUD	GPT1 Timer T4 Ext.Up/Down Ctrl.Input
	3	I	P5.15	T2EUD	GPT1 Timer T2 Ext.Up/Down Ctrl.Input
XTAL1	5	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator		
XTAL2	6	O	XTAL2: Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.		
P3.0 – P3.13, P3.15	8- 21 22	I/O I/O	15-bit (P3.14 is missing) bidirectional I/O port, bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The following Port 3 pins have alternate functions:		
	9	O	P3.1	T6OUT	GPT2 Timer T6 Toggle Latch Output
	10	I	P3.2	CAPIN	GPT2 Register CAPREL Capture Input
	11	IO	P3.3	T3OUT	GPT1 Timer T3 Toggle Latch Output
	12	I	P3.4	T3EUD	GPT1 Timer T3 Ext.Up/Down Ctrl.Input
	13	I	P3.5	T4IN	GPT1 Timer T4 Input for Count/Gate/Reload/ Capture
	14	I	P3.6	T3IN	GPT1 Timer T3 Count/Gate Input
	15	I	P3.7	T2IN	GPT1 Timer T2 Input for Count/Gate/Reload/ Capture
	18	O	P3.10	TxD0	ASC0 Clock/Data Output (Asyn./Syn.)
	19	I/O	P3.11	RxD0	ASC0 Data Input (Asyn.) or I/O (Syn.)
	20	O	P3.12	$\overline{BHE}$	Ext. Memory High Byte Enable Signal,
		O		$\overline{WRH}$	Ext. Memory High Byte Write Strobe
	22	O	P3.15	CLKOUT	System Clock Output (=CPU Clock)

Table 1 Pin definitions and functions

Symbol	Pin Number (TQFP)	Input (I) Output (O)	Function		
P4.0 – P4.7	23-26 29-32	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. For external bus configuration, Port 4 can be used to output the segment address lines:		
	23	O	P4.0	A16	Least Significant Segment Addr. Line
	...	...	...	...	...
	26	O	P4.3	A19	Segment Address Line
	29	O	P4.4	A20	Segment Address Line
		O		SSPCE1	SSP Chip Enable Line 1
	30	O	P4.5	A21	Segment Address Line
		O		SSPCE0	SSP Chip Enable Line 0
	31	O	P4.6	A22	Segment Address Line
		I/O		SSPDAT	SSP Data Input/Output Line
	32	O	P4.7	A23	Most Significant Segment Addr. Line
		O		SSPCLK	SSP Clock Output Line
$\overline{RD}$	33	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.		
$\overline{WR}$/$\overline{WRL}$	34	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.		
$\overline{READY}$	35	I	Ready Input. When the $\overline{READY}$ function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level.		
ALE	36	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.		
$\overline{EA}$	37	I	External Access Enable pin. A low level at this pin during and after Reset forces the device to begin instruction execution out of external memory. A high level forces execution out of the internal flash EPROM.		

Table 1 Pin definitions and functions (Continued)

Symbol	Pin Number (TQFP)	Input (I) Output (O)	Function
PORT0: P0L.0- P0L.7 P0H.0- P0H.7	 41-48 51-58	I/O	Two 8-bit bidirectional I/O ports P0L and P0H, bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: D0 – D7 D0 - D7 P0H.0 – P0H.7: I/O D8 - D15 **Multiplexed bus modes** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: AD0 – AD7 AD0 - AD7 P0H.0 – P0H.7: A8 – A15 AD8 – AD15
PORT1: P1L.0- P1L.7 P1H.0- P1H.7	 59-66 67, 68 71-76	I/O	Two 8-bit bidirectional I/O ports P1L and P1H, bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode.
$\overline{\text{RSTIN}}$	79	I	Reset Input with Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running resets the device. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
$\overline{\text{RSTOUT}}$	80	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{NMI}}$	81	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the ST10R65 to go into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.

Table 1 Pin definitions and functions (Continued)

Symbol	Pin Number (TQFP)	Input (I) Output (O)	Function		
P6.0- P6.7	82-89	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The following Port 6 pins have alternate functions:		
	82	O	P6.0	$\overline{CS0}$	Chip Select 0 Output
	...	...	...	...	...
	86	O	P6.4	$\overline{CS4}$	Chip Select 4 Output
	87	I	P6.5	$\overline{HOLD}$	External Master Hold Request Input (Master mode: O, Slave mode: I)
	88	I/O	P6.6	$\overline{HLDA}$	Hold Acknowledge Output
	89	O	P6.7	$\overline{BREQ}$	Bus Request Output
P2.8 – P2.15	90 - 97	I/O	Port 2 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The following Port 2 pins also serve for alternate functions:		
	90	I	P2.8	EX0IN	Fast External Interrupt 0 Input
	...	...	...	...	...
	97	I	P2.15	EX7IN	Fast External Interrupt 7 Input
V_{PP}	40	-	Flash programming voltage. This pin accepts the programming voltage for the on-chip flash EPROM. In the ST10F163, bit 4of SYSCON register serves as an enable/disable control for the OWD.		
V_{DD}	7, 28, 38, 49, 69, 78	-	Digital Supply Voltage: + 5 V during normal operation and idle mode. $\geq$ 2.5 V during power down mode		
V_{SS}	4, 27, 39, 50, 70, 77	-	Digital Ground.		

Table 1 Pin definitions and functions (Continued)

3 Functional Description

The architecture of the ST10F163 combines the advantages of both RISC and CISC processors and an advanced peripheral subsystem. The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure.

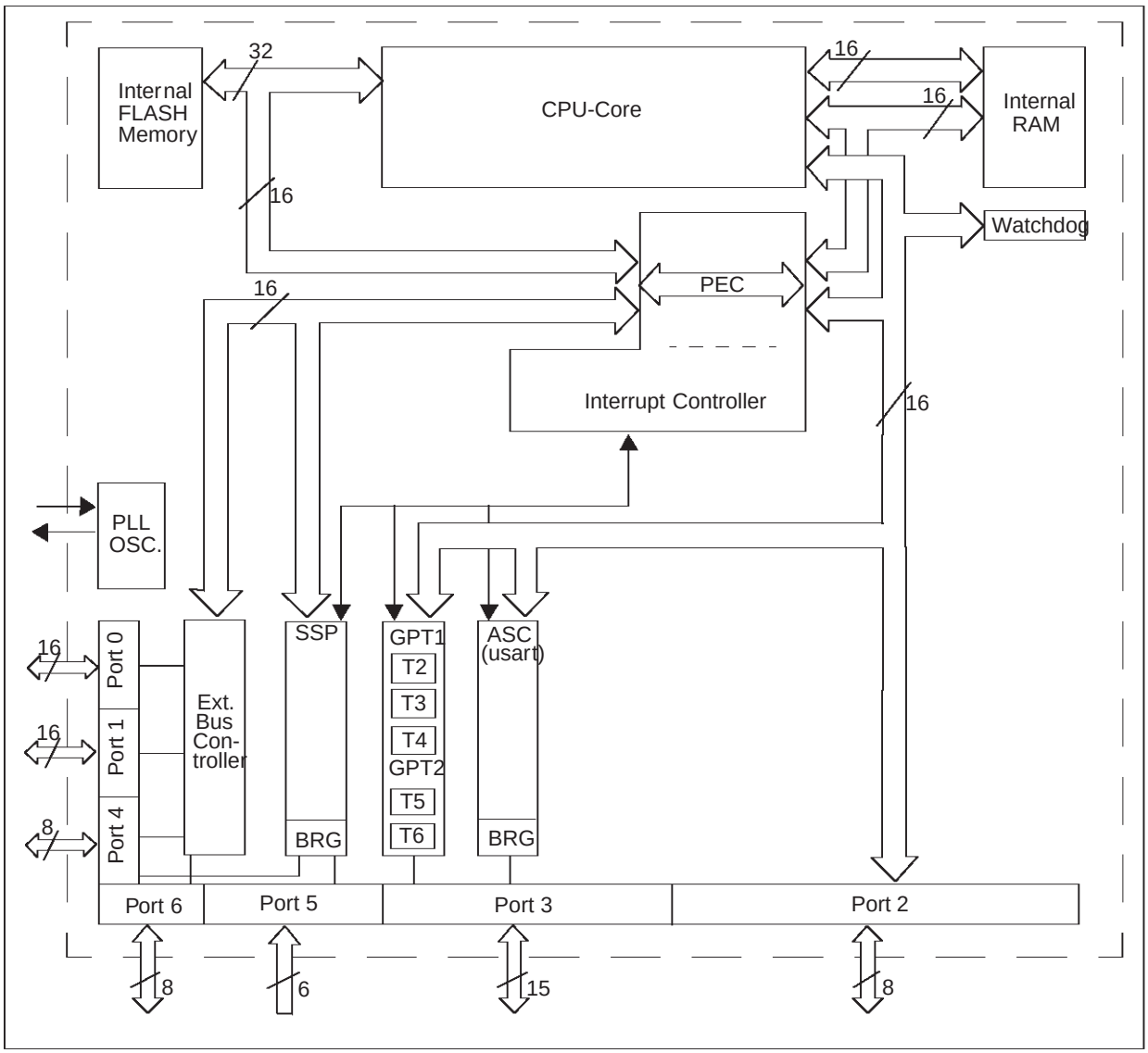


Figure 3 Block diagram

4 Memory Organization

The memory space of the ST10F163 is configured in a Von-Neumann architecture. Code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 MBytes. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have additionally been made directly bit addressable.

1 KByte of on-chip RAM is provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, …, RL7, RH7) General Purpose Registers (GPRs).

1024 bytes (2 * 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for other/future members of the ST10 family.

In order to meet the needs of system designs where more memory is required than is provided on chip, up to 16 MBytes of external RAM and/or ROM can be connected to the microcontroller.

5 Flash Memory

The ST10F163 provides 128KBytes of on-chip, electrically erasable and re-programmable Flash EPROM. The flash memory is organized in 32 bit wide blocks. This allows double word instructions to be fetched in one machine cycle. The flash memory can be used for both code and data storage. The flash memory is organized into four banks of sizes 8K, 24K, 48K and 48Kbytes (table 2). Each of these banks can be erased independently. This prevents unnecessary erasing of the whole flash memory when only a partial erasing is required.

Bank	Addresses (Segment 0)	Addresses (Segment 1)	Size (bytes)
0	000000h to 001FFFh	010000h to 011FFFh	8K
1	002000h to 007FFFh	012000h to 017FFFh	24K
2	018000h to 023FFFh	018000h to 023FFFh	48K
3	024000h to 02FFFFh	024000h to 02FFFFh	48K

Table 2 FLASH memory bank organisation

Typical timing characteristics give 80µs for word or double word programming and 800 ms for block erasing, at 25mhz system clock. the flash memory has a typical endurance of 1000 erasing/programming cycles. the flash memory can be programmed, either in a programming board, or in the target system. the code to program or erase the flash memory is executed from an external memory or from the on-chip ram, but not from the flash memory itself. as a flexible and cost-saving alternative, the on-chip bootstrap loader may be used to load and start the programming code.

the following considerations must be taken into account for programming or erasing ‘on-line’ in the target system:

- While operations are in progress, the flash memory can not be accessed as usual, no branch can be made to the flash memory and no data reads can be taken from the flash memory.
- If the two first blocks (8KB + 24KB) of the flash memory are mapped to segment 0, no interrupt or hardware trap must occur during programming or erasing, as this would require a ‘forbidden’ branch to the flash memory.

A flash memory protection option, when activated, prevents view access to the contents of the ROM and the on-chip RAM, code operation from within the flash memory continues as normal. During the initialization phase, the first two blocks of the flash memory (8KB + 24KB) can be mapped to segment 0 (addresses 00000h to 07FFFh), or to segment 1 (addresses 10000h to 17FFFh). This makes it possible to use external memory for additional system flexibility.

5.1 Programming/erasing with ST Embedded Algorithm Kernel

In order to secure flash programming and erasing operations, and also to simplify the software development for programming and erasing the Flash, the ST10F163 Flash is programmed or erased by executing a specific sequence of instructions (called 'Unlock Sequence') with command and parameters loaded into GPRs. The Unlock Sequence' invokes embedded kernel routines that checks the validity of the parameters provided by the user, and decodes the command (programming or erasing) and executes it.

When performing a programming command, the Embedded Algorithm Kernel automatically times the program pulse widths (taking in account the CPU period provided as a parameter by the user) and verifies proper cell programming.

When performing an erasing command, the Embedded Algorithm Kernel automatically pre-programs the bank to be erased if it is not already programmed. During erase, the Embedded Algorithm Kernel automatically times the erase pulse widths (taking in account the CPU period provided as a parameter by the user) and verifies proper cell erasing.

To start a program/erase operation, the user's application must perform an 'Unlock Sequence' to trigger the flash ST Embedded Algorithms Kernel (STEAK). Before using STEAK, proper parameters must be assigned through the R0-R4 registers. The R0 register is the command register. The other registers handle the address and data to be programmed or sector to be erased. Table 3 defines the command sequence. A definition of the codes used in Table 3 is given in Table 4.

COMMAND	R0	R1	R2	R3	R4
Single word programming	55Ash	AddOff	W	nu	2TCL
Double Word programming	DD4sh	AddOff	DWL	DWH	2TCL
Block programming	AA5sh	BegAddOff	EndAddOff	SourceAddr	2TCL
Sector Erasing	EEEEh	5555h	Bnk	Bnk	2TCL
Read Status	7777h	nu	nu	nu	2TCL

Table 3 Command -parameters definition

Note The read status for registers R1 to R3 is not used except for the return values, refer to “Return values” on page 16

Abbreviation	Definition
s	Segment of the target flash memory cell
AddOff	Segment Offset of the target flash memory cell which must be even an value (word-aligned address).
W	Data (word) to be written in flash.
DWL,DWH	Data (double word, DHL = low word, DWH = high word to be written in Flash,
BegAddOff	Segment Offset of the FIRST target flash memory word to be written in a multiple programming command. This value must be even (word-aligned address)
EndAddOff	Segment Offset of the LAST Target Flash Memory word to be written in a Multiple programming command. Must be even value (word-aligned address). The value D = (EndAddOff - BegAddOff) must be: 0 <= D < 16384 (ie. up to one page (16 KBytes) can be written in the flash with one multi-word programming command).
SourceAdd	Start address for the source data (block) to be programmed. This address uses implicitly the data paging mechanism of the CPU. SourceAdd value must respect the rules: SourceAdd + (EndAddOff - BegAddOff) < 16384. Page 0 and 1 can NOT be used for source data if SYSCON bit ROMS1 = ‘1’ **Note**: source data can be located in flash (In pages 0, 1, 6, 7, 8, 9, 10 or 11 if bit ROMS1 = ‘0’, or in pages 4, 5, 6, 7, 8, 9, 10 or 11 if bit ROMS1 = ‘1’.
Bnk	Number of the Bank to be erased. Note that for security, R2 and R3 must hold the same value.
2TCL	CPU clock period in nseconds (e.g. R4 = 40d means CPU frequency is 25MHz).

Table 4 Code definition

The Flash Unlock Sequence consists of two consecutive writes: the direct addressing mode and the indirect addressing mode. The FCR must represent an even address in the active address space of the flash memory. Rwn can be any unused word GPR (R6 to R15), loaded with a value that results in the same even address as for FCR

```
EXTS      #1, #2        ; assumes flash is mapped in seg 1
MOV       FCR, R7       ; first part
```

```
MOV       [R7], R7      ; second part
```

For easier coding, the standard data paging addressing scheme is overridden for the two MOV instruction of the Flash Trigger Sequence (EXTS instruction). This also locked both standard and PEC interrupts and class A hardware traps. Must be replace by ATOMIC instruction if standard DPP addressing scheme must be preserved.

When the embedded programming/erasing algorithm returns to trigger point, information can be collected through register R0 so the user can take specific actions. Table 5 lists all of the error codes that can be returned in R0.

ERROR CODE	MEANING
00h	Operation was successful
01h	ROMEN bit inside SYSCON is not set
02h	Vpp voltage not present
03h	Programming operation failed
04h	Address value (R1) incorrect: not in Flash address area or odd
05h	CPU period out of range (must be between 10 ns to 1000 ns)
06h	Not enough free space on system stack for proper operation
07h	Incorrect bank number (R2,R3) specified
08h	Erase operation failed
09h	Bad source address for multi-word programming command
0Ah	Bad number of words to be copied in multi-word programming command: one destination will be out of flash, or one source operand will be out of the source page
FFh	Unknown or bad command

Table 5 Error code definition

Note The Flash Embedded Presto Algorithms require at least 45 words on the Internal System Stack for proper operation. The program verifies itself that there is enough free space on the System Stack before performing a programming or erasing operation (by comparing SP value with STKOV+90d).

5.1.1 Return values

After a single or double word programming command, R0 contains error code, R1 remains unchanged, R2 will contain the data in Flash for location Segment+Segment Offset (R0.[3:0] with R1), R3 will contain the data in Flash for location Segment+Segment Offset +2 (R0[3:0] with R1+2), R4 to R15 remain unchanged.

After a multi-word programming command, R0 contains error code, R1 will contains the last segment offset address of the last written word in flash (failing flash address if R0 is not equal to zero), R2 and R3 are undefined, R4 to R15 remain unchanged.

After erasing command, only R4 to R15 remain unchanged, R0 will contain error code, R1 to R3 are undefined.

After status read command, R0 contains error code, R1 contains flash embedded revision, R2 and R3 contains circuit identifiers (R2 = #0787h and R3 = #0101h for this device), R4 to R15 remain unchanged.

5.1.2 Programming examples

Programming a double word:

```
; code hereafter assumes that flash is mapped in segment 1
; i.e. bit ROMS1 = ‘1’ in SYSCON register
; Flash must also be enabled, i.e. bit ROMEN = ‘1’ in SYSCON.
MOV         R0, #PROGDW  ; DD4xh: Double word programming command
OR          R0, #01h     ; Selects segment 1 in flash memory
MOV         R1, #00224h  ; Address to be programmed is 01’0224h
MOV         R2, #03456h  ; Data to be programmed at 01’0224h
MOV         R3, #04567h  ; Data to be programmed at 01’0226h
MOV         R4, #050d    ; 50ns is 20 MHz CPU clock frequency
MOV         R7, #08000h  ; R7 used for Flash trigger sequence
#define FCR 08000h
; Flash Unlock Sequence: consists in two consecutive writes, with the
direct addressing mode and then the indirect addressing mode. FCR must
represent an even address in the active address space of the Flash memory,
and Rwn can be any unused word GPR (R6 to R15)loaded with a value resulting
in the same even address than FCR
EXTS        #1, #2       ; flash can be mapped in segment 0 or 1
MOV         FCR, R7      ; first part
MOV         [R7], R7     ; second part
NOP                      ; WARNING: place 2 NOP operations after
NOP                      ; the Unlock sequence to avoid all possible
                         ; pipeline conflict in STEAK programs
```

Note *For easier coding, the standard data paging addressing scheme is overrides for the two MOV instruction of the Flash Trigger Sequence (EXTS instruction).This also locked both standard and PEC interrupts and class A hardware traps. Must be replace by ATOMIC instruction if standard DPP addressing scheme must be preserved.*

Programming a block of data:

Address 01'9000h to 01'9FFEh (inclusive) is to be programmed. Source data (data to be copied into flash) is located in external RAM from address 03'1000h (to 03'1FFEh, implicitly):

```
; code hereafter assumes that flash is mapped in segment 1
; i.e. bit ROMS1 = '1' in SYSCON register
; Flash must also be enabled, i.e. bit ROMEN = '1' in SYSCON.
MOV      R0, #PROGMW    ; AA5xh: Multi word programming command
OR       R0, #01h       ; Selects segment 1 in flash memory
MOV      R1, #09000h    ; First Flash Segment Offset Address
MOV      R2, #09FFEh    ; Last Flash Segment Offset Address
MOV      R3, #01000h    ; Source data address: use DPP2 as
                        ; data page pointer
SCXT     DPP2,#0Ch      ; Source is in page 12 (0Ch): save previous
                        ; DPP2 value and load it with source page
                        ; number
MOV      R4, #050d      ; 50ns is 20 MHz CPU clock frequency
MOV      R7, #08000h    ; R7 used for Flash trigger sequence
#define FCR 08000h
EXTS     #1, #2         ; flash can be mapped in segment 0 or 1
MOV      FCR, R7        ; first part
MOV      [R7], R7       ; second part
NOP                     ; WARNING: place 2 NOP operations after
NOP                     ; the Unlock sequence to avoid all possible
                        ; pipeline conflict in STEAK programs
POP      DPP2           ; restore DPP2
```

5.2 Flash memory configuration

The default memory configuration is determined by the state of the $\overline{EA}$ pin at reset. This value is stored in the Internal ROM enable bit: ROMEN of the SYSCON Register.

When ROMEN=0, the internal ROM is disabled and external ROM is used for start-up control. The first 32KBytes of the flash memory area must be re-mapped to segment 1, to enable their later use. This is done by setting the ROMS1 bit of SYSCON to 0. This is done by the externally supplied program, before the execution of the EINIT instruction.

If program execution starts from external memory, but access to the flash memory (re-mapped to Bank 1) is required later, one of the following values has to be written to the SYSCON register, before the end of initialization:

- If flash is to be mapped to segment 1: xxx100xxxxxxxxxxb (ROMS1=1,SGTDIS=0)
- If flash is to be mapped to segment 0: xxx000xxxxxxxxxxb (ROMS1=0,SGTDIS=0)

All other parts of the flash memory (addresses 18000h - 1FFFFh) remain unaffected.

The SGTDIS Segmentation Disable/Enable must be set to 0 so that the 64KBytes of on-chip memory can be used in addition to the external boot memory. The correct procedure for changing the segmentation registers must be observed, to prevent unwanted trap conditions:

- Instructions that configure the internal memory must only be executed from external memory or from the internal RAM.
- Whenever the internal memory is disabled, enabled or re-mapped, the DPPs must be explicitly (re)loaded to enable correct data accesses to the internal memory and/or external memory.

5.3 Flash protection

The flash protection mode, prevents the reading of data operands in the flash memory by anything but a program executed from the flash memory itself. Flash protection mode permits program branches from, or into the flash memory, but does not permit erasing and programming of the flash memory.

Flash protection is controlled by the Protection UPROM Programming Bit (UPROG). UPROG is a 'hidden' one-time programmable bit. It is only accessible in a special mode, entered, for example, via a flash EPROM programming board. If UPROG is set to '1', flash protection is active after reset. By default flash protection is disabled (UPROG=0).

For deactivation of flash protection, where the flash memory has to be reprogrammed with updated program/variables, a zero value must be written at every even address in the active address space of the flash memory. This write can only be done by an instruction executed from the internal flash memory itself, e.g. MOV FLASH,ZEROS

6 External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes:

- 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
- 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable. This gives the choice of a wide range of different types of memories and external peripherals. In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx). This gives access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0. Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. Access to very slow memories is supported via a particular 'Ready' function.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration so that external resources can be shared with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register SYSCON. After setting HLDEN once, pins P6.7...P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{HLDA}$ pin is an output.

By setting bit DP6.7 to'1' the Slave Mode is selected where pin $\overline{HLDA}$ is switched to input. This allows to directly connect the slave controller to another master controller without glue logic.

For applications which require less than 16 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte or to 64 KByte. In this case Port 4 outputs four, two or no address lines at all. If an address space of 16 MBytes is used, it outputs all 8 address lines.

Note *When the on-chip SSP Module is to be used the segment address output on Port 4 must be limited to 4 bits (i.e. A19...A16) in order to enable the alternate function of the SSP interface pins.*

6.1 Programmable chip select timing control

The position of the CSx lines can be changed by setting the CSCFG bit in the SYSCON register. By default the CSx lines change half a CPU clock cycle after the rising edge of ALE (20ns @ f_{CPU} = 25 MHz). With the CSCFG bit set (section *Figure 7*), the CSx lines change with the rising edge of ALE. In this case, the CSx lines and address lines change at the same time.

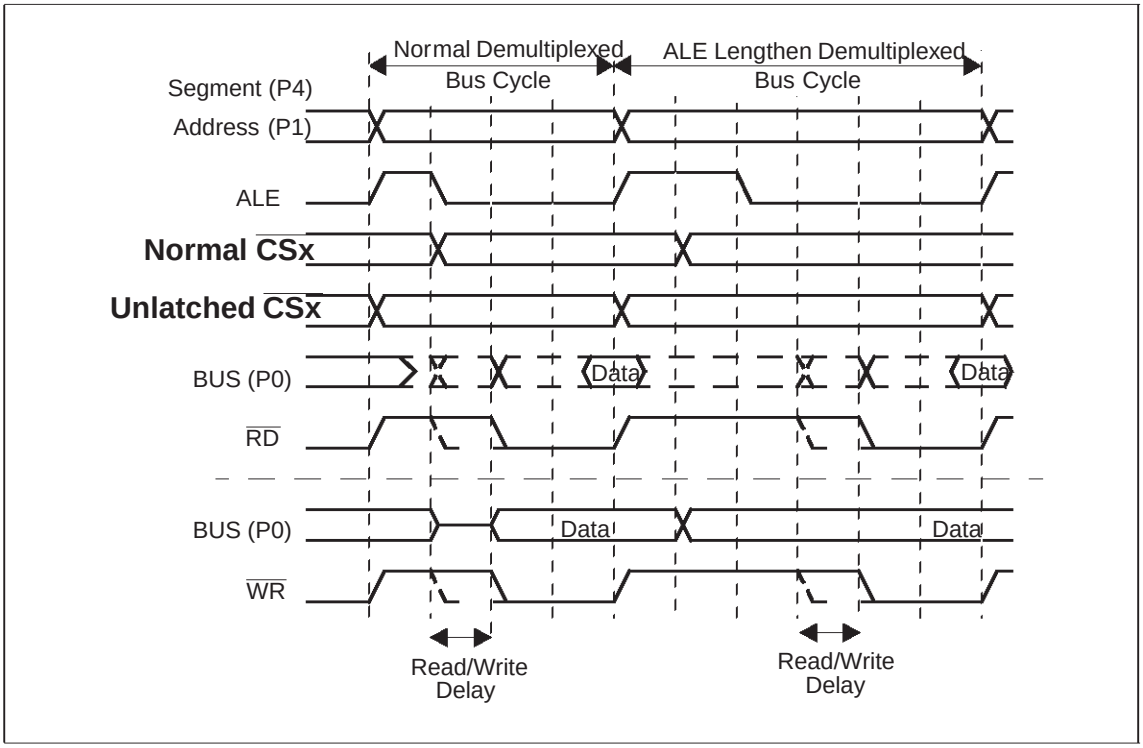


Figure 4 Chip select delay

7 Central Processing Unit (CPU)

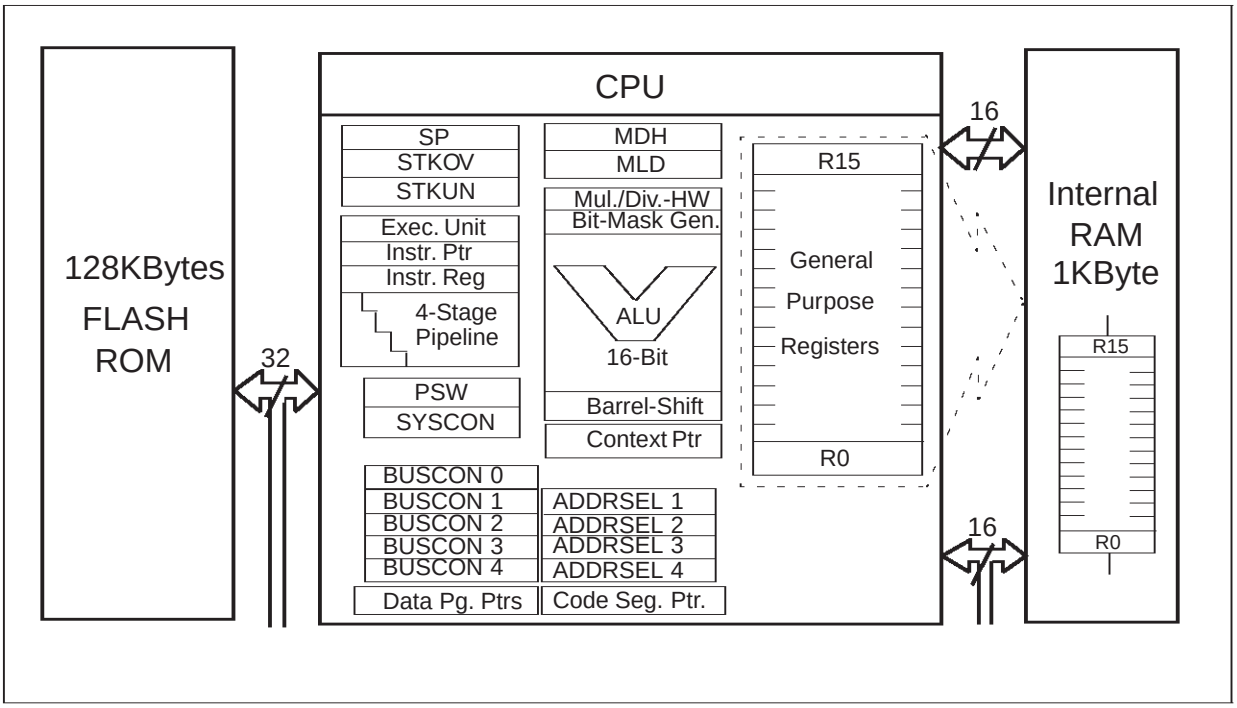


Figure 5 CPU block diagram

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been added for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the ST10F163's instructions can be executed in one machine cycle. This requires 80ns at 25MHz CPU clock. For example, shift and rotate instructions are always processed in one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized for speed: branches in 2 cycles, a 16 x 16 bit multiplication in 5 cycles and a 32-/16 bit division in 10 cycles. The 'Jump Cache' pipeline optimization, reduces the execution time of repeatedly performed jumps in a loop, from 2 cycles to 1 cycle.

The CPU includes an actual register context. This consists of up to 16 wordwide GPRs physically allocated in the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, one register bank may overlap others.

A system stack of up to 1024 bytes is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack

pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes exist.

8 Interrupt System

With an interrupt response time from 200 ns to 480ns (in the case of internal program execution), the ST10F163 reacts quickly to the occurrence of non-deterministic events.

The architecture of the ST10F163 supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In a standard interrupt service, program execution is suspended and a branch to the interrupt vector table is performed. For a PEC service, just one cycle is 'stolen' from the current CPU activity. A PEC service is a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is decremented for each PEC service, except for the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are suited to, for example, the transmission or reception of blocks of data. The ST10F163 has 8 PEC channels, each of which offers fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield, exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs, feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

Table 6 shows all of the possible ST10F163 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers:

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
External Interrupt 0	CC8IR	CC8IE	CC8INT	00'0060h	18h
External Interrupt 1	CC9IR	CC9IE	CC9INT	00'0064h	19h
External Interrupt 2	CC10IR	CC10IE	CC10INT	00'0068h	1Ah
External Interrupt 3	CC11IR	CC11IE	CC11INT	00'006Ch	1Bh
External Interrupt 4	CC12IR	CC12IE	CC12INT	00'0070h	1Ch
External Interrupt 5	CC13IR	CC13IE	CC13INT	00'0074h	1Dh
External Interrupt 6	CC14IR	CC14IE	CC14INT	00'0078h	1Eh
External Interrupt 7	CC15IR	CC15IE	CC15INT	00'007Ch	1Fh
GPT1 Timer 2	T2IR	T2IE	T2INT	00'0088h	22h
GPT1 Timer 3	T3IR	T3IE	T3INT	00'008Ch	23h
GPT1 Timer 4	T4IR	T4IE	T4INT	00'0090h	24h
GPT2 Timer 5	T5IR	T5IE	T5INT	00'0094h	25h
GPT2 Timer 6	T6IR	T6IE	T6INT	00'0098h	26h
GPT2 CAPREL Register	CRIR	CRIE	CRINT	00'009Ch	27h
ASC0 Transmit	S0TIR	S0TIE	S0TINT	00'00A8h	2Ah
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	00'011Ch	47h
ASC0 Receive	S0RIR	S0RIE	S0RINT	00'00ACh	2Bh
ASC0 Error	S0EIR	S0EIE	S0EINT	00'00B0h	2Ch
SSP Interrupt	XP1IR	XP1IE	XP1INT	00'0104h	41h
PLL Unlock / OWD	XP3IR	XP3IE	XP3INT	00'010Ch	43h

Table 6 List of possible interrupt sources, flags, vector and trap numbers

The ST10F163 provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, called'Hardware Traps'. Hardware traps cause an

immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 7 shows all of the possible exceptions or error conditions that can arise during run time.

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions:					
Hardware Reset		RESET	00'0000h	00h	III
Software Reset		RESET	00'0000h	00h	III
Watchdog Timer Overflow		RESET	00'0000h	00h	III
Class A Hardware Traps:					
Non-Maskable Interrupt	NMI	NMITRAP	00'0008h	02h	II
Stack Overflow	STKOF	STOTRAP	00'0010h	04h	II
Stack Underflow	STKUF	STUTRAP	00'0018h	06h	II
Class B Hardware Traps:					
Undefined Opcode	UNDOPC	BTRAP	00'0028h	0Ah	I
Protected Instruction Fault	PRTFLT	BTRAP	00'0028h	0Ah	I
Illegal Word Operand Access	ILLOPA	BTRAP	00'0028h	0Ah	I
Illegal Instruction Access	ILLINA	BTRAP	00'0028h	0Ah	I
Illegal External Bus Access	ILLBUS	BTRAP	00'0028h	0Ah	I
Reserved			[2Ch –3Ch]	[0Bh – 0Fh]	
Software Traps: TRAP Instruction			Any [00'0000h–00'01FCh] in steps of 4h	Any [00h – 7Fh]	Current CPU Priority

Table 7 Exceptions or error conditions that can arise during run-time

9 General Purpose Timer (GPT) Unit

The GPT unit is a flexible multifunctional timer/counter structure which is used for time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication. The GPT unit contains five 16-bit timers organized into two separate modules GPT1 and GPT2. Each timer in each module may operate independently in several different modes, or may be concatenated with another timer of the same module.

9.1 GPT1

Each of the three timers T2, T3, T4 of module GPT1 can be configured individually for one of three basic modes of operation: **timer**, **gated timer**, and **counter** mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable pre-scaler. In counter Mode a timer is clocked in reference to external events. Gated timer mode supports pulse width or duty cycle measurement, where the operation of a timer is controlled by the 'gate' level on an external input pin. Each timer has one associated port pin (TxIN) which serves as gate or clock input.

Table 8 GPT1 timer input frequencies, resolution and periods lists the timer input frequencies, resolution and periods for each pre-scaler option at 25 MHz CPU clock.

f_{CPU} = 25MHz	Timer Input Selection T2I / T3I / T4I							
	000_B	001_B	010_B	011_B	100_B	101_B	110_B	111_B
Pre-scaler factor	8	16	32	64	128	256	512	1024
Input Frequency	3.125 MHz	1.563 MHz	781.3 kHz	390.6 kHz	195.3 kHz	97.66 kHz	48.83 kHz	24.41 kHz
Resolution	320 ns	640 ns	128 ns	2.56 µs	5.12 µs	10.24 µs	20.48 µs	40.96 µs
Period	21.0 ms	41.9 ms	83.9 ms	167 ms	336 ms	671 ms	1.34 s	2.68 s

Table 8 GPT1 timer input frequencies, resolution and periods

The count direction (up/down) for each timer is programmable by software or is altered dynamically by an external signal on a port pin (TxEUD). For example, this facilitates position tracking.

Timer T3 has output toggle latches (TxOTL) which changes state on each timer over-flow/ underflow. The state of this latch may be output on port pins (TxOUT) e. g. for time out

monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as reload or capture registers, timers T2 and T4 are stopped. The content of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4, triggered, either by an external signal or by a selectable state transition of its toggle latch, T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

9.2 GPT2

The GPT2 module provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6 which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, or it may be output on a port pin (T6OUT). The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

Table 9 GPT2 timer input frequencies, resolution and period lists the timer input frequencies, resolution and periods for each pre-scaler option at 25 MHz CPU clock.

f_{CPU} = 25MHz	Timer Input Selection T5I / T6I							
	000_B	001_B	010_B	011_B	100_B	101_B	110_B	111_B
Pre-scaler factor	4	8	16	32	64	128	256	512
Input Frequency	6.25 MHz	3.125 MHz	1.563 MHz	781.3 kHz	390.6 kHz	195.3 kHz	97.66 kHz	48.83 kHz
Resolution	160ns	320 ns	640 ns	128 ns	2.56 µs	5.12 µs	10.24 µs	20.48 µs
Period	10.49ms	21.0 ms	41.9 ms	83.9 ms	167 ms	336 ms	671 ms	1.34 s

Table 9 GPT2 timer input frequencies, resolution and period

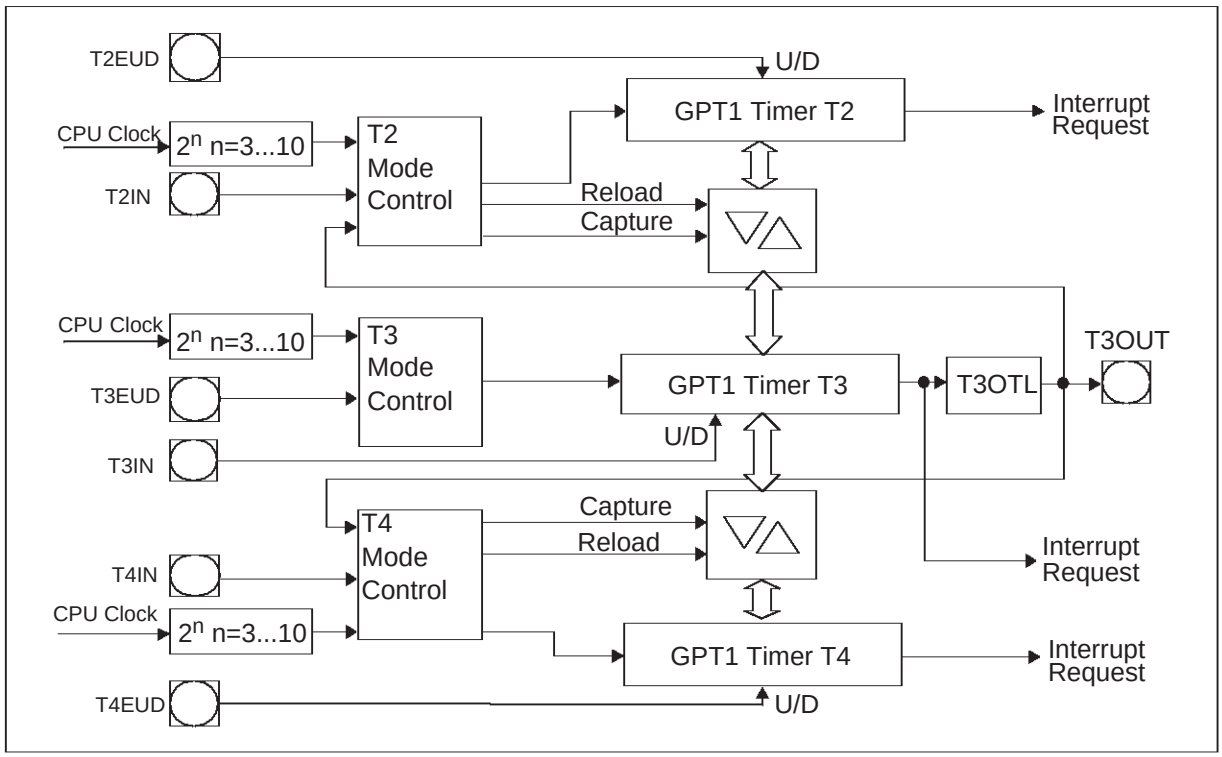


Figure 6 Block diagram of GPT1

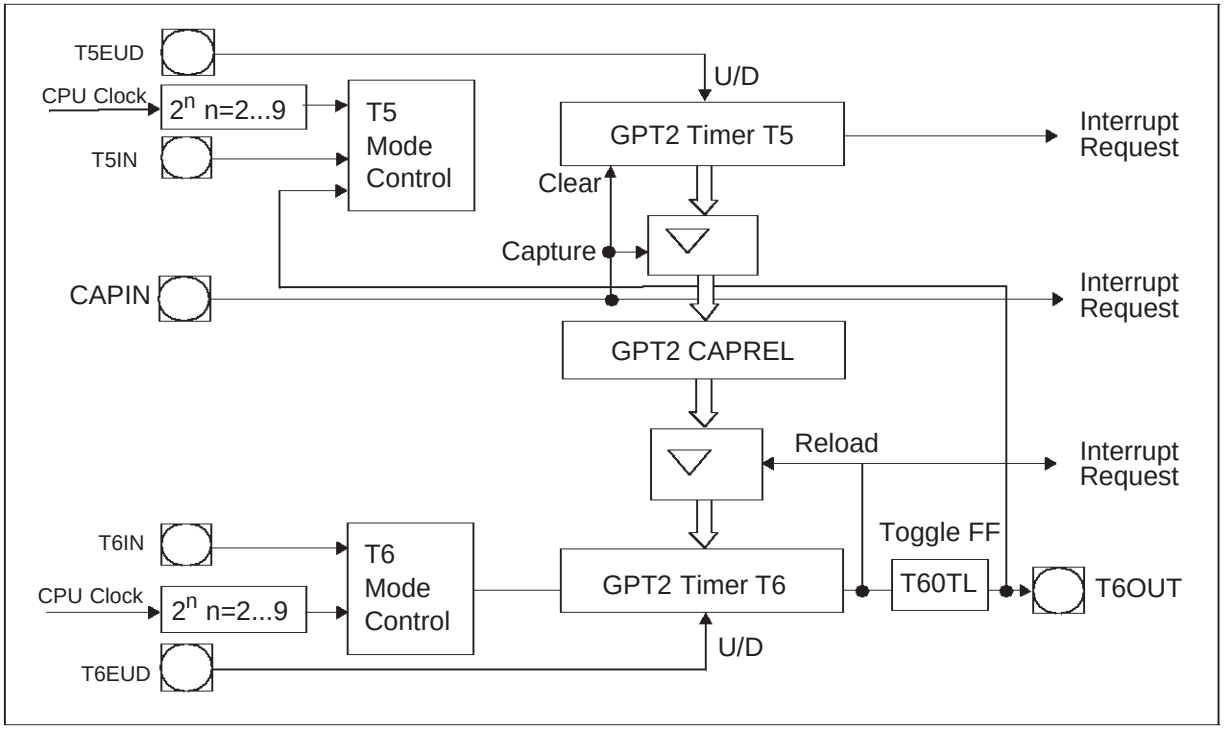


Figure 7 Block diagram of GPT2

10 Parallel Ports

The ST10F163 provides up to 77 I/O lines which are organized into six input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as, either inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of three I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

All port lines have associated, programmable, alternate input or output functions. PORT0 and PORT1 may be used as address and data lines when accessing external memory. Port 4 outputs the additional segment address bits A23/19/17...A16 in systems where segmentation is enabled to access more than 64 KBytes of memory. Port 6 provides optional bus arbitration signals ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) and chip select signals. Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal $\overline{BHE}$ and the system clock output (CLKOUT). Port 5 is used for timer control signals. All port lines that are not used for these alternate functions may be used as general purpose I/O lines.

11 Serial Channels

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces, an Asynchronous/Synchronous Serial Channel (ASC0) and a Synchronous Serial Port (SSP).

ASC0: The table below shows the baud rates for the asynchronous/synchronous serial channel.

A dedicated baud rate generator is used to set up all standard baud rates without oscillator tuning. 3 separate interrupt vectors are provided for transmission, reception, and erroneous reception. In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data + wake up bit mode).

In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The ASC0 always shifts the LSB first. A loop back option is available for testing purposes.

A number of optional hardware error detection capabilities have been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not

been read out of the receive buffer register by the time the reception of a new character is complete.

S0BRS = '0', f_{CPU} = 25MHz			S0BRS = '1', f_{CPU} = 25MHz		
Baud Rate (Baud)	**Deviation Error**	**Reload Value**	**Baud Rate (Baud)**	**Deviation Error**	**Reload Value**
781250	±0.0%	0000_H	520833	±0.0%	0000_H
56000	+7.3% /-0.4%	$000C_H$ / $000D_H$	56000	+3.3% / -7.0%	0008H / 0009H
38400	+1.7% / -3.1%	0013_H / 0014_H	38400	+4.3% / -3.1%	000CH / 000DH
19200	+1.7% / -0.8%	0027_H / 0028_H	19200	+0.5% / -3.1%	001AH / 001BH
9600	+0.5% / -0.8%	0050_H/ 0051_H	9600	+0.5% / -1.4%	0035H / 0036H
4800	+0.5% / -0.1%	$00A1_H$ / $00A2_H$	4800	+0.5% / -0.5%	006BH / 006CH
2400	+0.2% / -0.1%	0144_H / 0145_H	2400	+0.0% / -0.5%	00D8H / 00D9H
1200	+0.0% / -0.1%	$028A_H$ / $028B_H$	1200	+0.0% / -0.2%	01B1H / 01B2H
600	+0.0% / -0.1%	0515_H / 0516_H	600	+0.0% / -0.1%	0363H / 0364H
95	+0.4% / 0.4%	$1FFF_H$ / $1FFF_H$	75	+0.0% / 0.0%	1B1FH / 1B20H
			63	+0.9% / 0.9%	1FFFH / 1FFFH

Table 10 Commonly used baud rates by reload value and deviation errors

Note The deviation errors given in the table above are rounded.
Using a baudrate crystal will provide correct baudrates without deviation errors.

SSP: The Synchronous Serial Port provides high-speed serial communication with external slave devices such as EEPROM. The SSP transmits 1...3 bytes or receives 1 byte after sending 1...3 bytes synchronously to a shift clock which is generated by the SSP. The SSP can start shifting with the LSB or with the MSB and is used to select shifting and latching clock edges as well as the clock polarity. Up to two chip select lines may be activated in order to direct data transfers to one or both of two peripheral devices.

SSPCKS Value		Synchronous baud rate
000	SSP clock = CPU clock divided by 2	12.5 MBit/s
001	SSP clock = CPU clock divided by 4	6.25 MBit/s
010	SSP clock = CPU clock divided by 8	3.13 MBit/s
011	SSP clock = CPU clock divided by 16	1.56 MBit/s
100	SSP clock = CPU clock divided by 32	781 KBit/s
101	SSP clock = CPU clock divided by 64	391 KBit/s
110	SSP clock = CPU clock divided by 128	195 KBit/s
111	SSP clock = CPU clock divided by 256	97.7 KBit/s

Table 11 Synchronous baud rate and SSPCKS reload values

12 Watchdog Timer

The Watchdog Timer is a fail-safe mechanism which the maximum malfunction time of the controller

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. In this way the chip's start-up procedure is always monitored. The software must be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided either by 2 or by 128. The high byte of the Watchdog Timer register can be set to a pre-specified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. The table below shows the watchdog time range which for a 25MHz CPU clock. Some numbers are rounded to 3 significant digits.

Reload value in WDTREL	Prescaler for f_{CPU}	
	2 (WDTIN = '0')	128 (WDTIN = '1')
FF_H	20.48 µs	1.31 ms
00_H	5.24 ms	336 ms

Table 12 Watchdog time range for 25MHz CPU clock

Note For security, rewrite WDTCON each time before the watchdog timer is serviced.

13 Oscillator Watchdog (OWD)

The Oscillator Watchdog (OWD) monitors the clock signal generated by the on-chip oscillator (either with a crystal or via external clock drive). For this operation the PLL provides a clock signal to supervise transitions on the oscillator clock. This PLL clock is independent from the XTAL1 clock. When the expected oscillator clock transitions are missing, the OWD activates the PLL Unlock/OWD interrupt node and supplies the CPU with the PLL clock signal. Under these circumstances the PLL will oscillate with its basic frequency.

A low level on pin OWE disables the OWD's interrupt output, so that the clock signal is derived from the oscillator clock. The CPU clock source is only switched back to the oscillator clock after a hardware reset.

When the direct-drive, or direct-drive-with-prescaler clock option is selected, an oscillator watchdog is implemented. This provides a fail-safe mechanism in the case of a loss of external clock.

After reset, the Oscillator Watchdog is enabled by default. To disable the OWD, the bit OWDDIS (bit 4 of SYSCON register) must be set. When the OWD is enabled, PLL runs on free-running frequency, and increments the Oscillator Watchdog counter. On each transition of XTAL1 pin, the Oscillator Watchdog is cleared. If an external clock failure occurs, then the Oscillator Watchdog counter overflows (after 16 PLL clock cycles). The CPU clock signal is switched to the PLL free-running clock signal, and the Oscillator Watchdog Interrupt Request (XP3INT) is flagged. The CPU clock will not switch back to the external clock even if a valid external clock exits on XTAL1 pin. Only a hardware reset can switch the CPU clock source back to direct clock input.

When the OWD is disabled, the CPU clock is always fed from the oscillator input and the PLL is switched off to decrease power supply current.

14 Instruction Set Summary

The table below lists the instruction set of the ST10F163. More detailed information such as address modes, instruction operation, parameters for conditional execution of instructions, opcodes and a detailed description of each instruction can be found in the **"ST10 Family Programming Manual"**

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise XOR, (word/byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4

Table 13 Instruction Set

Mnemonic	Description	Bytes
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS	Move byte operand to word operand with sign extension	2 / 4
MOVBZ	Move byte operand to word operand. with zero extension	2 / 4
JMPA, JMPI, JMPR	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET	Return from intra-segment subroutine	2

Table 13 Instruction Set (Continued)

Mnemonic	Description	Bytes
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT	Disable Watchdog Timer	4
EINIT	Signify End-of-Initialization on RSTOUT-pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4
NOP	Null operation	2

Table 13 Instruction Set (Continued)

15 Special Function Register Overview

The following table lists SFRs in alphabetical order. Bit-addressable SFRs are marked with the letter “b” in column “Name”. SFRs within the Extended SFR-Space (ESFRs) are marked with the letter “E” in column “Physical Address”. Registers with on-chip X-peripherals (CAN) are marked with the letter “X” in column physical address.

An SFR can be specified by its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Name	Physical Address	8-Bit Address	Description	Reset Value
ADDRSEL1	FE18h	0Ch	Address Select Register 1	0000h
ADDRSEL2	FE1Ah	0Dh	Address Select Register 2	0000h
ADDRSEL3	FE1Ch	0Eh	Address Select Register 3	0000h
ADDRSEL4	FE1Eh	0Fh	Address Select Register 4	0000h
BUSCON0 b	FF0Ch	86h	Bus Configuration Register 0	0XX0h
BUSCON1 b	FF14h	8Ah	Bus Configuration Register 1	0000h
BUSCON2 b	FF16h	8Bh	Bus Configuration Register 2	0000h
BUSCON3 b	FF18h	8Ch	Bus Configuration Register 3	0000h
BUSCON4 b	FF1Ah	8Dh	Bus Configuration Register 4	0000h
CAPREL	FE4Ah	25h	GPT2 Capture/Reload Register	0000h
CC8IC b	FF88h	C4h	EX0IN Interrupt Control Register	0000h
CC9IC b	FF8Ah	C5h	EX1IN Interrupt Control Register	0000h
CC10IC b	FF8Ch	C6h	EX2IN Interrupt Control Register	0000h
CC11IC b	FF8Eh	C7h	EX3IN Interrupt Control Register	0000h
CC12IC b	FF90h	C8h	EX4IN Interrupt Control Register	0000h
CC13IC b	FF92h	C9h	EX5IN Interrupt Control Register	0000h
CC14IC b	FF94h	CAh	EX6IN Interrupt Control Register	0000h
CC15IC b	FF96h	CBh	EX7IN Interrupt Control Register	0000h
CP	FE10h	08h	CPU Context Pointer Register	FC00h

Table 14 Special Function Register List

Name		Physical Address		8-Bit Address	Description	Reset Value
CRIC	b	FF6Ah		B5h	GPT2 CAPREL Interrupt Control Register	0000h
CSP		FE08h		04h	CPU Code Segment Pointer Register (read only)	0000h
DP0L	b	F100h	E	80h	P0L Direction Control Register	00h
DP0H	b	F102h	E	81h	P0h Direction Control Register	00h
DP1L	b	F104h	E	82h	P1L Direction Control Register	00h
DP1H	b	F106h	E	83h	P1h Direction Control Register	00h
DP2	b	FFC2h		E1h	Port 2 Direction Control Register	0000h
DP3	b	FFC6h		E3h	Port 3 Direction Control Register	0000h
DP4	b	FFCAh		E5h	Port 4 Direction Control Register	00h
DP6	b	FFCEh		E7h	Port 6 Direction Control Register	00h
DPP0		FE00h		00h	CPU Data Page Pointer 0 Register (10 bits)	0000h
DPP1		FE02h		01h	CPU Data Page Pointer 1 Register (10 bits)	0001h
DPP2		FE04h		02h	CPU Data Page Pointer 2 Register (10 bits)	0002h
DPP3		FE06h		03h	CPU Data Page Pointer 3 Register (10 bits)	0003h
EXICONb	b	F1C0h	E	E0h	External Interrupt Control Register	0000h
IDCHIP		F07Ch	E	3Eh	Device Identifier Register	0A3Xh[1]
IDMANUF		F07Eh	E	3Fh	Manufacturer Identifier Register	0400h
IDMEM		F07Ah	E	3Dh	On-chip Memory Identifier Register	3020h
IDPROG		F078h	E	3Ch	Programming Voltage Identifier Register	9A40h
MDC	b	FF0Eh		87h	CPU Multiply Divide Control Register	0000h
MDH		FE0Ch		06h	CPU Multiply Divide Register – High Word	0000h
MDL		FE0Eh		07h	CPU Multiply Divide Register – Low Word	0000h
ODP2	b	F1C2h	E	E1h	Port 2 Open Drain Control Register	0000h
ODP3	b	F1C6h	E	E3h	Port 3 Open Drain Control Register	0000h

Table 14 Special Function Register List (Continued)

Name		Physical Address		8-Bit Address	Description	Reset Value
ODP6	b	F1CEh	E	E7h	Port 6 Open Drain Control Register	00h
ONES		FF1Eh		8Fh	Constant Value 1's Register (read only)	FFFFh
P0L	b	FF00h		80h	Port 0 Low Register (Lower half of PORT0)	00h
P0H	b	FF02h		81h	Port 0 High Register (Upper half of PORT0)	00h
P1L	b	FF04h		82h	Port 1 Low Register (Lower half of PORT1)	00h
P1H	b	FF06h		83h	Port 1 High Register (Upper half of PORT1)	00h
P2	b	FFC0h		E0h	Port 2 Register	0000h
P3	b	FFC4h		E2h	Port 3 Register	0000h
P4	b	FFC8h		E4h	Port 4 Register (8 bits)	00h
P5	b	FFA2h		D1h	Port 5 Register (read only)	XXXXh
P6	b	FFCCh		E6h	Port 6 Register (8 bits)	00h
PECC0		FEC0h		60h	PEC Channel 0 Control Register	0000h
PECC1		FEC2h		61h	PEC Channel 1 Control Register	0000h
PECC2		FEC4h		62h	PEC Channel 2 Control Register	0000h
PECC3		FEC6h		63h	PEC Channel 3 Control Register	0000h
PECC4		FEC8h		64h	PEC Channel 4 Control Register	0000h
PECC5		FECAh		65h	PEC Channel 5 Control Register	0000h
PECC6		FECCh		66h	PEC Channel 6 Control Register	0000h
PECC7		FECEh		67h	PEC Channel 7 Control Register	0000h
PSW	b	FF10h		88h	CPU Program Status Word	0000h
RP0H	b	F108h	E	84h	System Start-up Configuration Register (Rd. only)	XXh
S0BG		FEB4h		5Ah	Serial Channel 0 Baud Rate Generator Reload Reg	0000h
S0CON	b	FFB0h		D8h	Serial Channel 0 Control Register	0000h

Table 14 Special Function Register List (Continued)

Name		Physical Address		8-Bit Address	Description	Reset Value
S0EIC	b	FF70h		B8h	Serial Channel 0 Error Interrupt Control Register	0000h
S0RBUF		FEB2h		59h	Serial Channel 0 Receive Buffer Register (read only)	XXh
S0RIC	b	FF6Eh		B7h	Serial Channel 0 Receive Interrupt Control Register	0000h
S0TBIC	b	F19Ch	E	CEh	Serial Channel 0 Transmit Buffer Interrupt Control Reg	0000h
S0TBUF		FEB0h		58h	Serial Channel 0 Transmit Buffer Register (write only)	00h
S0TIC	b	FF6Ch		B6h	Serial Channel 0 Transmit Interrupt Control Register	0000h
SP		FE12h		09h	CPU System Stack Pointer Register	FC00h
SSPCON0		EF00h	X	---	SSP Control Register 0	0000h
SSPCON1		EF02h	X	---	SSP Control Register 1	0000h
SSPRTB		EF04h	X	---	SSP Receive/Transmit Buffer	XXXXh
SSPTBH		EF06h	X	---	SSP Transmit Buffer High	XXXXh
STKOV		FE14h		0Ah	CPU Stack Overflow Pointer Register	FA00h
STKUN		FE16h		0Bh	CPU Stack Underflow Pointer Register	FC00h
SYSCON	b	FF12h		89h	CPU System Configuration Register	0xx0h[2]
T2		FE40h		20h	GPT1 Timer 2 Register	0000h
T2CON	b	FF40h		A0h	GPT1 Timer 2 Control Register	0000h
T2IC	b	FF60h		B0h	GPT1 Timer 2 Interrupt Control Register	0000h
T3		FE42h		21h	GPT1 Timer 3 Register	0000h
T3CON	b	FF42h		A1h	GPT1 Timer 3 Control Register	0000h
T3IC	b	FF62h		B1h	GPT1 Timer 3 Interrupt Control Register	0000h
T4		FE44h		22h	GPT1 Timer 4 Register	0000h
T4CON	b	FF44h		A2h	GPT1 Timer 4 Control Register	0000h
T4IC	b	FF64h		B2h	GPT1 Timer 4 Interrupt Control Register	0000h

Table 14 Special Function Register List (Continued)

Name		Physical Address		8-Bit Address	Description	Reset Value
T5		FE46h		23h	GPT2 Timer 5 Register	0000h
T5CON	b	FF46h		A3h	GPT2 Timer 5 Control Register	0000h
T5IC	b	FF66h		B3h	GPT2 Timer 5 Interrupt Control Register	0000h
T6		FE48h		24h	GPT2 Timer 6 Register	0000h
T6CON	b	FF48h		A4h	GPT2 Timer 6 Control Register	0000h
T6IC	b	FF68h		B4h	GPT2 Timer 6 Interrupt Control Register	0000h
TFR	b	FFACh		D6h	Trap Flag Register	0000h
WDT		FEAEh		57h	Watchdog Timer Register (read only)	0000h
WDTCON		FFAEh		D7h	Watchdog Timer Control Register	000xh[3]
XP1IC	b	F18Eh	E	C7h	SSP Interrupt Control Register	0000h
XP3IC	b	F19Eh	E	CFh	PLL unlock Interrupt Control Register	0000h
ZEROS	b	FF1Ch		8Eh	Constant Value 0's Register (read only)	0000h

Table 14 Special Function Register List (Continued)

1. The value depends on the silicon revision and is given in the errata sheet.
2. The system configuration is selected during reset.
3. Bit WDTR indicates a watchdog timer triggered reset.

16 Electrical Characteristics

16.1 Absolute maximum ratings

- Ambient temperature under bias (T_A): ..... 0 to +70 °C
- Storage temperature (T_{ST}): ..... – 65 to +150 °C
- Voltage on V_{DD} pins with respect to ground (V_{SS}): ..... – 0.5 to +6.5 V
- Voltage on any pin with respect to ground (V_{SS}): ..... –0.5 to V_{DD} +0.5 V
- Input current on any pin during overload condition: ..... –10 to +10 mA
- Absolute sum of all input currents during overload condition: ..... |100mA|
- Power dissipation: ..... 1.5 W

Note *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN}>V_{DD}$ or $V_{IN}<V_{SS}$) the voltage on pins with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.*

16.2 Parameter Interpretation

The parameters listed in the Electrical Characteristics tables, Table 15 to Table 18, give the characteristics of the ST10F163 and its demands on the system.

Where the ST10F163 logic provides signals with their respective timing characteristics, the symbol "CC" for Controller Characteristics, is included in the "Symbol" column.

Where the external system must provide signals with their respective timing characteristics, to the ST10F163, the symbol "SR" for System Requirement, is included in the "Symbol" column.

16.3 DC characteristics

V_{DD} = 5 V ± 10% V_{SS} = 0 V Reset active T_A = 0 to +70°C

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Input low voltage	V_{IL}	SR	– 0.5	0.2 V_{DD} – 0.1	V	–
Input high voltage (all except $\overline{RSTIN}$ and XTAL1)	V_{IH}	SR	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V	–
Input high voltage $\overline{RSTIN}$	V_{IH1}	SR	0.6 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage XTAL1	V_{IH2}	SR	0.7 V_{DD}	V_{DD} + 0.5	V	–
Output low voltage[1] (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OL}	CC	–	0.45	V	I_{OL} = 2.4 mA
Output low voltage[1] (all other outputs)	V_{OL1}	CC	–	0.45	V	I_{OL1} = 1.6 mA
Output high voltage [1] (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OH}	CC	0.9 V_{DD} 2.4	–	V	I_{OH} = – 500 µA I_{OH} = –2.4 mA
Output high voltage [1 2] (all other outputs)	V_{OH1}	CC	0.9 V_{DD} 2.4	–	V V	I_{OH} = – 250 µA I_{OH} = – 1.6 mA
Input leakage current (all other)	I_{OZ2}	CC	–	±1	µA	0 V < V_{IN} < V_{DD}
$\overline{RSTIN}$ pull-up resistor [3]	R_{RST}	CC	50	250	KΩ	–
Read/Write inactive current [4]	I_{RWH} [5]		–	-40	µA	V_{OUT} = 2.4 V
Read/Write active current [4]	I_{RWL} [6]		-500	–	µA	V_{OUT} = V_{OLmax}
ALE inactive current [4]	I_{ALEL} [5]		40	–	µA	V_{OUT} = V_{OLmax}
ALE active current [4]	I_{ALEH} [6]		–	500	µA	V_{OUT} = 2.4 V
Port 6 inactive current [4]	I_{P6H} [5]		–	-40	µA	V_{OUT} = 2.4 V
Port 6 active current[4]	I_{P6L} [6]		-500	–	µA	V_{OUT} = V_{OL1max}

Table 15 DC characteristics

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
PORT0 configuration current [4]	I_{P0H} [5]	–	-10	µA	$V_{IN} = V_{IHmin}$
	I_{P0L} [6]	-100	–	µA	$V_{IN} = V_{ILmax}$
XTAL1 input current	I_{IL} CC	–	±20	µA	$0\ V < V_{IN} < V_{DD}$
Pin capacitance [4] (digital inputs/outputs)	C_{IO} CC	–	10	pF	f = 1 MHz T_A = 25 °C
Power supply current	I_{CC}	–	20 + 3.5 * f_{CPU}	mA	$\overline{RSTIN} = V_{IL2}$ f_{CPU} in [MHz] [7]
Idle mode supply current	I_{ID}	–	10 + 1.2 * f_{CPU}	mA	$\overline{RSTIN} = V_{IH1}$ f_{CPU} in [MHz] [8]
Power-down mode supply current	I_{PD}	–	50	µA	V_{DD} = 5.5 V[9]

Table 15 DC characteristics

1. ST10F163 pins are equipped with Low-Noise output drivers, which significantly improve the device's EMI performance. These Low-Noise drivers deliver their maximum current only until the respective target output level is reached. After that, the output current is reduced. This results in an increased impedance of the driver, which attenuates electrical noise from the connected PCB tracks. The current specified in column "Test Conditions" is delivered in any case.
2. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.
3. Not 100% tested, guaranteed by design characterization.
4. This specification is only valid during Reset, or during Hold- or Adapt-mode. Port 6 pins are only affected, if they are used for $\overline{CS}$ output and the open drain function is not enabled.
5. The maximum current may be drawn while the respective signal line remains inactive.
6. The minimum current must be drawn in order to drive the respective signal line active.
7. The power supply current is a function of the operating frequency. This dependency is illustrated in the figure below. These parameters are tested at V_{DDmax} and 25 MHz CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}. The chip is configured with a demux 16-bit bus, direct clock drive, 5 chip select lines and 2 segment address lines, $\overline{EA}$ pin is low during reset. After reset, Port0 is driven with the value '00CCh' that produces infinite execution of NOP instruction with 15 wait-state, R/W delay, memory tristate waitstate, normal ALE. Peripherals are not activated.

8. Idle mode supply current is a function of the operating frequency. This dependency is illustrated in the figure below. These parameters are tested at V_{DDmax} and 25 MHz CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.
9. This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} – 0.1 V to V_{DD}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

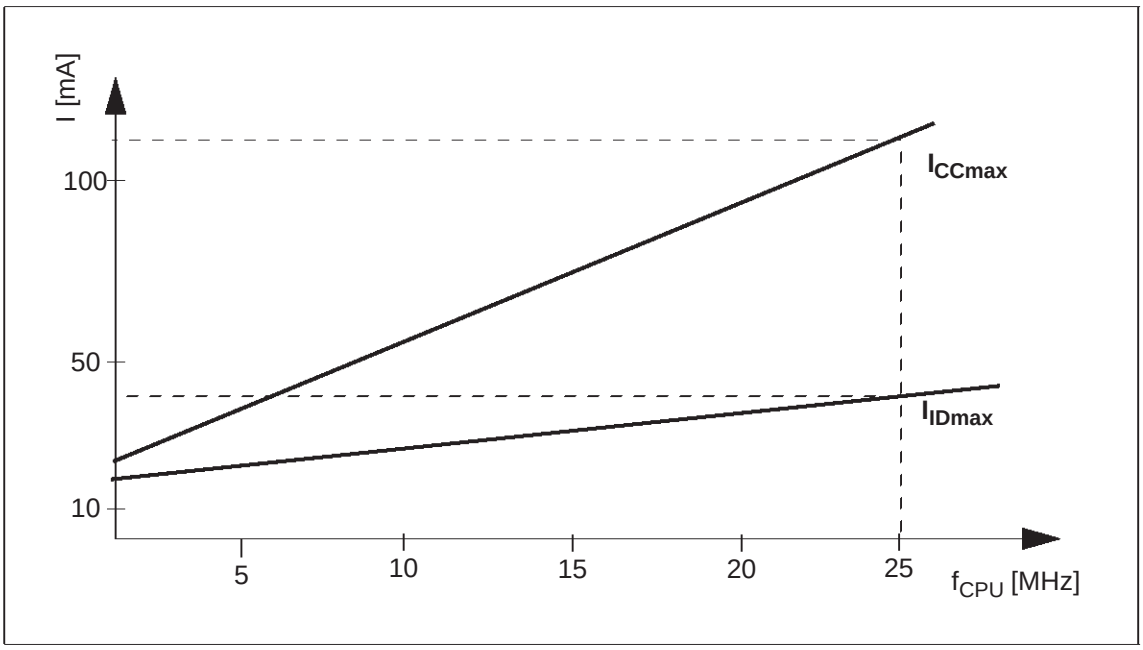
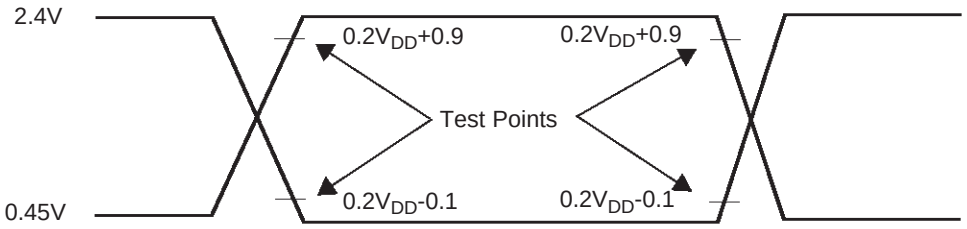


Figure 8 Supply/idle current as a function of operating frequency

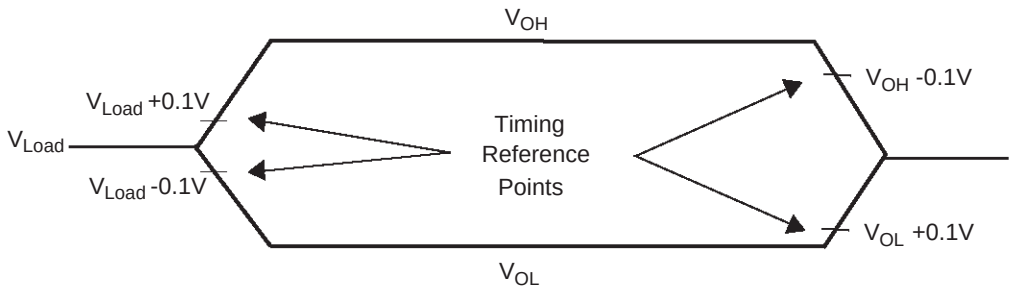
16.4 AC characteristics

16.4.1 Test waveforms



AC inputs during testing are driven at 2.4 V for a logic '1' and 0.4 V for a logic '0'. Timing measurements are made at VIH min for a logic '1' and VIL max for a logic '0'.

Figure 9 Input/output waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

Figure 10 Float waveforms

16.4.2 Definition of internal timing

The internal operation of the ST10F163 is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called "TCL" (see figure below).

The CPU clock signal can be generated by different mechanisms. The duration of TCLs and their variation (and also the derived external timing) depends on the used mechanism to

generate f_{CPU}. This influence must be regarded when calculating the timings for the ST10F163.

The example for PLL operation shown in the figure above refers to a PLL factor of 4.

The mechanism used to generate the CPU clock is selected during reset by the logic levels on pins P0.15-13 (P0H.7-5).

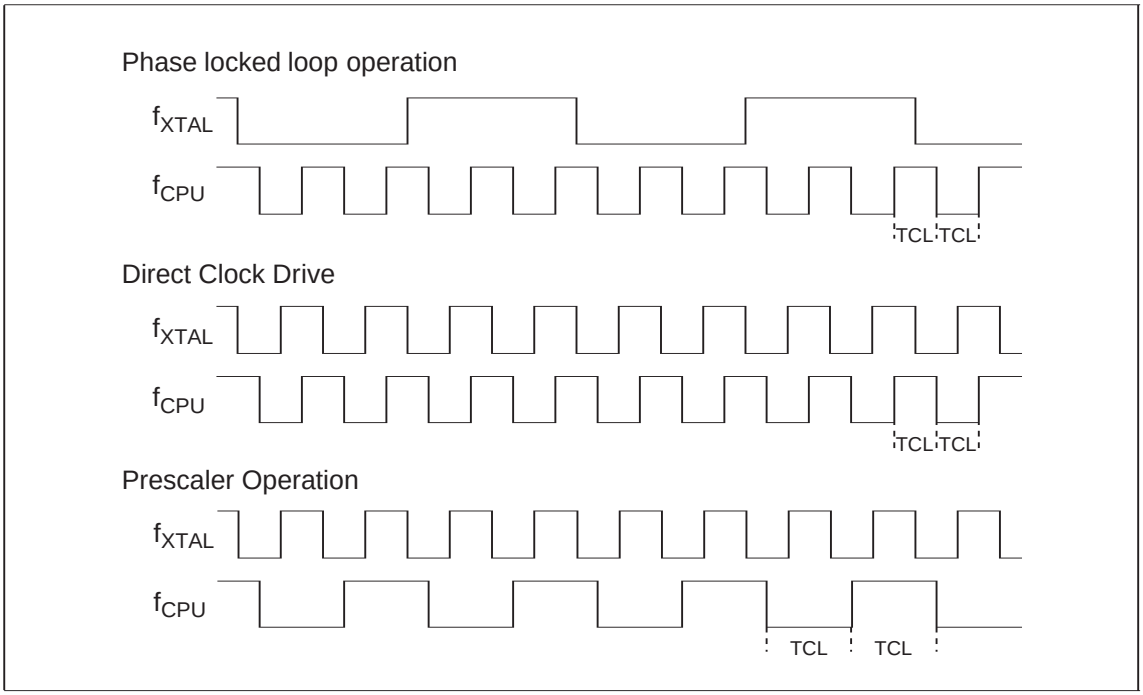


Figure 11 Generation mechanisms for the CPU clock

16.4.3 Clock generation modes

The table below associates the combinations of these three bits with the respective clock generation mode.

P0.15-13 (P0H.7-5)			CPU Frequency $f_{CPU} = f_{XTAL} * F$	External Clock Input Range[1]	Notes
1	1	1	$F_{XTAL} * 4$	2.5 to 6.25 MHz	Default configuration
1	1	0	$F_{XTAL} * 3$	3.33 to 8.33 MHz	
1	0	1	$F_{XTAL} * 2$	5 to 12.5 MHz	
1	0	0	$F_{XTAL} * 5$	2 to 5 MHz	
0	1	1	$F_{XTAL} * 1$	1 to 25 MHz	Direct drive [2]
0	1	0	$F_{XTAL} * 1.5$	6.66 to 16.6 MHz	
0	0	1	$F_{XTAL} / 2$	2 to 50 MHz	CPU clock via prescaler[3]
0	0	0	$F_{XTAL} * 2.5$	4 to 10 MHz	

1. The external clock input range refers to a CPU clock range of 1...25 MHz.
2. The maximum depends on the duty cycle of the external clock signal.
3. The maximum input frequency is 25 MHz when using an external crystal with the internal oscillator; providing that internal serial resistance of the crystal is less than 40 Ω.
   However, higher frequency can be applied with an external clock source, but in this case, the input clock signal must reach the defined levels V_{IL} and V_{IH2}.

16.4.4 Prescaler operation

When pins P0.15-13 (P0H.7-5) equal '001' during reset, the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of f_{CPU} is half the frequency of f_{XTAL} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{XTAL}.

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of f_{XTAL} for any TCL.

Note that if the bit OWDDIS in SYSCON register is cleared, the PLL is running on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

16.4.5 Direct drive

When pins P0.15-13 (P0H.7-5) equal'011' during reset the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.
The frequency of f_{CPU} directly follows the frequency of f_{XTAL} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{XTAL}.

The timings listed below that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. This minimum value can be calculated by the following formula:

$$TCL_{min} = 1/f_{XTAL} * DC_{min}$$

DC= duty cycle

For two consecutive TCLs the deviation caused by the duty cycle of f_{XTAL} is compensated so the duration of 2TCL is always $1/f_{XTAL}$. The minimum value TCL_{min} therefore has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula:

$$2TCL = 1/f_{XTAL}$$

Note *The address float timings in Multiplexed bus mode (t_{11} and t_{45}) use the maximum duration of TCL ($TCL_{max} = 1/f_{XTAL} * DC_{max}$) instead of TCL_{min}.*

If bit OWDDIS in the SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

16.4.6 Oscillator Watchdog (OWD)

When the clock option selected is direct drive or direct drive with prescaler, in order to provide a fail safe mechanism in case of a loss of the external clock, an oscillator watchdog is implemented as an additional functionality of the PLL circuitry. This oscillator watchdog operates as follows:

After a reset, the Oscillator Watchdog is enabled by default. To disable the OWD, the bit OWDDIS (bit 4 of SYSCON register) must be set.

When the OWD is enabled, the PLL is running on its free-running frequency, and increment the Oscillator Watchdog counter. On each transition of XTAL1 pin, the Oscillator Watchdog is cleared. If an external clock failure occurs, then the Oscillator Watchdog counter overflows (after 16 PLL clock cycles). The CPU clock signal will be switched to the PLL free-running clock signal, and the Oscillator Watchdog Interrupt Request (XP3INT) is flagged. The CPU

clock will not switch back to the external clock even if a valid external clock exits on XTAL1 pin. Only a hardware reset can switch the CPU clock source back to direct clock input.

When the OWD is disabled, the CPU clock is always fed from the oscillator input and the PLL is switched off to decrease power supply current.

16.4.7 Phase locked loop

For all other combinations of pins P0.15-13 (P0H.7-5) during reset the on-chip phase locked loop is enabled and provides the CPU clock (see table above). The PLL multiplies the input frequency by the factor F which is selected via the combination of pins P0.15-13 (i.e. f_{CPU} = f_{XTAL} * F). With every F'th transition of f_{XTAL} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, i.e. the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{XTAL}. The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

The timings listed in the AC Characteristics that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

The actual minimum value for TCL depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCL is lower than for one single TCL (see formula and figure below).
For a period of *N* * TCL the minimum value is computed using the corresponding deviation D_N:

$$\mathrm{TCL}_{min} = \mathrm{TCL}_{NOM} * (1 - |\mathrm{D}_N| / 100)$$

$$\mathrm{D}_N = \pm(4 - N/15)[\%]$$

where ***N*** = number of consecutive TCLs and 1 ≤ N ≤ 40. So for a period of 3 TCLs (N = 3):

$$\begin{aligned} \mathrm{D}_3 &= 4 - 3/15 \\ &= 3.8\% \\ 3\mathrm{TCL}_{min} &= 3\mathrm{TCL}_{NOM} \times (1 - 3.8/100) \\ &= \mathrm{TCL}_{NOM} \times 0.962 \\ &(57.72\,\mathrm{nsec}@\mathrm{f}_{CPU} = 25\mathrm{MHz}) \end{aligned}$$

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train

generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

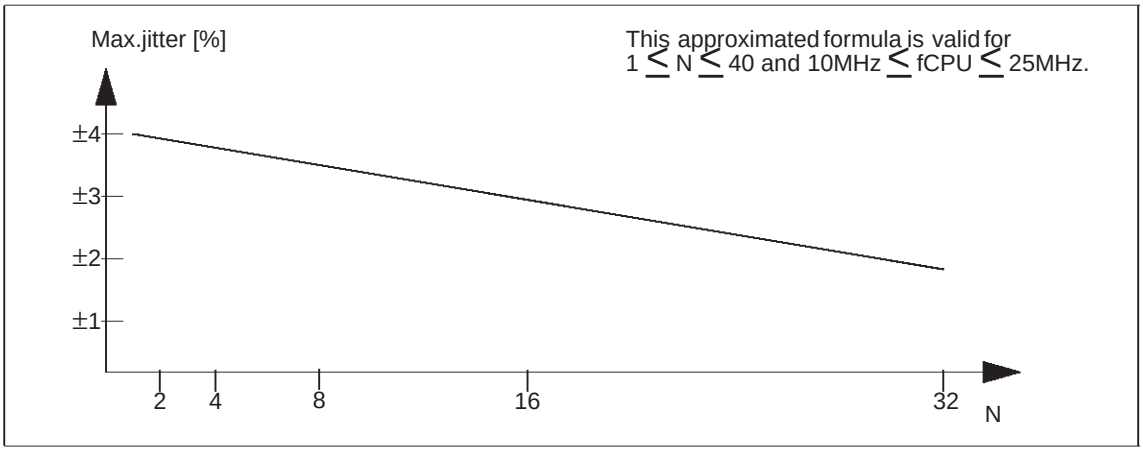


Figure 12 Approximated maximum PLL jitter

16.4.8 Memory cycle variables

The tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Description	Symbol	Values
ALE Extension	t_A	TCL * <ALECTL>
Memory Cycle Time Waitstates	t_C	2TCL * (15 - <MCTC>)
Memory Tristate Time	t_F	2TCL * (1 - <MTTC>)

16.4.9 External clock drive XTAL1

V_{DD} = 5 V ± 10% V_{SS} = 0 V T_A = 0 to +70 °C

Parameter	Symbol		$f_{CPU} = f_{XTAL}$		$f_{CPU} = f_{XTAL} / 2$		$f_{CPU} = f_{XTAL} * N$ N = 1.5/2,/2.5/3/4/5		Unit
			min	max	min	max	min	max	
Oscillator period	t_{OSC}	SR	40[1]	1000	20	500	40 * N	100 * N	ns
High time	t_1	SR	18[2]	–	6[2)]	–	10[2]	–	ns
Low time	t_2	SR	18[2]	–	6[2)]	–	10[2]	–	ns
Rise time	t_3	SR	–	10[2]	–	6[3)]	–	10[2]	ns
Fall time	t_4	SR	–	10[2]	–	6[2)]	–	10[2]	ns

1. Theoretical minimum. The real minimum value depends on the duty cycle of the input clock signal.
2. The input clock signal must reach the defined levels VIL and VIH2.

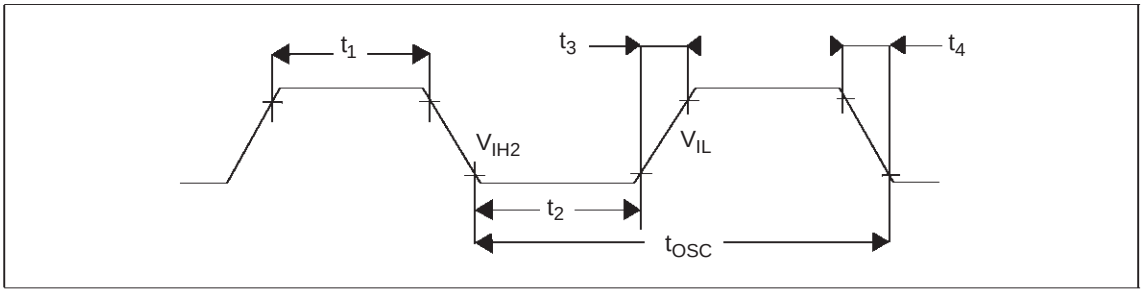


Figure 13 External clock drive XTAL1

16.4.10 Multiplexed bus

V_{DD} = 5 V ± 10% V_{SS} = 0 V T_A = 0 to +70°C C_L = 100 pF

ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (120 ns at 25-MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock 25 MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6	CC	4 + t_A	–	TCL - 16+ t_A	–	ns
Address hold after ALE	t_7	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-10 + t_A	–	-10 + t_A	–	ns
Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_{10}	CC	–	6	–	6	ns
Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_{11}	CC	–	26	–	TCL + 6	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	20 + t_C	–	2TCL - 20+ t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	40 + t_C	–	3TCL - 20+ t_C	ns
ALE low to valid data in	t_{16}	SR	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address/Unlatched $\overline{CS}$ to valid data in	t_{17}	SR	–	50 + $2t_A$ + t_C	–	4TCL - 30 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns

Table 16 Multiplexed bus characteristics

Parameter	Symbol		Max. CPU Clock 25 MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
			min.	max.	min.	max.	
Data float after $\overline{RD}$	t_{19}	SR	–	26 + t_F	–	2TCL - 14 + t_F	ns
Data valid to $\overline{WR}$	t_{22}	CC	20 + t_C	–	2TCL - 20 + t_C	–	ns
Data hold after $\overline{WR}$	t_{23}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
Address/Unlatched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	t_{27}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
ALE falling edge to Latched $\overline{CS}$	t_{38}	CC	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns
Latched $\overline{CS}$ low to Valid Data In	t_{39}	SR	–	40 + t_C + 2t_A	–	3TCL - 20 + t_C + 2t_A	ns
Latched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	t_{40}	CC	46 + t_F	–	3TCL - 14 + t_F	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{42}	CC	16 + t_A	–	TCL - 4 + t_A	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{43}	CC	-4 + t_A	–	-4 + t_A	–	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{44}	CC	–	0	–	0	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{45}	CC	–	20	–	TCL	ns
$\overline{RdCS}$ to Valid Data In (with RW delay)	t_{46}	SR	–	16 + t_C	–	2TCL - 24 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW delay)	t_{47}	SR	–	36 + t_C	–	3TCL - 24 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW delay)	t_{48}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW delay)	t_{49}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns

Table 16 Multiplexed bus characteristics

Parameter	Symbol		Max. CPU Clock 25 MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
			min.	max.	min.	max.	
Data valid to $\overline{WrCS}$	t_{50}	CC	26 + t_C	–	2TCL - 14+ t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{RdCS}$	t_{52}	SR	–	20 + t_F	–	2TCL - 20 + t_F	ns
Address hold after $\overline{RdCS}$, $\overline{WrCS}$	t_{54}	CC	20 + t_F	–	2TCL - 20 + t_F	–	ns
Data hold after $\overline{WrCS}$	t_{56}	CC	20 + t_F	–	2TCL - 20 + t_F	–	ns

Table 16 Multiplexed bus characteristics

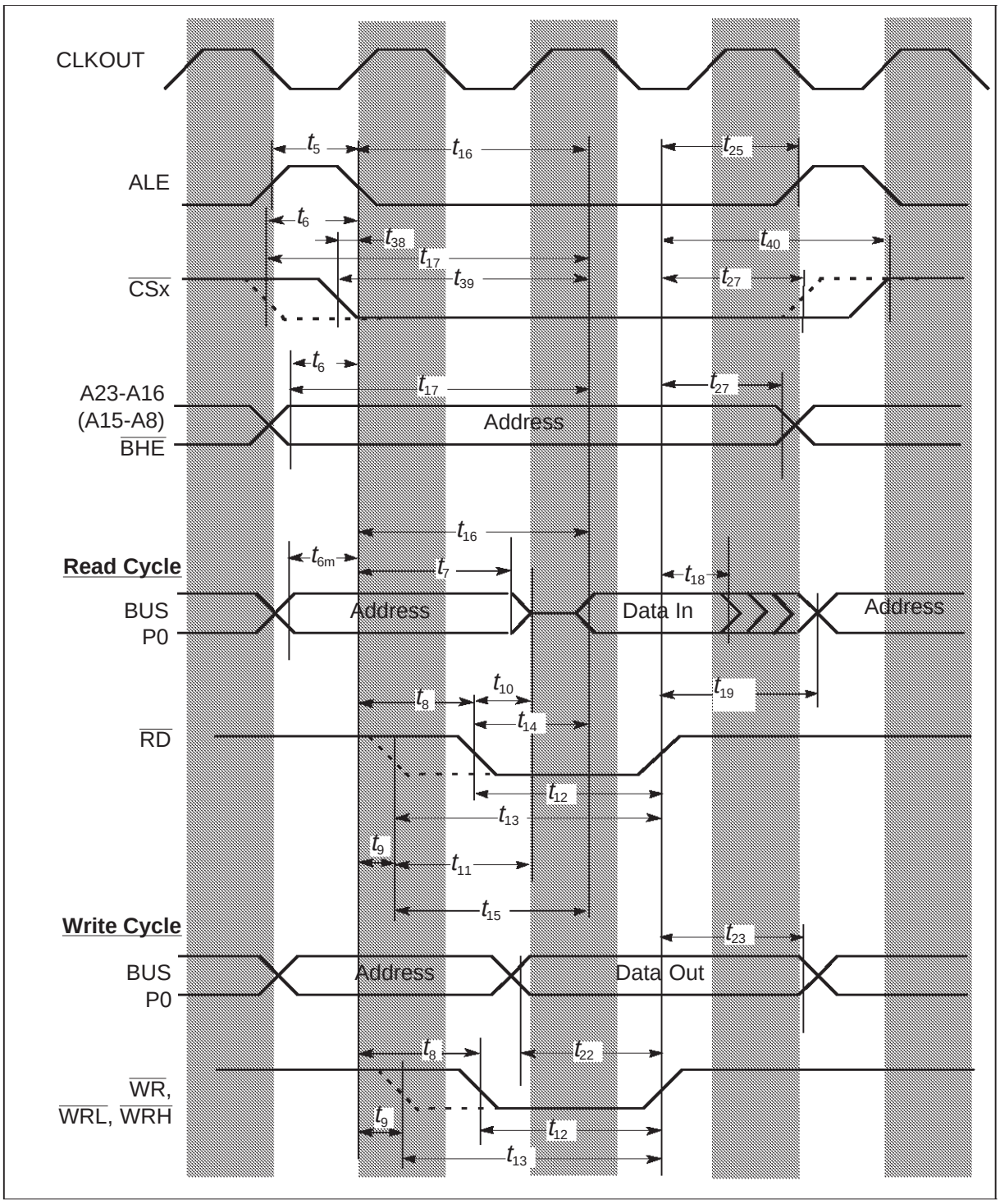


Figure 14 External Memory Cycle:
multiplexed bus, with/without read/write delay, normal ALE

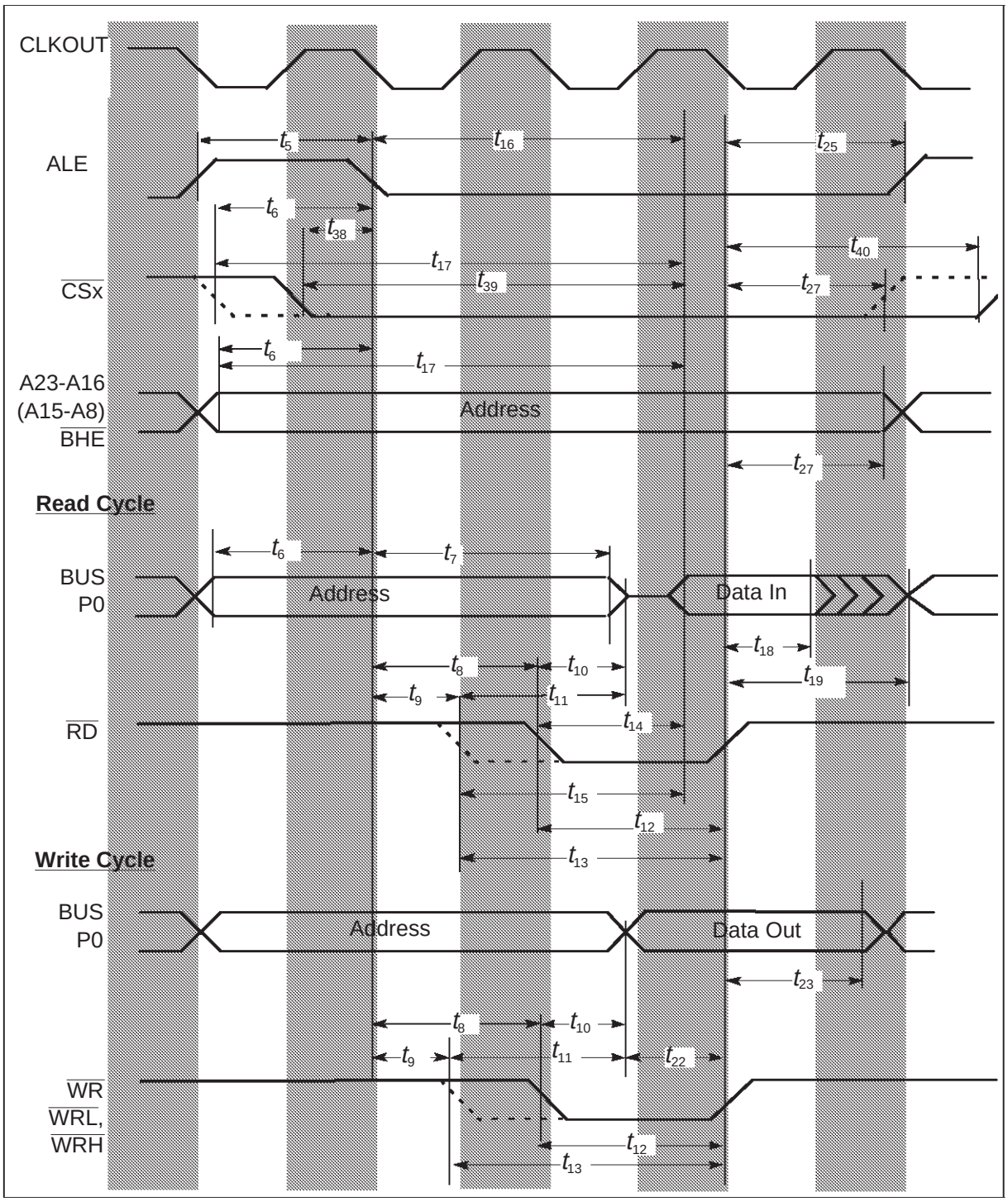


Figure 15 External Memory Cycle:
multiplexed bus, with/without read/write delay, extended ALE

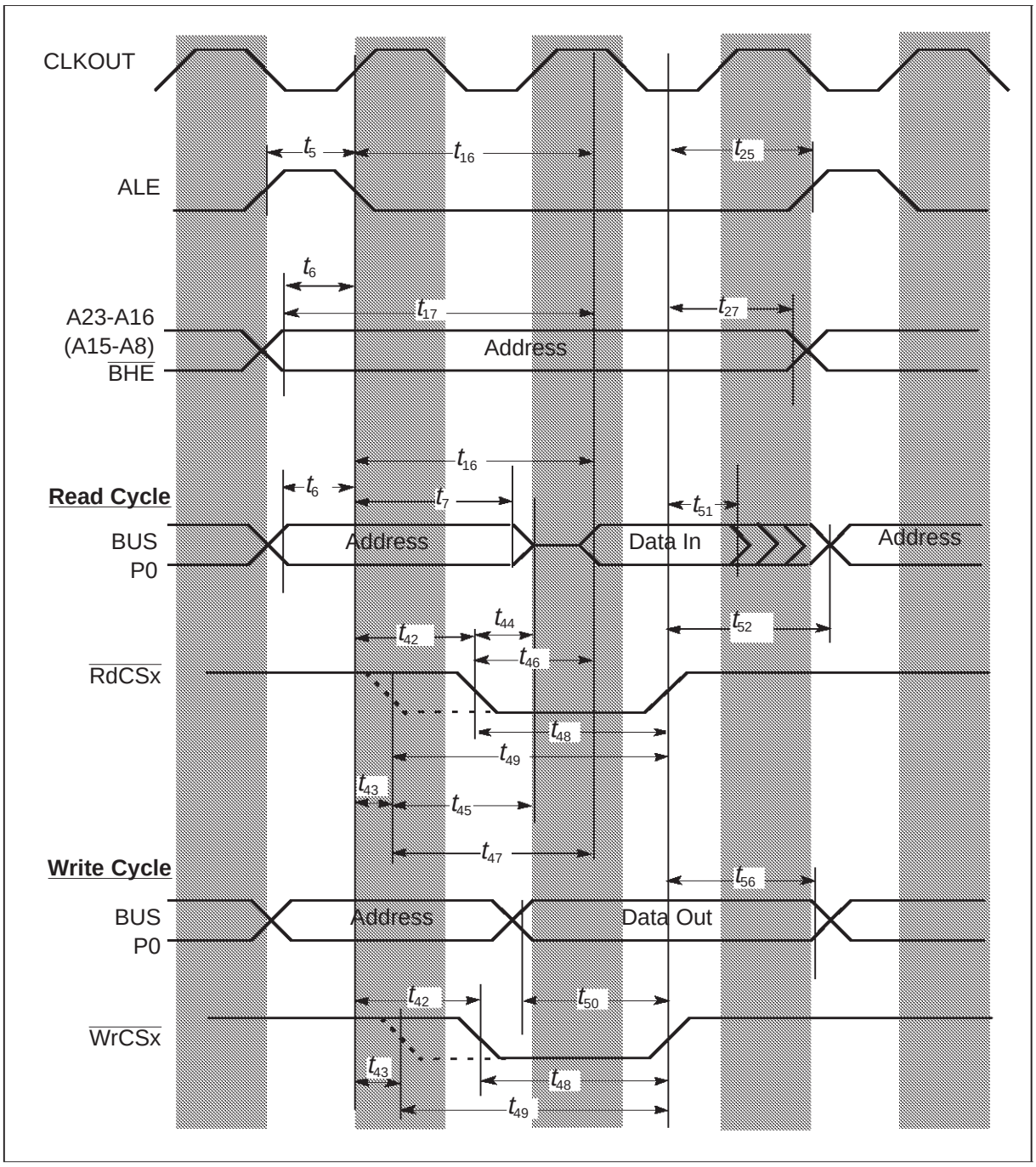


Figure 16 External Memory Cycle:
multiplexed bus, with/without read/write delay, normal ale, read/write chip select

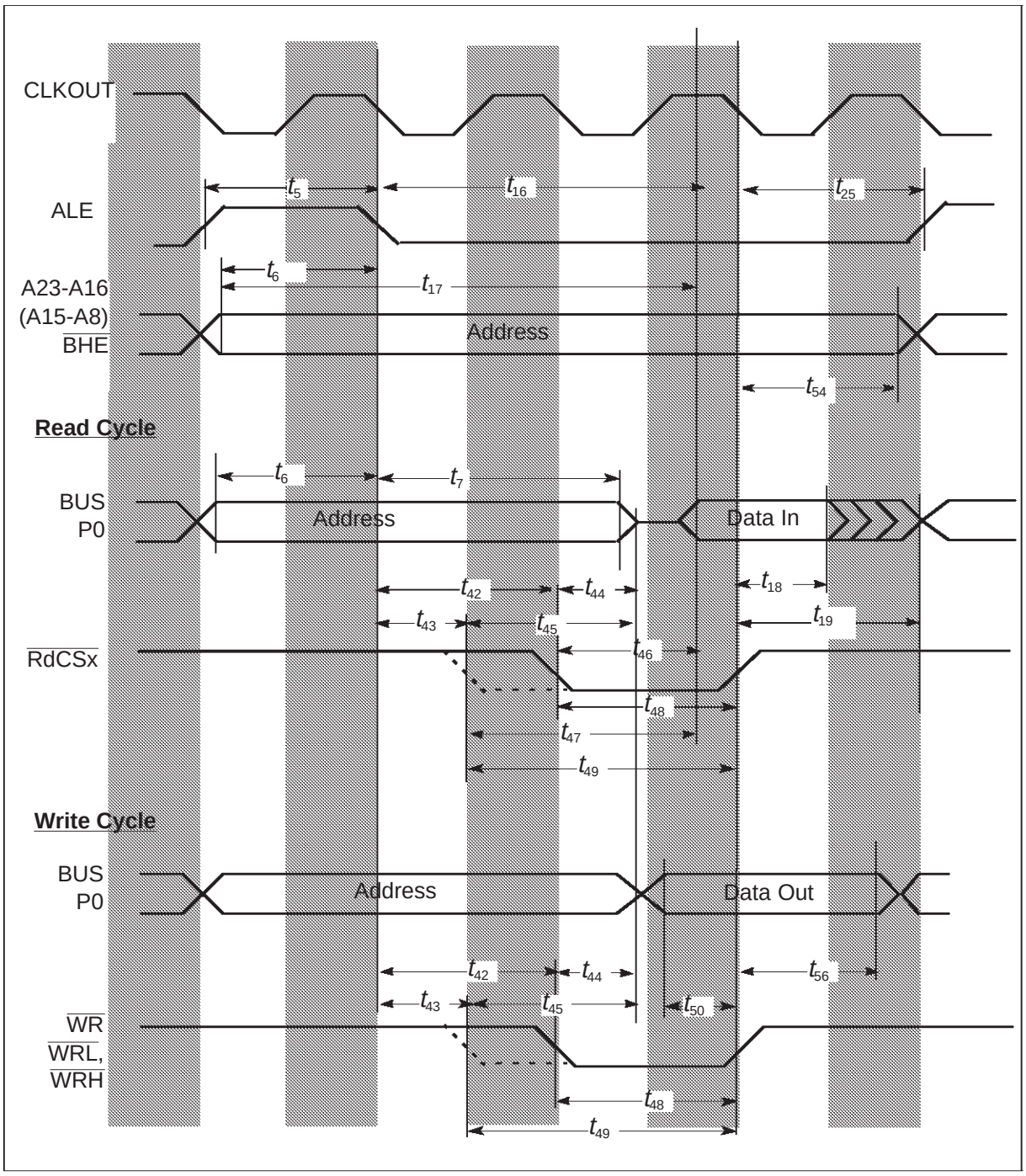


Figure 17 External Memory Cycle:
multiplexed bus, with/without read/write delay, extended ale, read/write chip select

16.4.11 Demultiplexed bus

V_{DD} = 5 V ± 10% V_{SS} = 0 V T_A = 0 to +70 °C C_L = 100 pF

ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	10 + t_A	–	TCL - 10+ t_A	–	ns
Address setup to ALE	t_6	CC	4 + t_A	–	TCL - 16+ t_A	–	ns
Address/Unlatched $\overline{CS}$ setup to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_{80}	CC	30 + $2t_A$	–	2TCL - 10 + $2t_A$	–	ns
Address/Unlatched $\overline{CS}$ setup to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_{81}	CC	10 + $2t_A$	–	TCL -10 + $2t_A$	–	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	20 + t_C	–	2TCL - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	40 + t_C	–	3TCL - 20 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address/Unlatched $\overline{CS}$ to valid data in	t_{17}	SR	–	50 + $2t_A$ + t_C	–	4TCL - 30 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge (with RW-delay[1])	t_{20}	SR	–	26 + t_F	–	2TCL - 14 + t_F + $2t_A$[1]	ns
Data float after $\overline{RD}$ rising edge (no RW-delay[1])	t_{21}	SR	–	10 + t_F	–	TCL - 10 + t_F + $2t_A$[1]	ns

Table 17 Demultiplexed bus characteristics

Parameter	Symbol		Max. CPU Clock = 25MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
			min.	max.	min.	max.	
Data valid to $\overline{WR}$	t_{22}	CC	20 + t_C	–	2TCL- 20 + t_C	–	ns
Data hold after $\overline{WR}$	t_{24}	CC	10 + t_F	–	TCL - 10+ t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{26}	CC	-10 + t_F	–	-10 + t_F	–	ns
Address/Unlatched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$ [2]	t_{28}	CC	0 + t_F	–	0 + t_F	–	ns
ALE falling edge to Latched $\overline{CS}$	t_{38}	CC	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns
Latched $\overline{CS}$ low to Valid Data In	t_{39}	SR	–	40 + t_C+ 2t_A	–	3TCL - 20 + t_C + 2t_A	ns
Latched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	t_{41}	CC	6 + t_F	–	TCL - 14 + t_F	–	ns
Address setup to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	t_{82}	CC	26 + 2t_A	–	2TCL - 14 + 2t_A	–	ns
Address setup to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	t_{83}	CC	6 + 2t_A	–	TCL -14 + 2t_A	–	ns
$\overline{RdCS}$ to Valid Data In (with RW-delay)	t_{46}	SR	–	16 + t_C	–	2TCL - 24 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW-delay)	t_{47}	SR	–	36 + t_C	–	3TCL - 24 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW-delay)	t_{48}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW-delay)	t_{49}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50}	CC	26 + t_C	–	2TCL - 14 + t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{RdCS}$ (with RW-delay)	t_{53}	SR	–	20 + t_F	–	2TCL - 20 + t_F	ns

Table 17 Demultiplexed bus characteristics

Parameter	Symbol		Max. CPU Clock = 25MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
			min.	max.	min.	max.	
Data float after $\overline{RdCS}$ (no RW-delay)	t_{68}	SR	–	0 + t_F	–	TCL - 20 + t_F	ns
Address hold after $\overline{RdCS}$, $\overline{WrCS}$	t_{55}	CC	-10 + t_F	–	-10 + t_F	–	ns
Data hold after $\overline{WrCS}$	t_{57}	CC	6 + t_F	–	TCL - 14 + t_F	–	ns

Table 17 Demultiplexed bus characteristics

1. RW-delay and t_A refer to the following bus cycle.
2. Read data are latched with the same clock edge that triggers the address change and the rising $\overline{RD}$ edge. Therefore address changes before the end of $\overline{RD}$ have no impact on read cycles

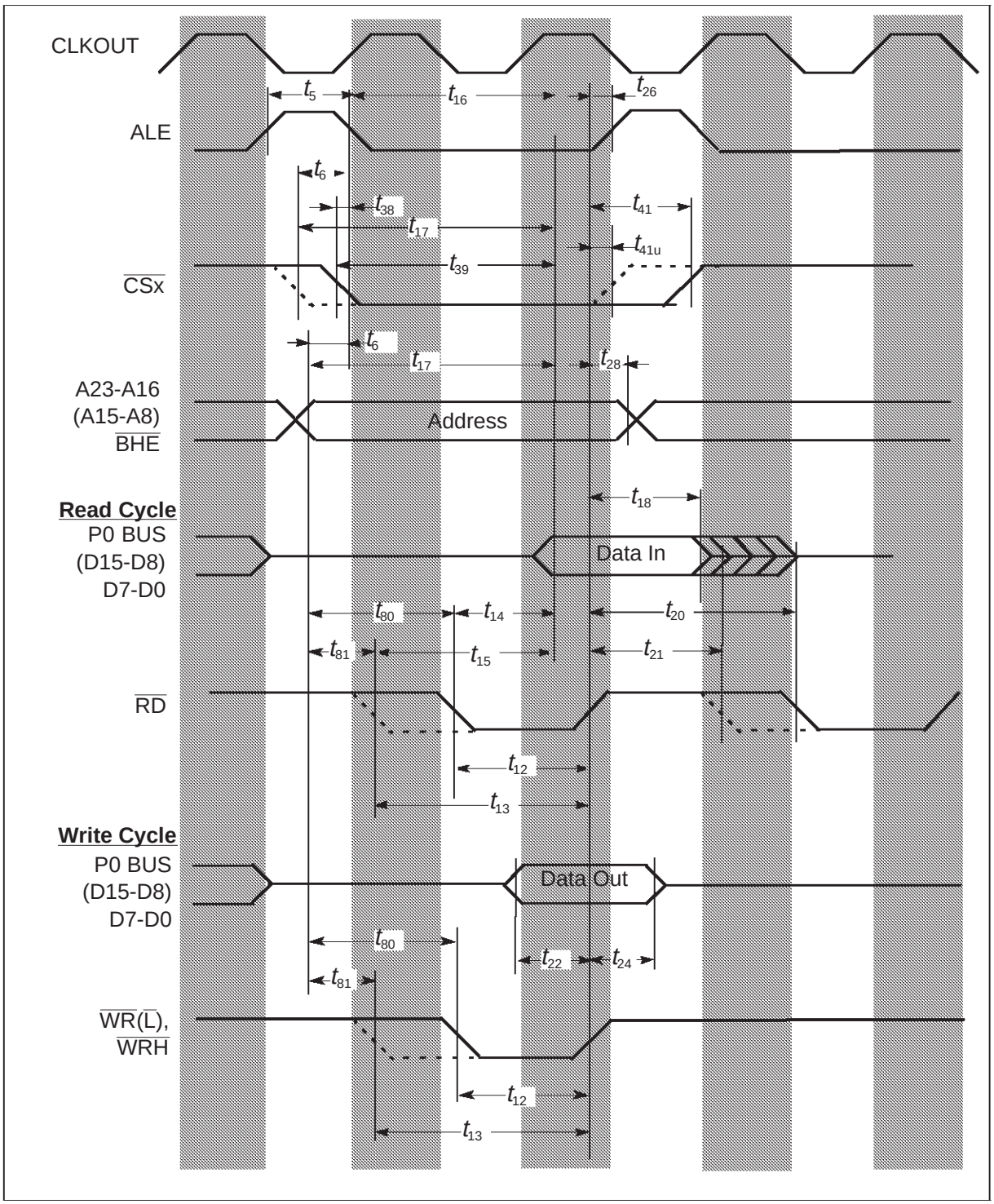


Figure 18 External Memory Cycle:
demultiplexed bus, with/without read/write delay, normal ALE

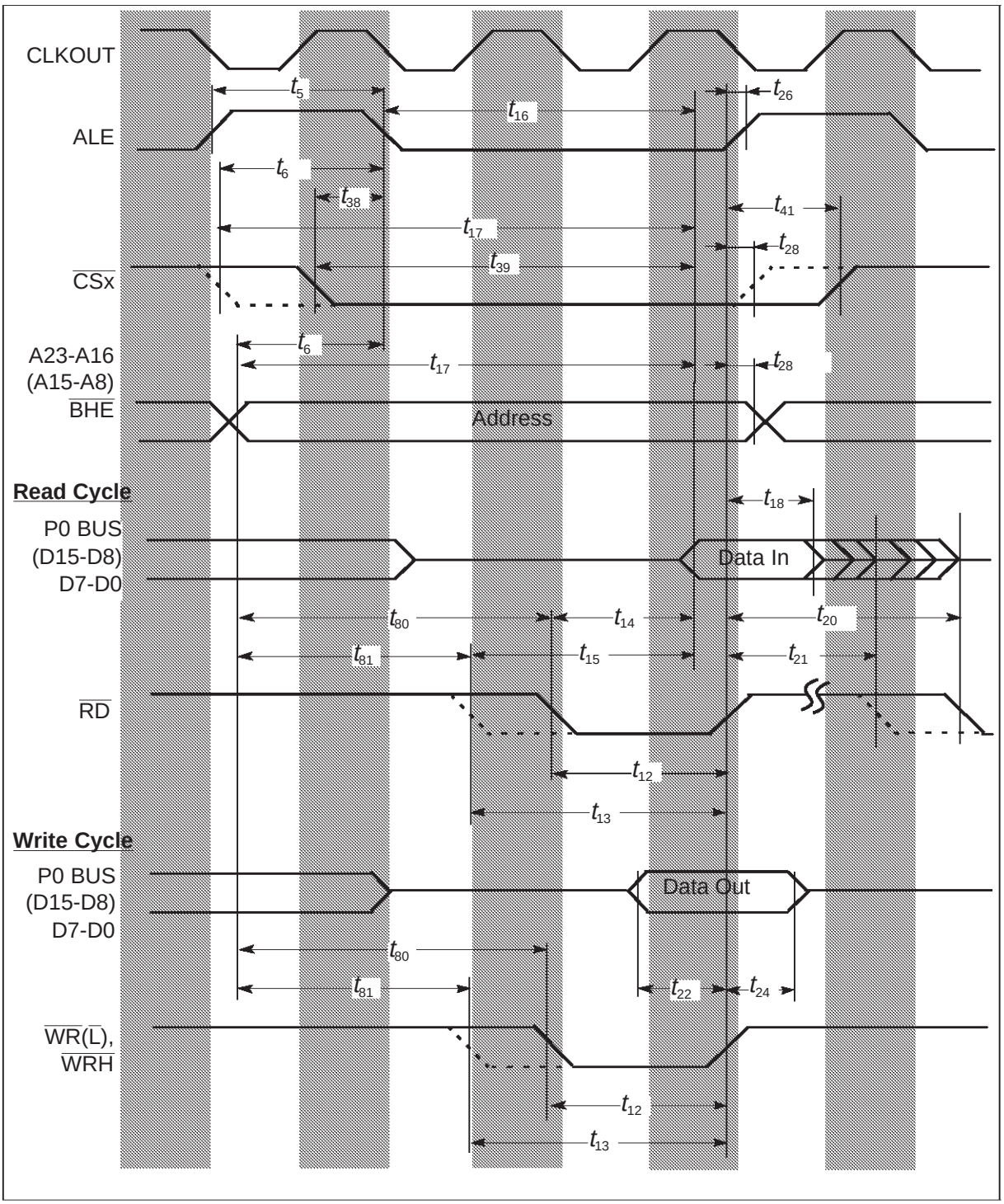


Figure 19 External Memory Cycle:
demultiplexed bus, with/without read/write delay, extended ALE

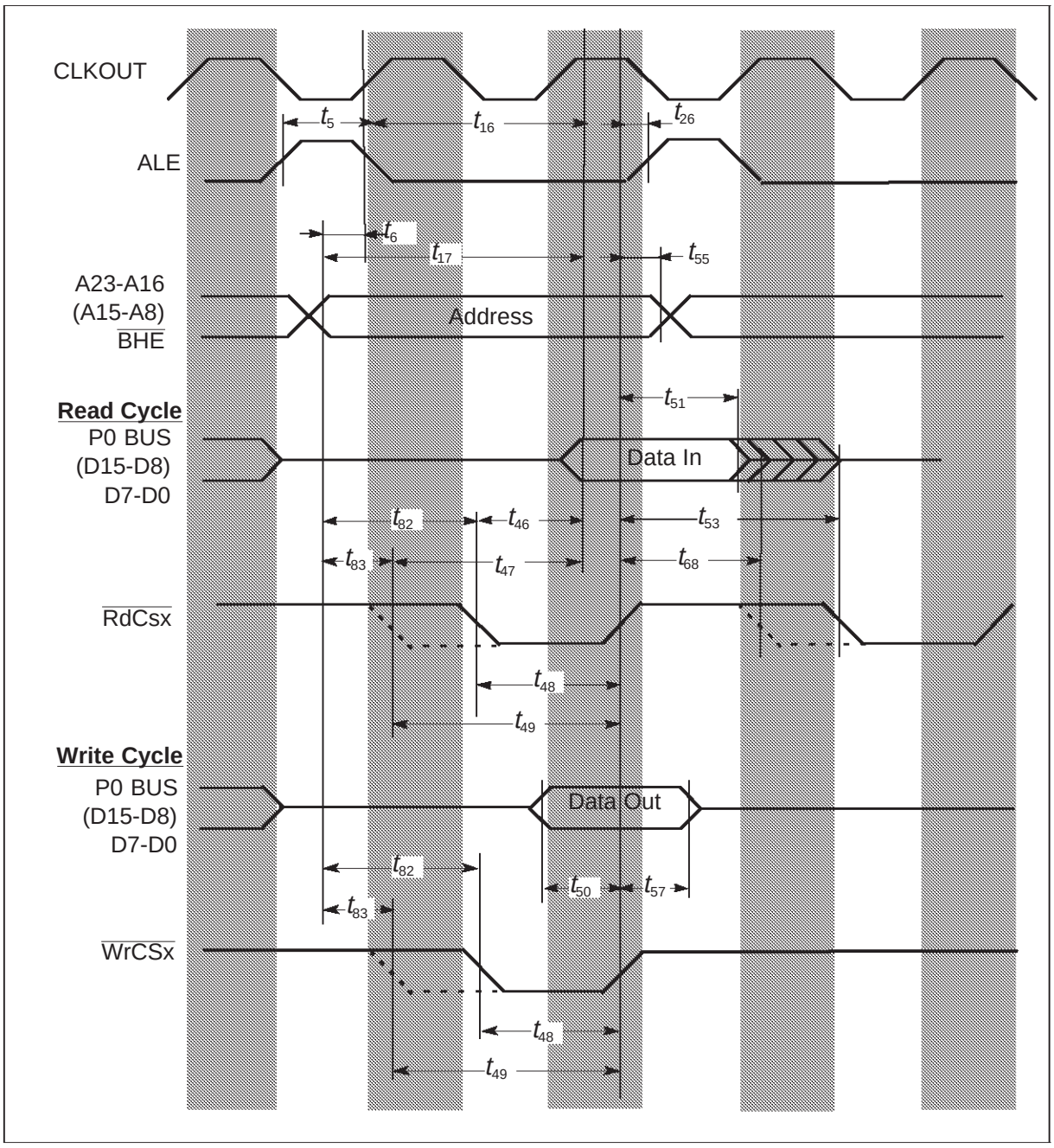


Figure 20 External Memory Cycle:
demultiplexed bus, with/without read/write delay, normal ale, read/write chip select

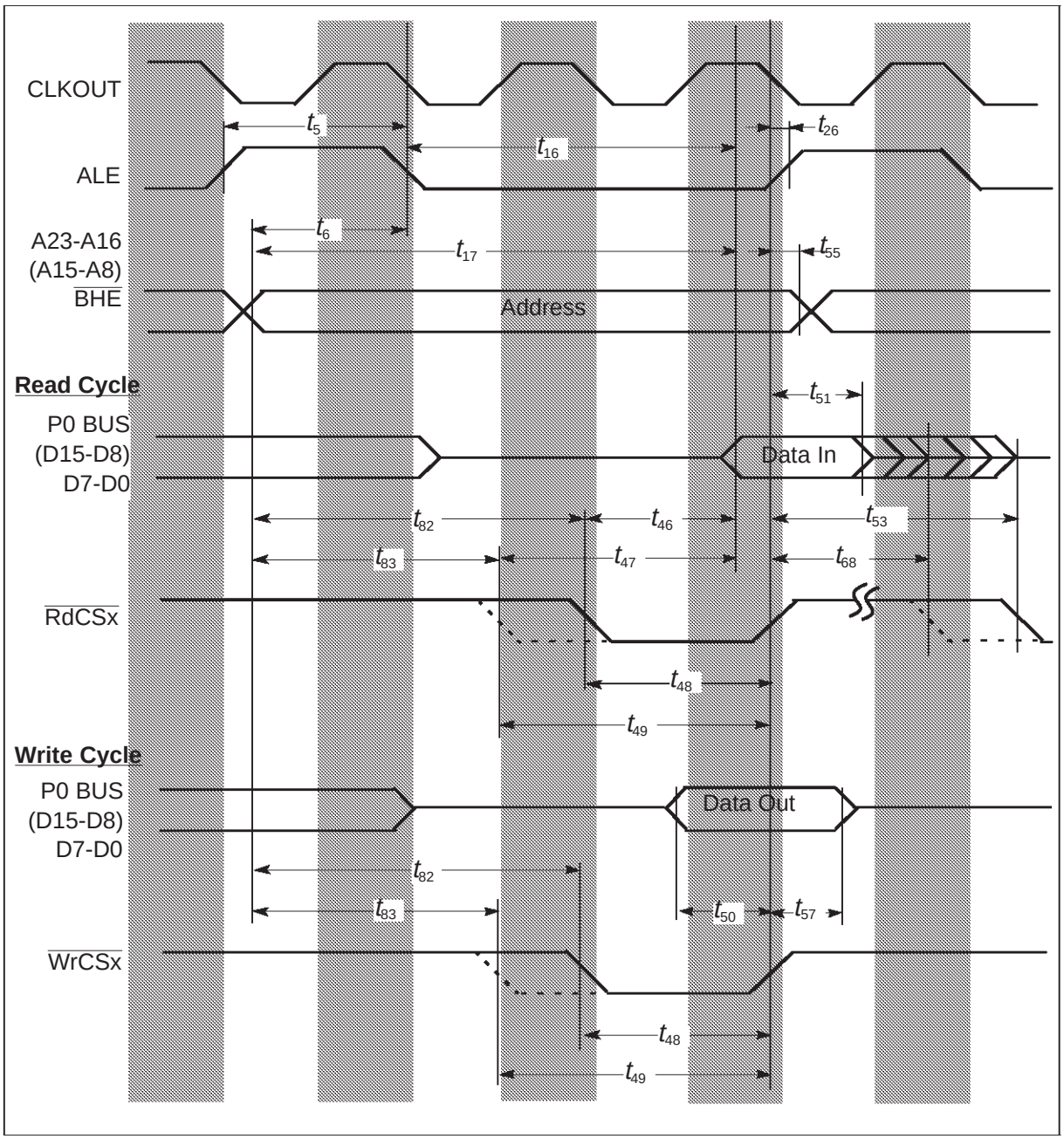


Figure 21 External Memory Cycle:
demultiplexed bus, no read/write delay, extended ale, read/write chip select

16.4.12 CLKOUT and $\overline{\text{READY}}$

V_{DD} = 5 V ± 10% V_{SS} = 0 V T_A = 0 to +70 °C C_L = 100 pF

Parameter	Symbol		Max. CPU Clock = 25MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
			min.	max.	min.	max.	
CLKOUT cycle time	t_{29}	CC	40	40	2TCL	2TCL	ns
CLKOUT high time	t_{30}	CC	14	–	TCL – 6	–	ns
CLKOUT low time	t_{31}	CC	10	–	TCL – 10	–	ns
CLKOUT rise time	t_{32}	CC	–	4	–	4	ns
CLKOUT fall time	t_{33}	CC	–	4	–	4	ns
CLKOUT rising edge to ALE falling edge	t_{34}	CC	0 + t_A	10 + t_A	0 + t_A	10 + t_A	ns
Synchronous $\overline{\text{READY}}$ setup time to CLKOUT	t_{35}	SR	14	–	14	–	ns
Synchronous $\overline{\text{READY}}$ hold time after CLKOUT	t_{36}	SR	4	–	4	–	ns
Asynchronous $\overline{\text{READY}}$ low time	t_{37}	SR	58	–	2TCL + 18	–	ns
Asynchronous $\overline{\text{READY}}$ setup time [1]	t_{58}	SR	14	–	14	–	ns
Asynchronous $\overline{\text{READY}}$ hold time [1]	t_{59}	SR	4	–	4	–	ns
Async. $\overline{\text{READY}}$ hold time after $\overline{\text{RD}}$, $\overline{\text{WR}}$ high (Demultiplexed Bus) [2]	t_{60}	SR	0	0 + $2t_A$ + t_C + t_F [2]	0	TCL - 20 + $2t_A$ + t_C + t_F [2]	ns

Table 18 CLKOUT and $\overline{\text{READY}}$ characteristics

1. These timings are given for test purposes only, in order to assure recognition at a specific clock edge.
2. Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating READY.
   The $2t_A$ and t_C refer to the next following bus cycle, t_F refers to the current bus cycle

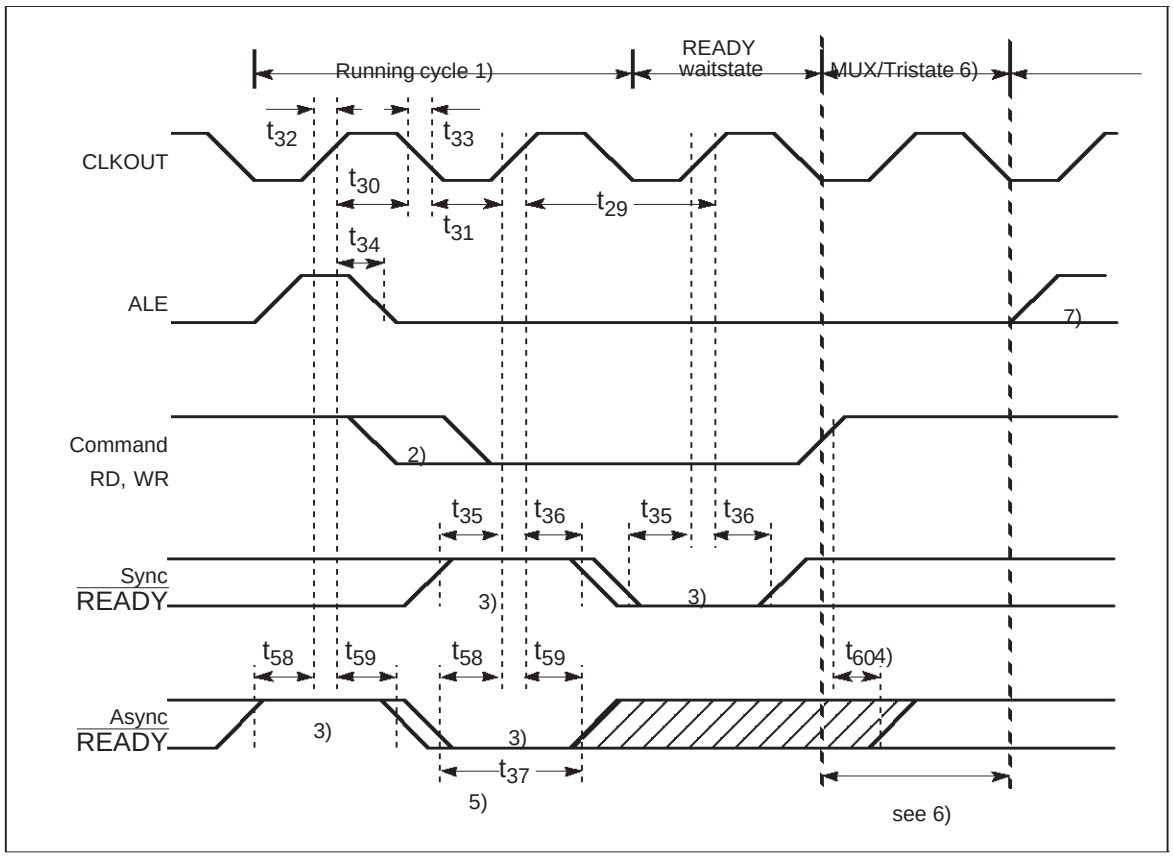


Figure 22 CLKOUT and $\overline{\text{READY}}$

1 Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).

2 The leading edge of the respective command depends on RW-delay.

3 $\overline{\text{READY}}$ sampled HIGH at this sampling point generates a READY controlled waitstate, $\overline{\text{READY}}$ sampled LOW at this sampling point terminates the currently running bus cycle.

4 $\overline{\text{READY}}$ may be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).

5 If the Asynchronous $\overline{\text{READY}}$ signal does not fulfill the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfill t_{37} in order to be safely synchronized. This is guaranteed, if READY is removed in response to the command (see Note 4)).

6 Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here.
For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC waitstate this delay is zero.

7 The next external bus cycle may start here.

16.4.13 External bus arbitration

V_{DD} = 5 V ± 10% V_{SS} = 0 V T_A = 0 to +70 °C

C_L (for PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100 pF

C_L (for Port 6, $\overline{CS}$) = 100 pF

Parameter	Symbol		Max. CPU Clock = 25MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
			min.	max.	min.	max.	
$\overline{HOLD}$ input setup time to CLKOUT	t_{61}	SR	20	–	20	–	ns
CLKOUT to $\overline{HLDA}$ high or $\overline{BREQ}$ low delay	t_{62}	CC	–	20	–	20	ns
CLKOUT to $\overline{HLDA}$ low or $\overline{BREQ}$ high delay	t_{63}	CC	–	20	–	20	ns
$\overline{CSx}$ release	t_{64}	CC	–	20	–	20	ns
$\overline{CSx}$ drive	t_{65}	CC	-4	24	-4	24	ns
Other signals release	t_{66}	CC	–	20	–	20	ns
Other signals drive	t_{67}	CC	-4	24	-4	24	ns

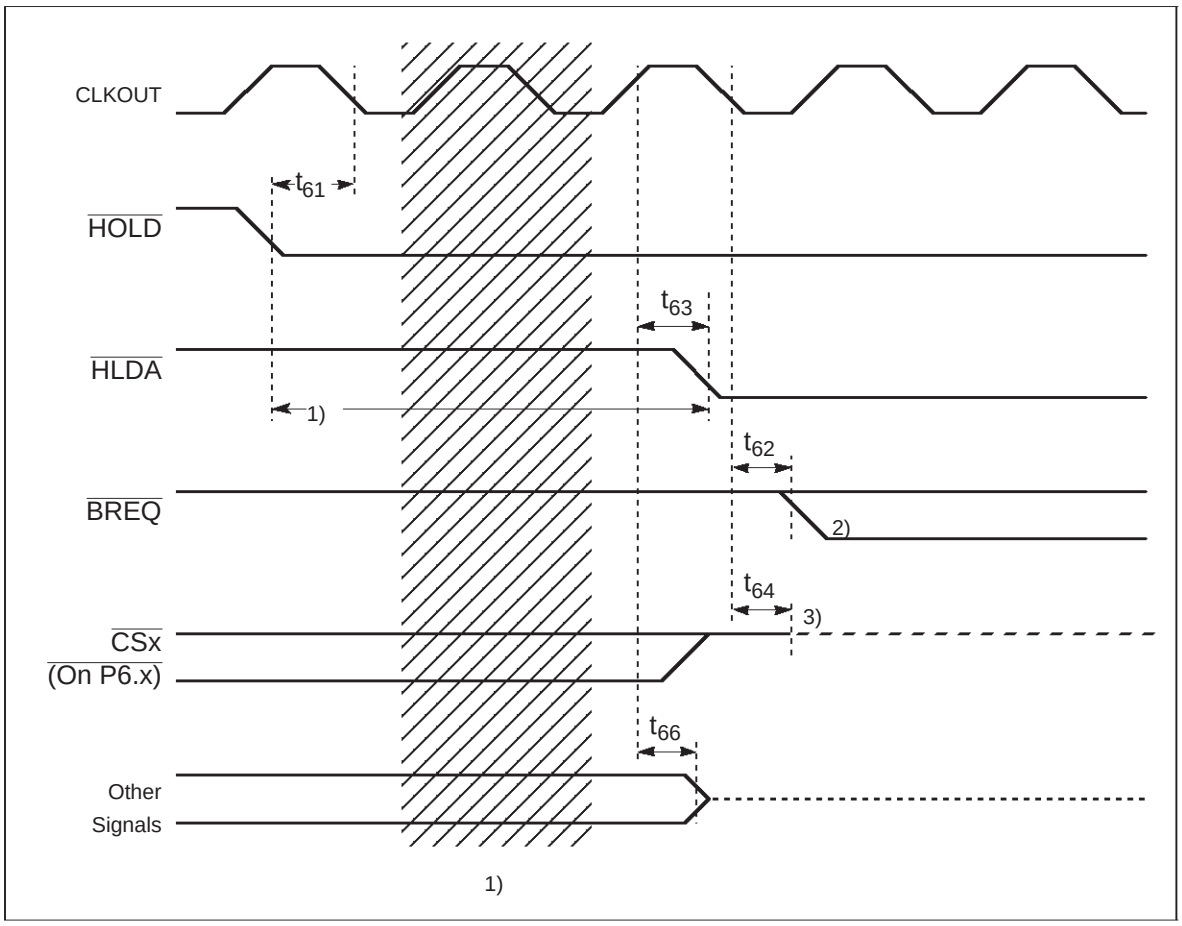


Figure 23 External bus arbitration, releasing the bus

1 The ST10F163 will complete the currently running bus cycle before granting bus access.

2 This is the first possibility for $\overline{BREQ}$ to get active.

3 The $\overline{CS}$ outputs will be resistive high (pullup) after t_{64}.

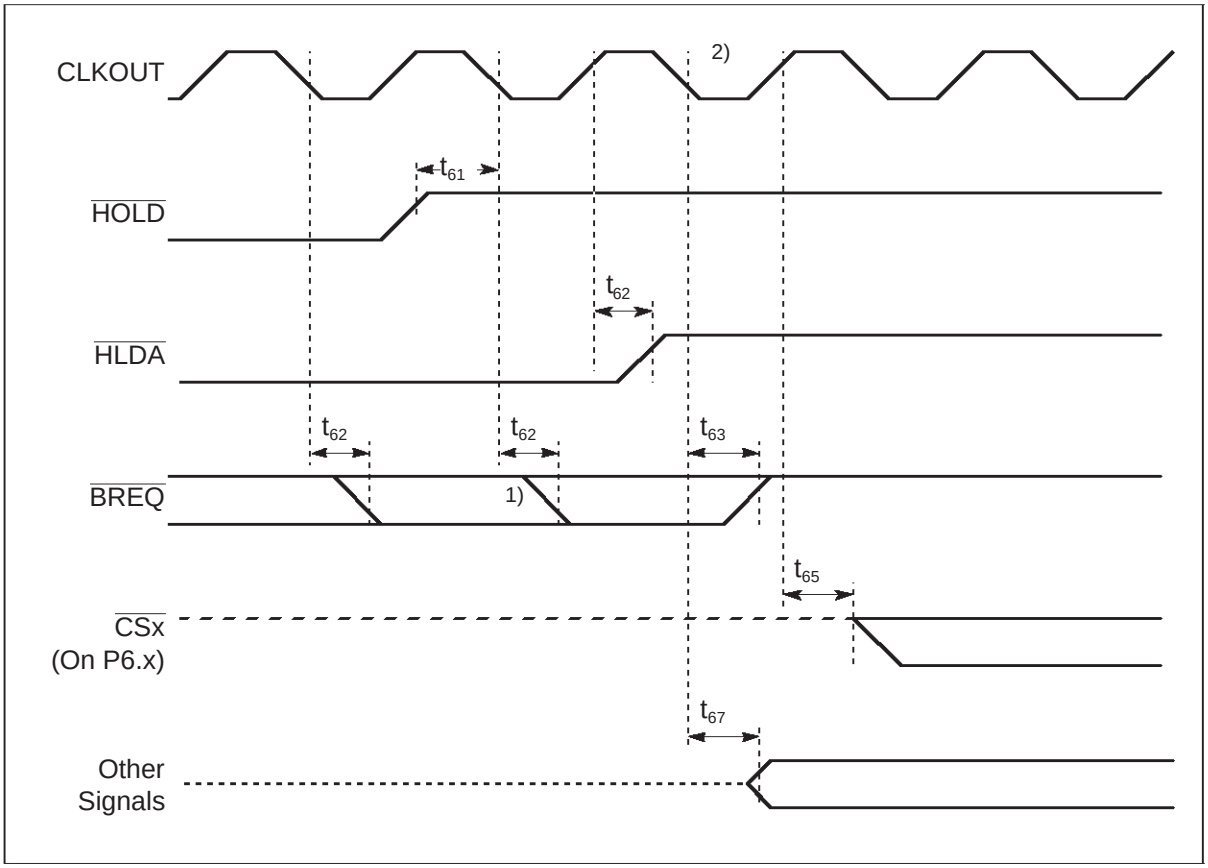


Figure 24 External bus arbitration, (regaining the bus)

1 This is the last chance for $\overline{\text{BREQ}}$ to trigger the indicated regain-sequence. Even if $\overline{\text{BREQ}}$ is activated earlier, the regain-sequence is initiated by $\overline{\text{HOLD}}$ going high. Please note that $\overline{\text{HOLD}}$ may also be deactivated without the ST10F163 requesting the bus.

2 The next ST10F163 driven bus cycle may start here.

16.4.14 Synchronous serial port timing

V_{CC} = 5 V ± 10% V_{SS} = 0 V T_A = 0 to +70 °C C_L = 100 pF

Parameter	Symbol		Max. Baudrate = 12.5 / 10 MBd		Variable Baudrate = 0.5 to 12.5 MBd		Unit
			min.	max.	min.	max.	
SSP clock cycle time	t_{200}	CC	80 / 100	80 /100	4 TCL	512 TCL	ns
SSP clock high time	t_{201}	CC	30 / 40	– / –	t_{200}/2 - 10	–	ns
SSP clock low time	t_{202}	CC	30 / 40	– / –	t_{200}/2 - 10	–	ns
SSP clock rise time	t_{203}	CC	– / –	6 / 6	–	6	ns
SSP clock fall time	t_{204}	CC	– / –	6 / 6	–	6	ns
CE active before shift edge	t_{205}	CC	30 / 40	– / –	t_{200}/2 - 10	–	ns
CE inactive after latch edge	t_{206}	CC	70 / 90	90 / 110	t_{200} - 10	t_{200} + 10	ns
Write data valid after shift edge	t_{207}	CC	– / –	10 / 10	–	10	ns
Write data hold after shift edge	t_{208}	CC	0 / 0	– / –	0	–	ns
Write data hold after latch edge	t_{209}	CC	34 / 44	46 / 56	t_{200}/2 - 6	t_{200}/2 + 6	ns
Read data active after latch edge	t_{210}	SR	50 / 60	– / –	t_{200}/2 + 10	–	ns
Read data setup time before latch edge	t_{211}	SR	20 / 20	– / –	20	–	ns
Read data hold time after latch edge	t_{212}	SR	0 / 0	– / –	0	–	ns

Table 19 Synchronous serial port timing characteristics

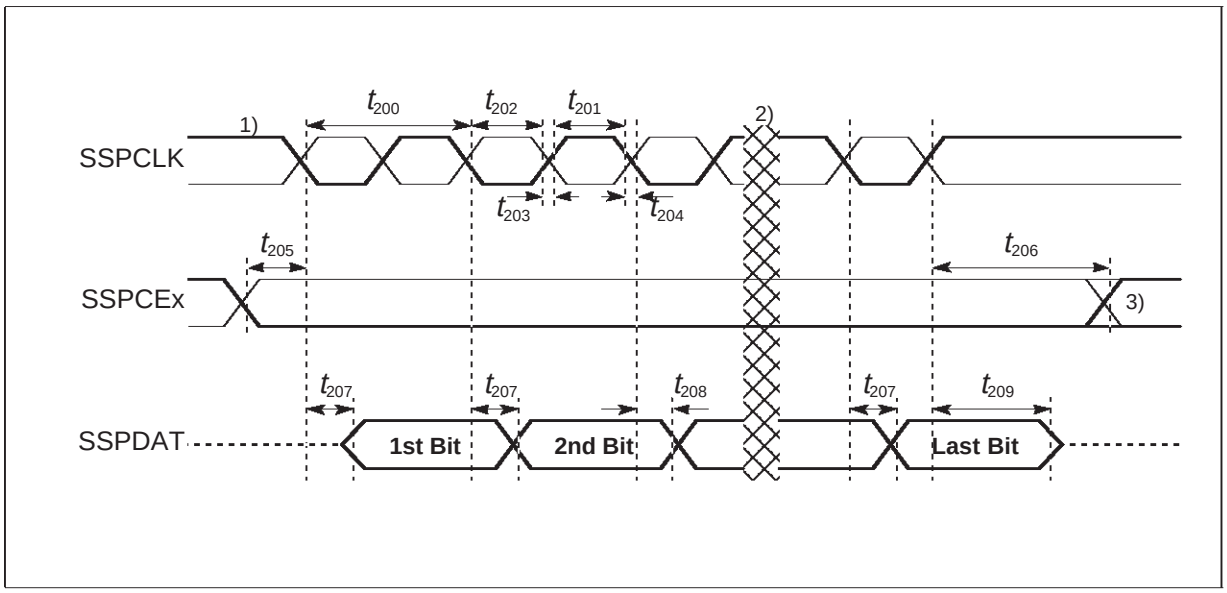


Figure 25 SSP write timing

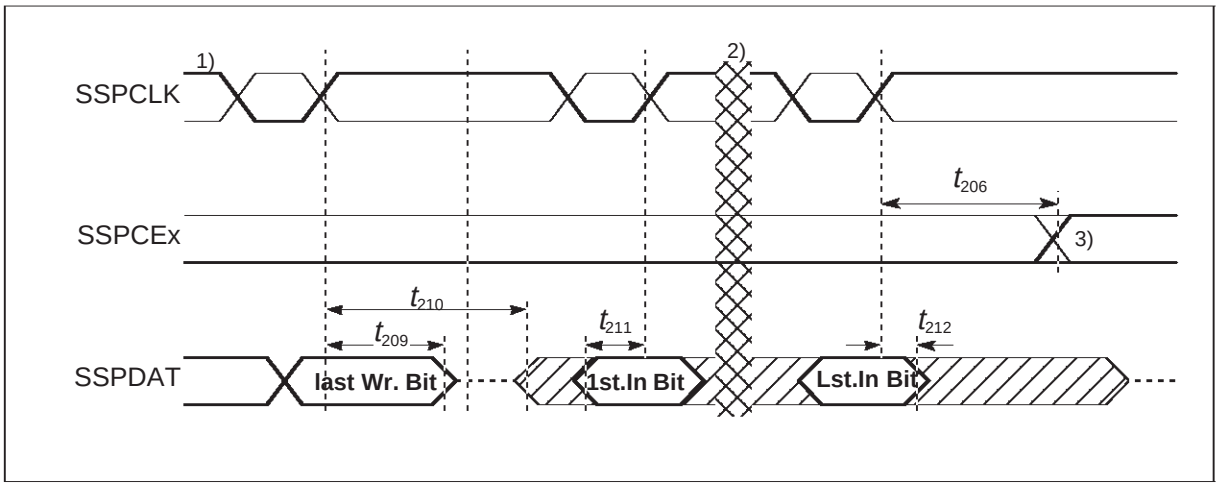


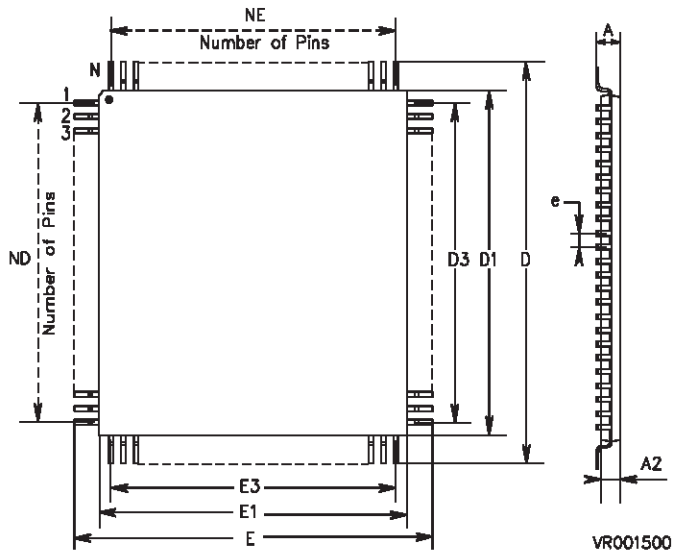
Figure 26 SSP read timing

1 The transition of shift and latch edge of SSPCLK is programmable. This figure uses the falling edge as shift edge (drawn bold).

2 The bit timing is repeated for all bits to be transmitted or received.

3 The active level of the chip enable lines is programmable. This figure uses an active low CE (drawn bold).
At the end of a transmission or reception the CE signal is disabled in single transfer mode. In continuous transfer mode it remains active.

17 Package Mechanical Data



Dim	mm			inches		
	Min	Type	Max	Min	Type	Max
A			1.60			0.063
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	15.75	16.00	16.25	0.620	0.630	0.640
D1	13.90	14.00	14.10	0.547	0.551	0.555
D3		12.00			0.472	
E	15.75	16.00	16.25	0.620	0.630	0.640
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.00			0.472	
e		0.50			0.020	
Number of Pins						
ND	25					
NE	25					
N	100					

Figure 27 Package outline TQFP100 (14 x 14 mm)

18 Ordering Information

Salestype	Temperature range	Package
ST10F163BT1	0°C to 70°C	TQFP100 (14x 14)

19 Revision History

The following changes have been made from ST10F163 Data Sheet revision 5 to create this revision 6:

Table added	Table 8 on page 26
Table added	Table 9 on page 27
Table added	Table 10 on page 30
Table added	Table 11 on page 31
Table added	Table 12 on page 32
Table added	Table 3 on page 13
Table added	Table 4 on page 14
Table added	Table 5 on page 15
Presentation changed	Figure 14 to Figure 21
Specification changed	t_{22} from 2TCL-16+t_c to 2TCL-20+t_c
Specification changed	t_8 - t_9 replaced with t_{80} - t_{81} for demultiplexed bus
Specification changed	t_{42} - t_{43} replaced with t_{82} - t_{83} for demultiplexed bus
Specification changed	t_{35} from 10ns to 14ns
Specification changed	t_{36} and t_{59} from 0ns to 4ns
Specification changed	t_{37} from ”min 54ns, Var min 2TCL+14ns” to ”min 58ns, Var min 2TCL+18ns”