

FEATURES

- Provides Reference Clock And Synthesized Clock
- 5 to 32 MHz Input Reference Frequency
- Pin-to-Pin Compatible to Avasem AV9107
- Programmable Analog Phase Locked Loop
- Low Power Single 5V CMOS Technology
- Up to 16 Frequencies Stored Internally
- 8/14 pin DIP or SOIC Package

GENERAL DESCRIPTION

The ST49C107A-04 is a mask programmable monolithic analog CMOS device designed to generate two simultaneous clocks. The output frequency can vary from 2 to 130MHz, with up to 16 single selectable preprogrammed frequencies stored in internal ROM.

The ST49C107A-04 is designed to replace existing CPU mother board clocks generated from individual oscillators

in order to reduce board space and number of oscillators. To provide high speed and low jitter clock, the parts utilize a high speed analog CMOS phase locked loop using 14.318 MHz system clock as the reference clock (note that reference clock can be changed to generate optional frequencies from a standard programmed device). The programmed clock outputs are selectable via four address lines.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
ST49C107ACP14-04	14 Lead 300 Mil PDIP	0°C to 70°C
ST49C107ACF14-04	14 Lead 150 Mil JEDEC SOIC	0°C to 70°C

BLOCK DIAGRAM

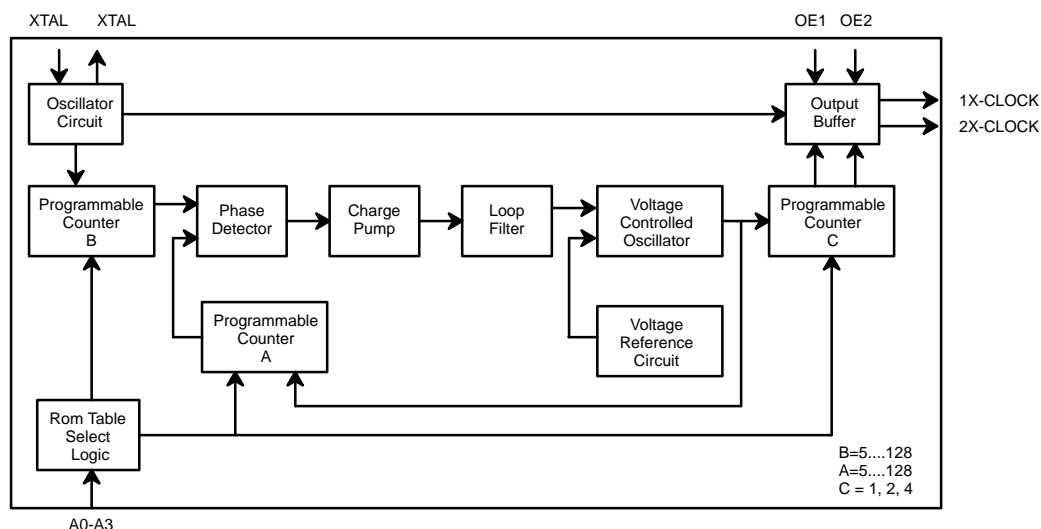
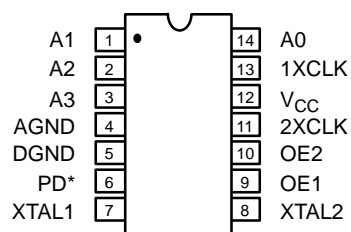
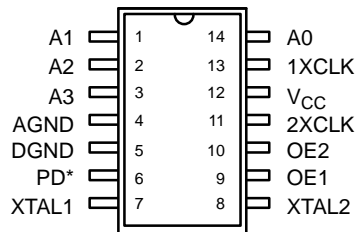


Figure 1. Block Diagram

PIN CONFIGURATION



14 Lead PDIP (0.300")



14 Lead SOIC (Jedec, 0.150")

PIN DESCRIPTION

Symbol	Pin #	Type	Description
A1	1 ¹	I	Frequency select address input 2.
A2	2 ¹	I	Frequency select address input 3.
A3	3 ¹	I	Frequency select address input 4.
AGND	4	O	Analog ground.
DGND	5	O	Digital ground.
PD	6 ¹	I	Power-down (Active low). Shuts off chip when low.
XTAL1	7	I	Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	8	O	Crystal output.
OE1	9 ¹	I	1X-CLOCK output enable (active high). 1X-CLOCK output is three stated when this pin is low.
OE2	10 ¹	I	2X-CLOCK output enable (active high). 2X-CLOCK output is three stated when this pin is low.
2XCLK	11	O	Programmed output clock.
V _{CC}	12	I	Positive supply voltage. Single +5 volts.
1XCLK	13	O	2X-CLOCK divide-by-two output.
A0	14 ¹	I	Frequency select address input 1.

Notes

¹Have internal pull-up resistors on inputs.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$ Unless Otherwise Specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	$I_{OL} = 8.0\text{ mA}$
V_{OH}	Output high level	2.4			V	$I_{OH} = 8.0\text{ mA}$
I_{IL}	Input low current			-10	μA	Exc. crystal input
I_{IH}	Input high current			1	μA	$V_{IN}=V_{CC}$
I_{CC}	Operating current		45	55	mA	No load. CLOCK=100MHz
I_{SB}	Standby current		25		μA	No load
R_{IN}	Input pull-up resistance	500	900	1300	k Ω	

DC ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$ Unless Otherwise Specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T_1	1X, 2X-CLOCK rise time		1	2	ns	$CL=20\text{pF}$ 0.8V - 2.0V
T_2	1X, 2X-CLOCK fall time		1	2	ns	$CL=20\text{pF}$ 2.0V - 0.8V
T_4	Duty cycle	40	48/52	60	%	1.4V switch point
T_5	Duty cycle	45	48/52	55	%	$V_{CC}/2$ switch point
T_3	Jitter 1 sigma		± 0.5	± 2	%	
T_3	Jitter absolute		± 3	± 5	%	
T	Input frequency	2		32	MHz	
T_7	Buffered clock rise time			20	ns	
T_8	Buffered clock fall time			20	ns	

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Supply Range 7 Volts
Voltage at Any Pin GND-0.3V to $V_{CC} + 0.3\text{V}$

Operating Temperature 0°C to $+70^{\circ}\text{C}$
Storage Temperature -40°C to $+150^{\circ}\text{C}$
Package Dissipation 500 mW

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup, it is recommended to connect 0.047 (F capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C107A-04 contains an analog phase locked loop circuit with digital closed loop dividers and a final output multiplexer to achieve the desired dividing ratios for the clock output.

The accuracy of the frequencies produced by the ST49C107A-04 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

$$\text{CLKOUT} = \text{CLKIN} * \text{Factor}$$

For proper output frequency, the ST49C107A-04 can accept a reference frequency from 5 - 32 MHz with max output frequency of 130 MHz (2X – clock).

CLOCK OUTPUT TABLE FOR ST49C107A-04 (using 14.318 MHz input. All frequencies in MHz).

A3	A2	A1	A0	Factor	2X-CLOCK	CLOCK
0	0	0	0	95/17	80.02	40.01
0	0	0	1	107/23	66.62	33.31
0	0	1	0	35/10	50.11	25.06
0	0	1	1	95/34	40.01	20.00
0	1	0	0	56/8	100.23	50.11
0	1	0	1	107/46	33.31	16.66
0	1	1	0	38/17	32.01	16.00
0	1	1	1	35/20	25.06	12.47
1	0	0	0	76/17	64.02	32.01
1	0	0	1	2	2X-Input	1X-Input
1	0	1	0	3	3X-Input	1.5X-Input
1	0	1	1	8	8X-Input	4X-Input
1	1	0	0	1/2	0.5X-Input	0.25X-Input
1	1	0	1	1/4	0.25X-Input	0.125X-Input
1	1	1	0	109/13	120.00	60.00
1	1	1	1	118/13	129.96	64.98

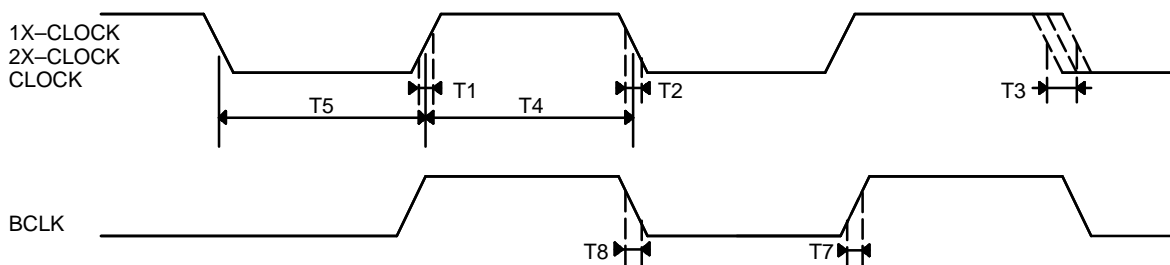
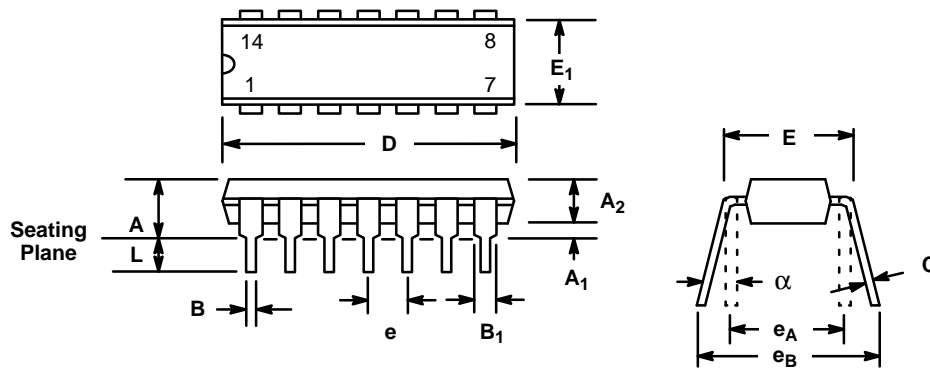


Figure 2. Timing Diagram

**14 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)**

Rev. 1.00

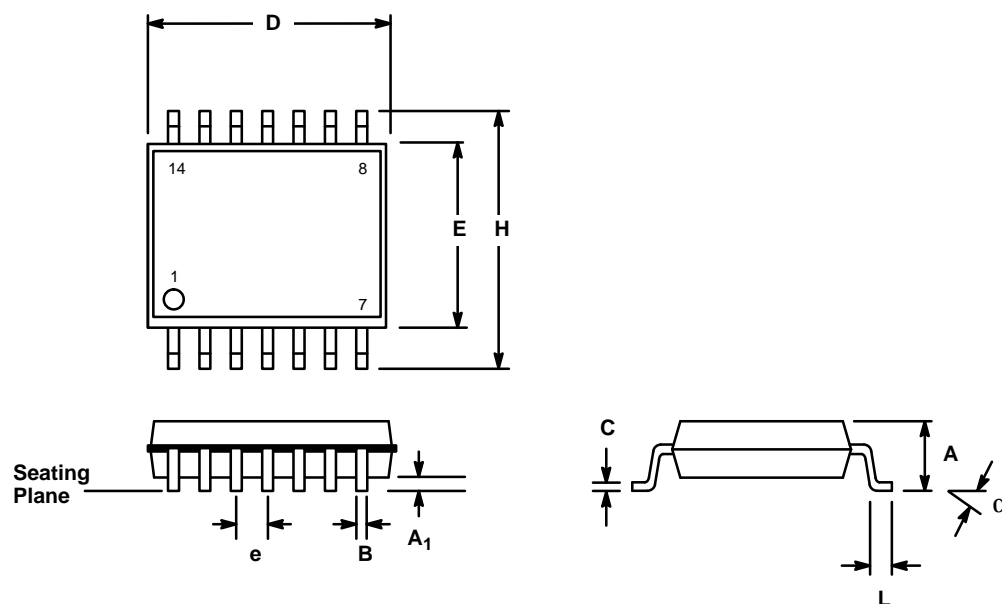


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A ₁	0.015	0.070	0.38	1.78
A ₂	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B ₁	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.725	0.795	18.42	20.19
E	0.300	0.325	7.62	8.26
E ₁	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e _A	0.300 BSC		7.62 BSC	
e _B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

14 LEAD SMALL OUTLINE (150 MIL JEDEC SOIC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A ₁	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.337	0.344	8.55	8.75
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

Notes

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Copyright 1996 EXAR Corporation

Datasheet September 1996

Reproduction, in part or whole, without the prior written consent of EXAR Corporation is prohibited.