

FEATURES

- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 25 μ A (Max.) @ $V_{DS} = 800V$
- Low $R_{DS(ON)}$: 3.800 Ω (Typ.)

$$BV_{DSS} = 800 V$$

$$R_{DS(on)} = 4.8 \Omega$$

$$I_D = 2.5 A$$

I-PAK



1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	800	V
I_D	Continuous Drain Current ($T_C=25^\circ C$)	2.5	A
	Continuous Drain Current ($T_C=100^\circ C$)	1.6	
I_{DM}	Drain Current-Pulsed ①	10	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy ②	233	mJ
I_{AR}	Avalanche Current ①	2.5	A
E_{AR}	Repetitive Avalanche Energy ①	5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.0	V/ns
P_D	Total Power Dissipation ($T_C=25^\circ C$)	50	W
	Linear Derating Factor	0.4	W/ $^\circ C$
T_J, T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	2.5	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient	--	110	

SSU3N80A

N-CHANNEL POWER MOSFET

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	800	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	1.01	--	V/ $^\circ\text{C}$	$I_D=250\mu A$ See Fig 7
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	3.5	V	$V_{DS}=5V, I_D=250\mu A$
I_{GSS}	Gate-Source Leakage, Forward	--	--	100	nA	$V_{GS}=30V$
	Gate-Source Leakage, Reverse	--	--	-100		$V_{GS}=-30V$
I_{DSS}	Drain-to-Source Leakage Current	--	--	25	μA	$V_{DS}=800V$
		--	--	250		$V_{DS}=640V, T_C=125^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	4.8	Ω	$V_{GS}=10V, I_D=0.85A$ ④*
g_{fs}	Forward Transconductance	--	2.0	--	$\bar{O}$	$V_{DS}=50V, I_D=0.85A$ ④
C_{iss}	Input Capacitance	--	580	750	pF	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$ See Fig 5
C_{oss}	Output Capacitance	--	60	75		
C_{rss}	Reverse Transfer Capacitance	--	23	30		
$t_{d(on)}$	Turn-On Delay Time	--	16	40	ns	$V_{DD}=400V, I_D=2A,$ $R_G=16\Omega$ See Fig 13 ④ ⑤
t_r	Rise Time	--	26	60		
$t_{d(off)}$	Turn-Off Delay Time	--	46	100		
t_f	Fall Time	--	24	60		
Q_g	Total Gate Charge	--	27	35	nC	$V_{DS}=640V, V_{GS}=10V,$ $I_D=2A$ See Fig 6 & Fig 12 ④ ⑤
Q_{gs}	Gate-Source Charge	--	5.3	--		
Q_{gd}	Gate-Drain("Miller") Charge	--	12.2	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	2.5	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	--	--	10		
V_{SD}	Diode Forward Voltage ④	--	--	1.4	V	$T_J=25^\circ\text{C}, I_S=2.5A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	--	330	--	ns	$T_J=25^\circ\text{C}, I_F=3A$
Q_{rr}	Reverse Recovery Charge	--	1.52	--	μC	$di_F/dt=100A/\mu s$ ④

Notes ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② $L=70\text{mH}, I_{AS}=2.5A, V_{DD}=50V, R_G=27\Omega$, Starting $T_J=25^\circ\text{C}$
- ③ $I_{SD}\leq 3A, di/dt\leq 100A/\mu s, V_{DD}\leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$
- ④ Pulse Test : Pulse Width = $250\mu s$, Duty Cycle $\leq 2\%$
- ⑤ Essentially Independent of Operating Temperature

N-CHANNEL POWER MOSFET

SSU3N80A

Fig 1. Output Characteristics

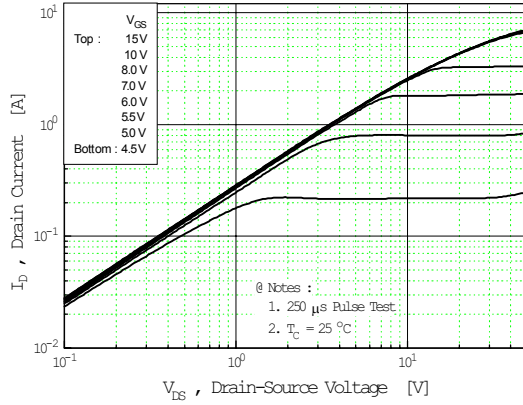


Fig 2. Transfer Characteristics

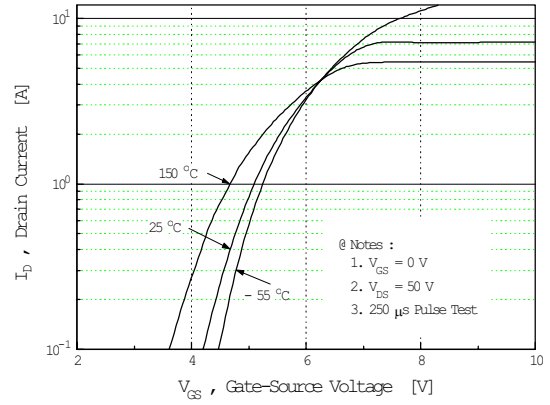


Fig 3. On-Resistance vs. Drain Current

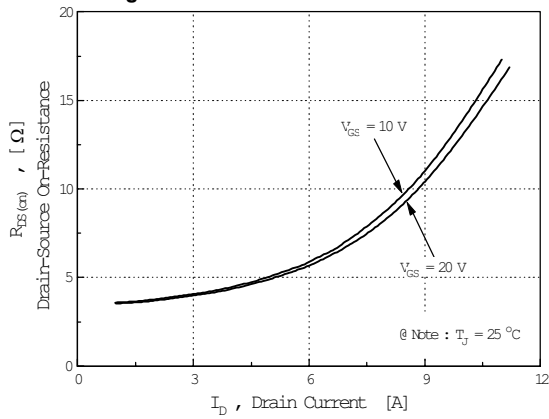


Fig 4. Source-Drain Diode Forward Voltage

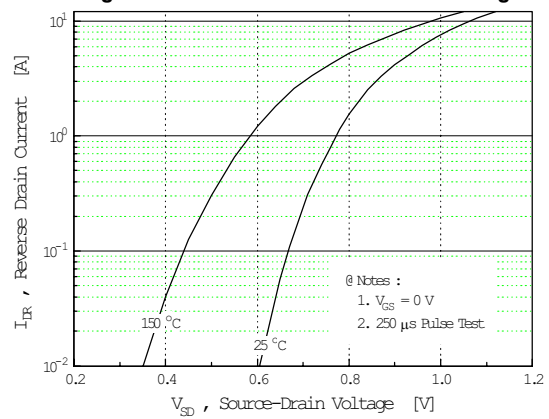


Fig 5. Capacitance vs. Drain-Source Voltage

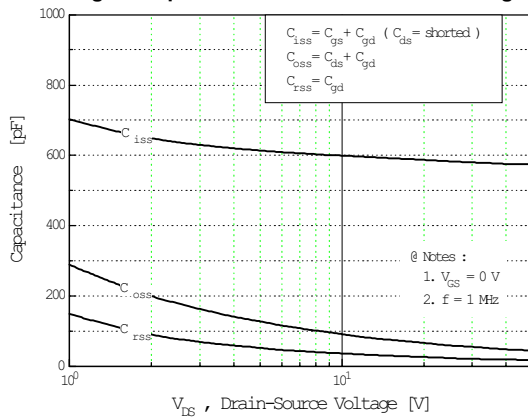
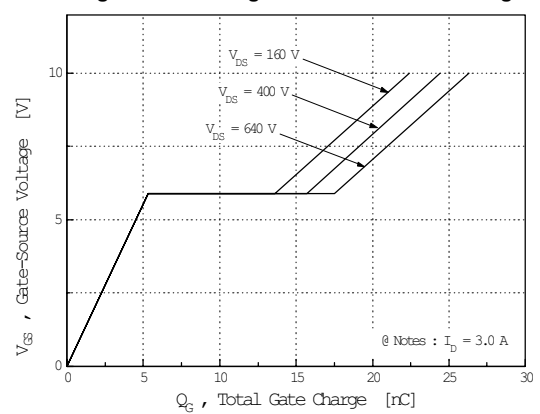


Fig 6. Gate Charge vs. Gate-Source Voltage



SSU3N80A

N-CHANNEL POWER MOSFET

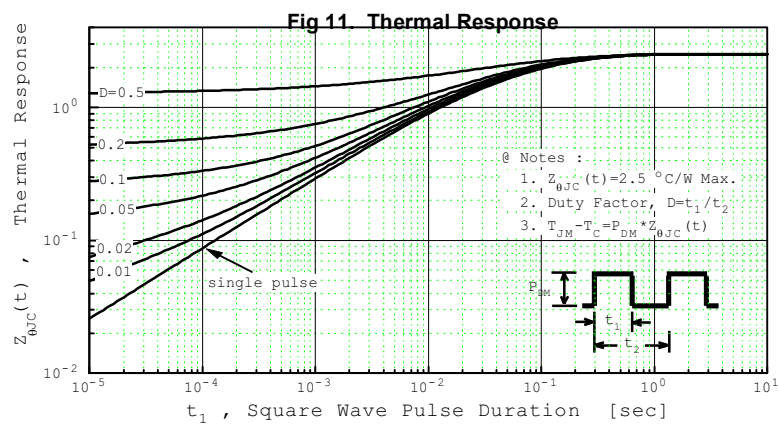
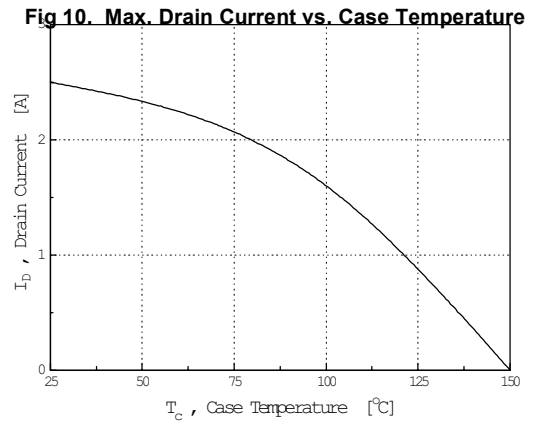
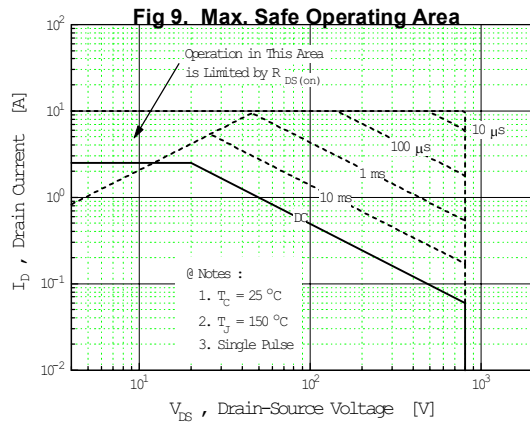
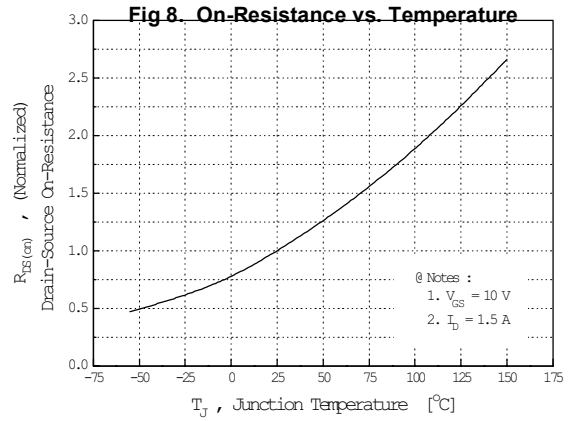
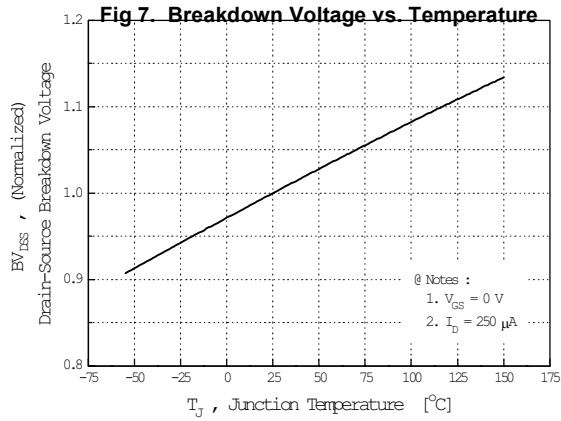


Fig 12. Gate Charge Test Circuit & Waveform

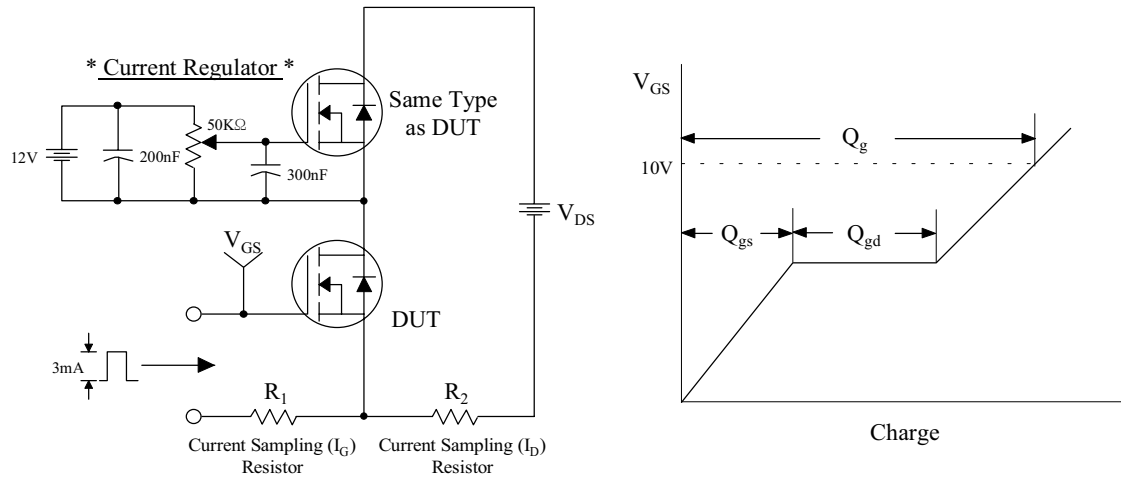


Fig 13. Resistive Switching Test Circuit & Waveforms

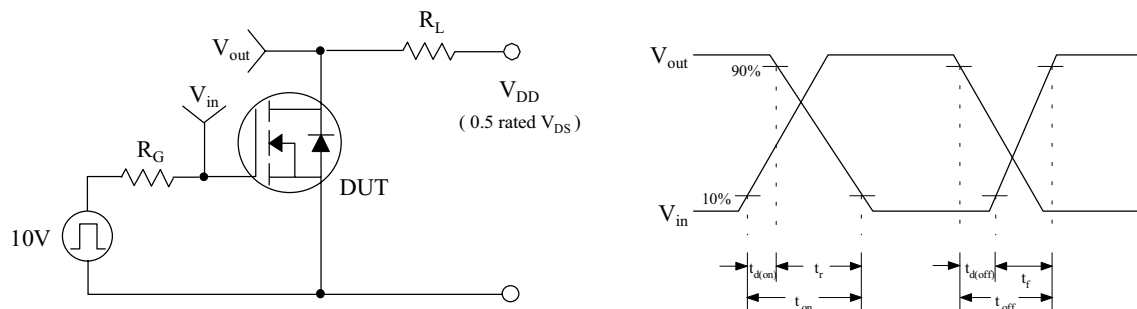


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

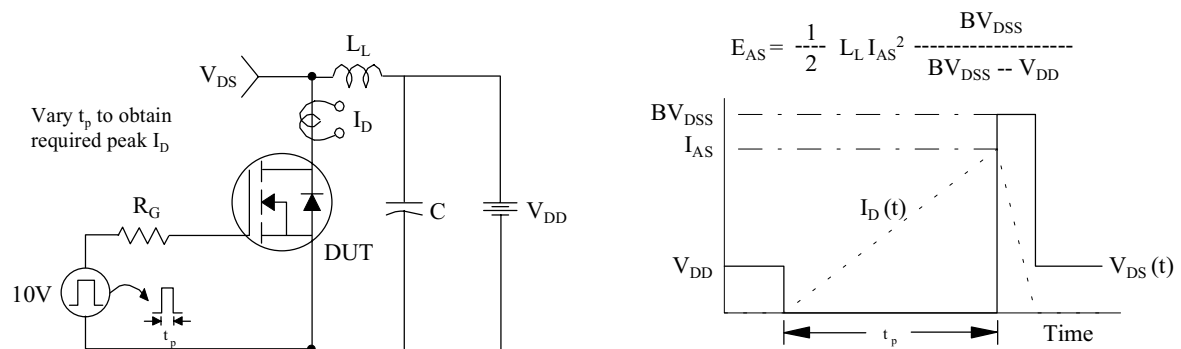


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

