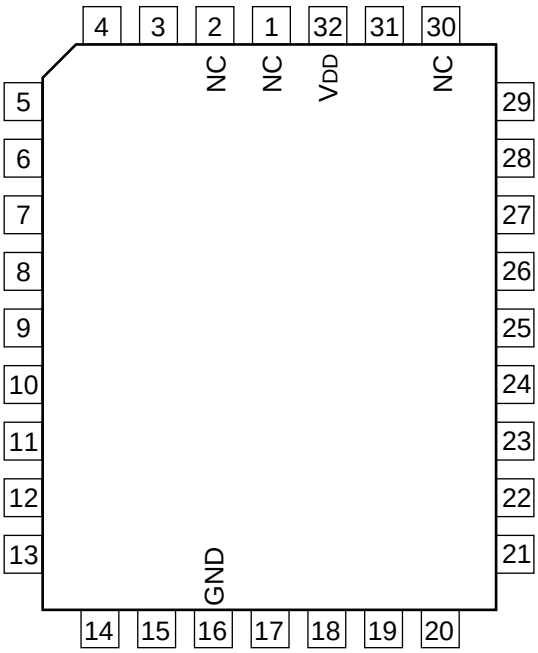
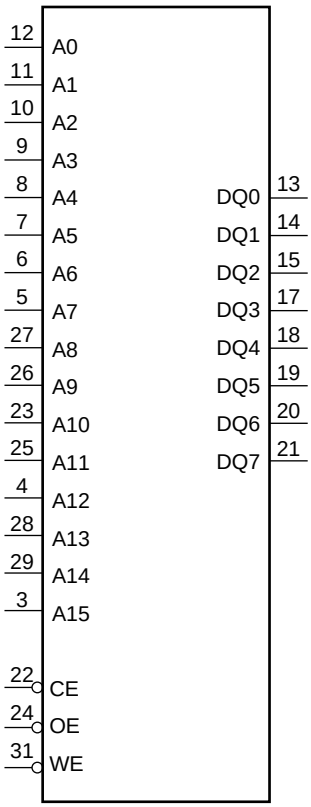
512 K-BIT FLASH MEMORY

—TOP VIEW—





PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	NC	17	I/O	DQ3
2	—	NC	18	I/O	DQ4
3	I	A15	19	I/O	DQ5
4	I	A12	20	I/O	DQ6
5	I	A7	21	I/O	DQ7
6	I	A6	22	I	$\overline{CE}$
7	I	A5	23	I	A10
8	I	A4	24	I	$\overline{OE}$
9	I	A3	25	I	A11
10	I	A2	26	I	A9
11	I	A1	27	I	A8
12	I	A0	28	I	A13
13	I/O	DQ0	29	I	A14
14	I/O	DQ1	30	—	NC
15	I/O	DQ2	31	I	$\overline{WE}$
16	—	GND	32	—	VDD

INPUTS

A0 - A15 : ADDRESS
$\overline{CE}$: CHIP ENABLE
$\overline{OE}$: OUTPUT ENABLE
$\overline{WE}$: WRITE ENABLE

INPUTS/OUTPUTS

DQ0 - DQ7 : DATA