Advanced Power MOSFET

SSP4N90A

FEATURES

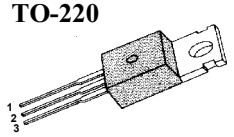
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 25 μA (Max.) @ V_{DS} = 900V
- Low $R_{DS(ON)}$: 4.181 Ω (Typ.)

BV_{DSS} = 900 V

$R_{DS(on)}$ = 5.0 Ω

I_D = 4 A

TO-220



1.Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	900	V
I_D	Continuous Drain Current (T_C=25 °C)	4	A
	Continuous Drain Current (T_C=100 °C)	2.5	
I_{DM}	Drain Current-Pulsed ①	16	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy ②	424	mJ
I_{AR}	Avalanche Current ①	4	A
E_{AR}	Repetitive Avalanche Energy ①	12	mJ
dv/dt	Peak Diode Recovery dv/dt ③	1.5	V/ns
P_D	Total Power Dissipation (T_C=25 °C)	120	W
	Linear Derating Factor	0.96	W/ °C
T_J , T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	°C
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8“ from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	1.04	°C /W
$R_{\theta CS}$	Case-to-Sink	0.5	--	
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	

SAMSUNG ELECTRONICS

Electrical Characteristics (T_C=25 °C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	900	--	--	V	V_{GS}=0V,I_D=250μA
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	1.14	--	V/ °C	I_D=250μA ***See Fig 7***
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	3.5	V	V_{DS}=5V,I_D=250μA
I_{GSS}	Gate-Source Leakage , Forward	--	--	100	nA	V_{GS}=30V
	Gate-Source Leakage , Reverse	--	--	-100		V_{GS}=-30V
I_{DSS}	Drain-to-Source Leakage Current	--	--	25	μA	V_{DS}=900V
		--	--	250		V_{DS}=720V,T_C=125 °C
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	5.0	Ω	V_{GS}=10V,I_D=2A ④*
g_{fs}	Forward Transconductance	--	2.85	--	℧	V_{DS}=50V,I_D=2A ④
C_{iss}	Input Capacitance	--	730	950	pF	V_{GS}=0V,V_{DS}=25V,f =1MHz ***See Fig 5***
C_{oss}	Output Capacitance	--	65	75		
C_{rss}	Reverse Transfer Capacitance	--	24	30		
$t_{d(on)}$	Turn-On Delay Time	--	18	45	ns	V_{DD}=450V,I_D=4A, R_G=13.6 Ω ***See Fig 13*** ④ ⑤
t_r	Rise Time	--	29	70		
$t_{d(off)}$	Turn-Off Delay Time	--	51	110		
t_f	Fall Time	--	28	65		
Q_g	Total Gate Charge	--	35	46	nC	V_{DS}=720V,V_{GS}=10V, I_D=4A ***See Fig 6 & Fig 12*** ④ ⑤
Q_{gs}	Gate-Source Charge	--	6.6	--		
Q_{gd}	Gate-Drain(“Miller”) Charge	--	15.0	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	4	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	--	--	16		
V_{SD}	Diode Forward Voltage ④	--	--	1.4	V	T_J=25 °C ,I_S=4A,V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	430	--	ns	T_J=25 °C ,I_F=4A di_F/dt=100A/μs ④
Q_{rr}	Reverse Recovery Charge	--	2.9	--	μC	

Notes ;

① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature

② L=50mH, I_{AS}=4A, V_{DD}=50V, R_G=27Ω, Starting T_J=25 °C

③ I_{SD} ≤ 4A, di/dt ≤ 100A/μs, V_{DD}≤ BV_{DSS} , Starting T_J=25 °C

④ Pulse Test : Pulse Width = 250μs, Duty Cycle≤ 2%

⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

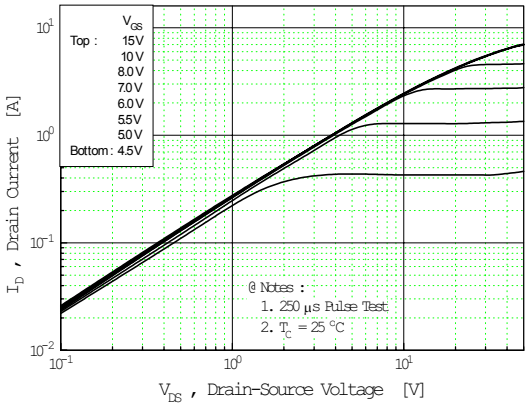


Fig 2. Transfer Characteristics

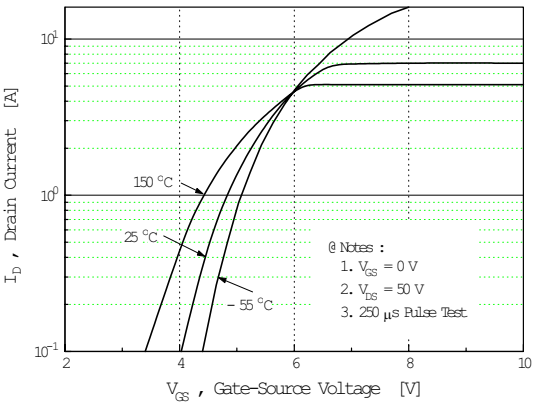


Fig 3. On-Resistance vs. Drain Current

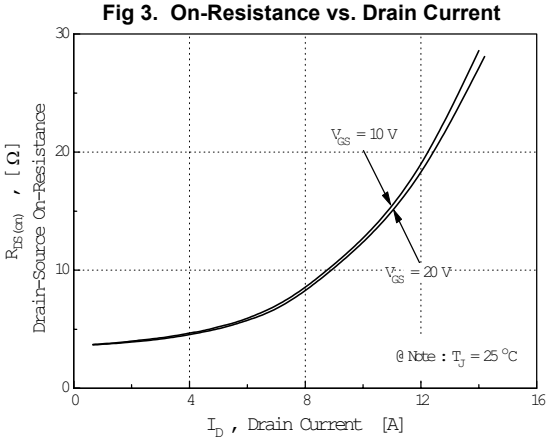


Fig 4. Source-Drain Diode Forward Voltage

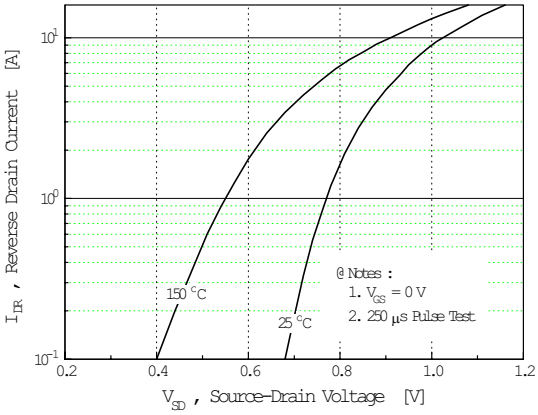


Fig 5. Capacitance vs. Drain-Source Voltage

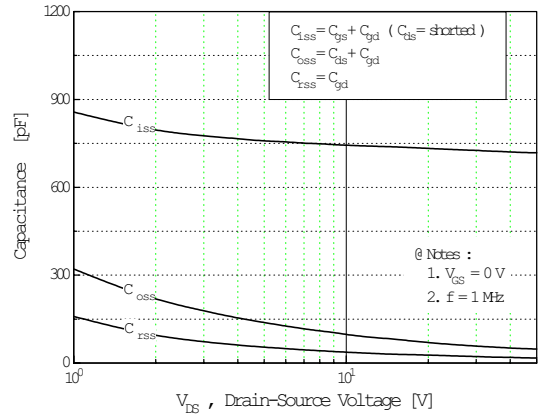


Fig 6. Gate Charge vs. Gate-Source Voltage

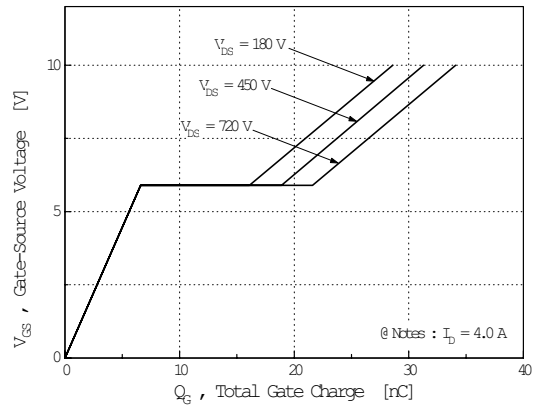


Fig 7. Breakdown Voltage vs. Temperature

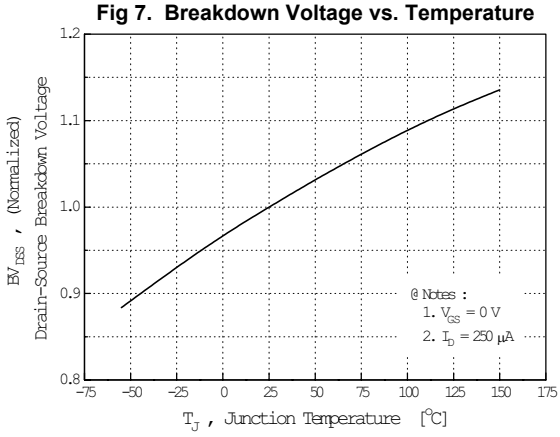


Fig 8. On-Resistance vs. Temperature

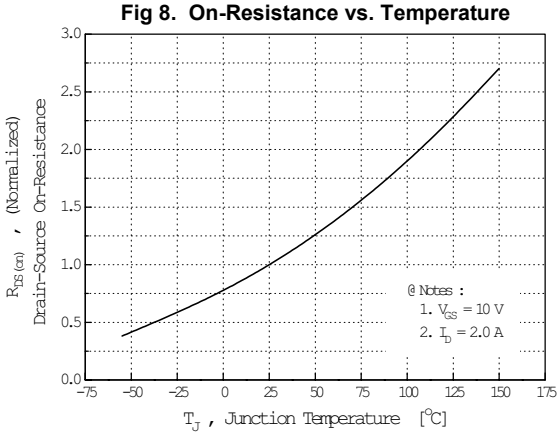


Fig 9. Max. Safe Operating Area

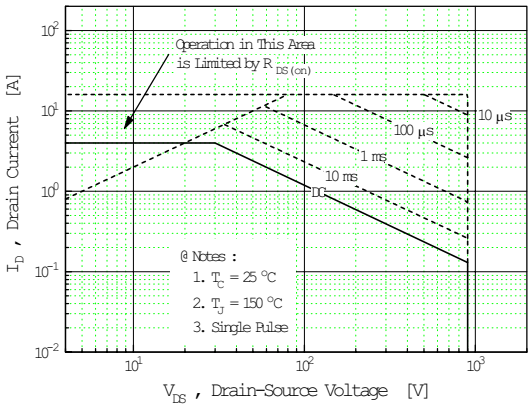


Fig 10. Max. Drain Current vs. Case Temperature

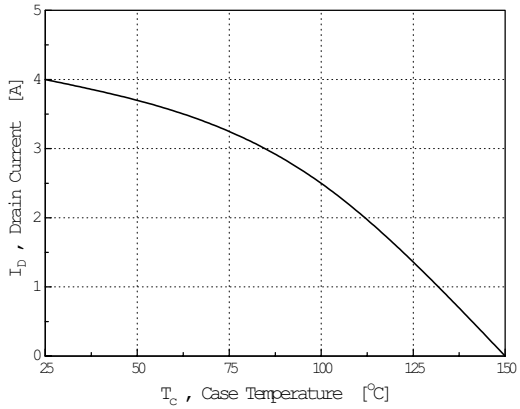


Fig 11. Thermal Response

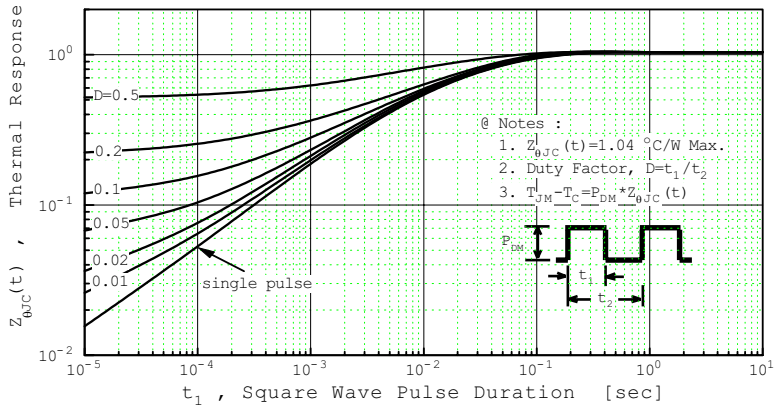


Fig 12. Gate Charge Test Circuit & Waveform

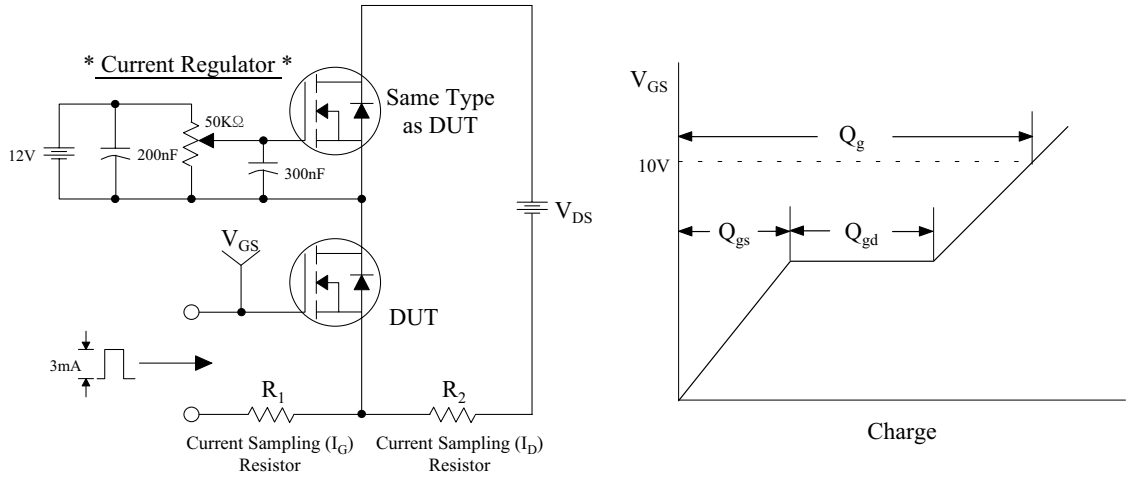


Fig 13. Resistive Switching Test Circuit & Waveforms

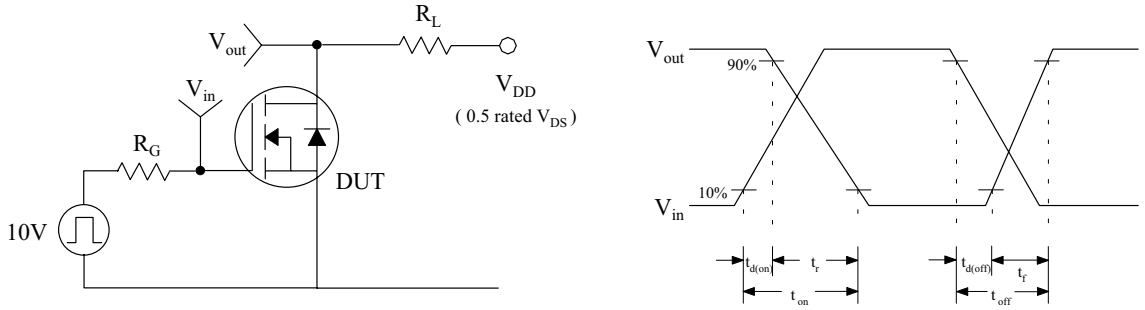


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

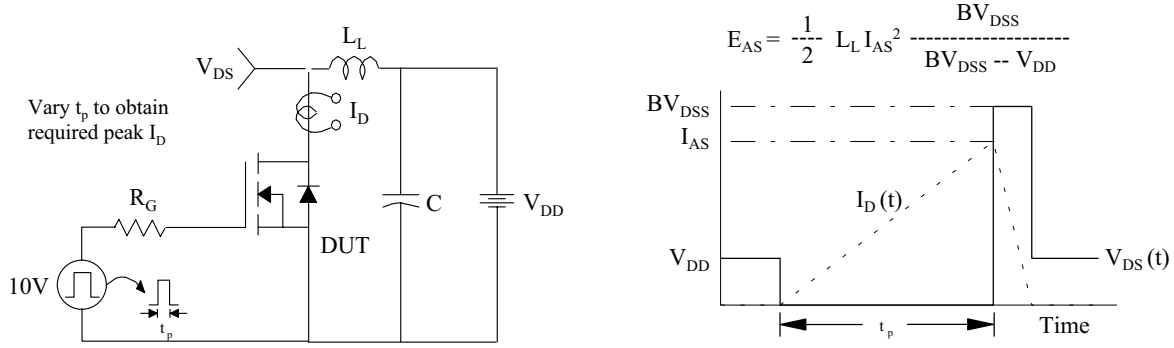


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms