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From equation 2:

$$\tau_2 = \frac{1}{(500 \text{ x } 2 \text{ x } \pi)^2 \text{ x } 1.318 \text{ x } 10^{-4}}$$

$$\tau_2 = 7.687 \text{ x } 10^{-4}$$

Using these values in equation 1:

$$\tau_1 = \frac{7.96 \text{ x } 10^{-3} \text{ x } 2 \text{ x } \pi \text{ x } 10\text{MHz/V}}{8000 \text{ x } (2\pi \text{ x } 500)^2}[A]^{½}$$

Where A is:

$$\frac{1 + \omega_n{}^2 \tau_2{}^2}{1 + \omega_n{}^2 \tau_3{}^2} = \frac{1 + (2\pi \text{ x } 500)^2 \text{ x } (7.687 \text{ x } 10^{-4})^2}{1 + (2\pi \text{ x } 500)^2 \text{ x } (1.318 \text{ x } 10^{-4})^2}$$

$$\tau_1 = \frac{500141.6}{7.896 \text{ x } 10^{10}} \left[\frac{6.832}{1.1714}\right]^{½}$$

$$\tau_1 = 6.334 \text{ x } 10^{-6} \text{ x } 2.415$$

$$\tau_1 = 1.53 \text{ x } 10^{-5}$$

now $\tau_1 = C_1 R_1$

$$\therefore C_1 = \frac{1.53 \text{ x } 10^{-5}}{1\text{k}\Omega} \quad (R_1 \textit{ is chosen as } 1\text{k})$$

$$C_1 = 0.0153\mu\text{F}$$

for figure 11a $\tau_2 = R_2 (C_1 + C_2)$

for figure 11a $\tau_3 = C_2 R_2$

substituting for C_2

$$\tau_2 = R_2\left[C_1 + \frac{\tau_3}{R_2}\right] \quad \therefore \tau_2 = R_2 C_1 + \tau_3$$

$$\therefore R_2 = \frac{\tau_2 - \tau_3}{C_1} = \frac{7.687 \text{ x } 10^{-4} - 1.318 \text{ x } 10^{-4}}{0.0153 \text{ x } 10^{-6}}$$

$$R_2 = 41627\Omega$$

$$\tau_3 = C_2 R_2 \quad \therefore C_2 = \frac{\tau_3}{R_2} = \frac{1.318 \text{ x } 10^{-4}}{41627}$$

$$C_2 = 3.17\text{nF}$$

for figure 11b $\tau_1 = C_1 R_1 \quad \therefore C_1 = \frac{1.53 \text{ x } 10^{-5}}{1\text{k}}$

$$C_1 = 0.0153\mu\text{F}$$

$$\tau_2 = C_1 R_2 \quad \therefore R_2 = \frac{7.687 \text{ x } 10^{-4}}{1.53 \text{ x } 10^{-8}}$$

$$R_2 = 50.242\text{k}\Omega$$

$$\tau_3 = C_2 R_3$$

Since both values are independent of the other components, either C_2 or R_3 can be chosen and the other calculated.

assume $R_3 = 1\text{k}\Omega \quad \therefore C_2 = \frac{1.318 \text{ x } 10^{-4}}{1000}$

$$C_2 = 1.318 \text{ x } 10^{-7}$$

$$C_2 = 0.1318\mu\text{F}$$

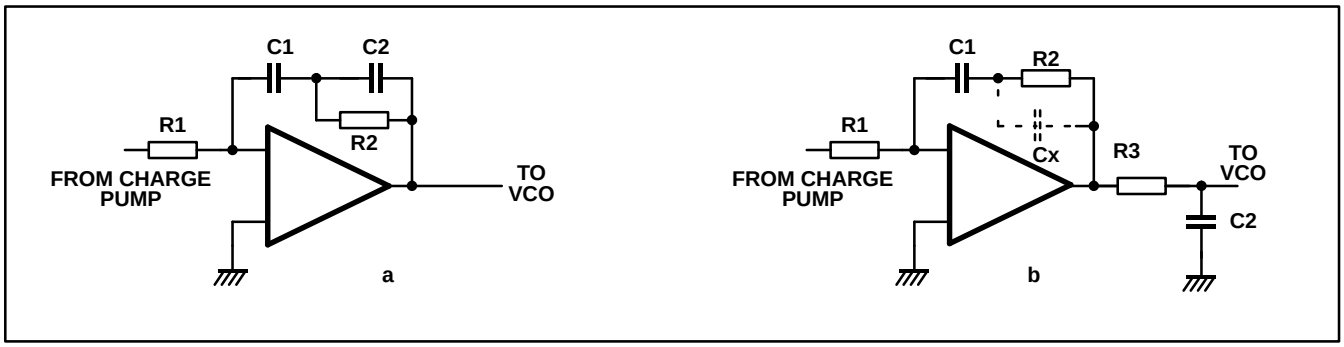


Fig. 11a and b Standard and modified form of third order loop filter

$$\tau_2 = C_1 R_1 \qquad \therefore C_1 = \frac{4.50 \times 10^{-4}}{6.33 \times 10^{-9}} = R_2$$

$$R_2 = 71000\ \text{OHms}$$

Third order loop

The third order loop filter is normally shown as in Fig. 11. Fig. 11b shows the circuit redrawn to use an RC time constant after the amplifier, allowing any feedthrough capacitance on the VCO line to be included in the loop calculations. Where the modified form in Fig. 11b is used it is advantageous to connect a small capacitor Cx of typically 100pF (shown dotted), across the amplifier to reduce sidebands caused by the amplifier being forced into non linear operation by the phase comparator pulses.

Three equations are required to determine the time constants, τ_1, τ_2 and τ_3 where:

for Fig. 11a

$\tau_1 = C_1 R_1$
$\tau_2 = R_2 (C_1 + C_2)$
$\tau_3 = C_2 R_2$

and for Fig. 11b

$\tau_1 = C_1 R_1$
$\tau_2 = C_1 R_2$
$\tau_3 = C_2 R_3$

The equations are:

1 $$\tau_1 = \frac{K_\theta K_0}{N\omega_n^2}\left[\frac{1 + \omega_n^2 \tau_2^2}{1 + \omega_n^2 \tau_3^2}\right] \text{½}$$

2 $$\tau_2 = \frac{1}{\omega_n^2 \tau_3}$$

3 $$\tau_3 = \frac{-\tan\Phi_0 + \frac{1}{\cos\Phi_0}}{\omega_n}$$

Where:

K_θ is the phase detector gain factor in V/Radian
K_0 is the VCO gain factor in radians second/Volt
N is the total division ratio from VCO to reference frequency
ω_n is the natural loop bandwidth
Φ_0 is the Phase margin normally set to 45°

As in the second order filter example a value for R1 can be assumed and an equivalent gain K_θ in V/radian calculated from:

$$\frac{\text{phase comparator current setting } \mu\text{A/radian}}{2\pi} \times 1\text{K}$$

Where 1K Ohm is the assumed value for R_1

These values can now be substituted in equation 1 to obtain a value for C_1 and equations 2 and 3 used to determine values for C_2 and R_2

EXAMPLE

Calculate values for a loop with the following parameters.

Frequency to be synthesised:	800MHz	
Reference frequency	100kHz	
Division ratio	$\frac{800\text{MHz}}{100\text{kHz}}$	=8000
ω_n natural loop frequency	500Hz	
K_0 VCO gain factor	2π x 10MHz/Volt	
Φ_0 phase margin	45°	
Phase comparator current	50μA	

assuming R_1 is 1K Ohm, then the equivalent phase comparator gain K_θ in V/radian is:

$$\frac{50\mu\text{A}}{2\pi} \times 1000 = 0.00796\ \text{V/radian}$$

From equation 3:

$$\tau_3 = \frac{-\tan 45^o + \frac{1}{\cos 45^o}}{500\text{Hz} \times 2\pi} = \frac{0.4142}{3141.6}$$

$$\tau_3 = 1.318 \times 10^{-4}$$

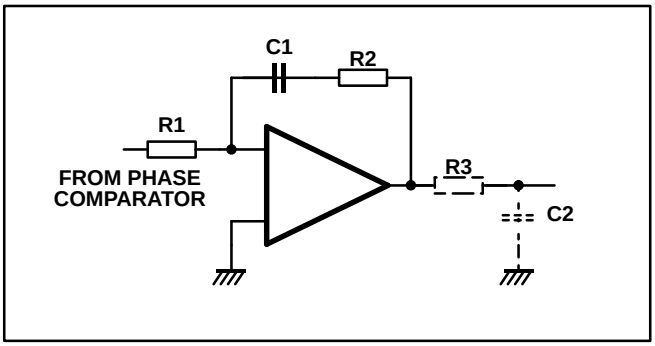


Fig. 9 Standard form of second order loop filter

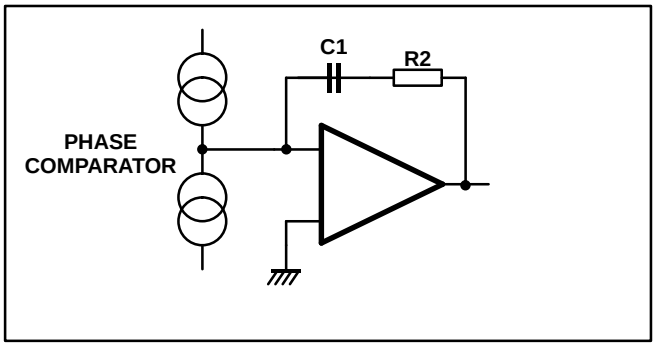


Fig. 10 Modified second order loop filter

Loop calculations

Many frequency synthesiser designs use a second order loop with a loop filter of the form shown in Fig. 9.

In practice an additional RC time constant (shown dotted in Fig. 9) is often added to reduce noise from the amplifier. In addition any feedthrough capacitor or local decoupling at the VCO will be added to the value of C2. These additional components in fact form a third order loop, and if the values are chosen correctly, the additional filtering provided can considerably reduce the level of reference frequency sidebands and noise without adversely affecting the loop settling time. The calculation of values for both forms of loop is shown below.

Second order loop

For this filter two equations are required to determine the time constants τ_1 and τ_2 where:

$$\tau_1 = C_1 R_1$$
$$\tau_2 = C_2 R_2$$

The equations are:

1 $$\tau_1 = \frac{K_\theta K_0}{\omega_n^2 N}$$

2 $$\tau_2 = \frac{2\zeta}{\omega_n}$$

where:

- K_θ is the phase detector gain factor in V/Radian
- K_0 is the VCO gain factor in radians second /Volt
- N is the division ratio from VCO to reference frequency
- ω_n is the natural loop bandwidth
- ζ is the damping factor: normally 0.7071

The SP8853 phase comparator is a current source rather than a conventional voltage source and has a gain factor specified in μA/radian. Since the equations deal with a filter where R_1 is feeding the virtual earth point of an operational amplifier from a voltage source, R_1 is setting the input current to the filter which is similar to the circuit shown in Fig.10 where a current source phase comparator is connected directly to the virtual earth point of the operational amplifier.

The equivalent voltage gain of the phase comparator can be calculated by assuming a value for R_1 and calculating a gain in volts/radian which would produce the set current.

The digital phase comparator used in the SP8853 is linear over a range of 2π radians and therefore the phase comparator gain is given by:

$$\frac{\text{phase comparator current setting } \mu\text{A/Radian.}}{2\pi}$$

The phase comparator gain in V/radian is therefore:

$$\frac{50\mu A}{2\pi} \; x \; 1K \text{ ohm}$$

assuming a value of 1K for R_1 and 50μA for the phase comparator current setting, these values can now be inserted in equation 1 to obtain values for C_1 and equation 2 used to determine a value for R_2.

Example:

Calculate values for a second order loop with the following parameters:

Frequency to be synthesised	800MHz
Reference frequency	100kHz
Division ratio N	$\frac{800MHz}{100kHz}$ =8000
Natural loop frequency ω_n	500Hz
VCO gain factor K_0	2π x 10MHz/Volt
Damping factor ζ	0.7071
Phase comparator current setting	50μA

Assuming R_1 is 1kΩ then the equivalent phase comparator gain K_θ in V/radian = $\frac{50\mu A}{2\pi}$ x 1000

$$K_\theta = 0.00796 \text{V/radian}$$

From equation 1 $$\tau_1 = \frac{0 . 00796 \text{ x } 2 \text{ x } \pi \text{ x } 10MHz}{(2 \text{ x } \pi \text{ x } 500)^2 \text{ x } 8000}$$

$$\tau_1 = 6 . 334 \text{ x } 10^{-6}$$

From equation 2 $$\tau_2 = \frac{2 \text{ x } 0 . 7071}{2 \text{ x } \pi \text{ x } 500}$$

$$\tau_2 = 4 . 50 \text{ x } 10^{-4}$$

Now $$\tau_1 = C_1 R_1 \quad \therefore C_1 = \frac{6 . 334 \text{ x } 10^{-6}}{1k\Omega}$$

1K is chosen value for R_1

C_1 = 6.33nF

APPLICATIONS

A basic application using a single phase comparator is shown in Fig. 6. The SP8853 is a 1.5 GHz part, so good RF design techniques should be employed, including the use of a ground plane and suitable high frequency capacitors at the RF input and for power supply decoupling.

The RF input should be coupled to either pin 10 or 11, and the other pin decoupled to ground. The reference oscillator is of conventional Colpitts type with two capacitors required to provide a low impedance tap for the feedback signal to the transistor emitter. Typical values are shown in Fig. 6 although these may be varied to suit the loading requirements of particular crystals. Where a suitable reference signal already exists or where a very stable source is required, it is possible to apply an external reference as shown inset in Fig. 6. The amplitude should be kept below 0.5V RMS to avoid forward biasing the transistor collector base junction.

In some systems, it is useful to have an indication of phase lock. The output from pin 27 goes low when the output of charge pump 2 is between 2.25 and 2.75V and can be used to operate an LED to give visual indication of phase lock. Alternatively a pull–up resistor may be connected to V_{CC} and the output used to signal to the control microprocessor that the loop is locked thus speeding up system operation. The output current available from pin 27 is limited to 1.5mA. If this current is exceeded the logic low level will be uncertain.

The circuit diagram shown in Fig.6 is a basic application with minimum component count which is nevertheless perfectly adequate for many applications. Charge pump 1 on pin 3 is used to drive the loop amplifier which provides the control voltage for the local oscillator. When charge pump 1 is used in this mode, the PD1 and PD2 bits in the reference programming word must be set to enable charge pump 1 continuously. This application could also use charge pump 2 output on pin 25 or if a higher phase comparator gain is required, pins 3 and 25 could be connected in parallel to use the combined output current from both charge pumps.

The lock detect circuit can be programmed to automatically disable charge pump 1 as shown in Table 4. This feature can be used to reduce the system lock up time by connecting the charge pump outputs in parallel to the loop amplifier with a resistor, (shown dotted) in series with charge pump 2. This connection allows a relatively high current to be used from charge pump 1 to give short lock up time, and a low current to be set on charge pump 2 giving low reference frequency sidebands. The degree of lock up time improvement depends on the ratio of charge pump 1 to charge pump 2 currents.

When the loop is out of lock, both charge pumps will be enabled and will feed current to the loop amplifier to bring the oscillator to phase lock. The current from charge pump 2 will produce a voltage drop across the series resistor allowing operation of the lock detect circuit and enabling charge pump 1. The resistor must be chosen to give a voltage drop greater than 0.25V at the current level programmed for charge pump 2. When phase lock is achieved, there will be no charge pump current and therefore the voltage at pin 25 will be equal to that on the virtual earth point of the loop amplifier (2.5V), disabling charge pump 1.

Charge pump 1 should not be left open circuit when enabled as this prevents correct operation of the phase detector. The output on pin 3 should be biased to half supply with a pair of 4k7 resistors connected between supplies.

When charge pump 2 is used to drive the loop amplifier, the lock detect circuit will only give an out of lock indication when large frequency changes are made or when a frequency outside the range of the local oscillator is programmed. At other times the loop amplifier input is maintained at 2.5V by the action of the loop filter components. Again a resistor connected between pin 25 and the loop amplifer, producing a voltage drop greater than 0.25V at the charge pump current programmed will allow sensitive out of lock detection.

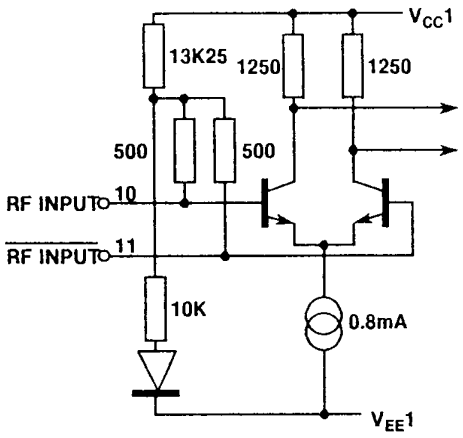
When phase lock detection is required using comparator 1 only, charge pump 2 output on (pin 25) should be biased to 2.5V using two equal value resistors across the supply. The values should be chosen to give a voltage change greater than 0.25V at the programmed comparator 2 charge pump current. A small capacitor connected from pin 28 to ground may be used to reduce chatter at the lock detect output (see inset Fig. 6). A detailed block diagram showing the lock detect circuitry is shown in Fig.3.

An amplifier is required to convert the current pulses from the phase comparator into a voltage of suitable magnitude to drive the chosen VCO. The choice of amplifier must be determined by the voltage swing required at the VCO to achieve the necessary frequency range, and in most cases an operational amplifier will be used to provide the essential characteristics of high input impedance, high gain and low output impedance required in this application.

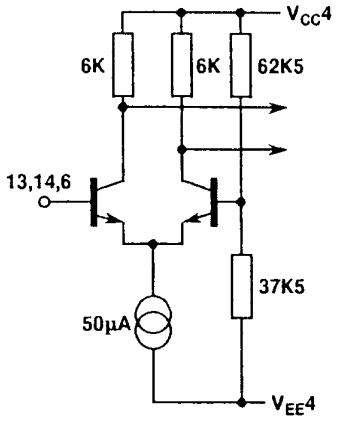
Although it is expected that an operational amplifier will be used in most cases, a simple discrete design can be used and a suitable design is shown inset in Fig. 6. This arrangement can be particularly useful when the minimum VCO control voltage must be close to ground and where negative supplies are inconvenient. This form of amplifier is not suitable for use with charge pump 2 when the lock detect circuit is required.

When an operational amplifier is used in the inverting configuration shown in Fig. 6, the charge pump output is connected directly to the virtual earth point and will therefore operate at a voltage similar to that set on the non–inverting input. Normally this operating point should be set at half supply using a potentiometer of two equal resistors, but if necessary this voltage can be set up to 1V higher or lower than half supply without detrimental effect. When the lock detect function is required on charge pump 2, the non–inverting input must be at half supply.

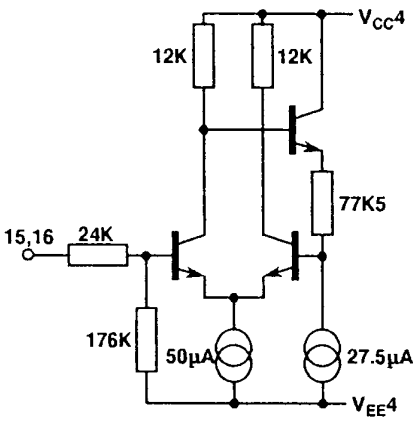
The digital phase comparator and charge pump used on the SP8853 produces bi–directional current pulses in order to correct errors between the reference and VCO divider outputs. Once synchronisataion is achieved, in theory no further output from the charge pump should be required, but in practice, due to leakage currents and particularly the input current of the amplifier, the capacitors forming the loop filter around the amplifier will gradually discharge, modifying the VCO voltage and requiring further outputs from the charge pump to restore the charge. The effect of this continuous correction of the local oscillator frequency, is to frequency modulate the VCO and thus produce sidebands at the reference frequency. In order to reduce this effect to a minimum, an amplifier with low input bias current is essential.



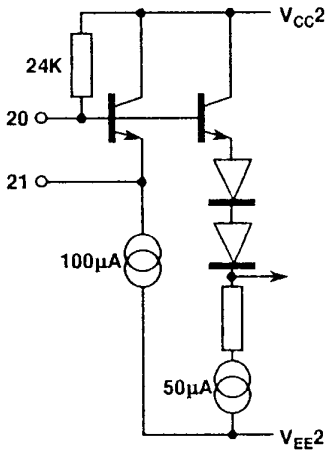
RF PRE-AMPLIFIER INPUTS



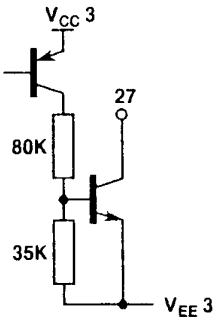
F1/F2 DATA AND POWER DOWN INPUTS



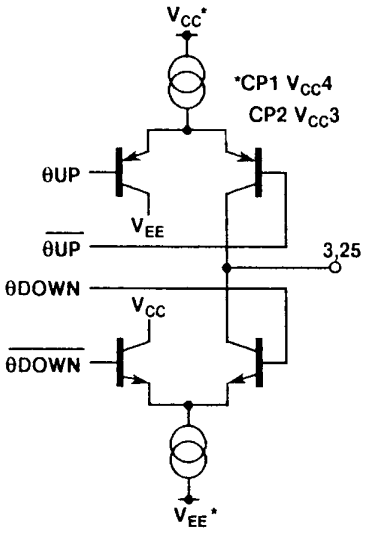
HYSTERESIS INPUTS DATA CLOCK AND ENABLE



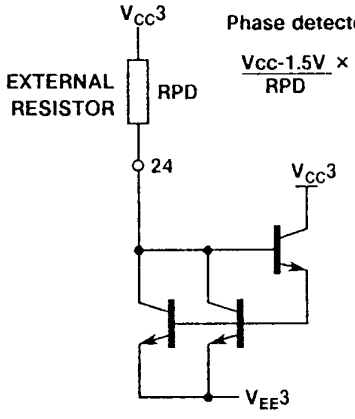
OSCILLATOR PINS



LOCK DETECT OUTPUT



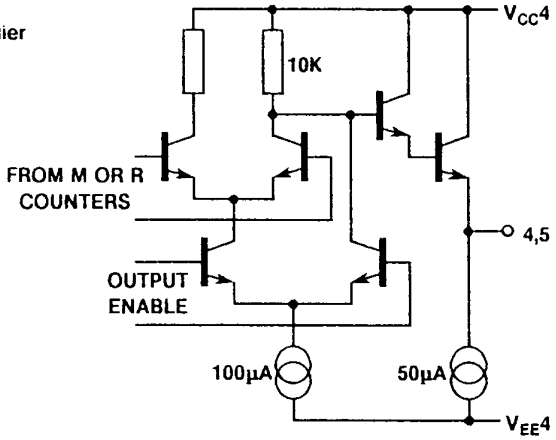
PHASE DETECTOR CHARGE PUMPS



Phase detector current =

$\frac{Vcc-1.5V}{RPD} \times$ charge pump multiplier

CHARGE PUMP 2 CURRENT PROGRAMMING



Fpd AND FREF OUTPUTS

Fig. 8 Input and output interface diagrams

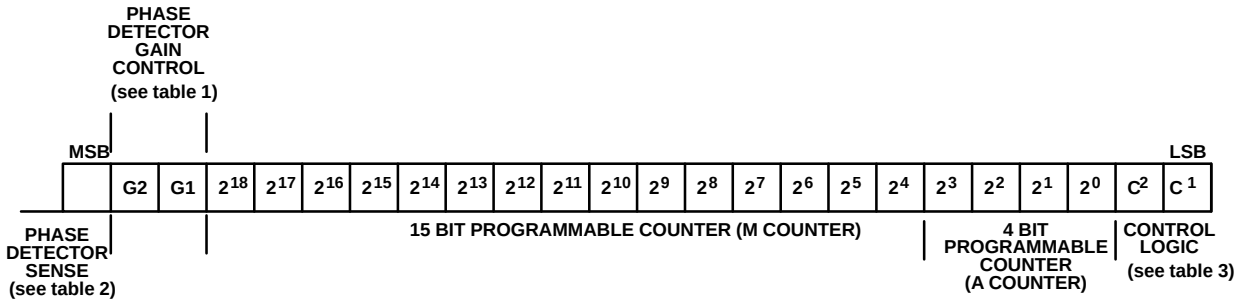


Fig. 7 (a) F1 or F2 word, bit allocation with 16/17 selected

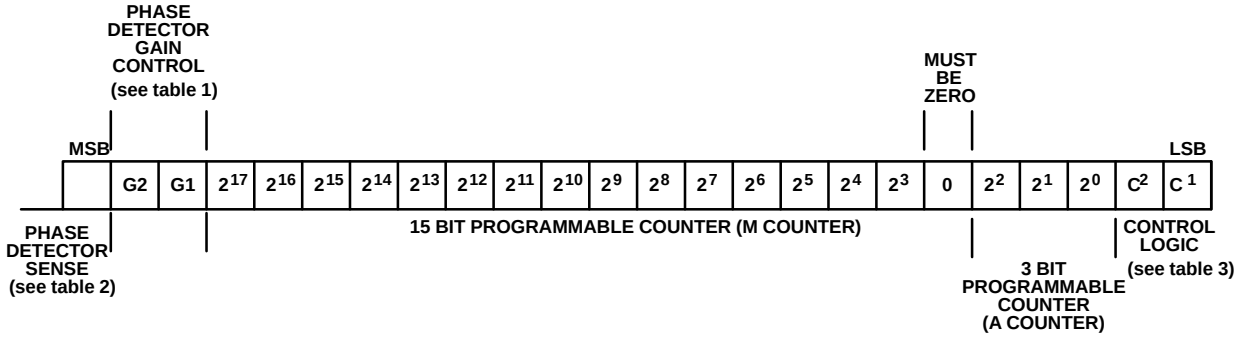


Fig. 7 (b) F1 or F2 word, bit allocation with 8/9 selected

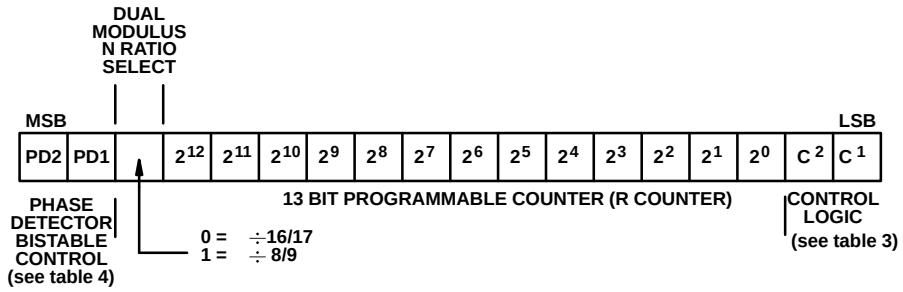


Fig. 7 (c) reference word bit allocation

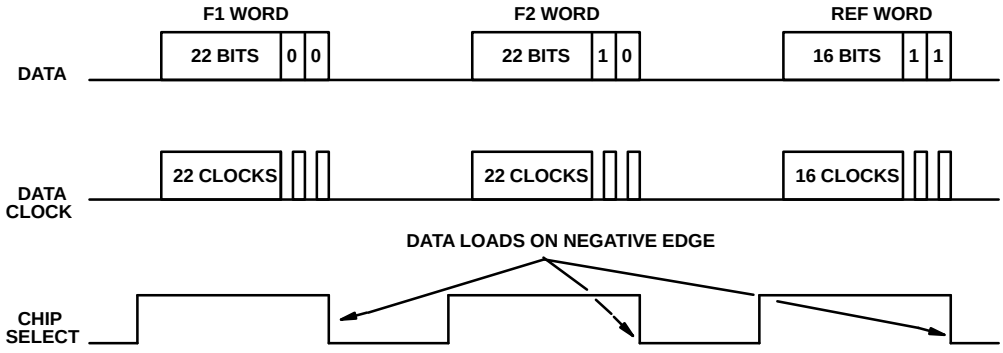


Fig. 7 (d) Typical data load sequence

Fig. 7 Data format diagrams

period, since the loop can be locked to F1 whilst F2 is updated by entering new data via the shift register. The F1/F2 input is high to select F1.

An F1 or F2 update cycle will consist of a byte containing 24 bits whereas the reference byte will contain 18 bits. The device requires 3 bytes, each with a chip select sequence, totalling 66 bits to fully program.

When the dual modulus counter (A count) is set to ÷8/9, the data required to set the counter is reduced by one bit, leaving an unused bit in the 22–bit F1/F2 buffer. This bit must always be set to zero when ÷8/9 mode is required. Various programming sequences are shown in Fig. 7.

The data entry and storage registers are always powered up, making it possible to enter data when the device is in the powered down state.

PD2	PD1	
0	0	F_{ref} and F_{pd} outputs off, charge pumps 1 and 2 on
0	1	F_{ref} and F_{pd} outputs on, charge pump 1 off. Charge pump 2 on
1	0	F_{ref} and F_{pd} outputs off, charge pump 1 disabled by lock detect. Charge pump 2 on
1	1	F_{ref} and F_{pd} outputs on, charge pump 1 disabled by lock detect. Charge pump 2 on

Table 4

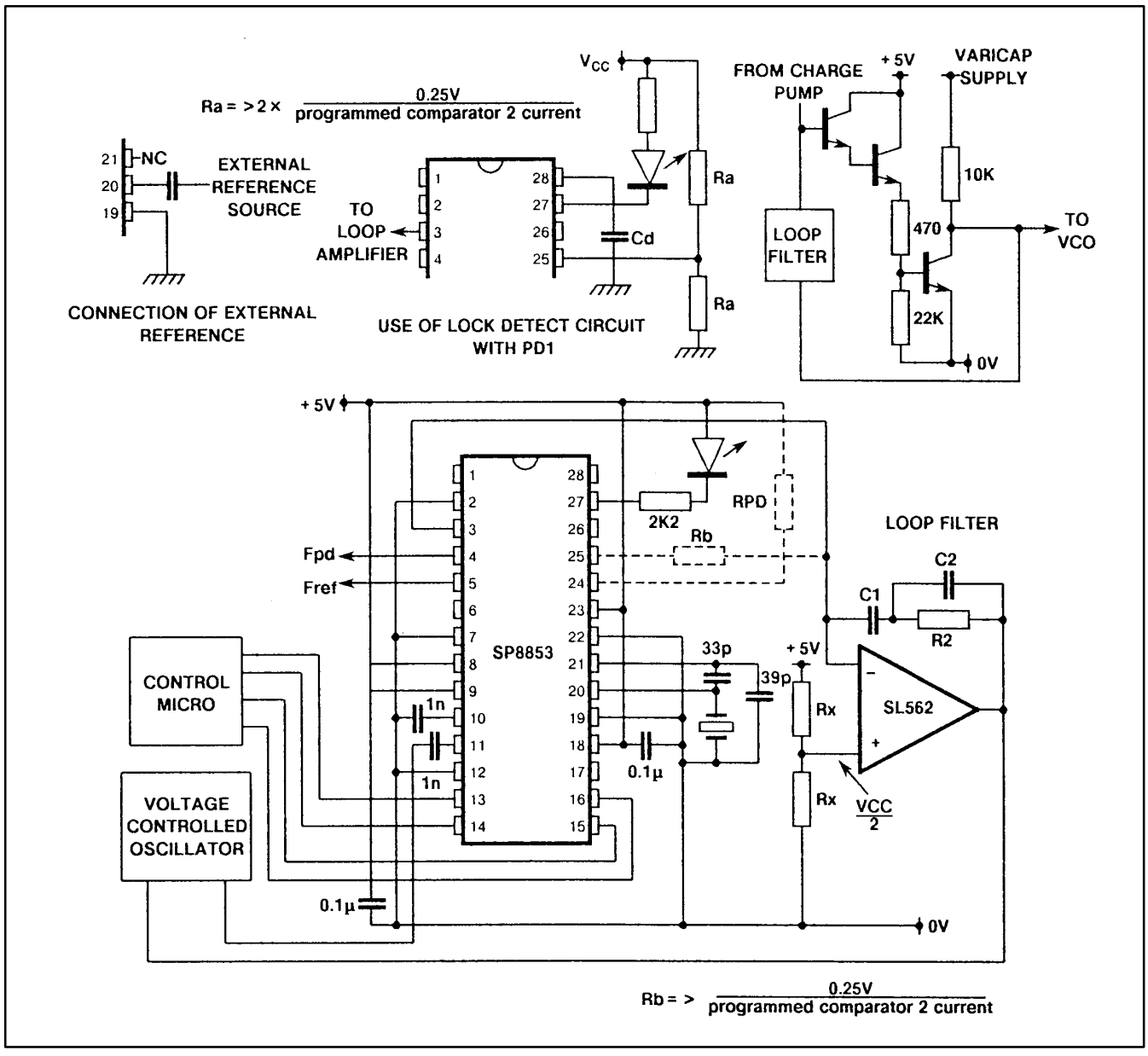


Fig. 6 Typical application diagram

DESCRIPTION

Prescaler and A M counter

The programmable divider chain is of A M counter construction and therefore contains a dual modulus front end prescaler, an A counter which controls the dual modulus ratio and an M counter which performs the bulk multi–modulus division. A programmable divider of this construction has a division ratio of MN + A and a minimum integer steppable division ratio of N(N–1).

In the SP8853 the dual modulus front end prescaler is a dual N ratio device capable of being statically switched between 16/17 and 8/9 ratios. The controlling A counter is of four bit design enabling a maximum count sequence of 15, (2^4–1) which begins with the start of the M counter sequence and stops when it has counted by the preloaded number of cycles. Whilst the A counter is counting the dual modulus prescaler is held in the N +1 mode, then relaxes back to the N mode at the completion of the sequence. The M counter is a 15–bit asynchronous divider which counts with a ratio set by a control word. In both A and M counters the controlling data from the F1/F2 buffer is loaded in sequence with every M count cycle. The N ratio of the dual modulus prescaler is selected by a one bit word in the reference divider buffer and,when a ratio of 8/9 is selected the A counter requires only three programming bits, having an impact on the frequency bit allocation as described in the data entry section.

Reference source and divider

The reference source in the SP8853 is obtained from an on board oscillator, frequency controlled by an external crystal. The oscillator can also function as a buffer amplifier allowing the use of an external reference source. In this mode the source is simply AC coupled into the oscillator transistor base on pin 20.

The oscillator output is coupled to a programmable reference divider whose output is the reference for the phase detector. The reference divider is a fully programmable 13–bit asynchronous design and can be set to any division ratio between 1 and 8191. The actual division ratio is controlled by a data word stored in the internal reference buffer.

Phase comparator

The SP8853 is provided with a digital phase comparator feeding two charge pump circuits. Charge pump 1 has preset currents programmable as shown in Table 1. Charge pump 2 has a current level set by an external resistor: the current is multiplied by a factor determined by the F1 or F2 word (see Table 1).

A lock detect circuit is connected to the output of charge pump 2. When the voltage level at pin 25 is between approximately 2.25 and 2.75 volts, pin 27 will be low and charge pump 1 disabled depending on the PD1 and PD2 programming bits as shown in Table 4.

The output signals from the reference and M counters are available on pins 4 and 5 when programmed by the reference programming word: the various options are shown in Table 4. An external phase detector may be connected to pins 4 and 5 and may be used independently or in conjunction with the on chip detector.

To allow for control direction changes introduced by the design of the control loop, a programming bit in the F1/F2 programming word interchanges the inputs to the on chip phase detector and reverses the functions on pins 4 and 5.

F1 OR F2 WORD		CHARGE PUMP 1	CHARGE PUMP 2
G2	G1	CURRENT	MULTIPLIER
0	0	50μA	1
1	0	75μA	1.5
0	1	125μA	2.5
1	1	200μA	4

Table 1 Charge pump currents

Note: **Charge pump 2** is pin 24 current x multiplication

$$\text{factor . I pin 24} = \frac{V_{CC} - 1.5V}{RPD}$$

Data entry and storage

The data section of the SP8853 consists of a data input interface, an internal data shift register and three internal data buffers.

Data is entered to the data input interface by a three wire data highway with data, clock and chip enable inputs. The input interface then routes this data to a 24–bit shift register with bus connections to three data buffers. Data entered via the serial bus is transferred to the appropriate data buffer on the negative transition of the chip enable input according to the two final data bits as shown in Table 3. The MSB of the data is entered first.

The dual F1/F2 buffer can receive two 22–bit words and controls the programmable divider A and M counters using 19–bits, the phase detector gain with two bits and the phase detector sense with one bit. A fourth input from the synthesiser control system selects the active buffer.

OUTPUT FOR RF PHASE LAG	
Sense Bit	Pins 3 and 25
0	Current source
1	Current sink

Table 2

The third buffer contains only 16 bits, 13 being used to set the reference counter division ratio, and 2 to control the phase comparator enable logic. The remaining bit sets the dual modulus prescaler N ratio.

2 Bit S.R. Contents	Buffer Loaded
00	F1
10	F2
01	Active A *
11	Reference

Table 3

** Transfer of A counter bits into buffer controlling the programmable counter*

The data words may be entered in any individual multiple sequence and the shift register can be updated whilst the data buffers retain control of the synthesiser with the previously loaded data. This enables four unique data words to be stored in the device, with three in the data buffers and a fourth in the shift register, whilst the chip is enabled. F1 word may also be updated whilst F2 is controlling the programmable divider and vice versa.

The dual F1/F2 buffer enables the device to be toggled between two frequencies using the F1/F2 select input at a rate determined by the comparison frequency and also enables random frequency hopping at a rate determined by a byte load

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated).

Supply Voltage V_{CC} +4.75 to +5.25V

Temperature A Grade T_{amb} = –55°C to +125°C

B Grade T_{amb} = –40°C to + 85°C

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	8, 9					
	18, 23		33	40	mA	
Supply Current in Power Down Mode	8		4.5	7.5	mA	
Input Sensitivity	10, 11					See Fig. 4a and b
Input Overload	10, 11					See Fig. 4a and b
RF Input Division Ratio	10,11,4	256		524287		With 16/17 selected
		56		262143		With 8/9 selected
Comparison Frequency	4, 5			5	MHz	
Reference Oscillator Input Frequency	20, 21	4		20	MHz	
External Reference Input Voltage	20	10		500	mVrms	
Reference Division Ratio	20, 5	1		8191		
Data Clock Repetition Rate t_{rep}	15			1	μs	See Fig. 5
Minimum Set up Time t_s	14, 15	50			ns	See Fig. 5
Data Input High	14	$0.6V_{CC}$		V_{CC}	V	
Low	14	V_{ee}		$0.3V_{CC}$	V	
Clock Input High	15	$0.6V_{CC}$		V_{CC}	V	
Low	15	V_{ee}		$0.3V_{CC}$	V	
Data Enable High	16	$0.6V_{CC}$		V_{CC}	V	
Low	16	V_{ee}		$0.3V_{CC}$	V	
F1/F2 Input High	13	$0.6V_{CC}$		V_{CC}	V	F1 buffer selected
Low	13	V_{ee}		$0.3V_{CC}$	V	F2 buffer selected
Power Down Input High	6	$0.6V_{CC}$		$0.9V_{CC}$	V	
Low	6	V_{ee}		$0.3V_{CC}$	V	
F1/F2 Input Current	13			5	μA	V pin 13 = 5.0V
Power Down Input Current	6			5	μA	V pin 6 = 4.5V
RPD External Resistance	24	68		330	KOhms	
Lock Detect Output Voltage “in lock”	27			1	V	I pin 27–1mA
Lock Detect Switching Voltage High	25	2.7			V	V_{CC} = 5V
Low	25			2.3	V	V_{CC} = 5V
F_{pd} and F_{ref} Output Voltage Swing			0.9		V	V_{CC} = 5V. External pull down may be required

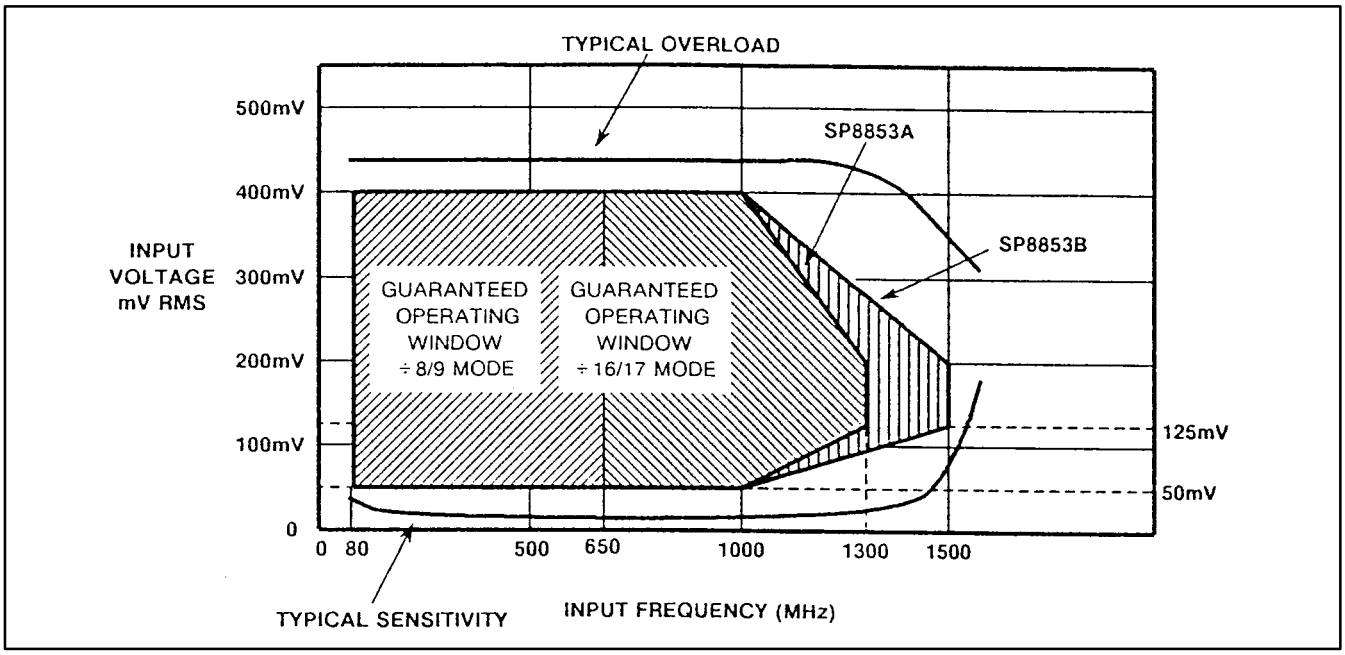


Fig. 4a Typical input characteristics and input drive requirements (DG package)

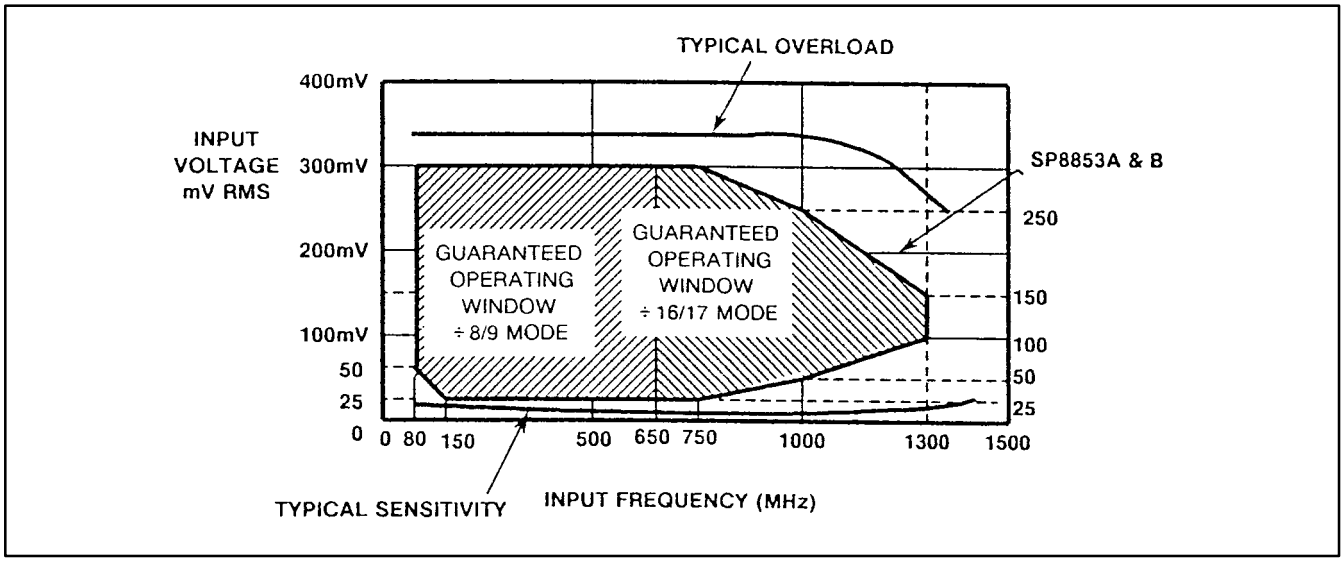


Fig. 4b Typical input characteristics and input drive requirements (HC package)

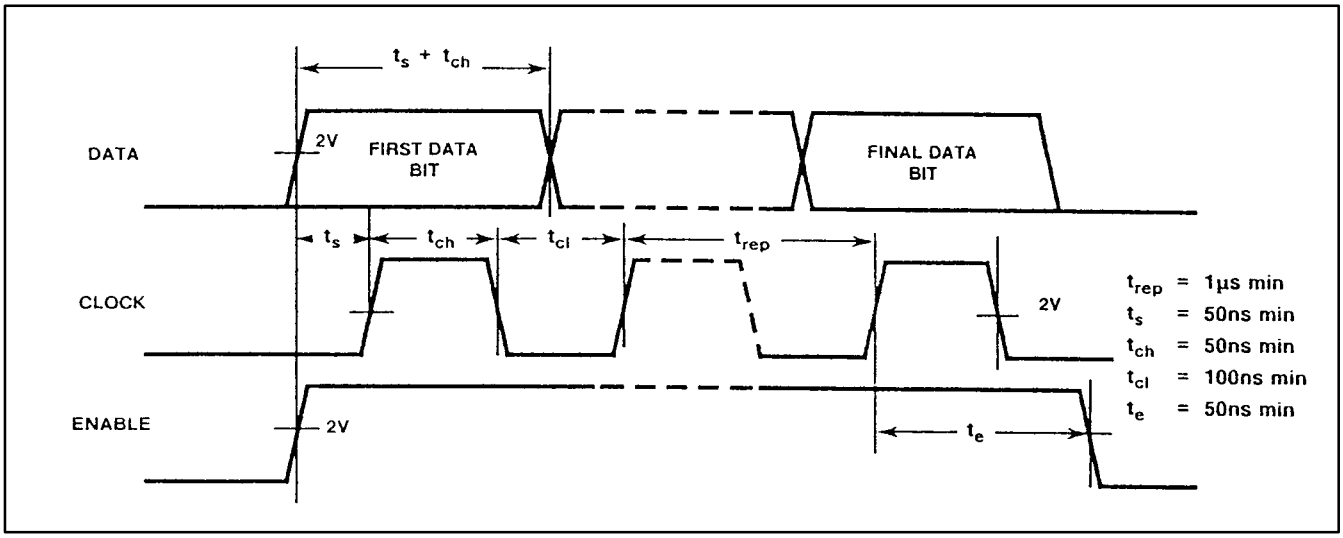


Fig. 5 Data and clock timing requirements

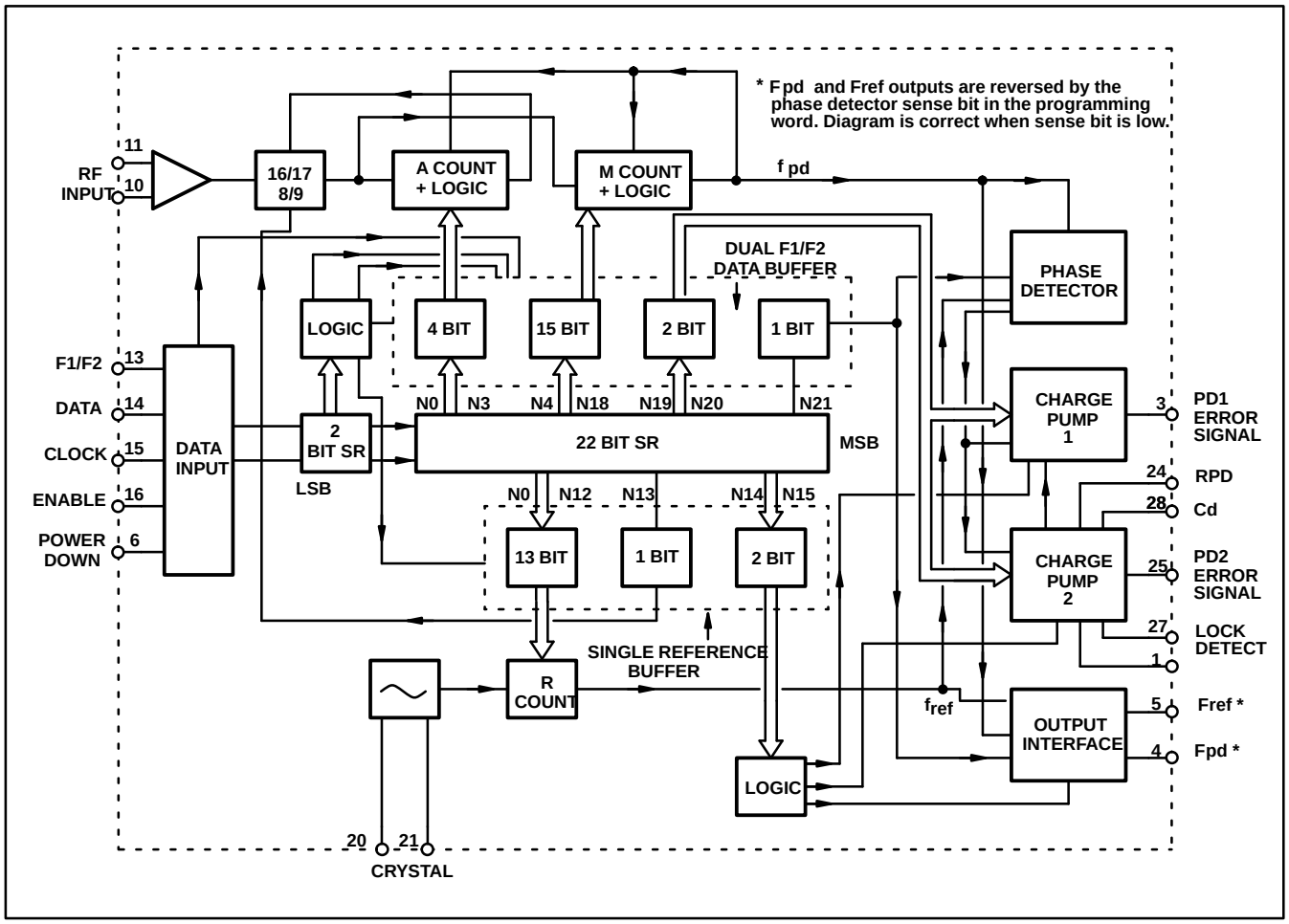


Fig. 2 SP8853 block diagram

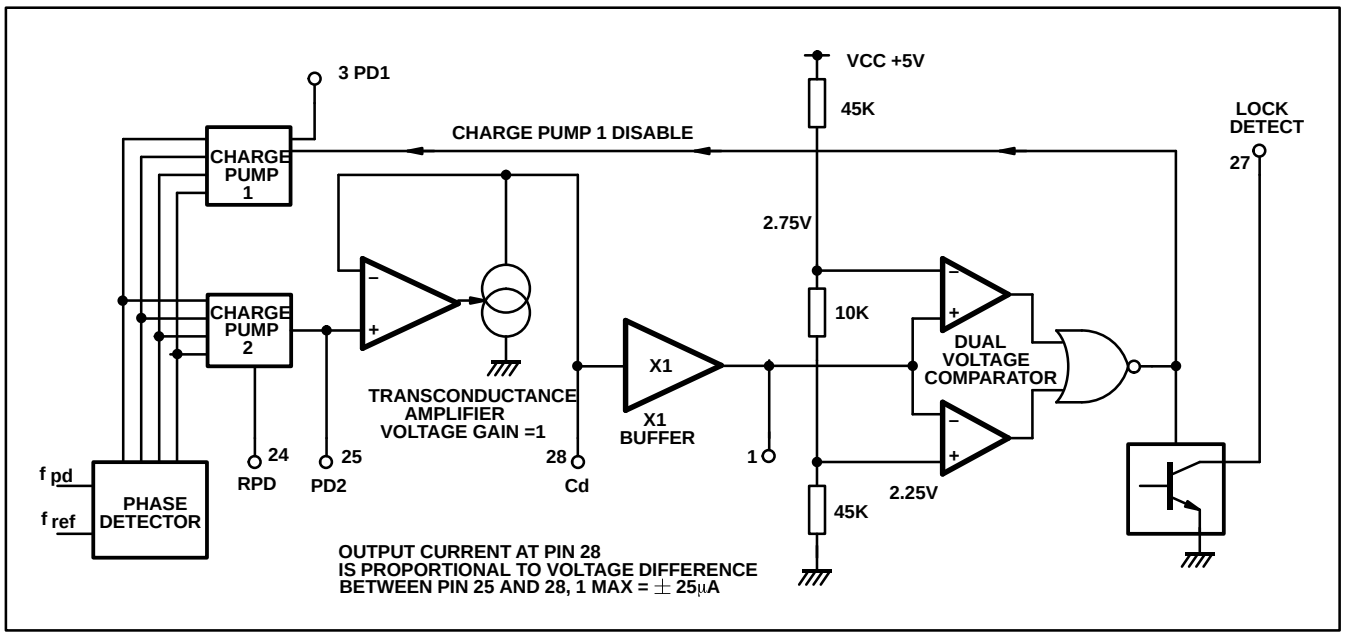


Fig. 3 Detailed block diagram of lock detect circuit

GEC PLESSEY
SEMICONDUCTORS

JANUARY 1995

D.S. 2352 2.3

SP8853A/B

1.3/1.5GHz PROFESSIONAL SYNTHESISER

(Supersedes the Edition in May 1991 Professional IC Handbook)

The SP8853 is a low power single chip synthesiser intended for professional radio applications, and contains all the elements (apart from the loop amplifier) to fabricate a PLL frequency synthesis loop.

The device is serially programmable by a three wire data highway and contains three independent buffers to store one reference divider word and two local oscillator divider words. A digital comparator, with two charge pumps, programmable in phase and gain are provided to improve lock up performance. The preset tandem operation of the charge pumps can be overwritten or the comparison frequencies switched to output ports under control of the divider word. The dual modulus ratio and so operating range is also programmable through the same word.

A power down mode is incorporated as a battery economy feature.

The part is specified to 1.5GHz at +85°C and to 1.3GHz at +125°C in the DG package. In the HC package the part is specified to 1.3GHz at +85°C and +125°C.

FEATURES

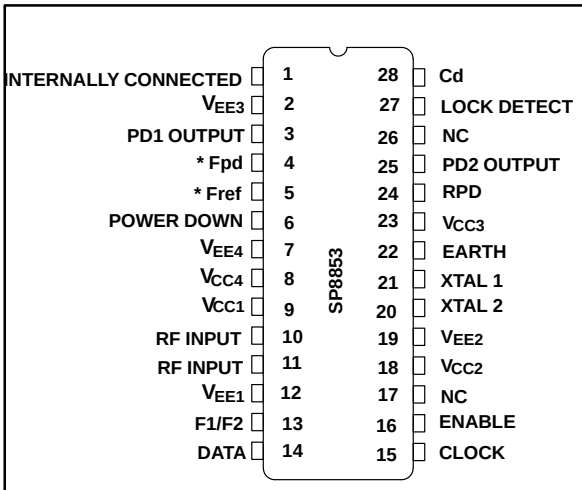
- Improved Digital Phase Detector to Eliminate ''Dead Band'' Effects
- Low Operating Power, Typically 175mW
- 1.5GHz Operating Frequency (DG package)
- Complete Phase Locked Loop
- High Input Sensitivity
- Programmed through Three Wire Data Bus
- Wide Range of Reference Division Ratios
- Local Storage for Two Frequency Words giving Rapid Frequency Toggling
- Programmable Phase Detector Gain
- Power Down Mode

ABSOLUTE MAXIMUM RATINGS

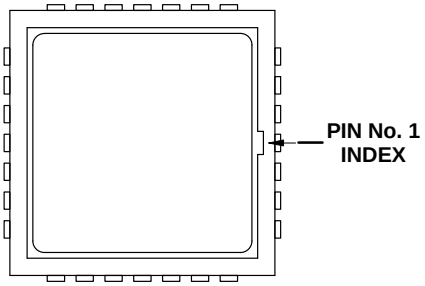
Supply voltage	–0.3V to 7V
Storage temperature	–55°C to + 150°C
Prescaler input voltage	2.5V p–p

ORDERING INFORMATION

SP8853/A/DG Military temperature range
SP8853/B/DG Industrial temperature range
SP8853/AC/DG Mil Std 883
SP8853/A/HC Military temperature range
SP8853/B/HC Industrial temperature range
SP8853/AC/HC Mil Std 883



DG28



HC28

1	IC	15	CLOCK
2	VEE3	16	ENABLE
3	PD1 OUTPUT	17	NC
4	* Fpd	18	VCC2
5	* Fref	19	VEE2
6	POWER DOWN	20	XTAL 2
7	VEE4	21	XTAL 1
8	VCC4	22	EARTH
9	VCC1	23	VCC3
10	RF INPUT	24	RPD
11	RF INPUT	25	PD2 OUTPUT
12	VEE1	26	NC
13	F1/F2	27	LOCK DETECT
14	DATA	28	Cd

* Fpd and Fref outputs are reversed by the phase detector sense bit in the programming word. Diagram above is correct when sense bit is low.

VCC1, VEE1 – Preamp and Prescaler
VCC2, VEE2 – Oscillator Supplies
VCC3, VEE3 – Charge Pump 2 Supplies
VCC4, VEE4 – ECL Supplies.

Fig. 1 Pin connections – top view