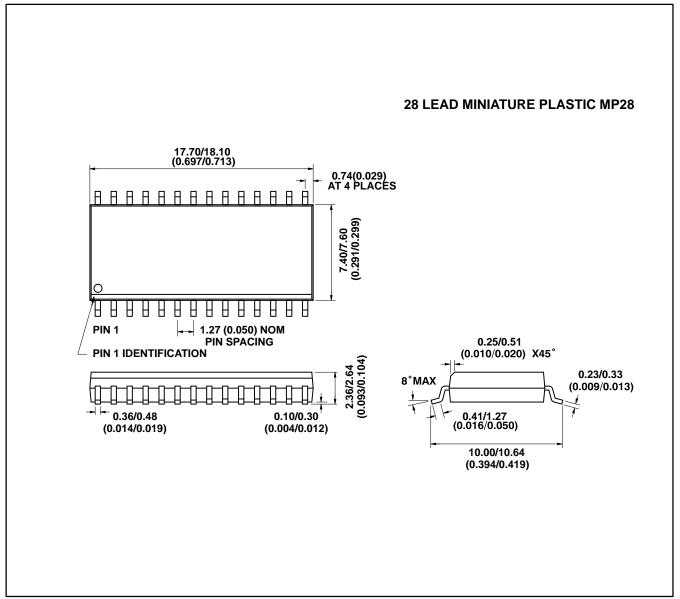
## SP8402

## PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information please contact your local Customer Service Centre.





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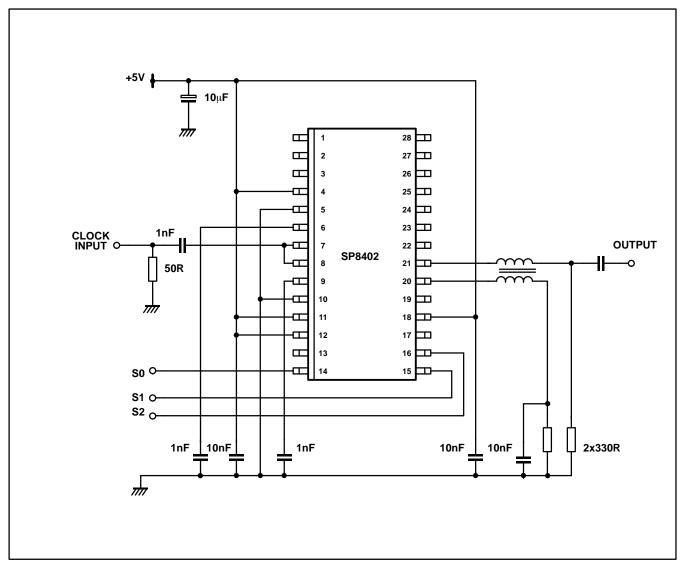


Fig. 6 Typical application – outputs combined in balun

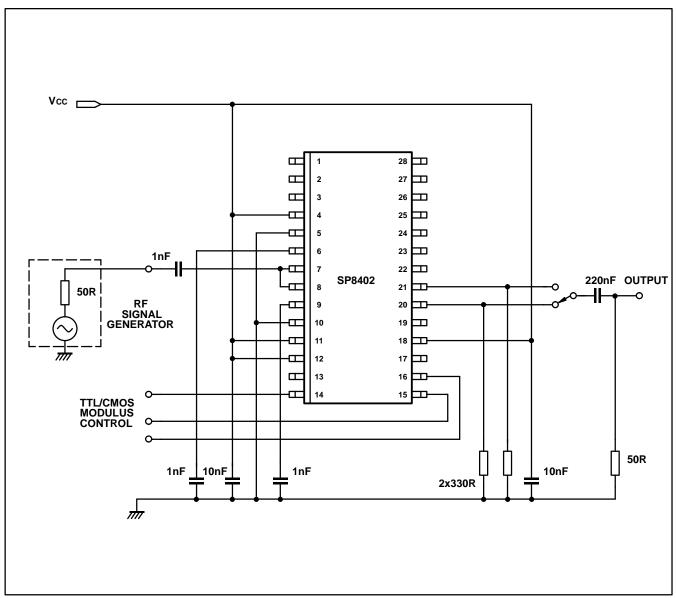


Fig. 5 Test circuit

## SP8402

**ELECTRICAL CHARACTERISTICS**Guaranteed over: Supply Voltage  $V_{CC}$  = +4.75V to +5.25V Temperature  $T_{amb}$  = -10°C to +75°C Tested at +4.75V and +5.25V at  $T_{amb}$  = +25°C

Characteristics	Pin	Value				
		Min	Тур	Max	Units	Conditions
Supply current	4,11,12, 18	82	92	102	mA	Outputs loaded with 330R See Fig.5
Output voltage swing	20,21	320	410		mV	p-p @ 1.4GHz input ÷ 256 mode outputs loaded with 330R See Fig. 5
Input sensitivity 200MHz to 1.4GHz	7,8			140 (-4)	mV dBm	RMS Sine wave into 50 Ohms (dBm equivalent) See Fig. 3
DATA INPUTS						
Logic high voltage		2.2			V	
Logic low voltage				0.8	V	
Input current				180	μΑ	5V Data input voltage

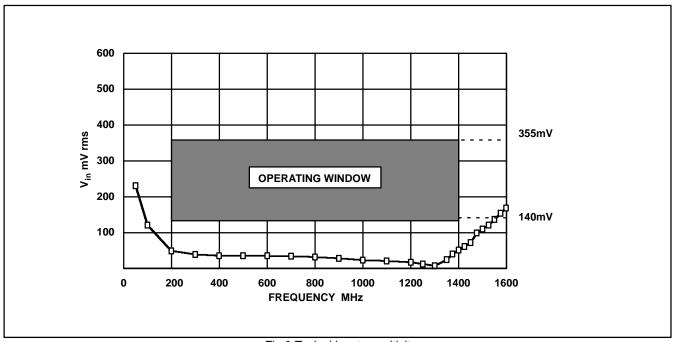


Fig.3 Typical input sensitivity

S0	S1	S2	DIVISION RATIO
L	L	L	2
Н	L	L	4
L	Н	L	8
Н	Н	L	16
L	L	Н	32
Н	L	Н	64
L	Н	Н	128
Н	Н	Н	256

Fig. 4 Truth table



# **SP8402**

## VERY LOW PHASE NOISE DIVIDE BY 2N

The SP8402 is a very low phase noise divider which divides by powers of two. The S0, S1, S2 data inputs select the division ratio in the range  $2^1$  to  $2^8$ . Special circuits techniques have been used to reduce the phase noise considerably below that produced by standard dividers. The data inputs are CMOS or TTL compatible.

The SP8402 is packaged in a 28 pin plastic SO package to be compatible with the SP8400 and SP8401 devices.

## **FEATURES**

- Very low Phase Noise (Typically –155 to 160dBc/Hz at 1kHz offset)
- Supply Voltage 5V

## **ABSOLUTE MAXIMUM RATINGS**

## **ORDERING INFORMATION**

SP8402 KG MPES (Commercial Grade)

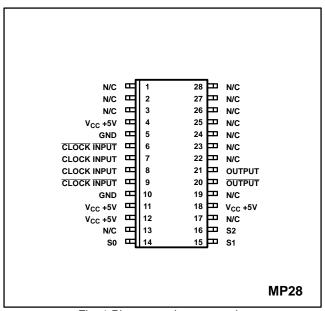


Fig. 1 Pin connections - top view

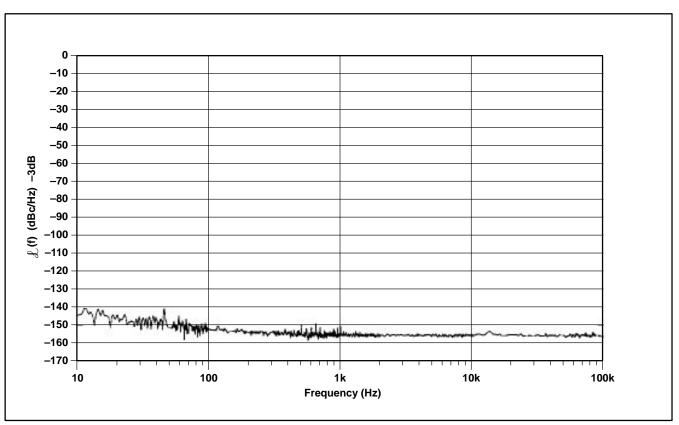


Fig. 2. Typical single sideband phase noise measured at 768MHz