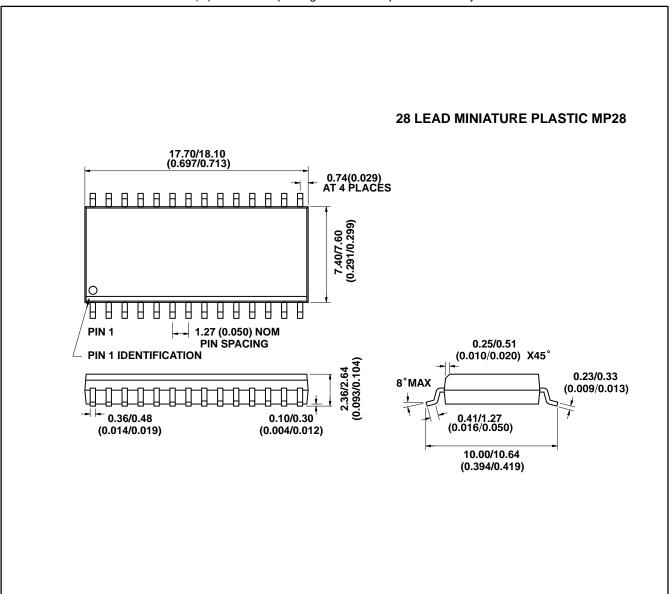
PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information please contact your local Customer Service Centre.





HEADQUARTERS OPERATIONS GEC PLESSEY SEMICONDUCTORS Cheney Manor, Swindon, Wiltshire SN2 2QW, United Kingdom. Tel: (0793) 518000 Fax: (0793) 518411

GEC PLESSEY SEMICONDUCTORS

P.O. Box 660017 1500 Green Hills Road, Scotts Valley, California 95066-0017, United States of America. Tel: (408) 438 2900 Fax: (408) 438 5576

CUSTOMER SERVICE CENTRES

- FRANCE & BENELUX Les Ulis Cedex Tel: (1) 64 46 23 45 Fax: (1) 64 46 06 07
- **GERMANY** Munich Tel: (089) 3609 06 0 Fax: (089) 3609 06 55 **ITALY** Milan Tel: (02) 66040867 Fax: (02) 66040993
- **JAPAN** Tokyo Tel: (03) 3296–0281 Fax: (03) 3296–0228 **NORTH AMERICA** Scotts Valley, USA Tel: (408) 438 2900 Fax: (408) 438 7023

- **SOUTH EAST ASIA** Singapore Tel: (65) 3827708 Fax: (65) 3828872 **SWEDEN** Stockholm Tel: 46 8 7029770 Fax: 46 8 6404736 **UK, EIRE, DENMARK, FINLAND & NORWAY**

Swindon Tel: (0793) 518510 Fax: (0793) 518582 These are supported by Agents and Distributors in major countries world—wide.

© GEC Plessey Semiconductors 1993 Publication No. D.S. 3739 Issue No. 2.1 April 1994

This publication is issued to provide outline information only, which (unless agreed by the Company in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. The Company reserves the right to alter without notice the specification, design, price of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication of data used is up to date and has not been superseded. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to the Company's conditions of sale, which are available on request.

Available division ratio

All division ratios of 64 to 4103 (Definition 1) will return the divider to the same internal state at the end of the count and hence these are the only divisional ratios to be used for fractional—N synthesiser application.

All division ratios of 56 to 4103 are available for general division purposes. Additional division ratios available for general division are:—

8,9 16, 17, 18 24, 25, 26, 27 32, 33, 34, 35, 36 40, 41, 42, 43, 44, 45 48, 49, 50, 51, 52, 53, 54

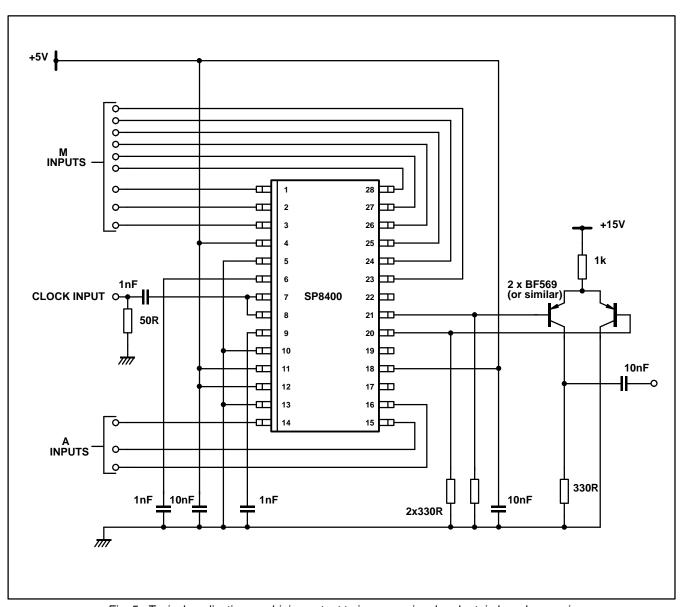


Fig. 5a Typical application combining output to increase signal and retain low phase noise

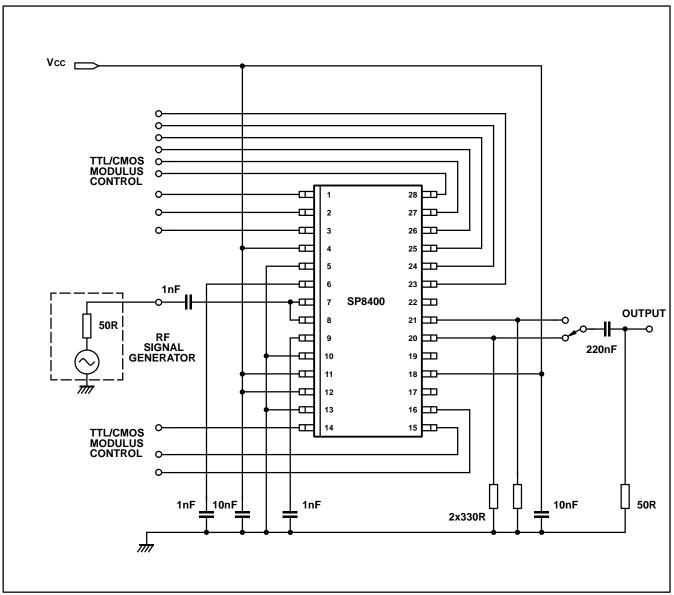


Fig. 4 Test circuit

APPLICATIONS INFORMATION

Circuit description, synthesiser divider

The divider is based on a divide by 8/9 modulus prescaler, and a 12 stage control counter. This gives minimum fractional – N division ratio of 64 (56 for general division), and a maximum division ratio of 4103. The inputs to the control counter are TTL/CMOS compatible. There is a fixed offset of 8 between the number on the data lines and the actual division ratio.

The output is one transition only per divide cycle. This eliminates the problem of where to put the redundant edge when the divider is used in a fractional–N system, and also avoids the problem of how to define the output pulse width. This means that the overall division ratio conventionally defined in terms of the rate of edges of the same polarity is twice the selected division ratio.

Equations for division

The M and A data inputs form a 12 bit number with A0 being the least significant bit and M8 being the most significant bit.

Definition 1: Division ratio – (input frequency to output edges, positive or negative).

= Number loaded + 8

Definition 2: Division ratio – (input frequency to output frequency).

= (Number loaded + 8) x 2

ELECTRICAL CHARACTERISTICSGuaranteed over: Supply Voltage V_{CC} = +4.75V to +5.25V Temperature T_{amb} = -10°C to +75°C Tested at +4.75V and +5.25V at T_{amb} = +25°C

Characteristics	Pin	Value				
		Min	Тур	Max	Units	Conditions
Supply current	4,11,12, 18	122	137	152	mA	Outputs loaded with 330R See Fig.4
Output voltage swing	20,21	320	410		mV	p-p @ 1.5GHz input ÷ 71 mode See Fig. 4
Input sensitivity 200MHz to 1.5GHz	7,8			140 (-4)	mV dBm	RMS Sine wave into 50 Ohms (dBm equivalent) See Fig. 3
DATA INPUTS						
Logic high voltage		2.2			V	
Logic low voltage				0.8	V	
Input current				180	μΑ	5V Data input voltage

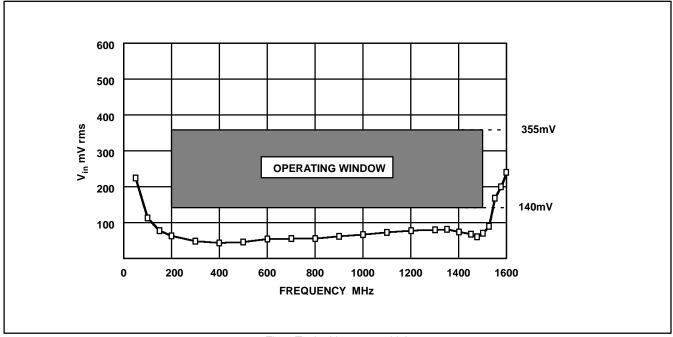


Fig.3 Typical input sensitivity



VERY LOW PHASE NOISE SYNTHESISER DIVIDER

The SP8400 is a very low phase noise programmable divider which is based on a divide by 8/9 dual modulus prescaler and a 12 stage control counter. This gives a minimum division ratio of 56 (64 for fractional - N synthesis applications), and a maximum division ratio of 4103. Special circuit techniques have been used to reduce the phase noise considerably below that produced by standard dividers. The data inputs are CMOS or TTL compatible.

The SP8400 is packaged in a 28 pin plastic SO package.

FEATURES

- Very low Phase Noise (Typically –156dBc/Hz at 1kHz offset)
- Supply Voltage 5V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.5V **Output Current** 20mA Storage Temperature Range -55°C to +125°C Maximum Clock Input Voltage 2.5V p-p

ORDERING INFORMATION

SP8400 KG MPES(Commercial Grade)

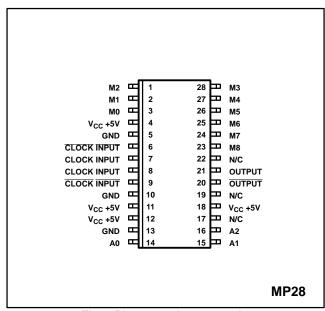


Fig. 1 Pin connections - top view

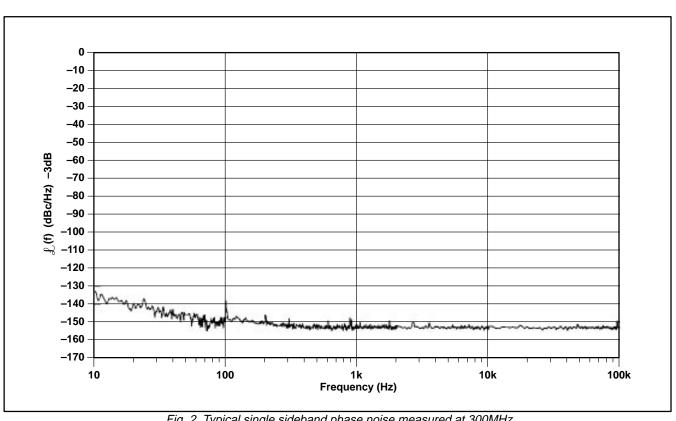


Fig. 2. Typical single sideband phase noise measured at 300MHz