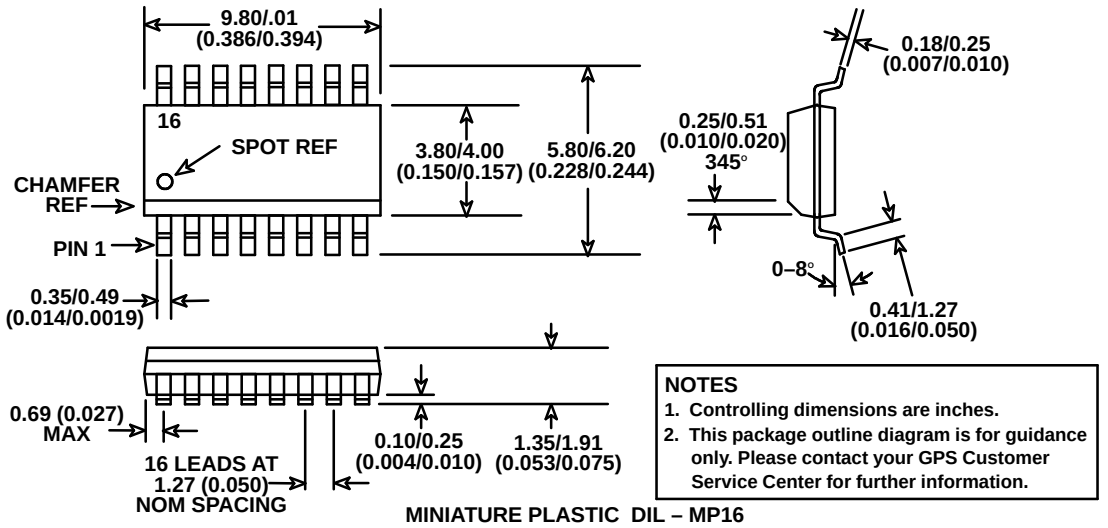
PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information please contact your local Customer Service Centre.



NOTES

1. **Controlling dimensions are inches.**
2. **This package outline diagram is for guidance only. Please contact your GPS Customer Service Center for further information.**

MINIATURE PLASTIC DIL – MP16

GEC PLESSEY SEMICONDUCTORS

HEADQUARTERS OPERATIONS

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P.O. Box 660017 1500 Green Hills Road,
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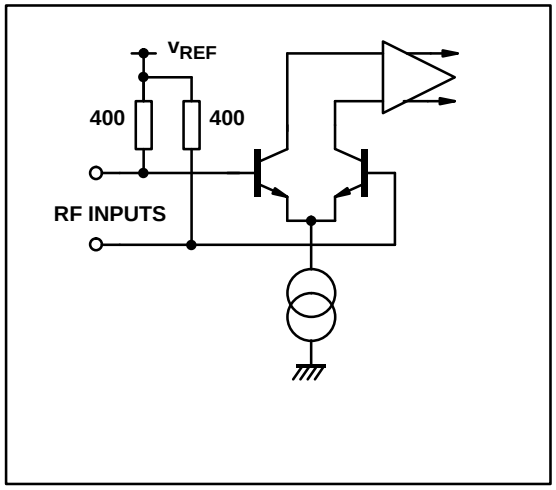
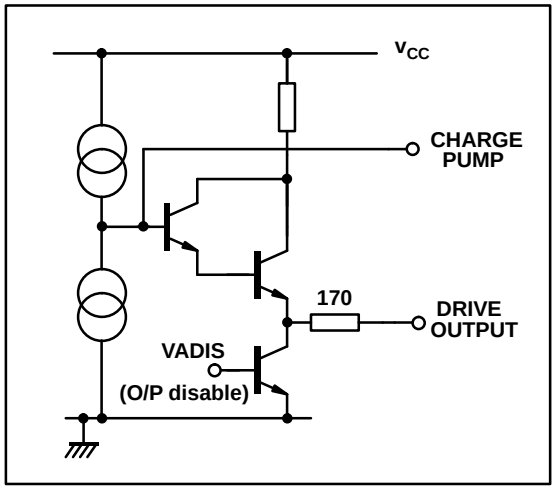
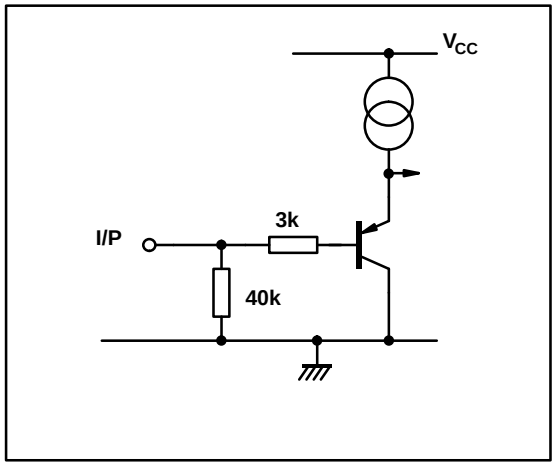


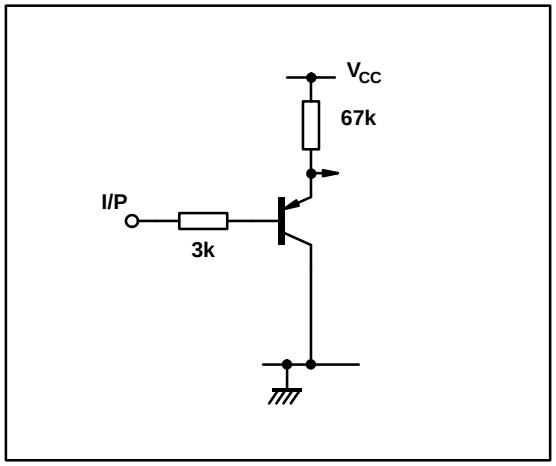
RF inputs



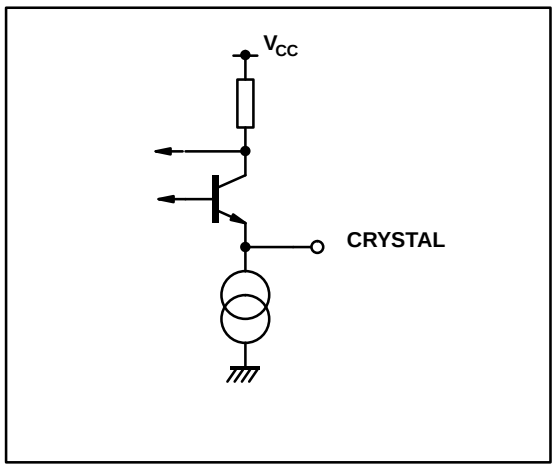
Loop amplifier



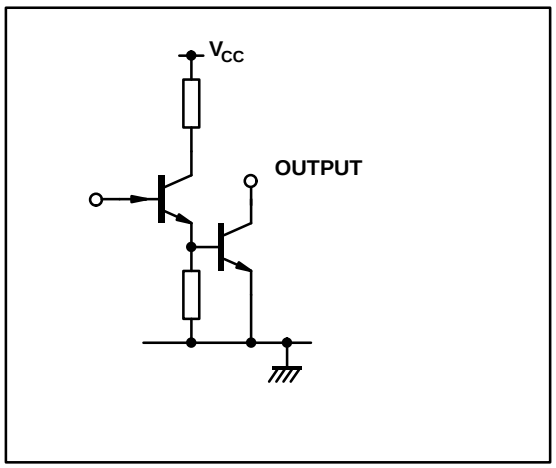
Div2 bypass input



Data, Clock, Enable inputs



Reference oscillator



Output ports P0–P3 and lock output

Fig. 7. Input/Output interface circuits

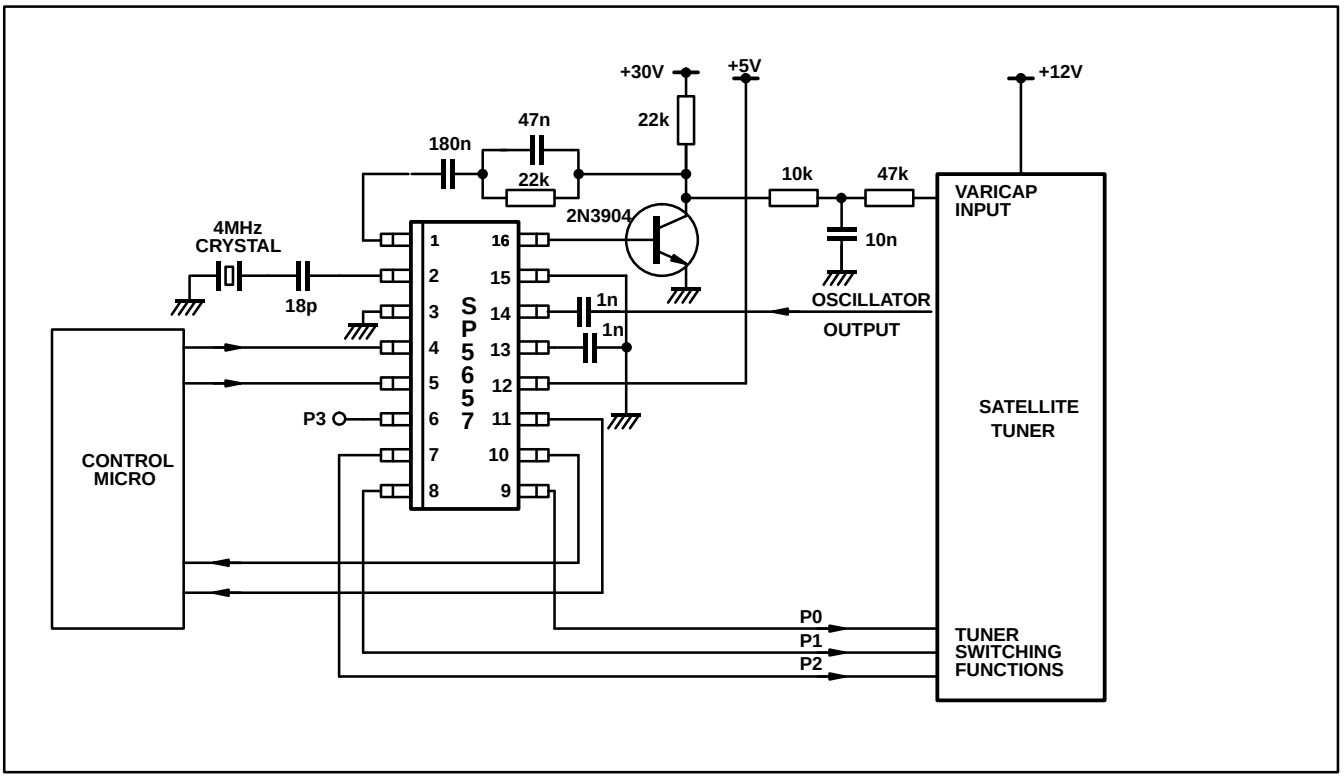


Fig. 5 Typical application

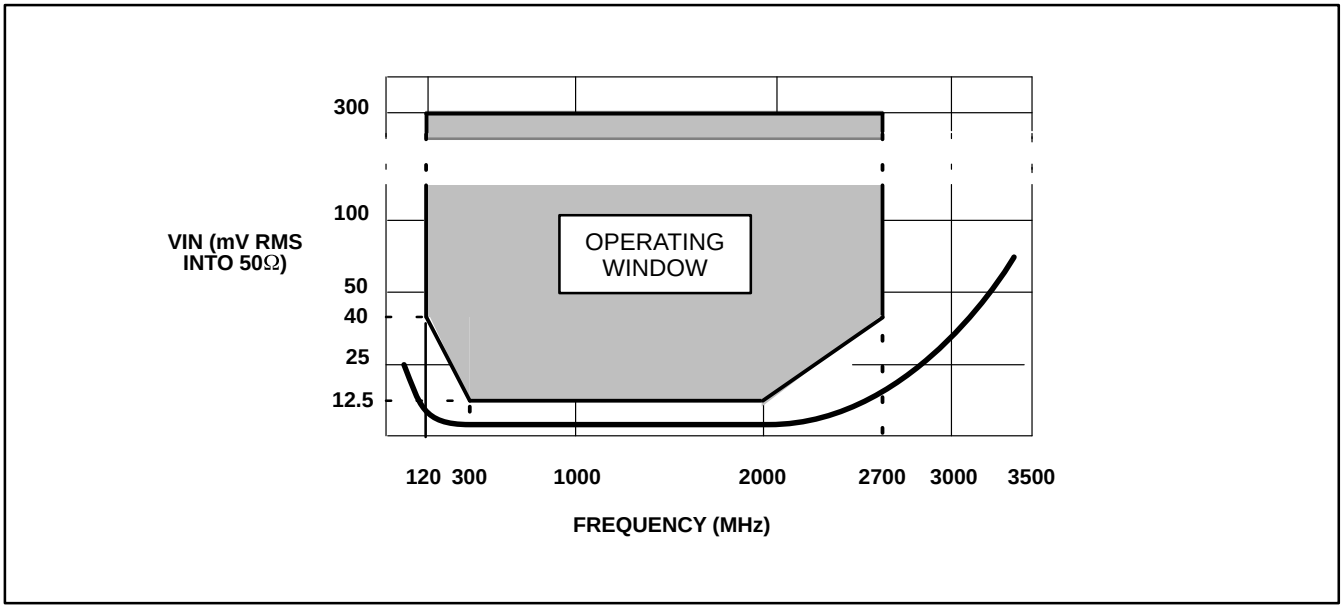


Fig. 6 Typical input sensitivity

MODE	DIV2 BYPASS INPUT (ACTIVE HIGH)	R0	R1	REFERENCE DIVIDER RATIO	LO FREQUENCY STEP SIZE (kHz)*	*MAX OPERATING FREQUENCY (GHz)
0	LOW	0	0	280	228.57	2.7
1	LOW	0	1	50	1280	2.7
2	LOW	1	0	500	128	2.0970
3	LOW	1	1	100	640	2.7
4	HIGH	0	0	140	457.14	2.7
5	HIGH	0	1	25	2560	2.7
6	HIGH	1	0	250	256	2.7
7	HIGH	1	1	50	1280	2.7

*When used with a 4MHz crystal

Table 1. Modes of operation

Test Mode	P1	P2	P3	Test Mode Description
0	0	0	0	Charge pump down 170μA
1	0	0	1	Charge pump up 170μA
2	1	0	0	Charge pump down 50μA
3	1	0	1	Charge pump up 50μA
4	d	1	0	F_{COMP} to P2; $F_{PD}/2$ to P3; Lock output switched to out of lock condition
5	d	1	1	Lock output switched to inlock condition

These test modes are invoked by taking the clock input below V_{EE}.
d=don‘t care

Table 2 Test mode options

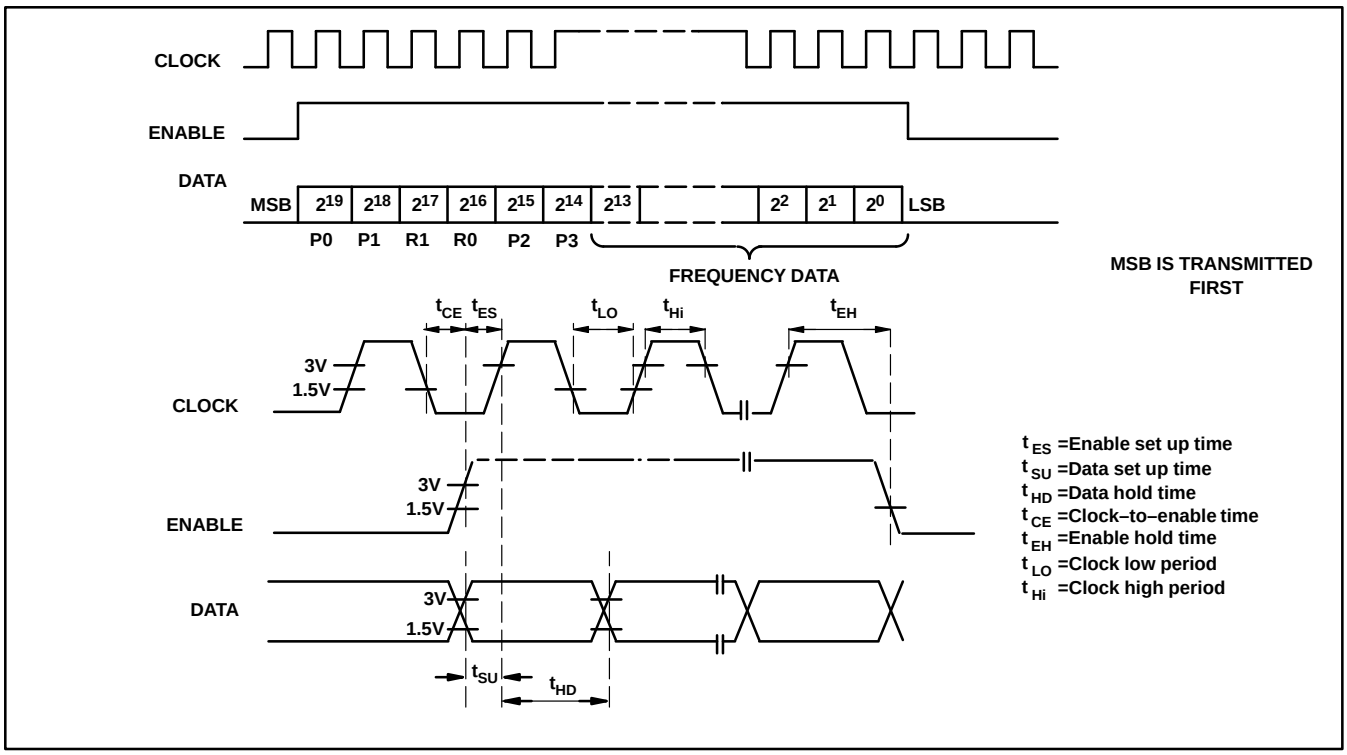


Fig. 4 Data format and timing

FUNCTIONAL DESCRIPTION

The SP5657 contains all the elements necessary, with the exception of reference crystal, loop filter and external high voltage transistor, to control a voltage controlled local oscillator, so forming a PLL frequency synthesised source.

The system is controlled by a microprocessor via a standard data, clock and enable three–wire bus. The data load consists of a single word, which contains frequency, reference ratio and port information, and is only transferred to the internal data shift register during an enable high period. The clock is disabled during low periods. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the enable, so giving improved fine tuning facility for digital AFC etc.

The frequency is set by first selecting the required mode of operation as detailed in Table 1, and then by loading the programmable divider with the required 14–bit divisor word. The output of this divider, F_{PD}, is fed to the phase comparator where it is compared in phase and frequency to the internally generated comparison frequency, F_{COMP}.

The comparison frequency F_{COMP} is obtained by dividing the output of the on–chip crystal controlled oscillator. The ratio of the reference divider is selected by the 'div2 bypass' input and bits R1, R0 of the programming data word as detailed in Table 1. The crystal frequency generally used is 4MHz, giving an F_{COMP} of 8kHz in mode 2, which when multiplied back up to the LO gives a minimum step size of 128kHz.

The programmable divider is preceded by an input RF preamplifier and high speed low radiation prescaler. The preamplifier is arranged to be self oscillating, so giving excellent input sensitivity. The input impedance and sensitivity are shown in Fig. 2 and 6 respectively.

The charge contains a lock detect circuit which generates a flag when the loop has attained lock. The 'out of lock' condition is indicated by a high impedance state.

The charge pump current is initially set to ±150μA. When the device attains frequency lock, the charge pump current is switched to ±50μA, so improving the local oscillator short term jitter.

The device also contains four general purpose open collector output ports P0–P3. These outputs are each capable of sinking at least 10mA, when the appropriate bits P0–P3 of the programming data, see Fig. 4 are set to a logic '1'.

PROGRAMMING COMPATIBILITY

With the 'div2 bypass' input low, modes 1–3, the SP5657 is programming and frequency step size compatible with the Sanyo LC7215/LC7215F/LC7215FM device combined with a ÷128 prescaler and gives step sizes of 1280kHz, 128kHz and 640kHz.

With the 'div2 bypass' input high, modes 5–7, the SP5657 is programming and frequency step size compatible with the Sanyo LC7215/LC7215F/LC7215FM device combined with a ÷256 prescaler and gives step sizes of 2560kHz, 256kHz and1280kHz.

For modes 0 and 4, programming compatibility, but not step size compatibility, is retained.

TEST FEATURES

Charge pump disable

The charge pump may be disabled by sourcing current from the data input, i.e. by forcing a negative input voltage.

Varactor line disable

The charge pump amplifier drive output may be disabled by sourcing current from the enable input, i.e. by forcing a negative voltage.

Device test mode

Further test modes can be invoked by sourcing current from the clock input, i.e. by forcing a negative input voltage. These test modes when invoked are determined by the data held in the P1, P2 and P3 internal registers as detailed in Table 2.

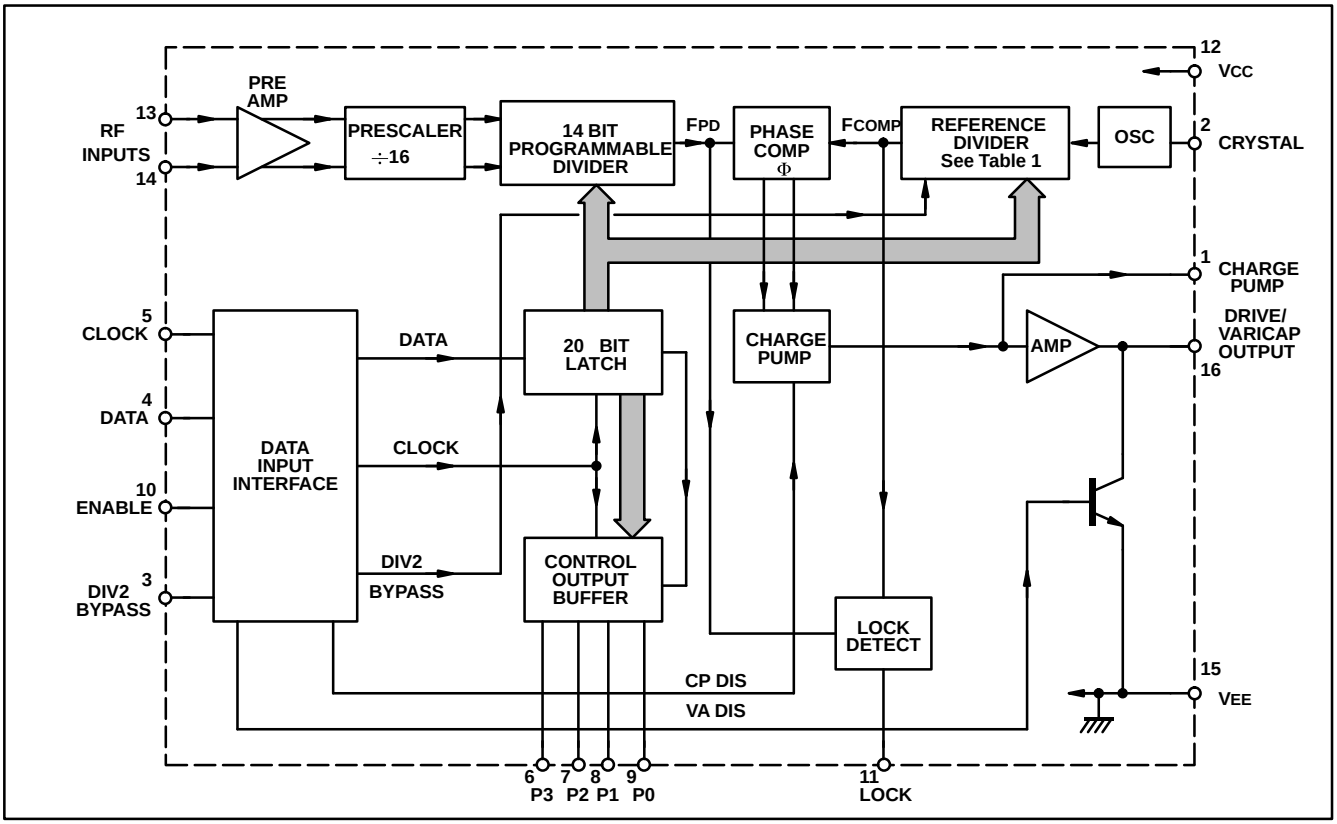


Fig. 3 Block diagram

ABSOLUTE MAXIMUM RATINGS (cont.)

All voltages are referred to V_{EE}=0V

Parameter	Pin	Value		Units	Conditions
		Min	Max		
Power consumption			220	mW	All ports off
ESD protection	All	4		kV	MIL STD 883 TM 3015

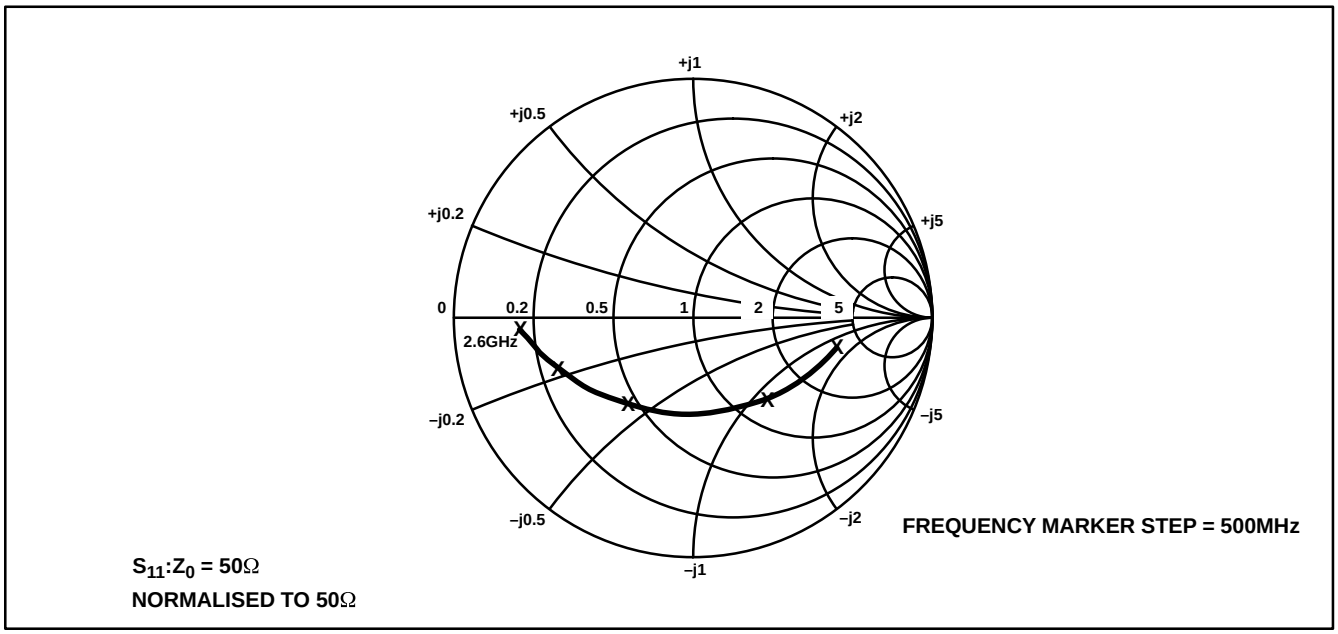


Fig. 2 Typical input impedance

ELECTRICAL CHARACTERISTICS

T_{amb}= –20°C to +80°C, V_{CC}=+4.5V to +5.5V. Reference frequency =4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Crystal Oscillator negative resistance		2	750			Ω	Includes temperature and process tolerances
Reference Crystal Frequency		2	4		8	MHz	
External Reference input Frequency		2	2		16	MHz	AC coupled sinewave
External Reference input Amplitude		2	400		1000	mV_{p-p}	AC coupled sinewave
Comparison Frequency (at phase detector)					160	kHz	
Ports and Lock output							
Sink Current		6–9, 11	10			mA	V_{out}=0.7V
Lock Leakage Current		11			10	µA	$V_{out}=V_{CC}$
Port Leakage Current		6–9			10	µA	V_{out}=13.2V
Varactor Drive Amp Disable		10	–50			µA	V_{pin} 10 < 0V. Current sourced from device
Charge Pump Disable		4	–50			µA	V_{pin} 4 < 0V. Current sourced from device
Test Mode Enable		5	–50			µA	V_{pin} 5 < 0V. Current sourced from device. See Table 2

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE}=0V

Parameter	Pin	Value		Units	Conditions
		Min	Max		
Supply voltage	12	–0.3	7	V	
Prescaler input voltage	13, 14		2.5	Vp–p	
Prescaler DC offset	13, 14	–0.3	V_{CC}+0.3	V	
Port voltage	6–9	–0.3	14	V	Port in off state
		–0.3	6	V	Port in on state
Total port output current	6–9		50	mA	
Loop amplifier DC offset	1, 16	–0.3	V_{CC}+0.3	V	
Crystal oscillator DC offset	2	–0.3	V_{CC}+0.3	V	
3–wire bus inputs	4, 5, 10	–0.7	6	V	
Div2 bypass input	3	–0.3	V_{CC}+0.3	V	
Lock output voltage	11	–0.3	V_{CC}+0.3	V	
Lock output current	11		15	mA	
Storage temperature		–55	+150	°C	
Junction temperature			+150	°C	
MP16 thermal resistance, chip–to–ambient			111	°C/W	
MP16 thermal resistance, chip–to–case			41	°C/W	

ELECTRICAL CHARACTERISTICS

T_{amb}= –20°C to +80°C, V_{CC}= +4.5V to +5.5V. Reference frequency =4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	12		30	40	mA	Typical applies to V_{CC} = 5V
Prescaler Input Voltage		13, 14	12.5		300	mV_{rms}	300MHz to 2GHz sinewave.
			40		300	mV_{rms}	120MHz & 2.7GHz See Fig. 6
Prescaler Input Impedance Input Capacitance		13, 14		50 2		Ω pF	
Data Clock and Enable							
High Level Input Voltage		4, 5, 10	3		V_{CC}	V	
Low Level Input Voltage		4, 5, 10	0		1.5	V	
High Level Input Current		4, 5, 10			10	µA	V_{IN}=5.5V V_{CC}=5.5V
Low Level Input Current		4, 5, 10			–10	µA	V_{IN}=0V V_{CC}=5.5V
Input Hysteresis		4, 5, 10		0.8		V	
Clock Rate		5			500	kHz	
Timing Information							
Data Setup Time	t_{SU}	4	300			ns	See Fig.4
Data Hold Time	t_{HD}	4	600			ns	See Fig. 4
Enable Setup time	t_{ES}	10	300			ns	See Fig. 4
Enable Hold Time	t_{EH}	10	600			ns	See Fig. 4
Clock–to–Enable Time	t_{CE}	10	300			ns	See Fig. 4
Clock Low Period	t_{LO}	5	600			ns	See Fig. 4
Clock High Period	t_{HI}	5	600			ns	See Fig. 4
Div2 Bypass							
High Level Input Voltage		3	3		V_{CC}	V	
Low Level Input Voltage		3	0		1.5	V	
High Level Input Current		3			300	µA	V_{IN}=5.5V V_{CC}=5.5V
Low Level Input Current		3			–10	µA	V_{IN}=0V V_{CC}=5.5V
Charge Pump Output Current		1		±150		µA	V pin 1 = 2.0V device ‘out of lock
Charge Pump Output Current		1		±50		µA	V pin 1=2.0V, device ‘locked’
Charge Pump Output Leakage Current		1			±5	nA	V pin 1 = 2.0V, charge pump disabled
Charge Pump Drive Output Current		16	1			mA	V pin 16 = 0.7V
Charge Pump Amplifier Gain				6400			Pin 18 Current = 100µA
Oscillator Temperature Stability					2	ppm/°C	
Oscillator Stability with Supply Voltage					2	ppm/V	
Recommended Crystal Series Resistance			10		200	Ω	“Parallel resonant crystal.” Figure quoted is under all conditions including start up.
Crystal Oscillator Drive Level		2		80		mV p–p	

GEC PLESSEY
SEMICONDUCTORS

FEBRUARY 1995
ADVANCE INFORMATION
D.S. 3932 1.7

SP5657

2.7GHz 3–WIRE BUS CONTROLLED SYNTHESISER

The SP5657 is a single chip frequency synthesiser designed for satellite TV tuning systems. The device when used with a satellite TV varicap tuner, forms a complete phase locked loop tuning system. The circuit consists of a divide–by–16 prescaler with its own preamplifier and a 14–bit programmable divider controlled by a serially loaded data register. Four independently programmable open collector outputs are included. The device has eight modes of operation, selected by the 'div2 bypass' input, and bits R1, R0 of the programming data. These modes are summarised in Table 1.

The comparison frequencies are obtained from a crystal controlled on–chip oscillator typically operating at 4MHz. The comparator has a charge pump output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

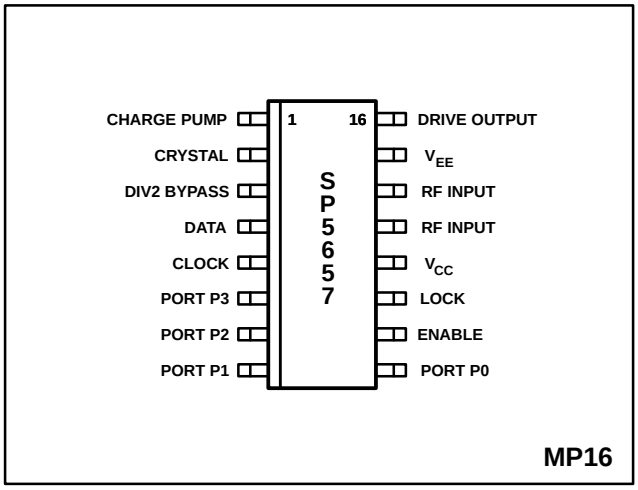


Fig. 1 Pin connections – top view

FEATURES

- Complete 2.7GHz Single Chip System
- High Sensitivity RF Inputs
- Low Power Consumption (5V 30mA)
- On chip oscillator with 1kΩ negative resistance
- On chip oscillator start–up circuit
- Programming Compatible with Sanyo LC7215, LC7215F, LC7215FM plus ÷128/256 prescaler #
- Pin Compatible with SP5054
- 8 Modes of operation with different step sizes, see Table 1
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- Charge Pump Disable
- Single Port 20–Bit Serial Data Entry
- Four Controllable Outputs
- ESD Protection †

See notes on programming compatibility

†Normal ESD handling procedures should be observed

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems
- Combined Satellite and Terrestrial tuners

ORDERING INFORMATION

SP5657/KG/MPAS (Tubes)
SP5657/KG/MPAD (Tape & Reel)