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SP5655

2.7GHz BI–DIRECTIONAL I²C BUS CONTROLLED SYNTHESISER

(Supersedes edition in 1995 Media IC Handbook)

The SP5655 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device contains 2 addressable current limited outputs and 4 addressable bi–directional open collector ports one of which is a 3 bit ADC. The information on these ports can be read via the I²C BUS. The device has one fixed I²C BUS address and 3 programmable addresses, programmed by applying a specific input voltage to one of the current limited outputs. This enables 2 or more synthesisers to be used in a system.

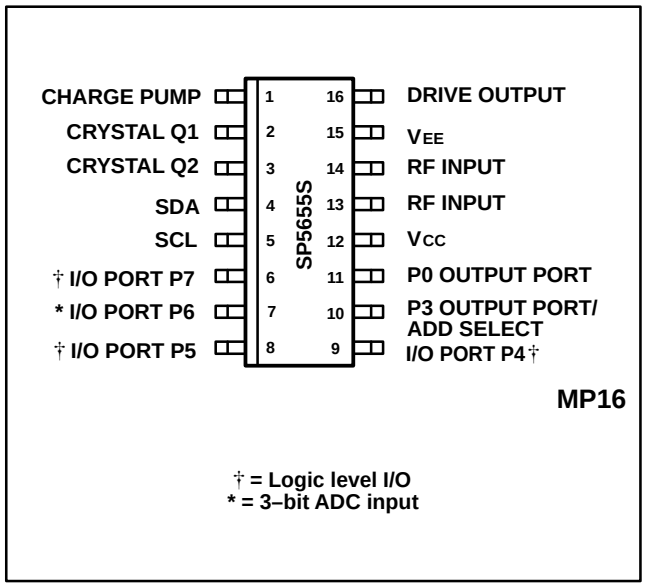


Fig. 1 Pin connections – top view

FEATURES

- Complete 2.7GHz Single chip System
- High Sensitivity RF Inputs
- Programmable via I²C Bus
- On Chip oscillator with 1kΩ negative resistance
- Low power consumption (5V 30mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 6 Controllable Outputs, 4 Bi–Directional
- 5 Level ADC
- Variable I²C BUS Address For Multi Tuner Applications
- ESD Protection *
- Switchable ÷512/1024 Reference Divider
- Pin and Function Compatible with SP5055S †

* Normal ESD handling procedures should be observed.

† The SP5055S does not have a switchable reference division ratio.

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

ORDERING INFORMATION

SP5655S/KG/MPAS (Tubes)
SP5655S/KG/MPAD (Tape and Reel)

ELECTRICAL CHARACTERISTICS

T_{amb}= –20°C to +80°C, V_{CC}=+4.5V to +5.5V. Reference frequency = 4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	12		30	40	mA	V_{CC} = 4.5V to 5.5V
Prescaler Input Voltage	13, 14	50		300	mV_{RMS}	120MHz to 2.7GHz sinewave See Fig. 5.
Prescaler Input Impedance Input Capacitance	13, 14		50 2		Ω pF	
SDA, SCL Input High Voltage Input Low Voltage Input High Current Input Low Current Leakage Current	4, 5 4, 5 4, 5 4, 5 4, 5	3 0		5.5 1.5 10 –10 10	V V µA µA µA	 Input Voltage = V_{CC} Input Voltage = 0V When V_{CC} = 0V
SDA Output Voltage	4			0.4	V	I_{sink} = 3mA
Charge Pump Current Low	1		±50		µA	Byte 4 Bit 2 = 0, Pin 1 = 2V
Charge Pump Current High	1		±170		µA	Byte 4 Bit 2 = 1, Pin 1 = 2V
Charge Pump Output Leakage Current	1			±5	nA	Byte 4 Bit 4 = 1, Pin 1 = 2V
Charge Pump Drive Output Current	16	500			µA	V_{pin} 16 = 0.7V
Charge Pump Amplifier Gain			6400			
Recommended Crystal series Resistance		10		200	Ω	“Parallel Resonant” crystal. Resistance specified is max under all conditions
Crystal Oscillator Drive Level			80		mVp–p	
Crystal Oscillator Negative Resistance	2	750	1000		Ω	
External Reference Input Frequency	2	2		8	MHz	AC coupled sinewave
External Reference Input amplitude	2	70		200	mVrms	AC coupled sinewave
Output Ports						
P0–P3 Sink Current	11 – 10	0.7	1	1.5	mA	V_{out} = 12V
P0–P3 Leakage Current	11 – 10			10	µA	V_{out} = 13.2V
P4–P7 Sink Current	9–6	10			mA	V_{out} = 0.7V
P4–P7 Leakage Current	9–6			10	µA	V_{out} = 13.2V
Input Ports						
P3 Input Current High	10			+10	µA	$V_{pin\ 10}$ = 13.2V
P3 Input Current Low	10			–10	µA	$V_{pin\ 10}$ = 0V
P4,P5,P7 Input Voltage Low	9,8,6			0.8	V	
P4,P5,P7 Input Voltage High	9,8,6	2.7			V	
P6 Input Current High	7			+10	µA	See Table 3 for ADC Levels
P6 Input Current Low	7			–10	µA	

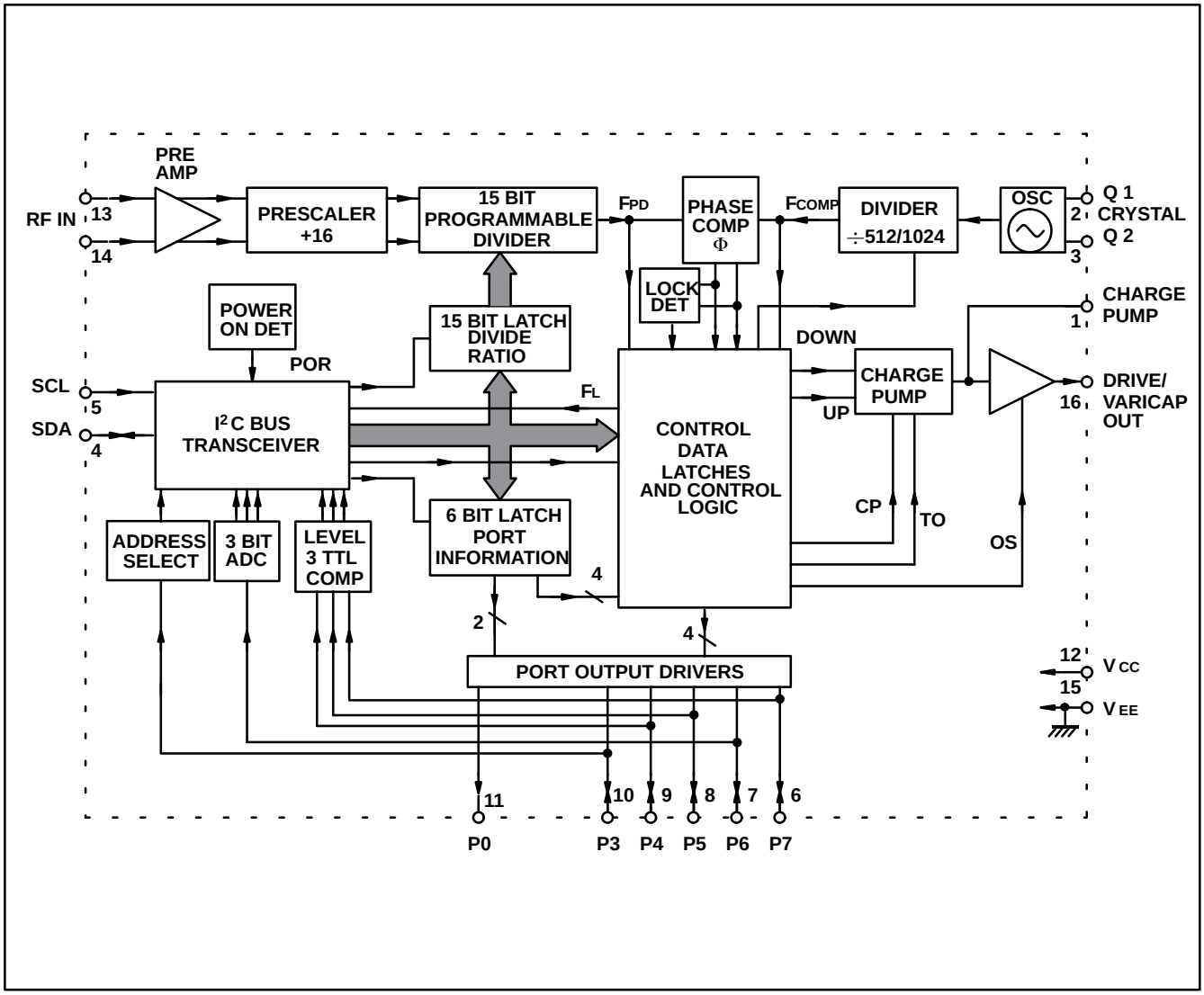


Fig 2. Block diagram

FUNCTIONAL DESCRIPTION

The SP5655 is programmed from an I^2C Bus. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I^2C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low and read mode if it is high. The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I^2C Bus system. Table 4 shows how the address is selected by applying a voltage to P3. When the device receives a correct address byte, it pulls the SDA line low during the acknowledge period, and during following acknowledge periods after further data bytes are programmed. When the device is programmed into the read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period, the device generates an internal STOP condition, which inhibits further reading.

WRITE MODE (Frequency Synthesis)

When the device is in write mode bytes 2+3 select the synthesised frequency, while bytes 4+5 control the output port states, charge pump, reference divider ratio and various test modes.

Once the correct address is received and acknowledged, the first bit of the next byte determines whether that byte is interpreted as byte 2 or 4; a logic 0 for frequency information and a logic 1 for control and output port information. When byte 2 is received the device always expects byte 3 next. Similarly, when byte 4 is received the device expects byte 5 next. Additional data bytes can be entered without the need to re–address the device until an I^2C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid–byte (e.g. by another device on the bus) then the previously programmed byte is maintained.

Frequency data from bytes 2 and 3 is stored in a 15–bit register and is used to control the division ratio of the 15–bit programmable divider. This is preceded by a divide–by–16 prescaler and amplifier to give excellent sensitivity at the local oscillator input, see Fig. 5. The input impedance is shown in Fig. 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 16 times the comparison frequency F_{COMP} .

When frequency data is entered, the phase comparator, via a charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phased locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2, or provided by an on–board crystal controlled oscillator. The comparison frequency F_{COMP} is derived from the reference frequency via the reference divider. The reference divider division ratio is switchable from 512 to 1024, and is controlled by bit 7 of byte 4 (TS0); a logic 1 for 512; a logic 0 for 1024. The SP5655 differs from the SP5055 in this respect, only 512 being available on the SP5055. Note, the comparison frequency is 7.8125kHz when a 4MHz reference is used, and divide by 512 is selected.

Bit 2 of byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for $\pm 170\mu A$ and a logic 0 for $\pm 50\mu A$ allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. When the device is 'frequency locked' the charge pump current is internally set to $\pm 50\mu A$ regardless of CP.

Bit 4 of byte 4 (T0) disables the charge pump when it is set to a logic 1.

Bit 8 of byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1.

Bit 3 of byte 4 (T1) enables various test modes when set high. These modes are selected by bits 5, 6, 7 of byte 4 (TS2, TS1, TS0) as detailed in Table 5. When T1 is set low, TS2, TS1 are assigned a 'don't care' condition, and TS0 selects the reference divider ratio as previously described.

Byte 5 programs the output ports P0, P3 to P7; a logic 0 for a high impedance output and a logic 1 for low impedance (on).

READ MODE

When the device is in read mode the status byte read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power–on reset indicator and is set to a logic 1 if the V_{CC} supply to the device has dropped below 3V (at 25°C), e.g. when the device is initially turned on. The POR is reset to 0 when the read sequence is terminated by a stop command. When POR is set high (at low V_{CC}), the programmed information is lost and the output ports are all set to high impedance.

Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked, and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2, I1, I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with TTL type voltage levels.

Bits 6, 7 and 8 (A2, A1, A0) combine to give the output of the 5 level ADC. The ADC can be used to feed AFC information to the microprocessor from the IF section of the receiver, as illustrated in the typical application circuit.

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6. The SP5655 is function and pin equivalent to the SP5055 device apart from the switchable reference divider, and has much lower power dissipation, improved RF sensitivity and better ESD performance.

MSB								LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	Byte 1
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	Byte 2
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	Byte 3
CONTROL DATA	1	CP	T1	T0	TS2	TS1	TS0	OS	A	Byte 4
IO PORT CONTROL DATA	P7	P6	P5	P4	P3	X	X	P0	A	Byte 5

Table 1 Write data format (MSB is transmitted first)

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	Byte 1
STATUS BYTE	POR	FL	I2	I1	I0	A2	A1	A0	A	Byte 2

Table 2 Read data format (MSB is transmitted first)

A:	Acknowledge bit
MA1, MA0:	Variable address bits (see Table 4)
CP:	Charge pump current select
T1:	Test mode enable
T0:	Charge pump disable
TS2, TS1, TS0:	Operation mode control bits (see Table 5)
OS:	Varactor drive Output disable Switch
P7,P6,P5,P4,P3,P0:	Control output states
POR:	Power On Reset indicator
FL:	Phase Lock detect Flag
I2, I1, I0:	Digital information from Ports P7, P5 and P4, respectively
A2, A1, A0:	5 Level ADC data from P6 (see Table 3)
X :	Don't care

A2	A1	A0	Voltage input to P6
1	0	0	$0.6V_{CC}$ to 13.2V
0	1	1	$0.45V_{CC}$ to $0.6V_{CC}$
0	1	0	$0.3V_{CC}$ to $0.45V_{CC}$
0	0	1	$0.15V_{CC}$ to $0.3V_{CC}$
0	0	0	0 to $0.15V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	$0 – 0.2V_{CC}$
0	1	ALWAYS VALID
1	0	$0.3V_{CC} – 0.7V_{CC}$
1	1	$0.8V_{CC} – 13.2V$

Table 4 Address selection

T1	TS2	TS1	TS0	OPERATION MODE DESCRIPTION
0	X	X	0	Normal operation, test modes disabled, reference divider ratio=1024
0	X	X	1	Normal operation, test modes disabled, reference divider ratio=512
1	0	0	X	Charge pump source (down). Status byte bit FL set to 0
1	0	1	X	Charge pump sink (up). Status byte bit FL set to 1
1	1	0	0	Ports P4,P5,P6,P7 set to state X
1	1	0	1	Port P7=F_{PD}/2; P4,P5,P6 set to state X
1	1	1	X	Port P7=F_{PD}; P6=F_{COMP}; P4, P5 set to state X

X=don't care

(For further details of test modes see Table 6).

Table 5 Operation modes

Fig. 3 Data formats

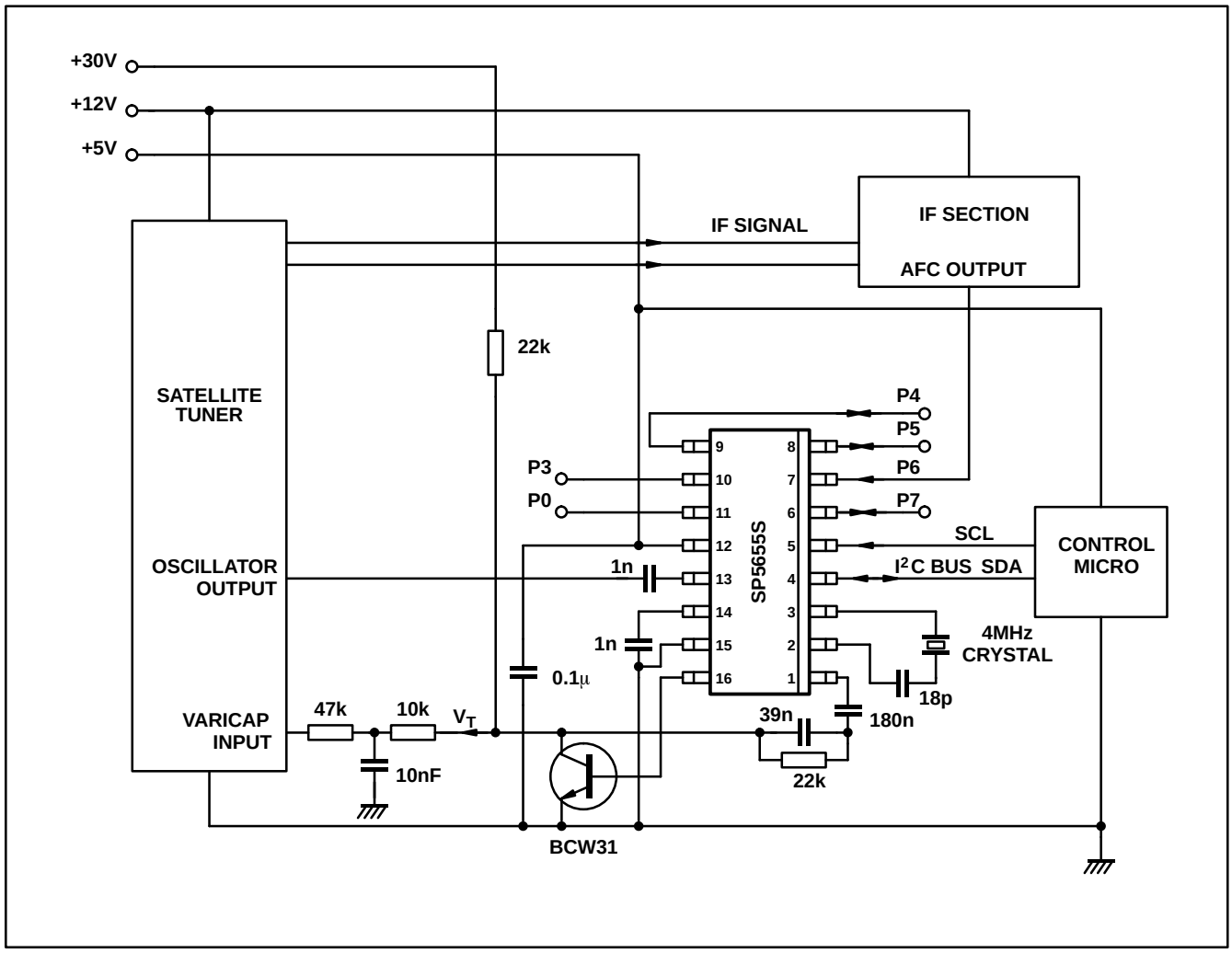


Fig. 4 Typical application

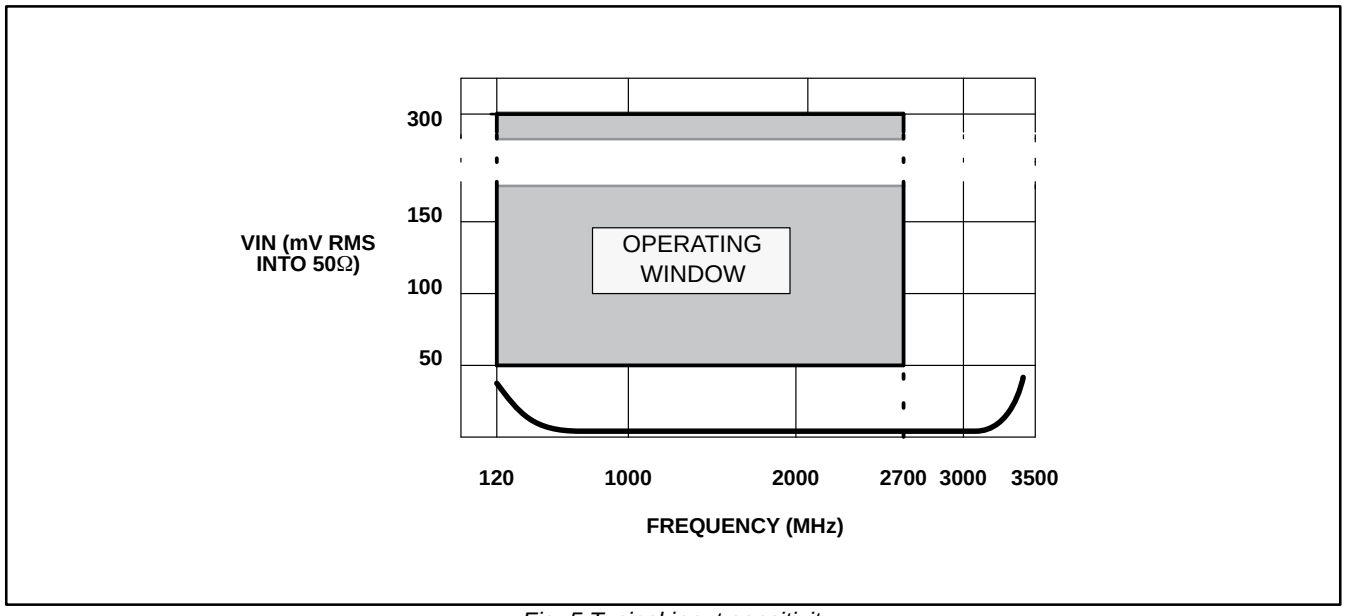
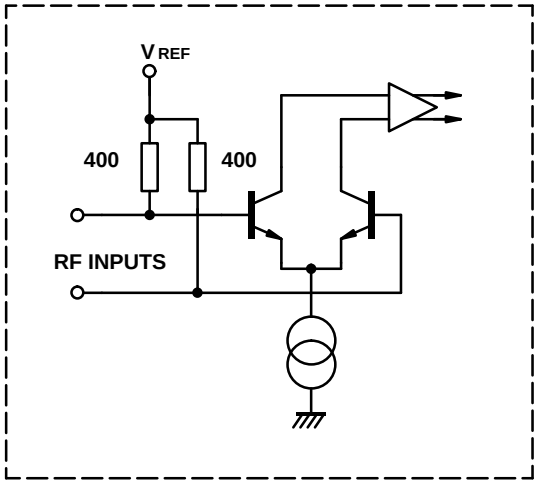
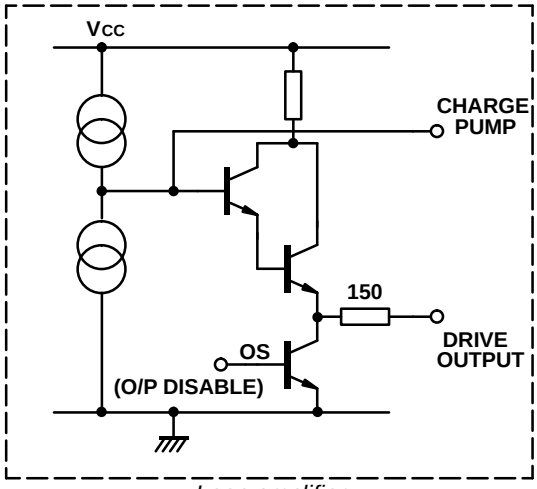


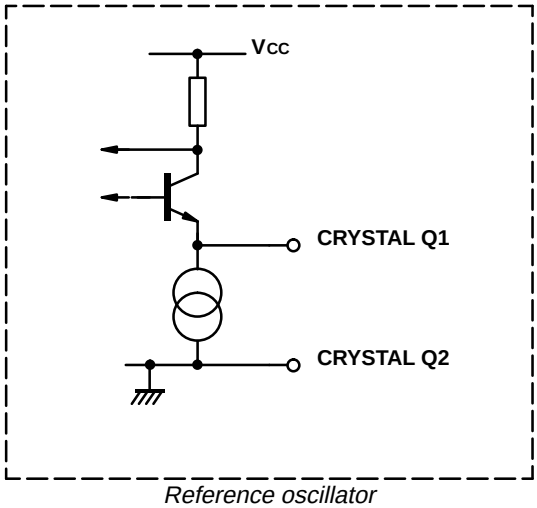
Fig. 5 Typical input sensitivity



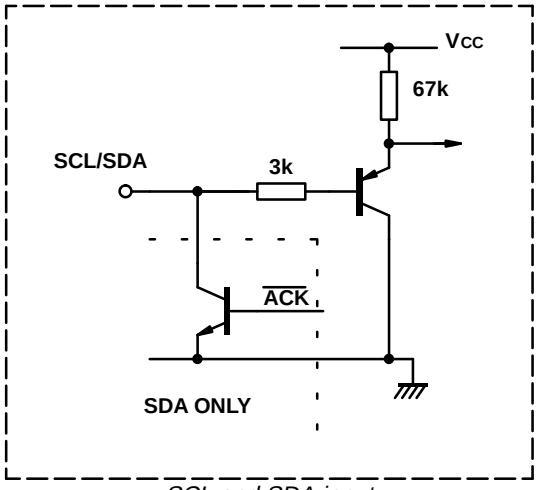
RF input



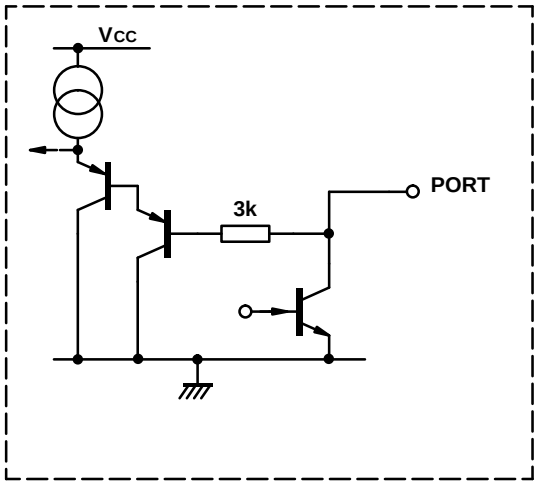
Loop amplifier



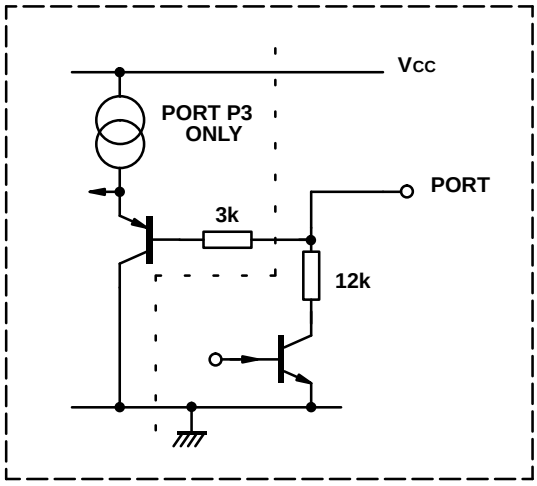
Reference oscillator



SCL and SDA input



Ports P7 – P4



Ports P0 – P3

Fig. 6 Input/output interface circuits

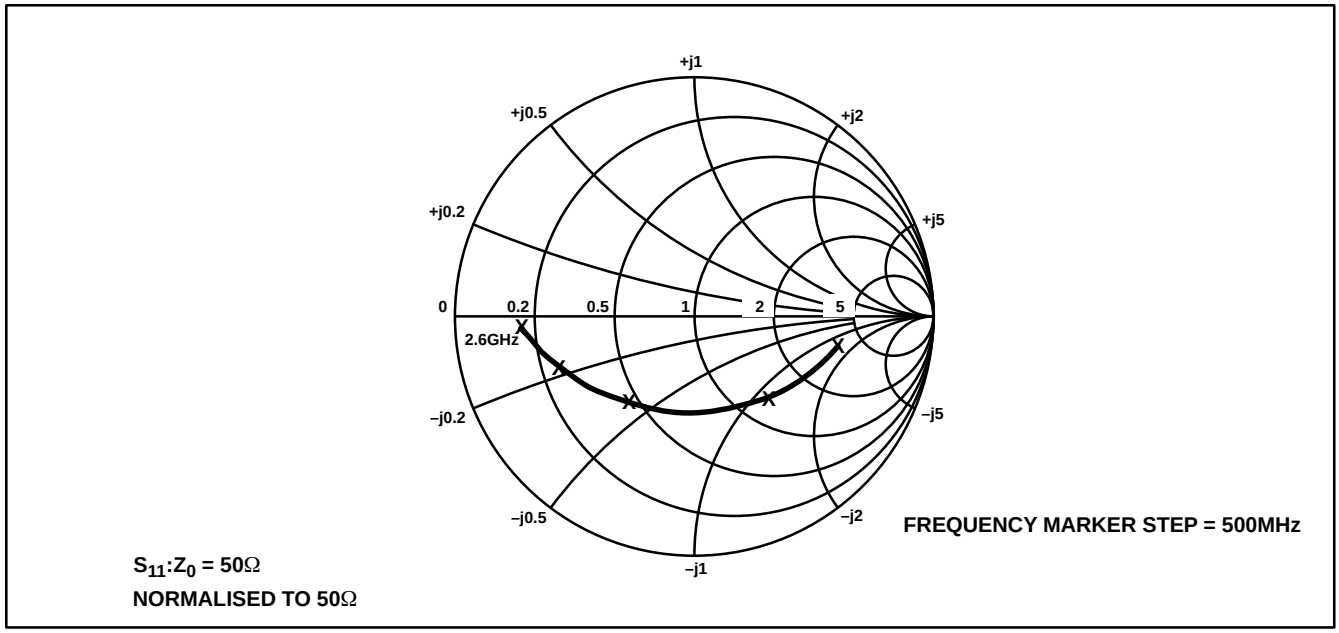


Fig. 7 Typical input impedance

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V.

Parameter	Pin	Value		Units	Conditions
		Min	Max		
Supply voltage	12	– 0.3	7	V	
RF input voltage	13, 14		2.5	Vp–p	
Port voltage	6–11 6–9 10, 11	– 0.3 – 0.3 – 0.3	14 6 14	V V V	Port in off state Port in on state Port in on state
Total port output current	6–11		50	mA	
RF input DC offset	13, 14	– 0.3	V_{CC} +0.3	V	
Charge Pump DC offset	1	– 0.3	V_{CC}+0.3	V	
Drive DC offset	16	– 0.3	V_{CC}+0.3	V	
Crystal oscillator DC offset	2	– 0.3	V_{CC}+0.3	V	
SDA,SCL input voltage	4, 5	– 0.3	6	V	
Storage temperature		– 55	+150	°C	
Junction temperature			+150	°C	
MP16 thermal resistance, chip–to–ambient			111	°C/W	
MP16 thermal resistance, chip–to–case			41	°C/W	
Power consumption at 5.5V			220	mW	All ports off
ESD protection	ALL	4		kV	MIL STD 883C TM 3015

APPLICATION NOTES

A generic set of application notes AN168 for designing with synthesisers such as the SP5655 has been written. This covers aspects such as loop filter design, decoupling and I^2C bus radiation problems.

This application note is featured in the Media October 1995 IC Handbook. A generic test/demo board has been produced which can be used for the SP5655. A circuit diagram and layout for the board is shown in Figs. 8 and 9.

The board can be used for the following purposes:

(A) Measuring RF sensitivity performance.
(B) Indicating port function.
(C) Synthesising a voltage controlled oscillator.
(D) Testing of external reference sources.

The programming codes relevant to these tests are shown in Table 6.

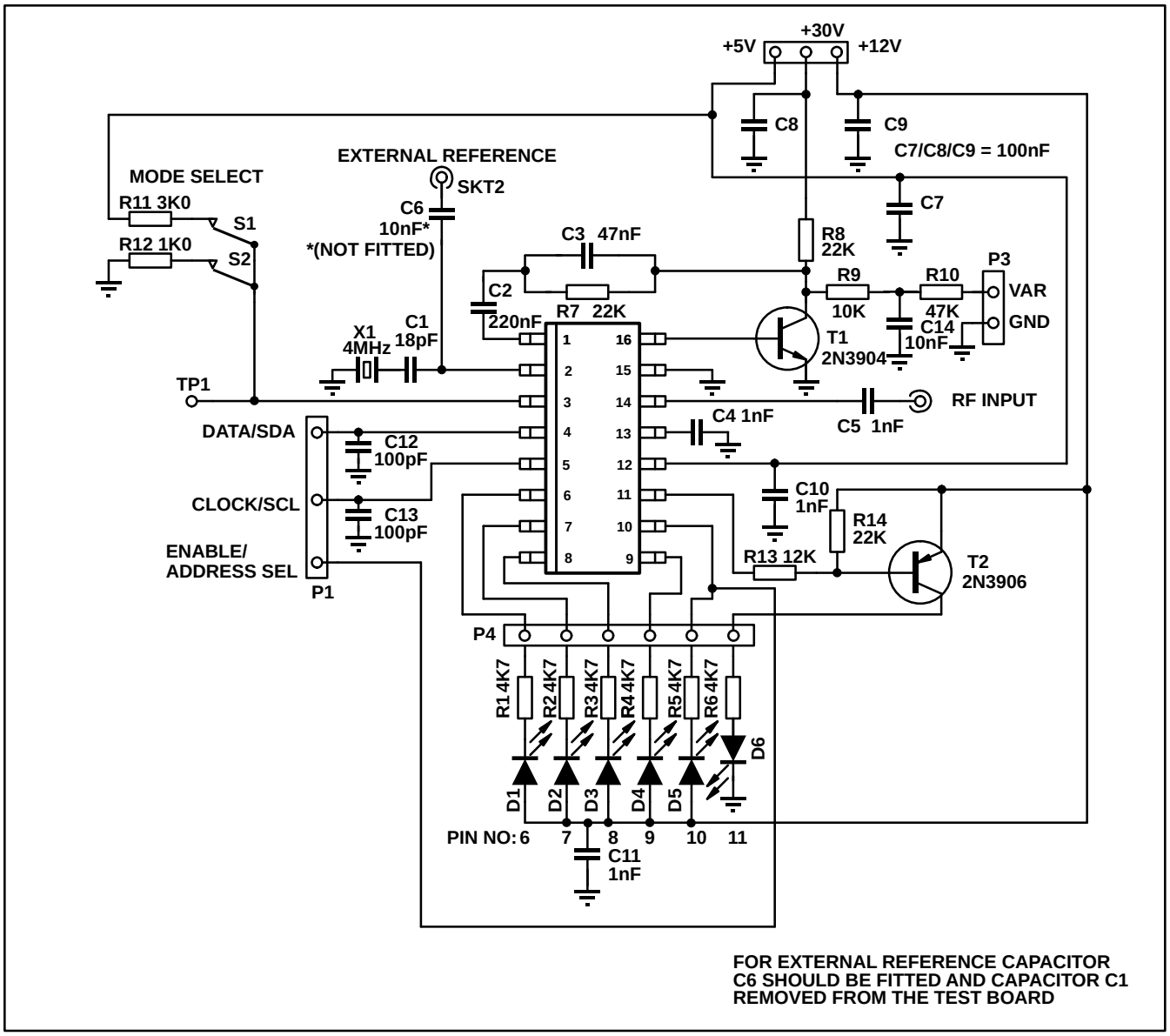
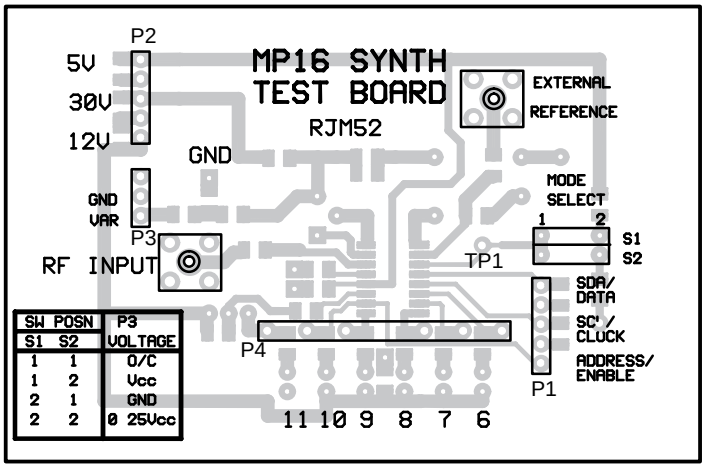
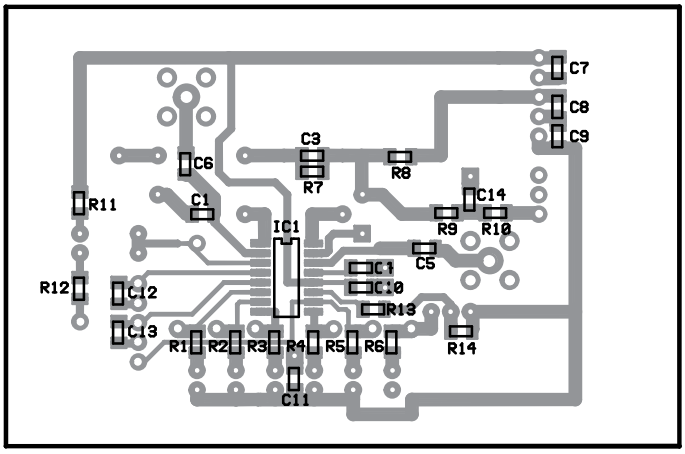


Fig. 8 Test board



TP1 = PIN 3 DC BIAS

Top view (Ground plane)



Underside (surface mount components side)

NOTES:
CIRCUIT SCHEMATIC IS SHOWN IN FIG. 8.

ALL SURFACE MOUNT COMPONENTS MOUNTED ON UNDERSIDE OF BOARD

Fig. 9 Test board (layout)

TEST MODES

As explained earlier in the data sheet, the device can be programmed into a number of test modes. These are invoked by programming the following HEX codes into Byte 4. The most commonly used codes are shown in Table 6

DESCRIPTION	HEX CODE (BYTE 4)	
	CP HI MODE	CP LO MODE
Normal operation, REF DIV =1024	CC	8C
Normal operation, REF DIV = 512	CE	8E
Charge Pump Source (Down), FL SET to 0	E2	A2
Charge Pump Sink (up), FL SET to 1	E6	A6
Port P7 = $F_{PD}/2$	EA	AA
Port P7 = F_{PD}; P6 = F_{COMP}	EE	AE
Charge Pump Disable, REF DIV ÷ 512	DE	9E
Varactor Line Disable, REF DIV ÷ 512	CF	8F
Charge Pump and Varactor Line Disable, REF DIV ÷ 512	DF	9F

Table 6 Useful test modes.

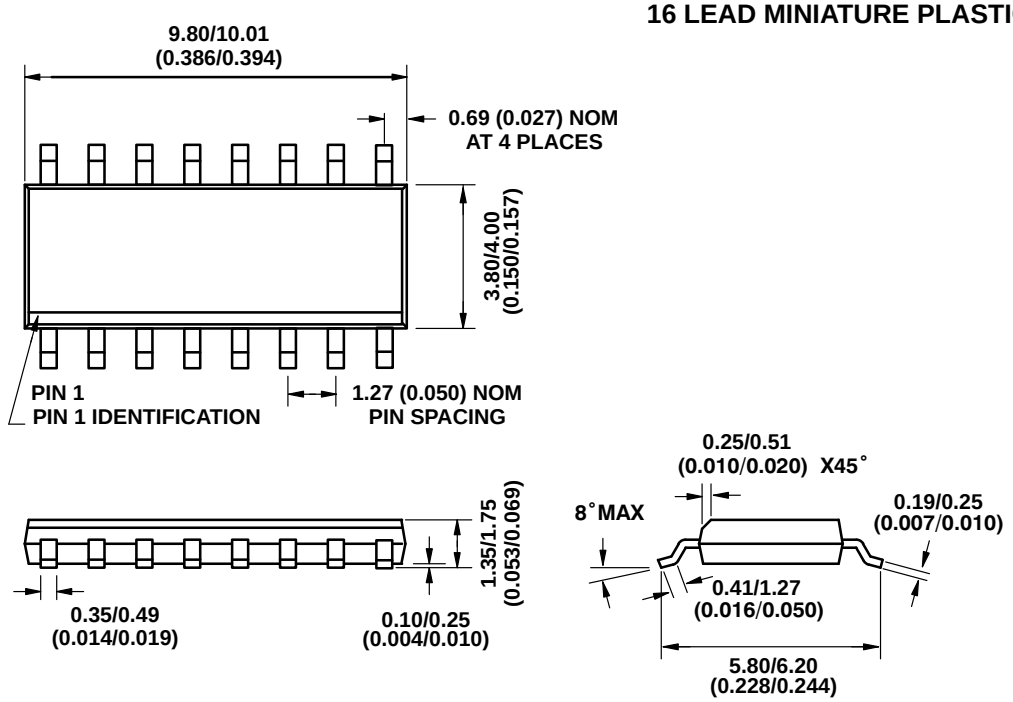
Other codes will also apply due to 'Don't Care' conditions, which are assumed to be 1 in the above Table.

NOTE:

When looking at F_{PD} or F_{COMP} signals from Ports P7 and P6, Byte 4 should be sent twice, firstly to set the desired reference divider ratio, (see Table 6) then secondly to switch on the chosen test mode.

The pulses can then be measured by simply connecting an oscilloscope or counter to the relevant output pin on the test board.

16 LEAD MINIATURE PLASTIC MP16



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