DS3212 - 2.1

SL2524

1.3GHz DUAL WIDEBAND LOGARITHMIC AMPLIFIER

The SL2524 is a pin compatible replacement for the SL2521 and SL2522 series of log amplifiers, and exhibits a superior stability performance. The amplifier is a successive detection type which provides linear gain and accurate logarithmic signal compression over a wide bandwidth. The two stages can be operated independently.

When six stages (three SL2524s) are cascaded the strip can be used for IFs between 30-650MHz whilst achieving greater than 65dB dynamic range with a log accuracy of <±1.0dB. The balanced limited output also offers accurate phase information with input amplitude.

FEATURES

- 1.3GHz Bandwidth (-3dB)
- Balanced IF limiting
- 3ns Rise Times/5ns Fall Times (six stages)
- 20ns Pulse Handling (six stages)
- Temperature Stabilised
- Surface Mountable

APPLICATIONS

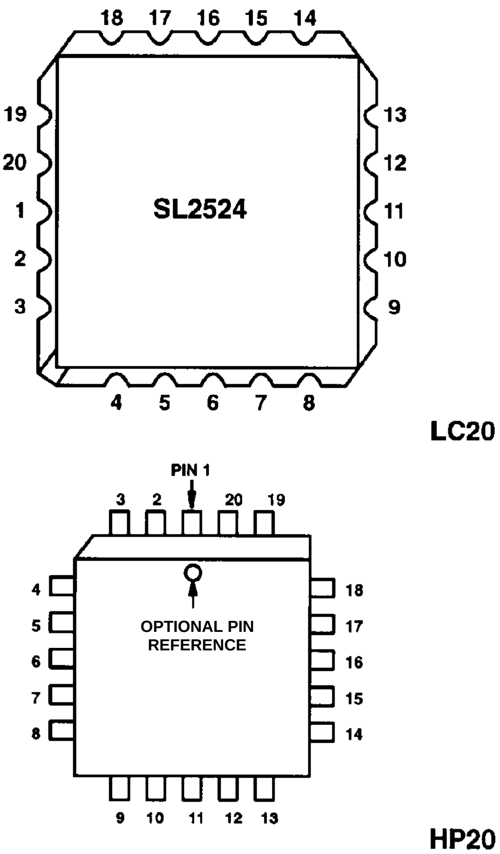
- Ultra Wideband Log Receivers
- Channelised Receivers
- Monopulse Applications

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} above V_{EE})	+7.0V
Storage temperature	-65°C to +150°C
Operating temperature range	
SL2524/B/LC	-40°C to +85°C
SL2524/C/HP	-30°C to +85°C
Junction temperature - LC20	+175°C
- HP20	+150°C
Applied DC voltage to RF input	±0.4V (between RF I/P pins)
Applied RF power to RF input	+15dBm
Value of R_{SET} resistors	NOT less than 180Ω
Thermal resistance:-	
Die to case -LC 20	28°C/W
- HP20	20°C/W
Die to ambient - LC20	73°C/W
- HP20	82°C/W

ORDERING INFORMATION

SL2524/B/LC (Ceramic leadless chip carrier package)
SL2524/C/HP (Plastic J lead chip carrier package)
SL2524/NA/1C (DC probe tested bare die)
5962 - 92315 (SMD)



PIN	DESCRIPTION	PIN	DESCRIPTION
1	SUB V_{EE}	11	N/C
2	IF OUTPUT (A)	12	R SET (B)
3	IF OUTPUT (A)	13	DET. OUTPUT (B)
4	V_{EE} (A)	14	V_{CC} (B)
5	OUTPUT V_C (A)	15	IF OUTPUT (B)
6	IF INPUT (A)	16	IF OUTPUT (B)
7	IF INPUT (A)	17	OUTPUT V_{CC} (B)
8	V_{CC} (A)	18	V_{EE} (B)
9	DET. OUTPUT (A)	19	IF INPUT (B)
10	R SET (A)	20	IF INPUT (B)

Fig.1 Pin connections top view

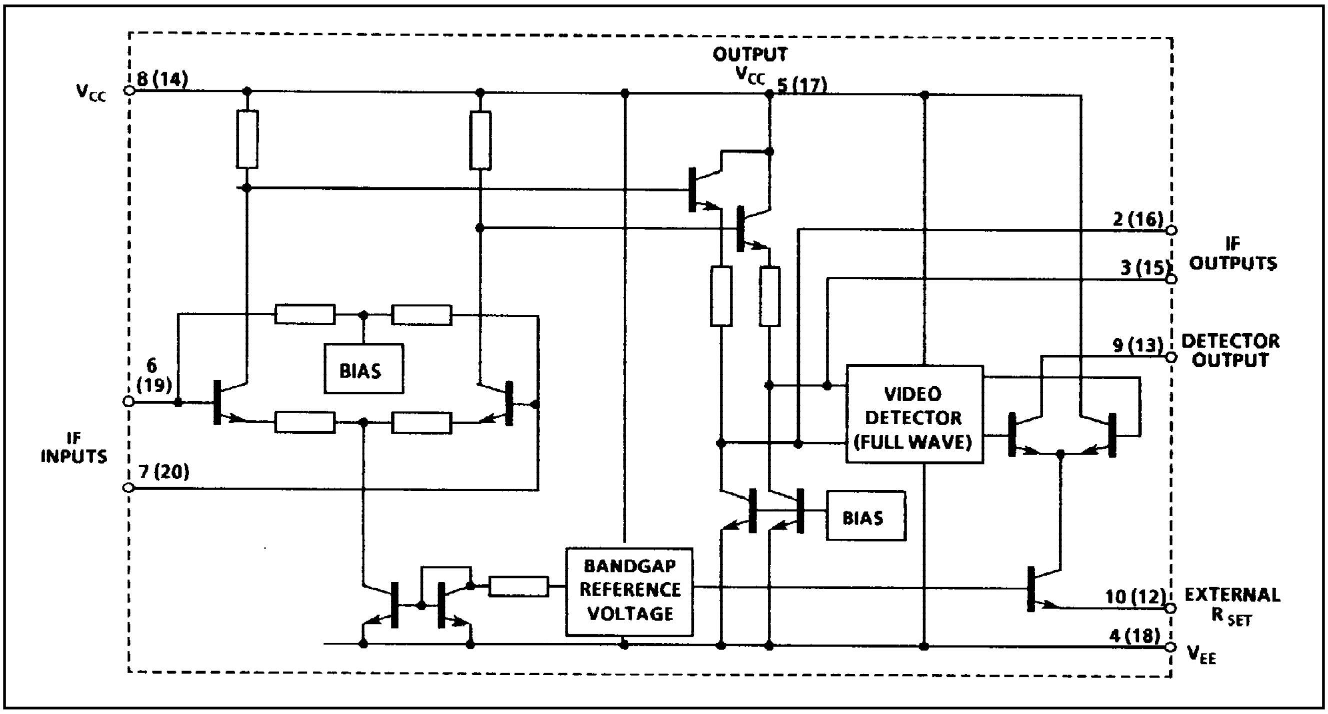
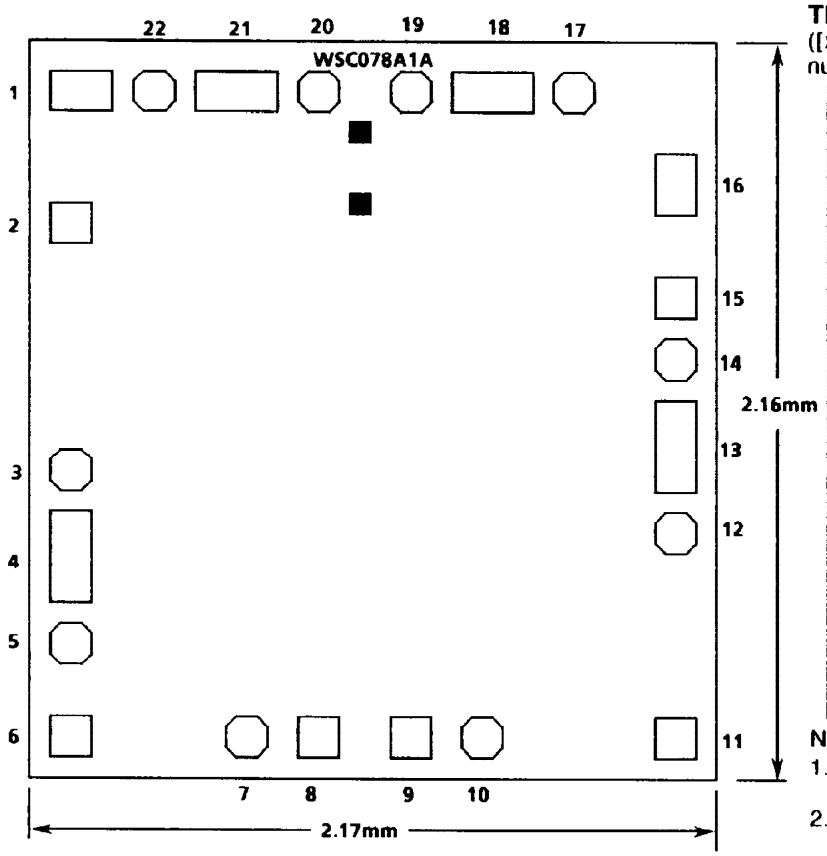


Fig.2 Circuit diagram of single stage A - (stage B pin Nos bracketed)



TERMINALS

([x] denotes LC20/HP20 package pin numbers)

PAD NO	FUNCTION	
1	V_{EE} (A)	[4]
2	O/P V_{CC} (A)	[5]
3	IF I/P (A)	[6]
4	TEST POINT	
5	IF I/P (A)	[7]
6	V_{CC} (A)	[8]
7	DETECTOR O/P (A)	[9]
8	R_{SET} (A)	[10]
9	R_{SET} (B)	[12]
10	DETECTOR O/P (B)	[13]
11	V_{CC} (B)	[14]
12	IF O/P (B)	[15]
13	TEST POINT	
14	IF O/P (B)	[16]
15	O/P V_{CC} (B)	[17]
16	V_{EE} (B)	[18]
17	IF I/P (B)	[19]
18	TEST POINT	
19	IF I/P (B)	[20]
20	IF O/P (A)	[2]
21	TEST POINT	
22	IF O/P (A)	[3]

NOTES

1. All pads with square cross-section = 120µm x 120µm
2. All pads with octagonal cross-section = 100µm x 100µm
3. Chip is passivated with polyimide

Fig.3 Pad map for SL2524 naked die

ELECTRICAL CHARACTERISTICS - SL2524B

Guaranteed at the following test conditions unless otherwise stated

Frequency = 200MHz, T_{amb} = +25°C, Input power = -30dBm, V_{CC} = 6V ±0.1V, Source Impedance = 50Ω.
Load impedance = 50Ω, Test Circuit = Fig. 4, R_{SET} = 300Ω. Tested as a dual stage.

Characteristic	Value Min	Value Typ	Value Max	Units	Conditions
Supply current	70	87	100	mA	
Small signal gain (dual stage, single ended)	9.6	11.4	13.0	dB	T_{amb} = +25°C f = 25MHz See Notes 1, 3
	10.1	11.6	13.1	dB	T_{amb} = -40°C f = 200MHz See Notes 2, 3
	9.9	11.3	12.7	dB	T_{amb} = +25°C f = 200MHz See Note 3
	9.5	11.0	12.5	dB	T_{amb} = +85°C f = 200MHz See Notes 2, 3
	9.7	11.2	12.7	dB	T_{amb} = -40°C f = 500MHz See Notes 2, 3
	9.3	10.7	12.1	dB	T_{amb} = +25°C f = 500MHz See Note 3
	8.2	9.7	11.2	dB	T_{amb} = +85°C f = 500MHz See Notes 2, 3
Detected output current (max)	3.20	3.45	3.70	mA	T_{amb} = +25°C, V_{IN} = 0dBm, f = 25MHz See Note 1
	3.05	3.25	3.45	mA	T_{amb} = -40°C, V_{IN} = 0dBm, f = 200MHz See Note 2
	3.15	3.30	3.45	mA	T_{amb} = +25°C, V_{IN} = 0dBm, f = 200MHz
	3.10	3.30	3.50	mA	T_{amb} = +85°C, V_{IN} = 0dBm, f = 200MHz See Note 2
	2.80	3.10	3.30	mA	T_{amb} = -40°C, V_{IN} = 0dBm, f = 500MHz See Note 2
	2.90	3.15	3.45	mA	T_{amb} = +25°C, V_{IN} = 0dBm, f = 500MHz
	2.85	3.10	3.65	mA	T_{amb} = +85°C, V_{IN} = 0dBm, f = 500MHz See Note 2
Detected output current (no signal)	0.85	0.95	1.15	mA	T_{amb} = -40°C, See Note 2
	0.80	0.93	1.10	mA	T_{amb} = +25°C, See Note 2
	0.80	0.90	1.10	mA	T_{amb} = +85°C, See Note 2
Upper cut off frequency (RF)	600	1100		MHz	-3dB w.r.t 200MHz, T_{amb} = -40°C See Note 2
	900	1100		MHz	-3dB w.r.t 200MHz, T_{amb} = +25°C
	600	800		MHz	-3dB w.r.t 200MHz, T_{amb} = +85°C See Note 2
Lower cut off frequency (RF)		0.35	1	MHz	-3dB w.r.t 200MHz, T_{amb} = +25°C
Detector cut off frequency		700		MHz	50% O/P current w.r.t. 200MHz
Limited IF O/P voltage	135	155	175	mV	I/P power = 0dBm, T_{amb} = +25°C
Phase variation with input level (normalised to -30dBm)		0±2.0	0±3.0	Degree	Frequency = 70MHz, -55 to +3dBm See Note 2
		-4.0±2.0	-4.0±3.0	Degree	Frequency = 200MHz, -55 to +3dBm See Note 2
Limited O/P var with temp.		±12	±25	mV	See Note 1
Noise figure		14		dB	
Max I/P before overload		15		dBm	
Input impedance		1		kΩ	1kΩ in parallel with 2pF
Output impedance		50		Ω	

NOTES
1. Parameter guaranteed but not tested
2. Tested at 25°C only, but guaranteed at temperature
3. Gain will typically increase by 6dB, when RF outputs use 1kΩ loads in place of 50Ω

ELECTRICAL CHARACTERISTICS - SL2524C

Guaranteed at the following test conditions unless otherwise stated

Frequency = 200MHz, T_{amb} = +25°C, Input power = -30dBm, V_{CC} = 6V ±0.1V, Source Impedance = 50Ω.
Load impedance = 50Ω, Test Circuit = Fig. 4, R_{SET} = 300Ω. Tested as a dual stage.

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Supply current	70	87	100	mA	
Small signal gain (dual stage, single ended)	9.6 9.6 9.4 9.0 9.2 8.8 7.7	11.4 11.6 11.3 11.0 11.2 10.7 9.7	13.0 13.6 13.2 13.0 13.2 12.6 11.7	dB dB dB dB dB dB dB	T_{amb} = +25°C f = 25MHz See Note 3 T_{amb} = -30°C f = 200MHz See Notes 2, 3 T_{amb} = +25°C f = 200MHz See Note 3 T_{amb} = +85°C f = 200MHz See Notes 2, 3 T_{amb} = -30°C f = 500MHz See Notes 1, 3 T_{amb} = +25°C f = 500MHz See Note 1 T_{amb} = +85°C f = 500MHz See Notes 1, 3
Detected output current (max)	3.20 2.95 3.05 3.00 2.70 2.80 2.75	3.45 3.25 3.30 3.30 3.10 3.15 3.10	3.70 3.55 3.55 3.50 3.30 3.55 3.75	mA mA mA mA mA mA mA	T_{amb} = +25°C, V_{IN} = 0dBm, f = 25MHz T_{amb} = -30°C, V_{IN} = 0dBm, f = 200MHz See Note 2 T_{amb} = +25°C, V_{IN} = 0dBm, f = 200MHz T_{amb} = +85°C, V_{IN} = 0dBm, f = 200MHz See Note 2 T_{amb} = -30°C, V_{IN} = 0dBm, f = 500MHz See Note 1 T_{amb} = +25°C, V_{IN} = 0dBm, f = 500MHz See Note 1 T_{amb} = +85°C, V_{IN} = 0dBm, f = 500MHz See Note 1
Detected output current (no signal)	0.75 0.70 0.70	0.95 0.93 0.90	1.25 1.20 1.20	mA mA mA	T_{amb} = -30°C, See Note 2 T_{amb} = +25°C, See Note 2 T_{amb} = +85°C, See Note 2
Upper cut off frequency (RF)		1000		MHz	-3dB w.r.t 200MHz, T_{amb} = +25°C See Note 1
Lower cut off frequency (RF)		0.35	2	MHz	-3dB w.r.t 200MHz, T_{amb} = +25°C
Detector cut off frequency		600		MHz	50% O/P current w.r.t. 200MHz
Limited IF O/P voltage	105	135	175	mV	I/P power = 0dBm, T_{amb} = +25°C
Phase variation with input level (normalised to -30dBm)		0±2.0 -4.0±2.0		Degree Degree	Frequency = 70MHz, -55 to +3dBm See Note 1 Frequency = 200MHz, -55 to +3dBm See Note 1
Limited O/P var with temp.		±12	±25	mV	See Note 1
Noise figure		14		dB	
Max I/P before overload		15		dBm	
Input impedance		1		kΩ	1kΩ in parallel with 2pF
Output impedance		50		Ω	

NOTES
1. Parameter guaranteed but not tested
2. Tested at 25°C only, but guaranteed at temperature
3. Gain will typically increase by 6dB, when RF outputs use 1kΩ loads in place of 50Ω

GENERAL DESCRIPTION

The SL2524 is primarily intended for use in Radar and EW receivers. Six stages (3 chip carriers) can be cascaded to form a very wideband logarithmic ampifier offering >65dB of input dynamic range, with pulse handling of better than 25ns. (See figs 5 and 6.)

A six stange strip also offers balanced IF limiting, linearity (log accuracy) of < ±1.0dB, temperature stabilisation and programmable detector characteristics.

The detector has an external resistor set (R_{SET}) pin which allows the major characteristics of the detector to be programmed. With six stage strip it is possible to vary the value of R_{SET} on each detector and so improve the overall log error/linearity.

The detector is full wave and good slew rates are achieved with 2ns rise and 5ns fall times (no video filter). The video bandwidth of a six stage strip is typically 600MHz (-3dB).

The amplifier also offers balanced IF limiting, low phase shift versus input amplitude, and at an IF of 120MHz, less than 5° of phase change is achievable over the input level of -55dBm to +5dBm.

The IF and Video ports can be used simultaneously, so offering phase, frequency and pulse (video) information. A slight loss of dynamic range (2dB) will be observed when the IF ports are used in conjunction with the video.

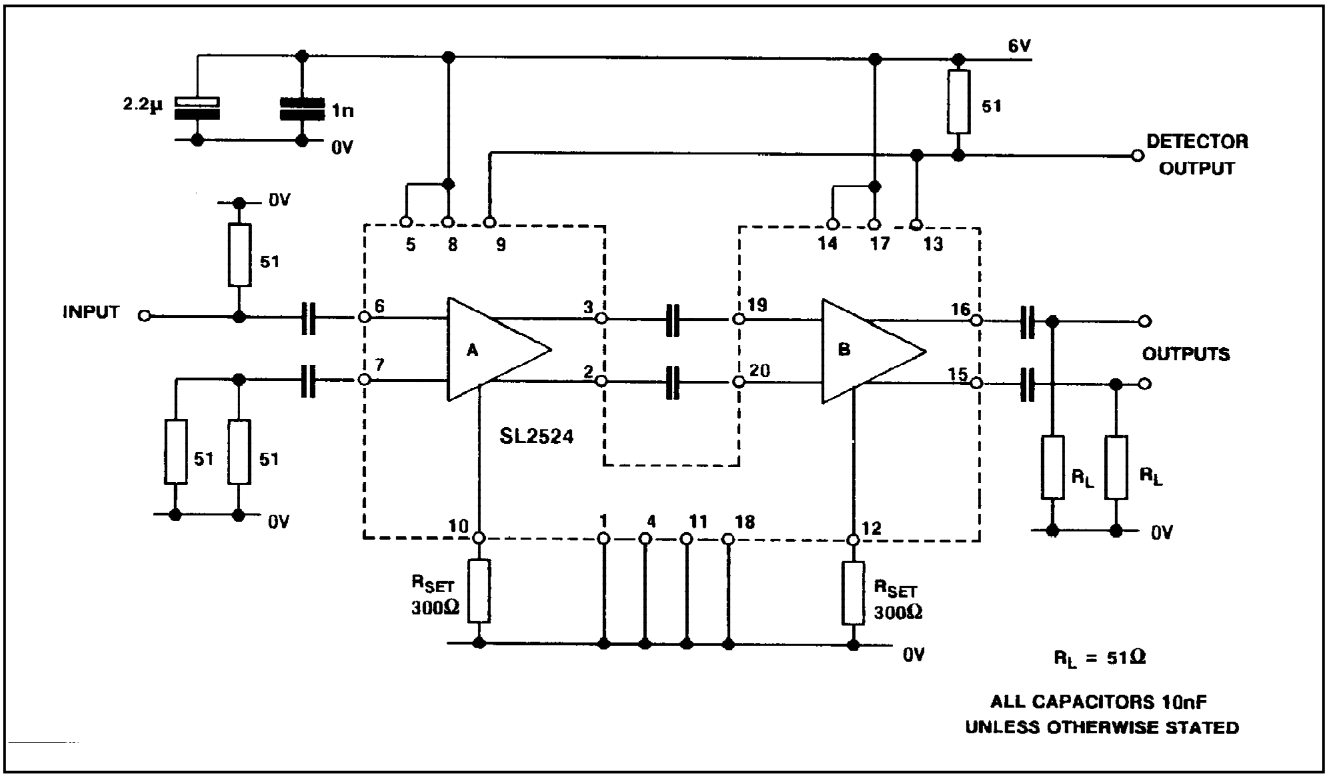


Fig.4 Test circuit

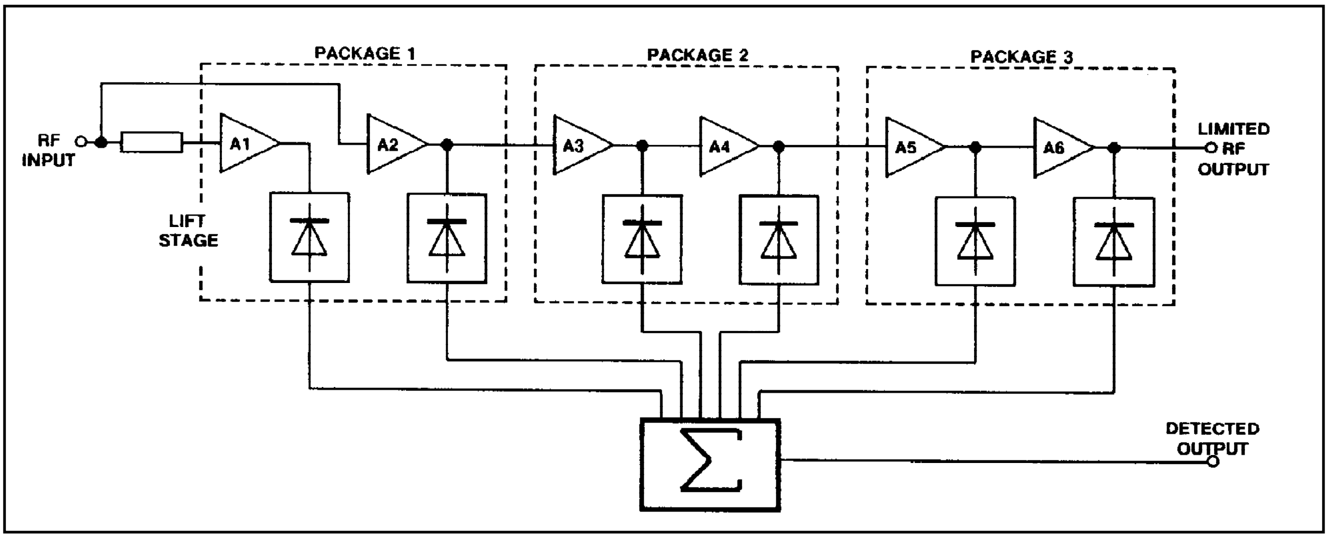


Fig.5 Schematic diagram showing configuration of SD Log strip

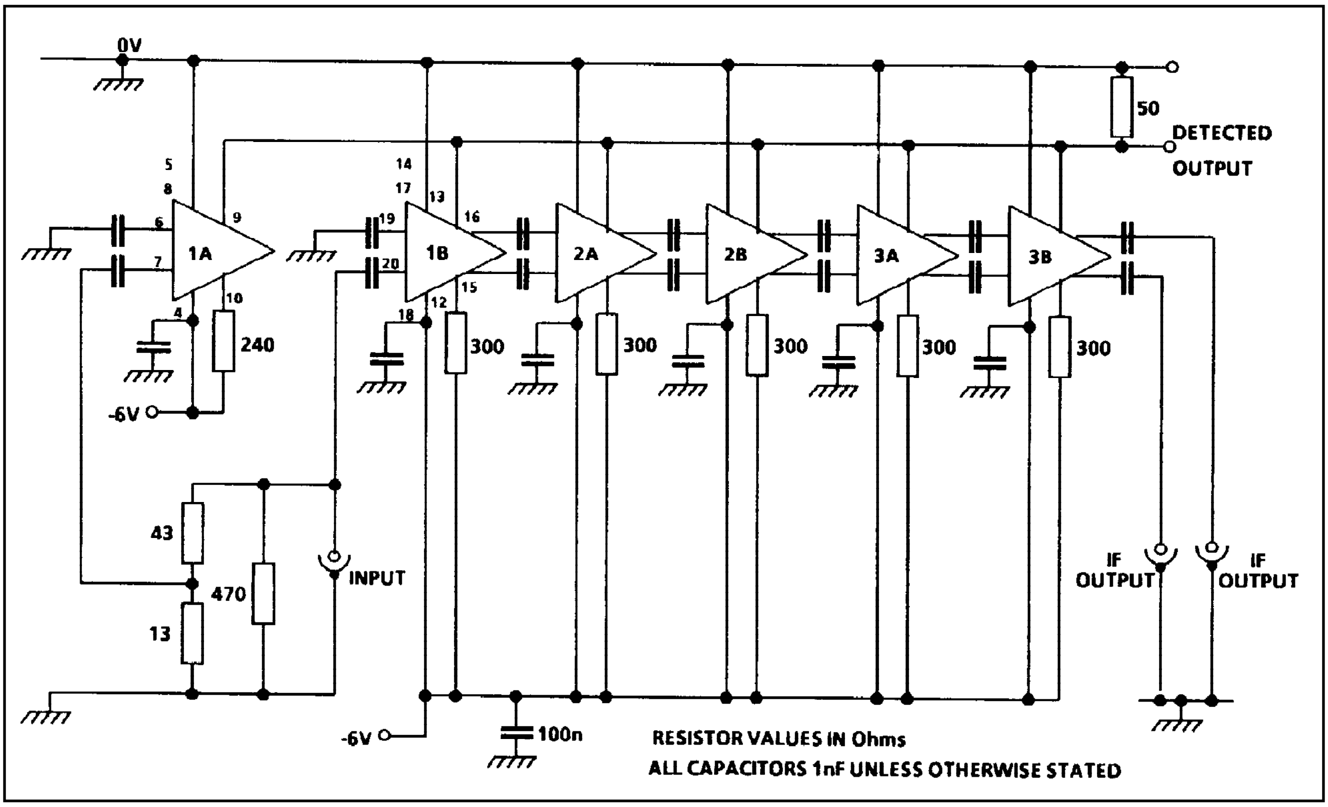


Fig.6 Circuit diagram for 6-log strip (results shown in figs. 11 to 24 were achieved with this circuit)

Typical characteristics for a dual - stage amplifier (i.e. One SL2524)

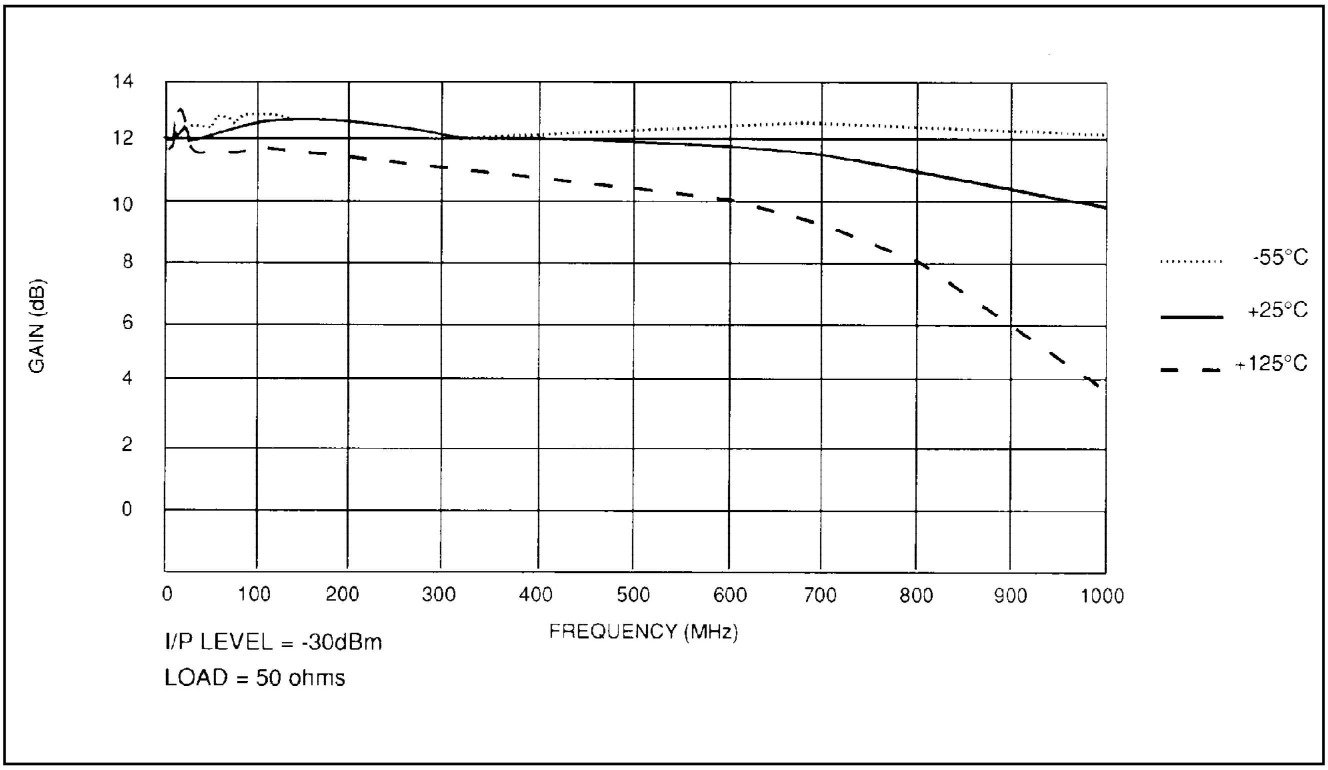


Fig.7 IF Gain vs frequency of 2 amplifiers (One SL2524)

Typical characteristics for a dual - stage amplifier (i.e. One SL2524) cont.

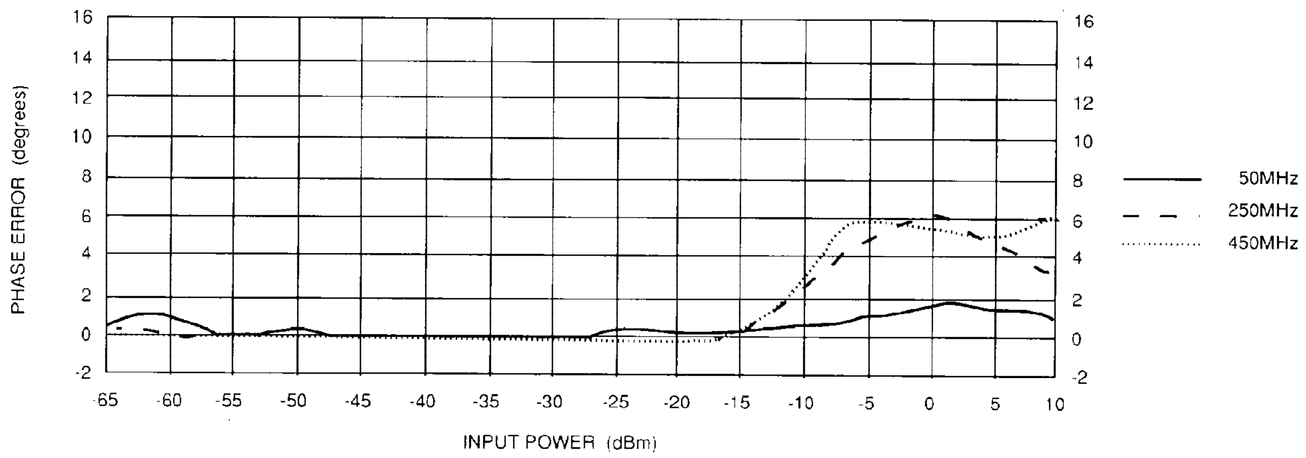


Fig.8 Normalised phase vs CW input level at 50, 250 and 450MHz for 50Ω O/P termination (25°C)

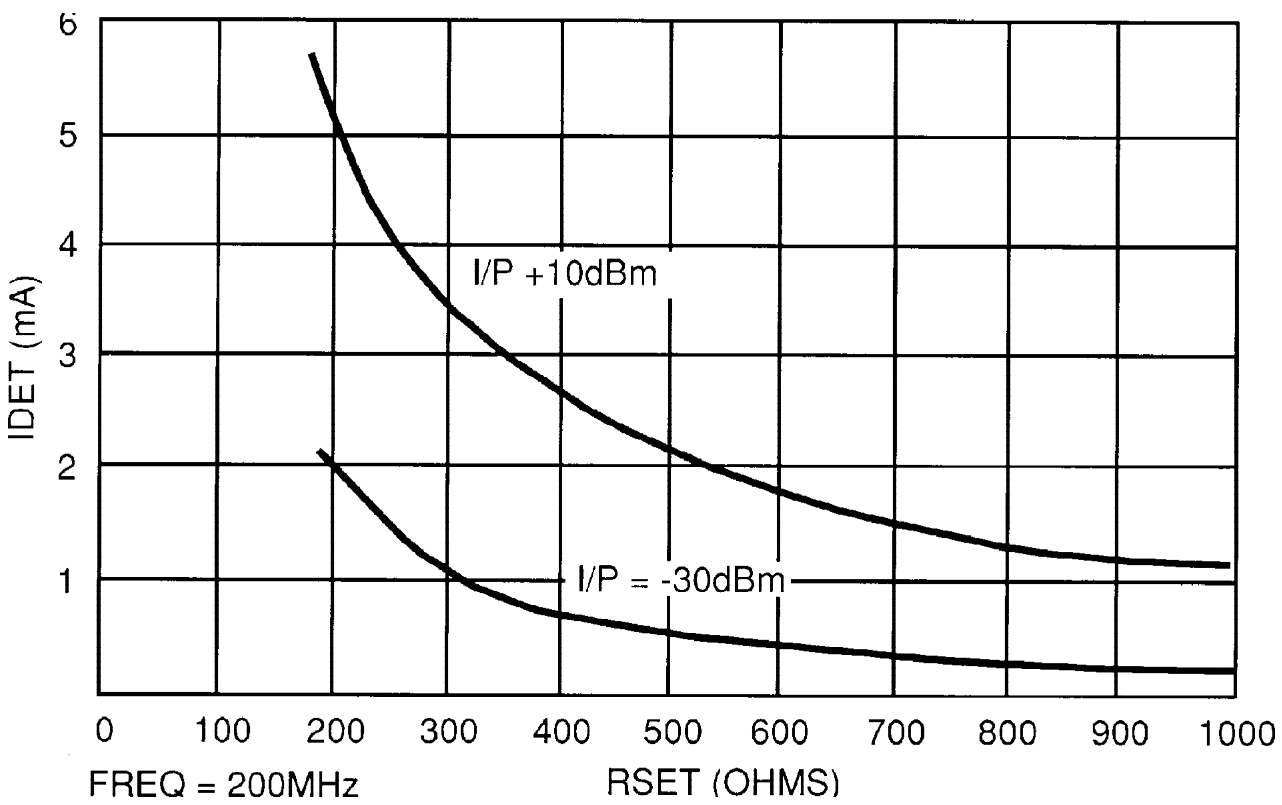


Fig.9 Detector current vs R_{SET} at 200MHz (25°C)

Typical characteristics for a dual - stage amplifier (i.e. One SL2524) cont.

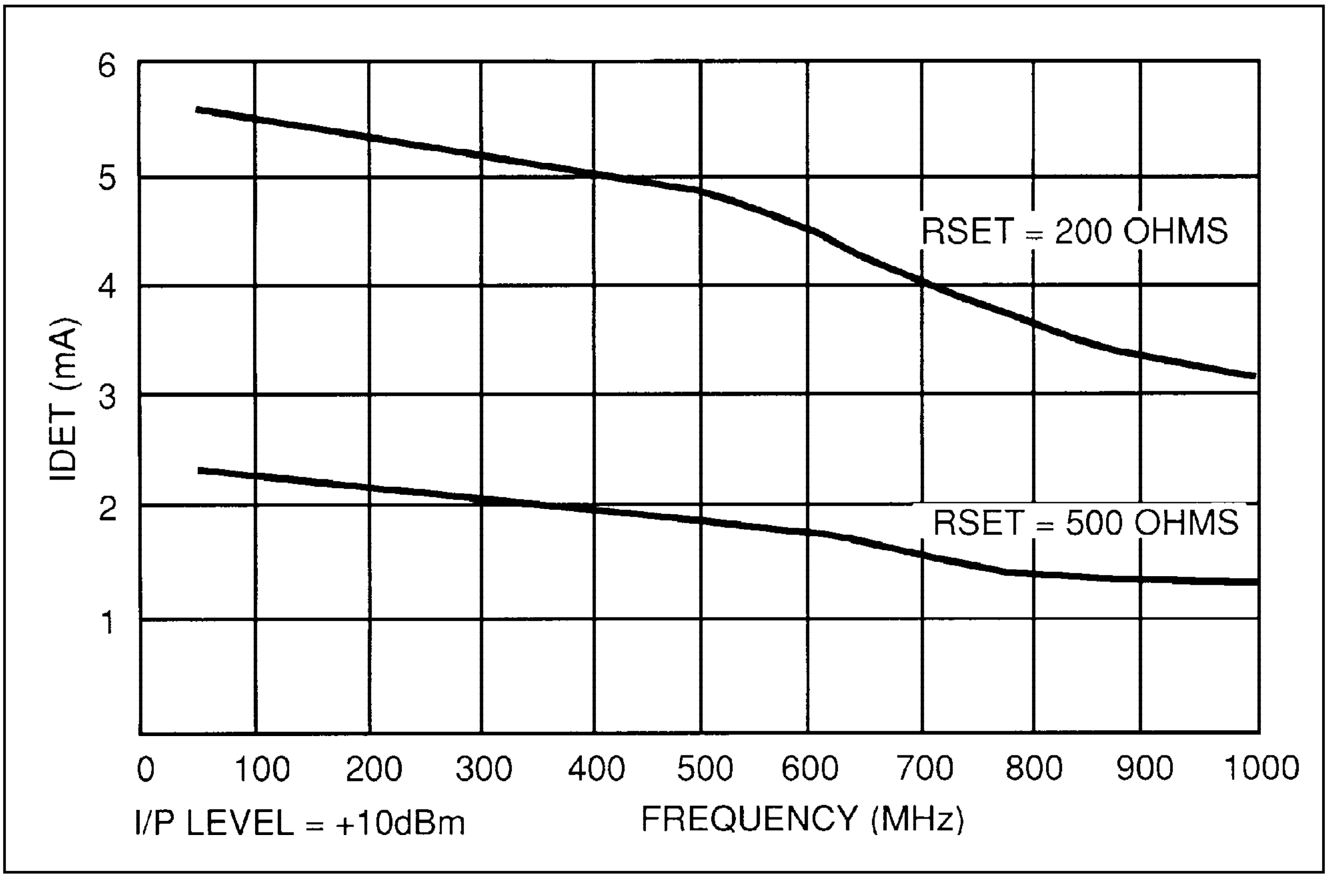


Fig.10 Detector current vs frequency at RSET = 200Ω and 500Ω (25°C)

Typical characteristics for a six stage strip, using detected output (Ref. figs 5 & 6)

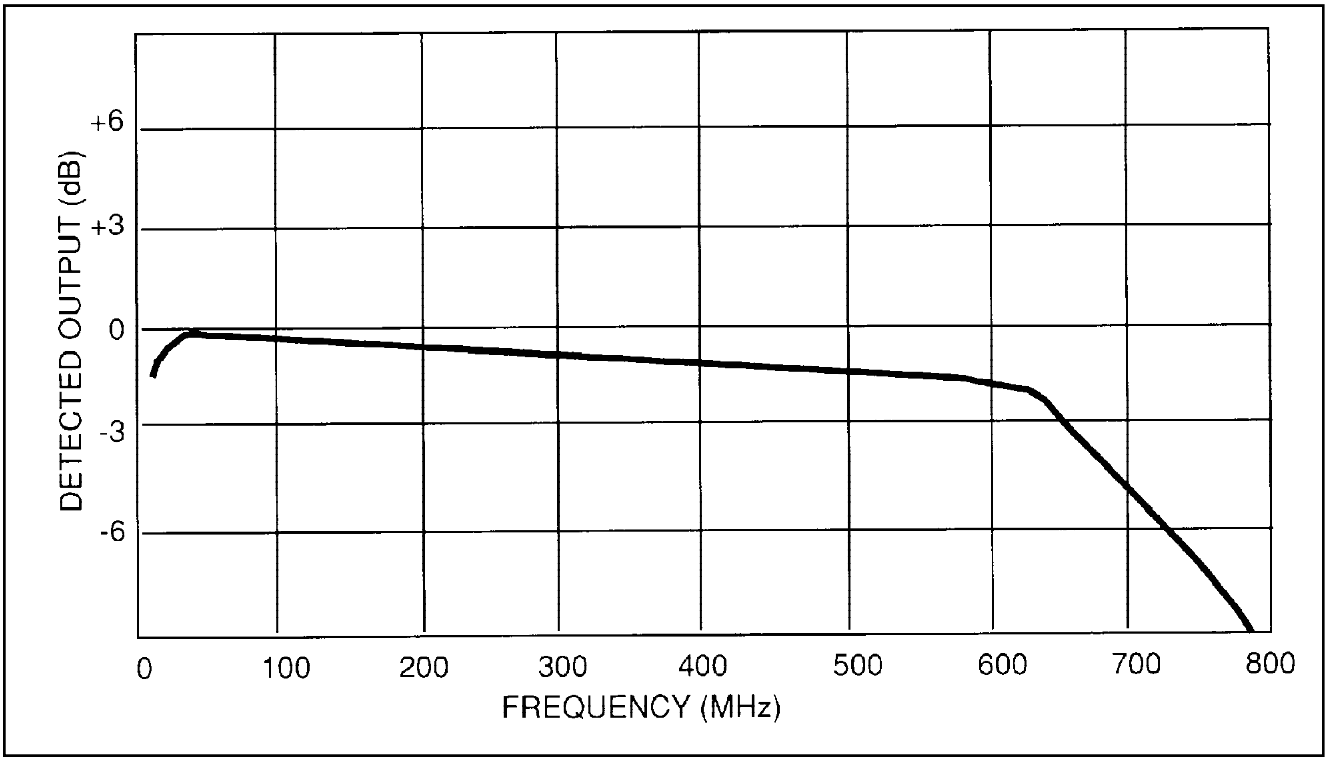


Fig.11 Detector bandwidth (25°C)

Typical characteristics for a six stage strip, using detected output (Ref. figs 5 & 6) cont.

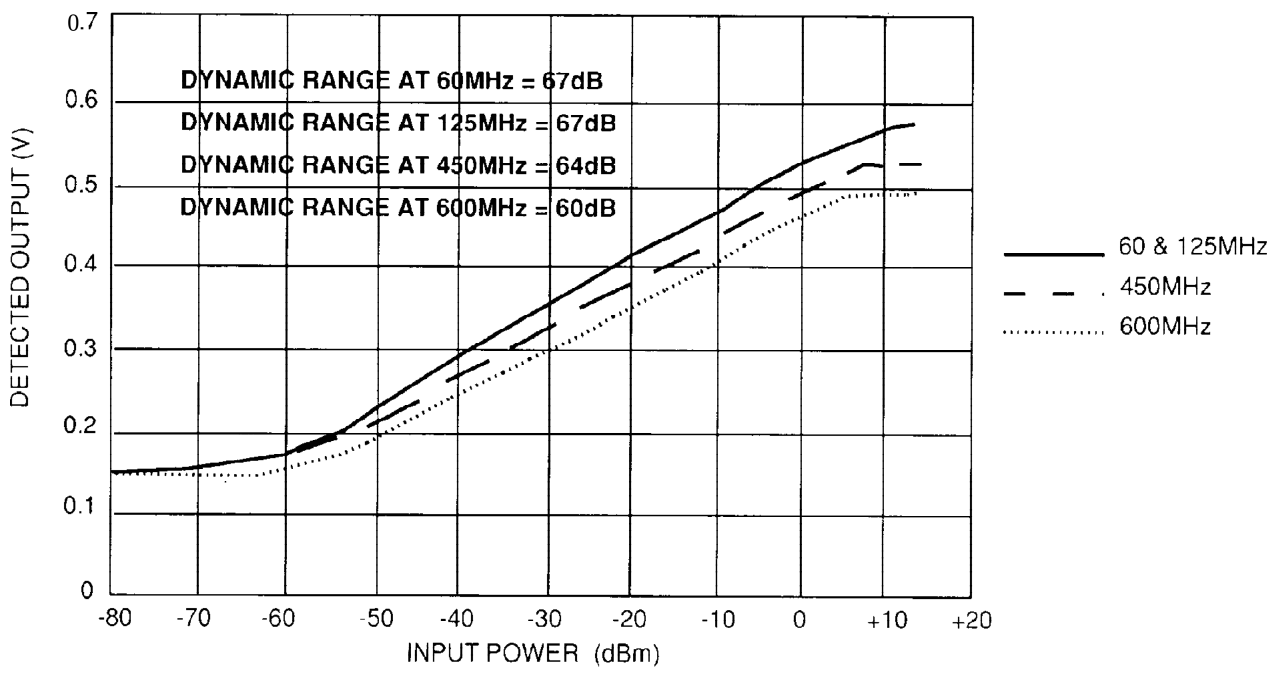


Fig.12 Detected O/P vs CW input at 60, 125, 450 and 600MHz at 25°C

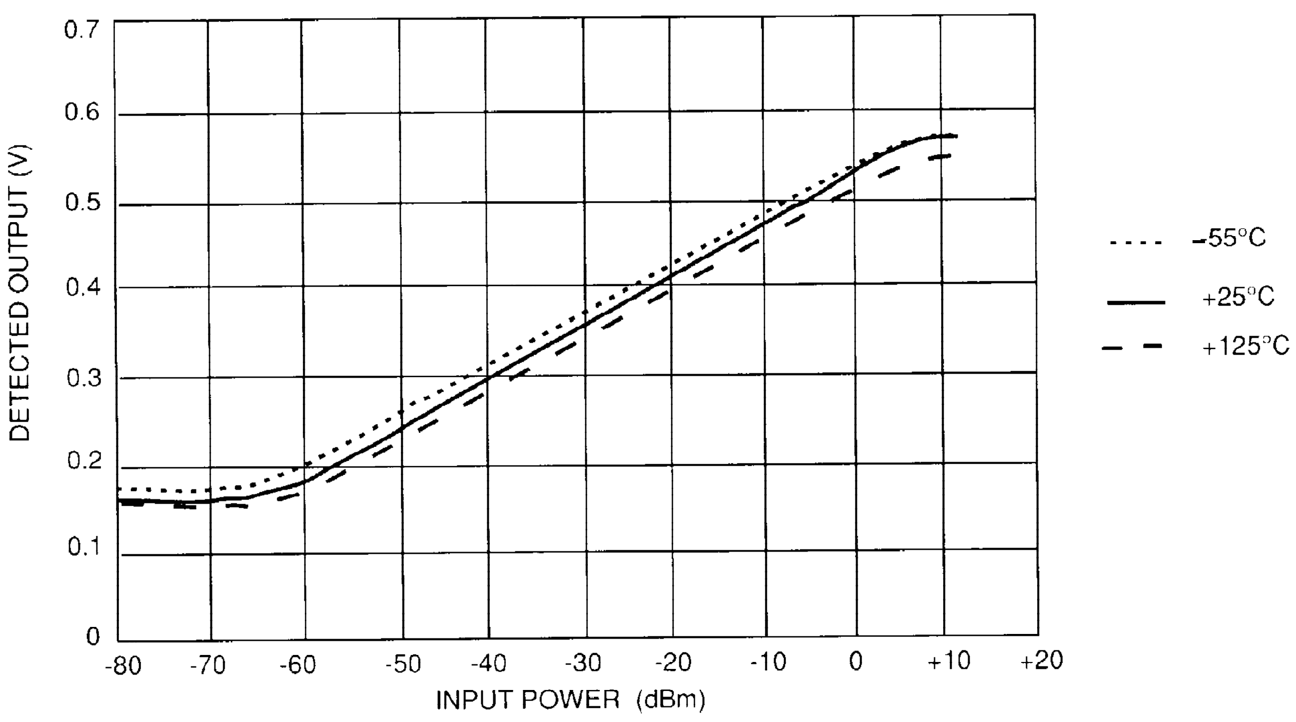


Fig.13 Detected O/P vs CW input level and temperature at 60 and 125MHz

Typical characteristics for a six stage strip, using detected output (Ref. figs 5 & 6) cont.

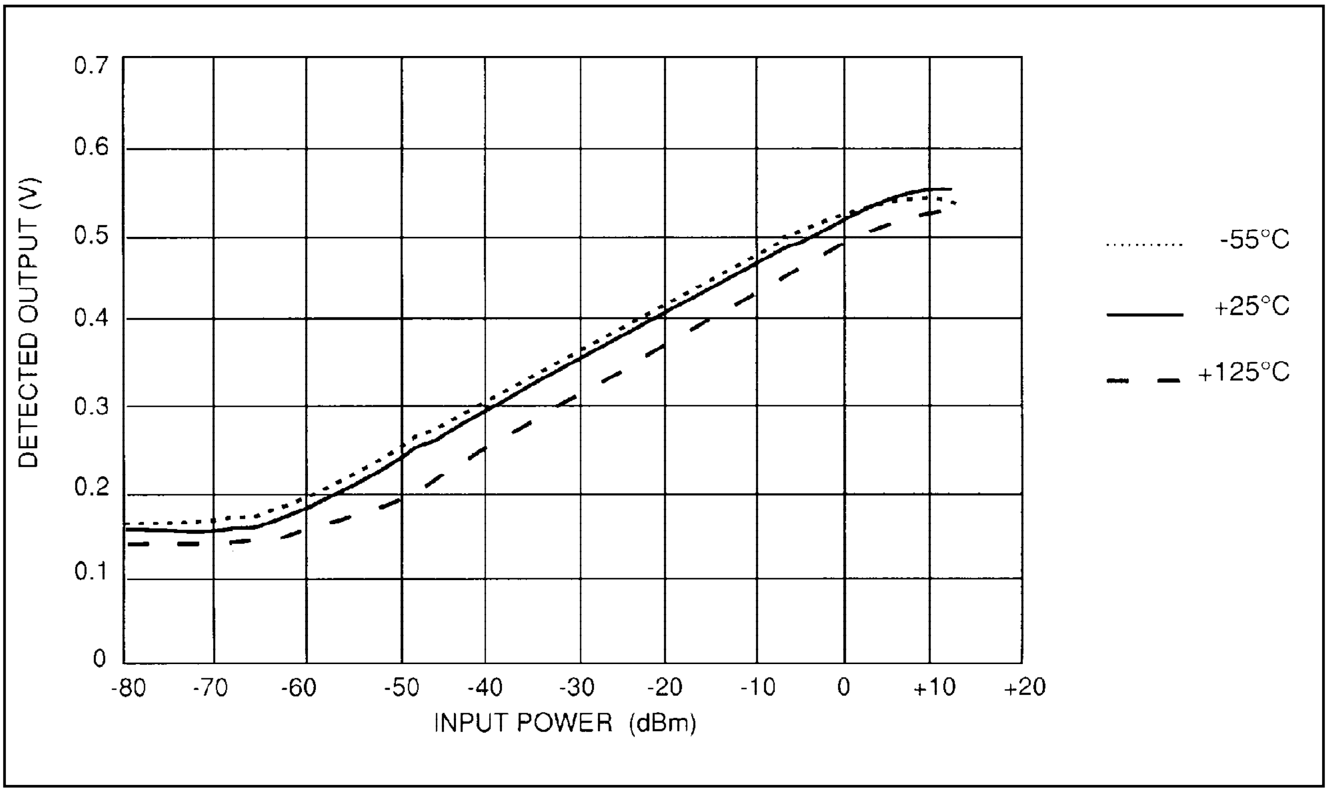


Fig.14 Detected O/P vs CW input level at 450MHz across temperature

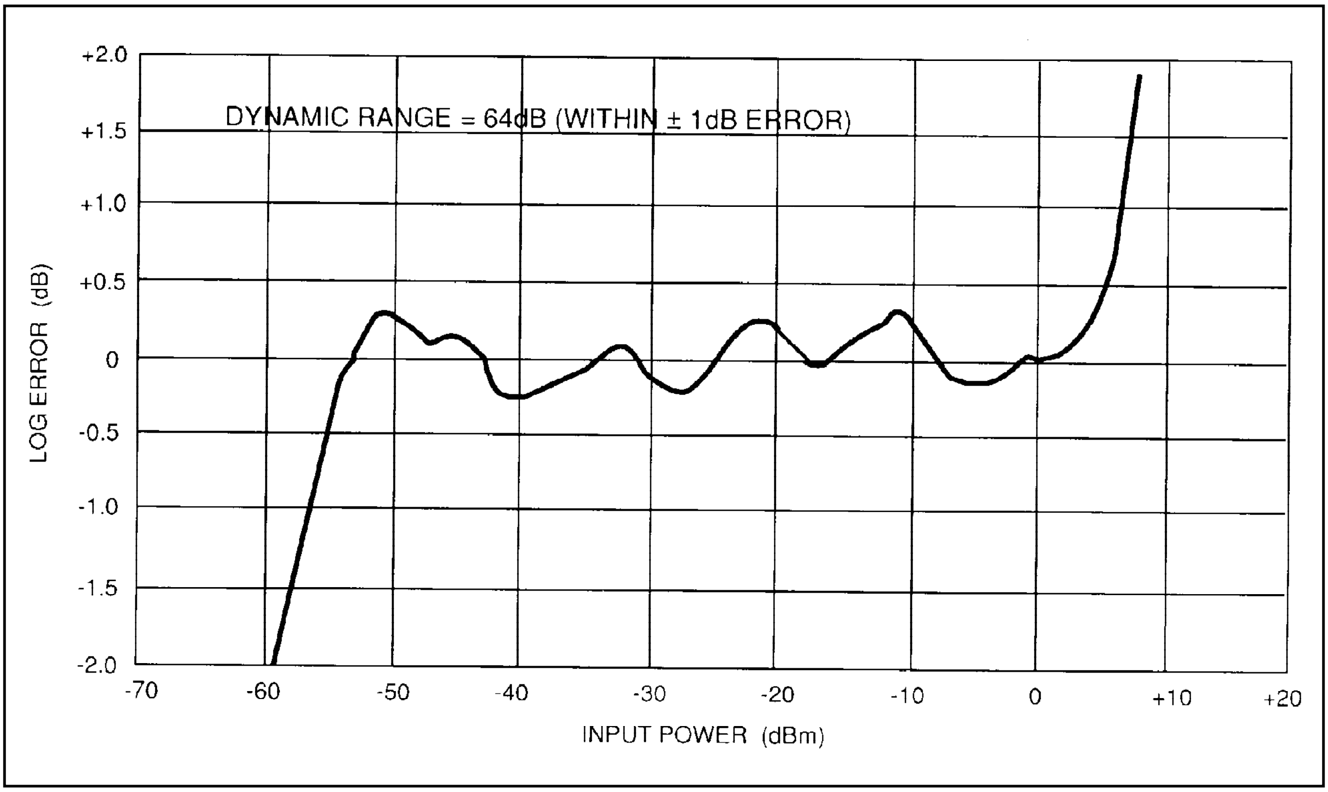


Fig.15 Typical log linearity of detected output measured at 450MHz (25°C)

Typical characteristics for a six stage strip as a low phase shift wideband limiter (Ref. figs 5 & 6)

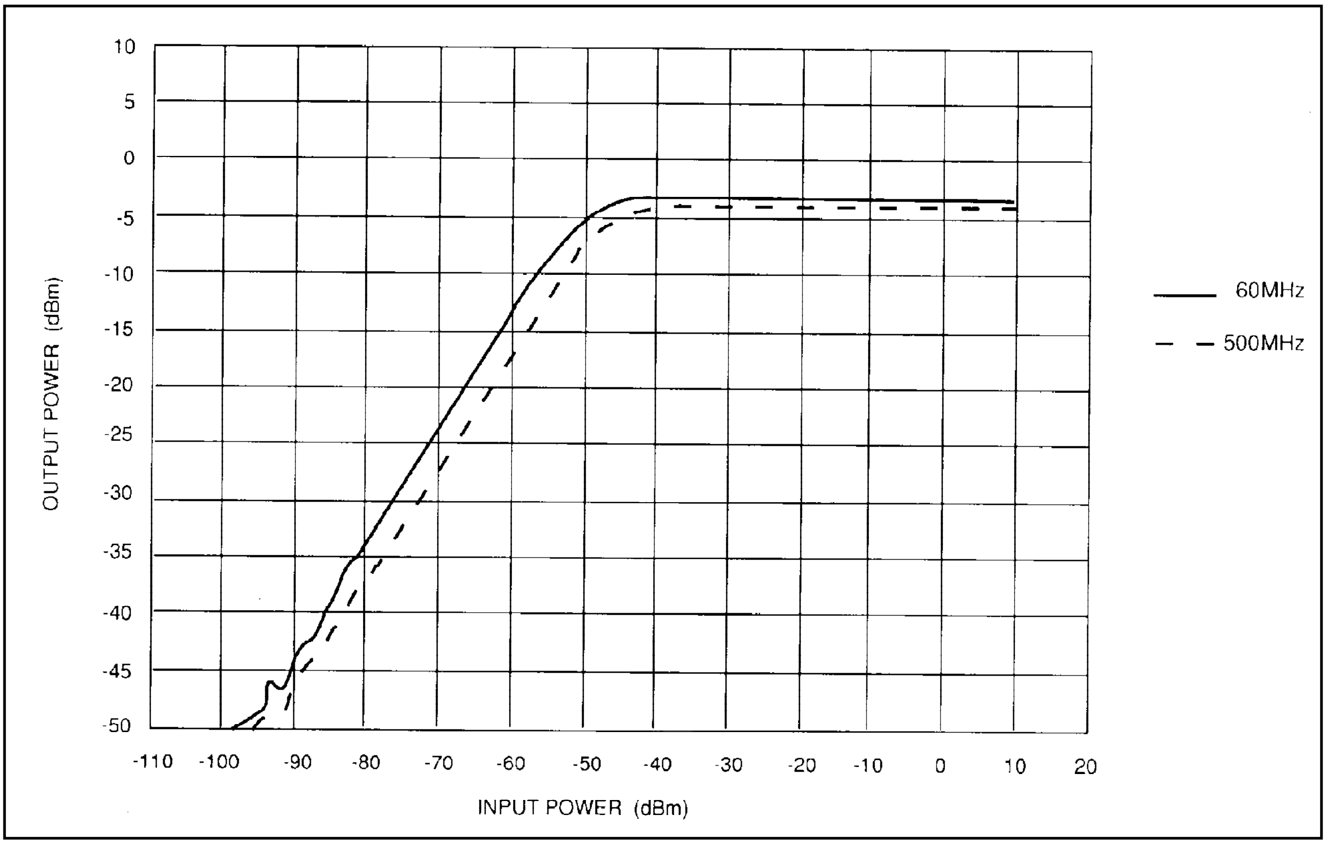


Fig.16 IF limiting characteristics at 60MHz and 500MHz (25°C)

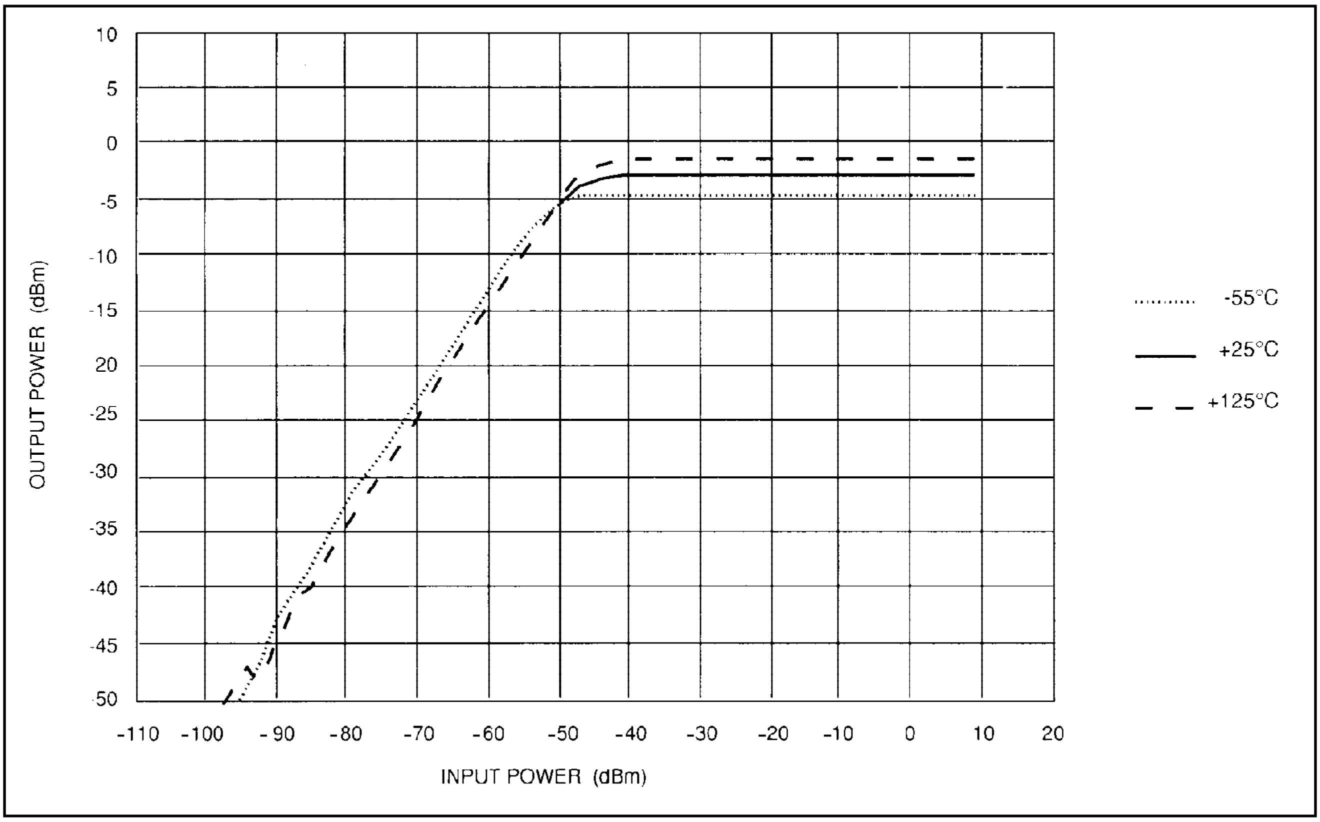


Fig.17 IF limiting characteristic at 60MHz across temperature

Typical characteristics for a six stage strip as a low phase shift wideband limiter (Ref. figs 5 & 6)

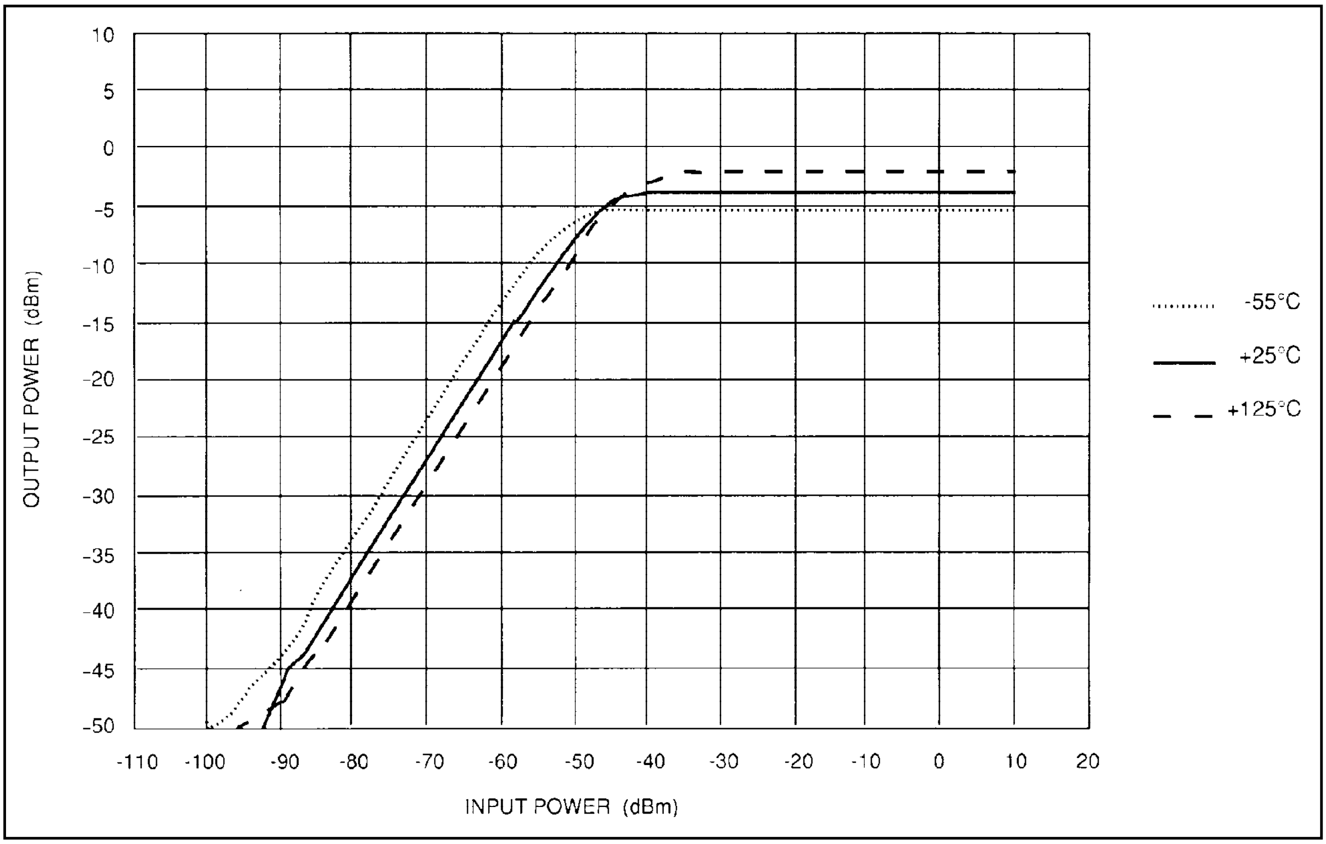


Fig.18 IF limiting characteristic at 500MHz across temperature

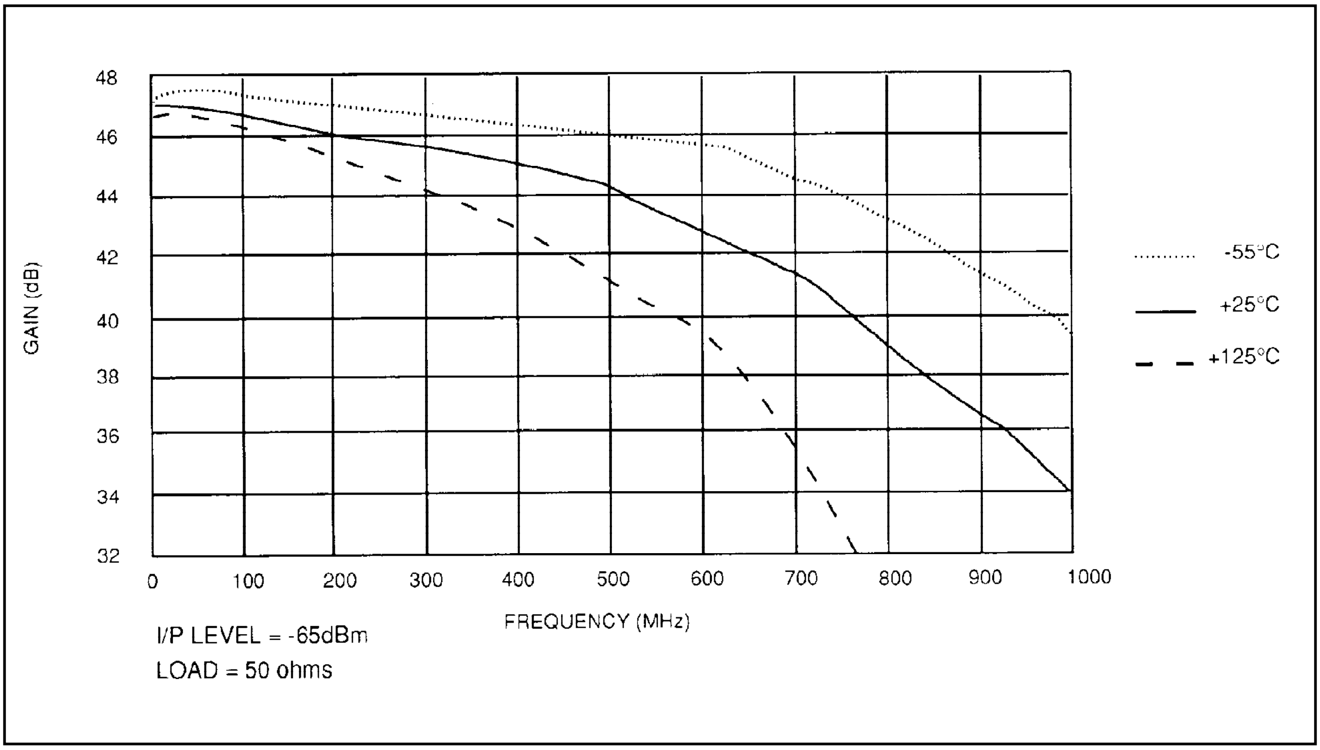


Fig.19 Small signal gain vs frequency across temperature

Typical characteristics for a six stage strip as a low phase shift wideband limiter (Ref. figs 5 & 6)

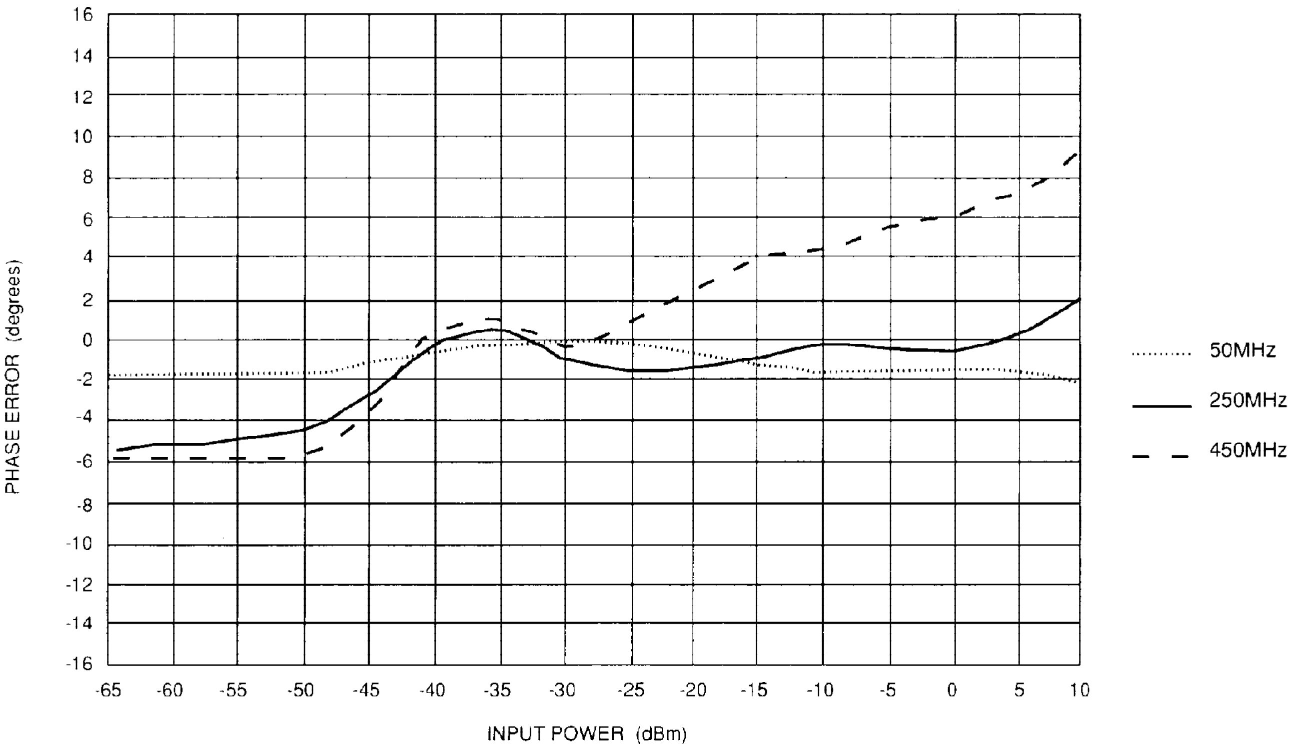


Fig.20 Phase deviation vs CW input level (normalised at -30dBm) at 25°C across input frequency

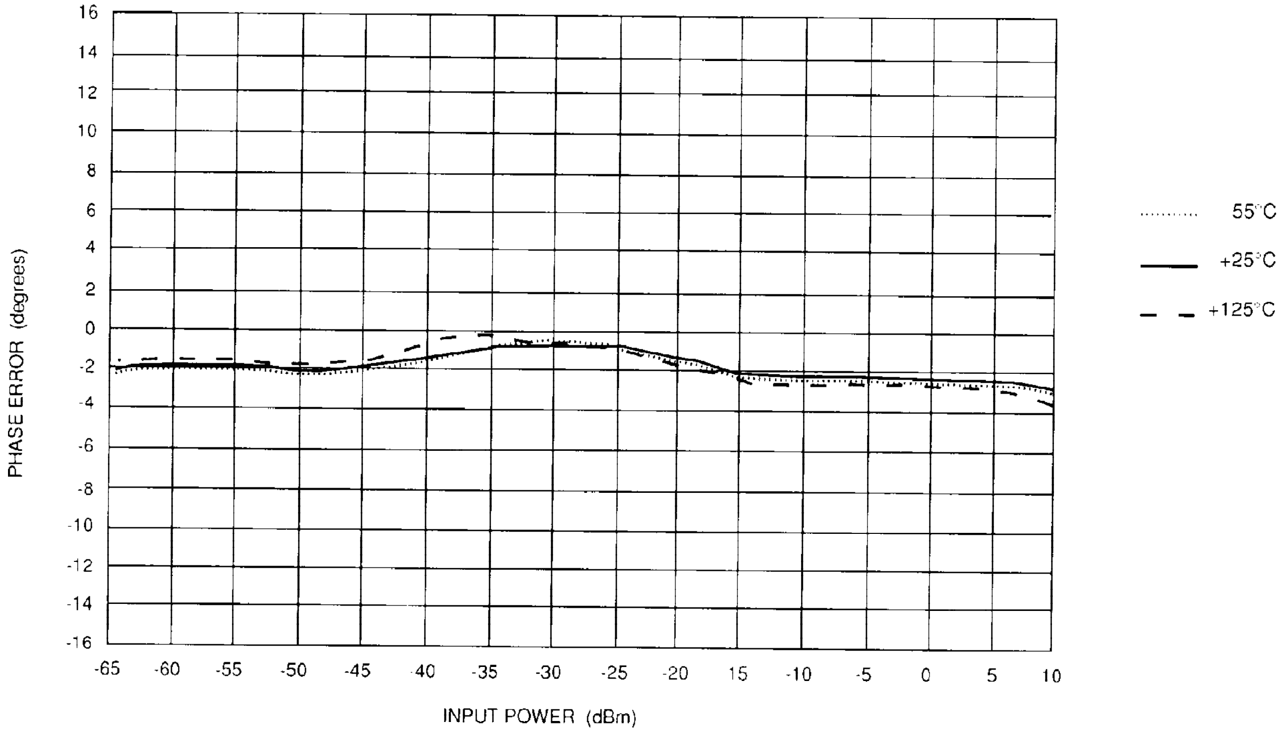


Fig.21 Phase deviation vs CW input level (normalised at -30dBm) at 50MHz across temperature

Typical characteristics for a six stage strip as a low phase shift wideband limiter (Ref. figs 5 & 6)

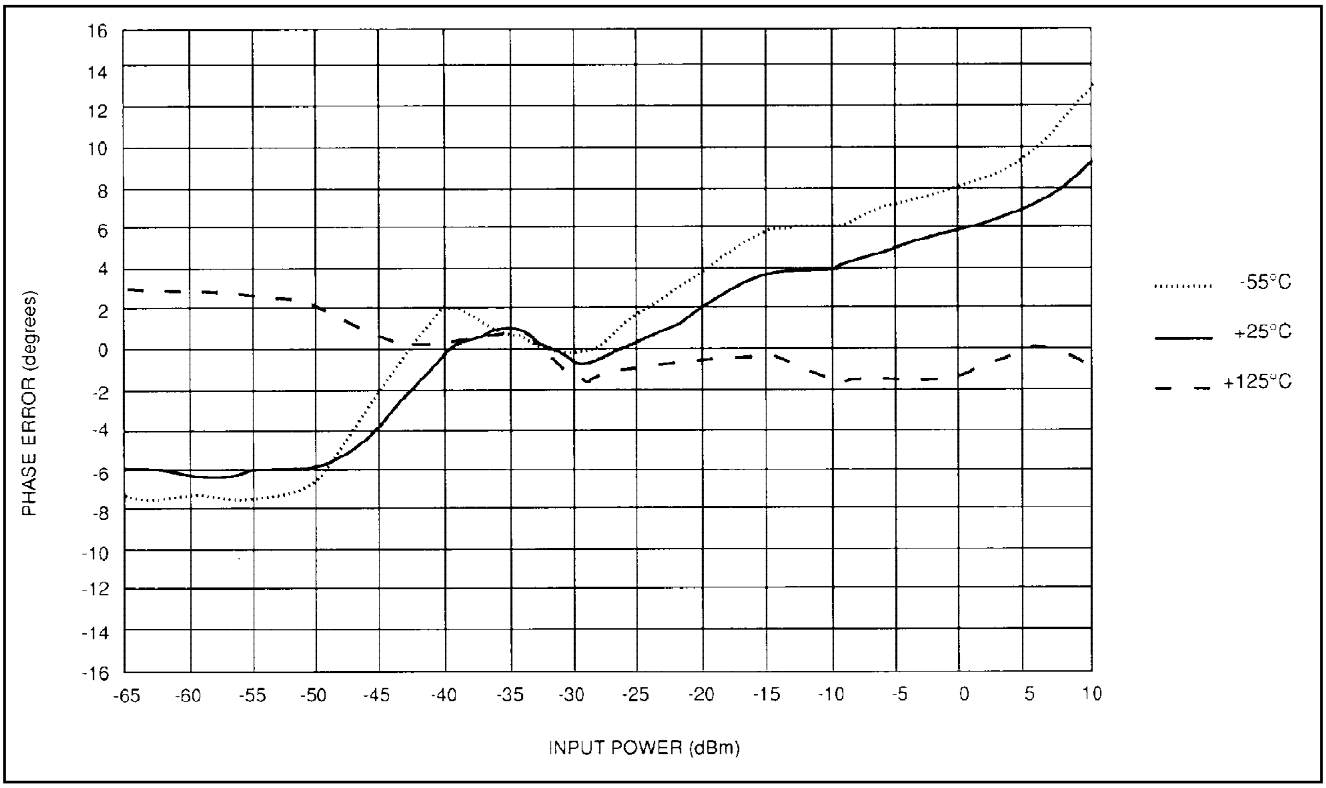


Fig.22 Phase deviation vs CW input level (normalised at -30dBm) at 450MHz across temperature

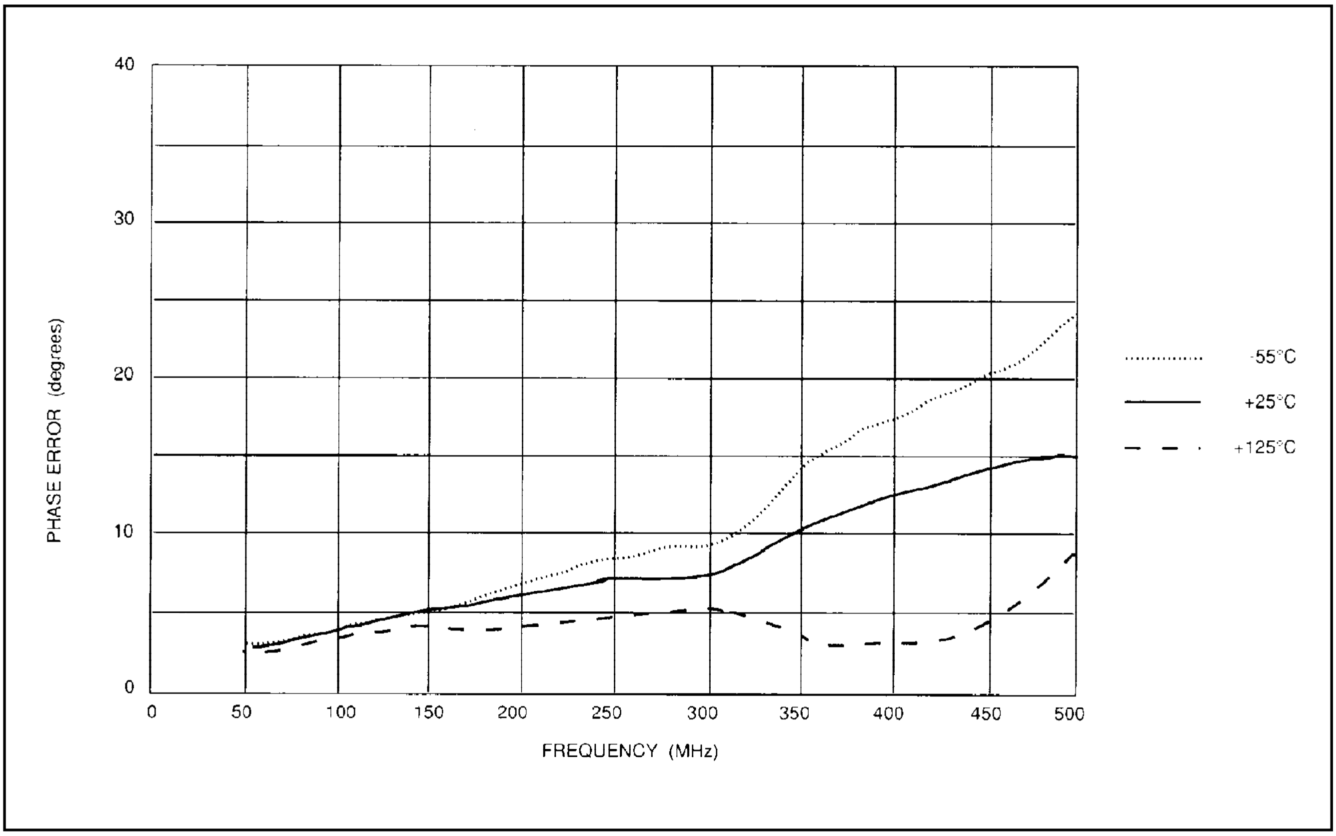


Fig.23 Peak phase deviation over -65dBm → +10dBm CW input level vs CW input frequency. Across temperature

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