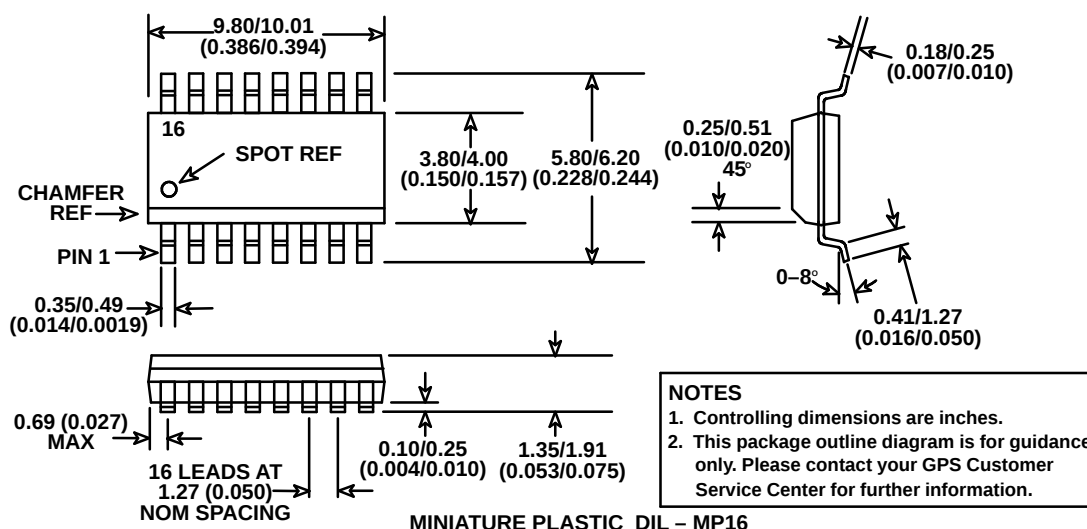


PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information please contact your local Customer Service Centre.



HEADQUARTERS OPERATIONS

GEC PLESSEY SEMICONDUCTORS

Cheney Manor, Swindon,
Wiltshire United Kingdom SN2 2QW.
Tel: (01793) 518000
Fax: (01793) 518411

GEC PLESSEY SEMICONDUCTORS

P.O. Box 660017 1500 Green Hills Road,
Scotts Valley, California 95067-0017,
United States of America. Tel: (408) 438 2900
Fax: (408) 438 5576

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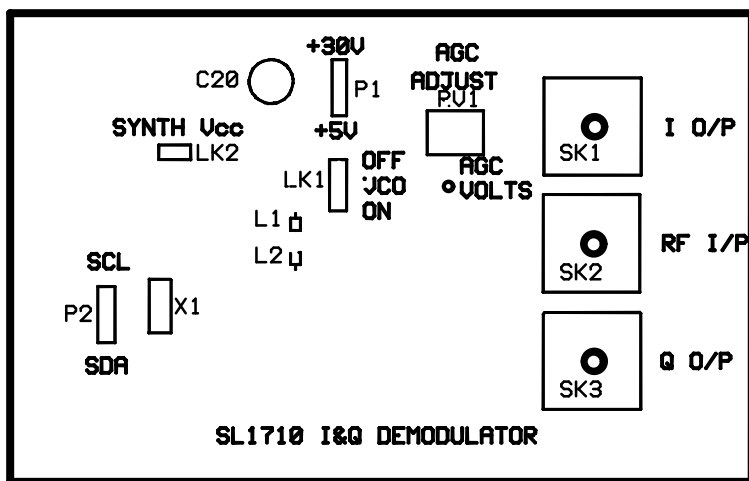


Fig.9 Demonstration PCB top view

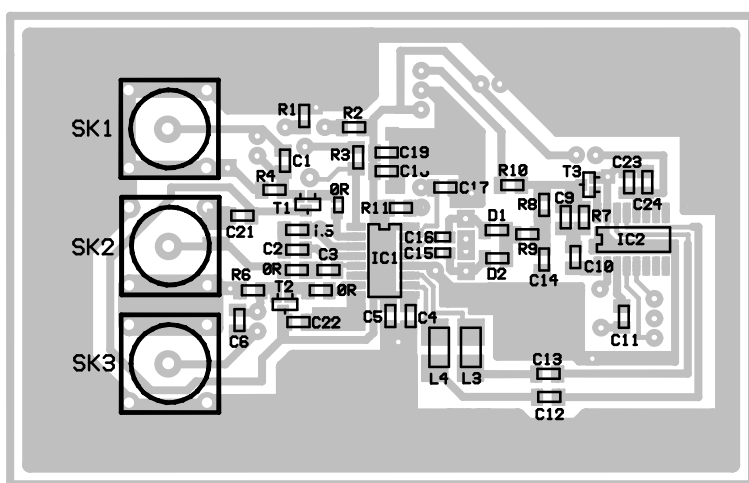


Fig.10 Demonstration PCB bottom view

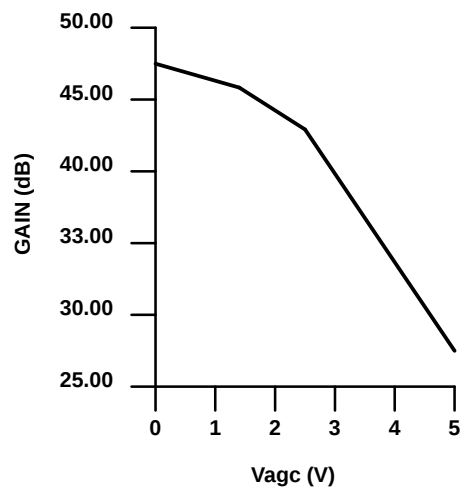


Fig. 6 AGC operation

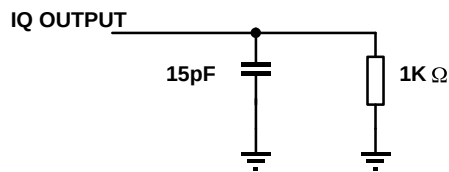


Fig. 7 Maximum IQ output load

Marker	Freq	Zreal	Zimag
1	500KHz	3.5 Ω	0.5 Ω
2	15MHz	4.5 Ω	32 Ω
3	30MHz	56 Ω	92 Ω

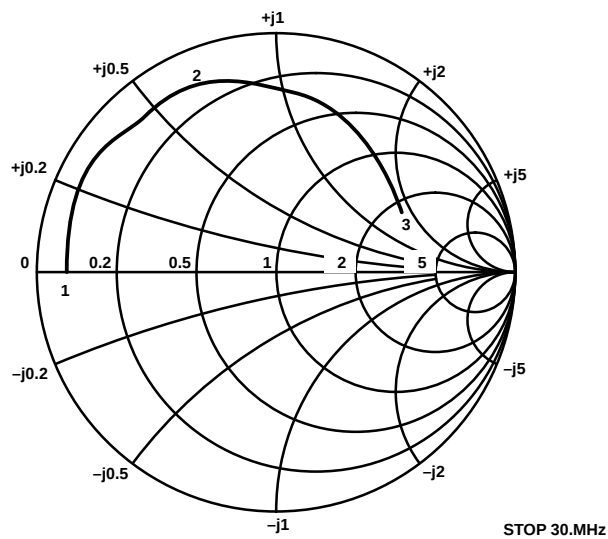


Fig. 8 Output impedance

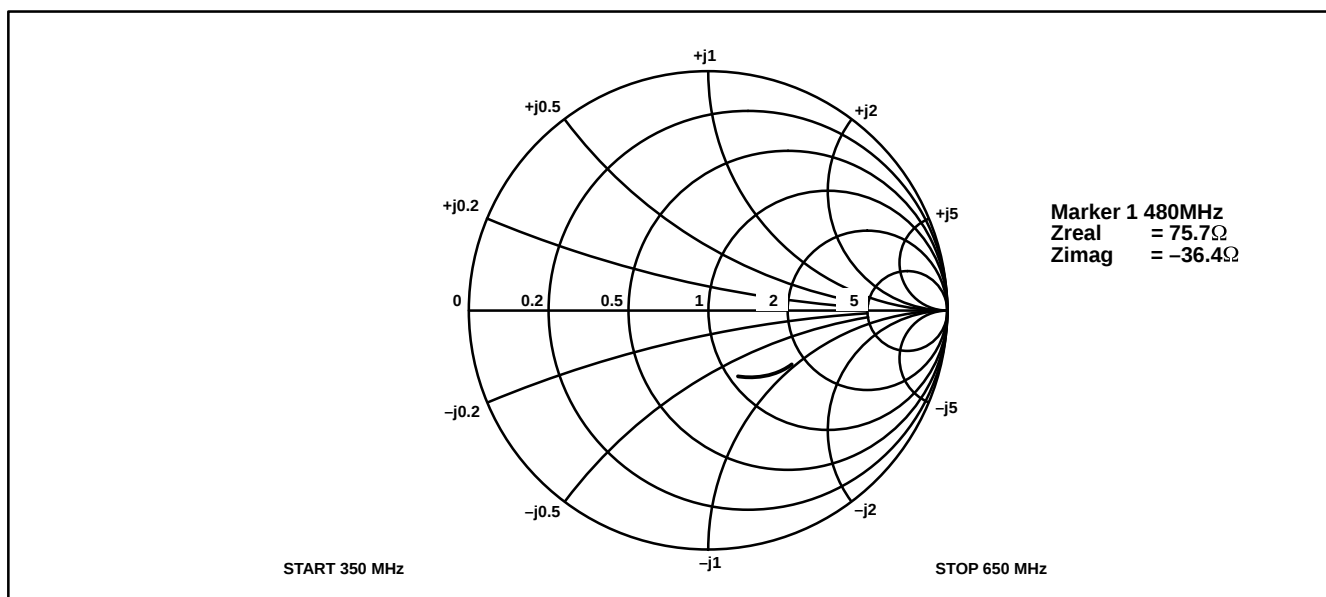


Fig. 4 Input impedance

APPLICATION NOTES

These application notes should be read in conjunction with the circuit diagram Fig 3. and the PCB layout illustrated in Figs 9 & 10. This board has been designed to permit the initial evaluation of the SL1710 performance.

OSCILLATOR

This application uses a synthesised VCO with a tuning range of 350MHz to 500MHz. The inductors L1 and L2 consist of 1.5 turns of 24SWG enamelled copper wire, of 2.5mm diameter. The VCO frequency is controlled by the SP5611 synthesiser which is programmed via an I²C bus. The RF input to the synthesiser is from the SL1710 prescaler outputs via RF inductors L3 and L4.

PRESCALER OUTPUTS

The VCO frequency/32 is available at the differential prescaler outputs, pins 10 and 11. This enables the on board VCO to be synthesised via a PLL.

VCO DISABLE

The on-chip oscillator can be disabled by connecting the VCO Disable (pin 15) to ground and enabled by connecting the pin to V_{CC} via a 4K7 pull up resistor.

AGC

The DC voltage measured at TP1 should be adjusted using VR1 to read 2.5 volts with respect to V_{EE}. This voltage equates

to the nominal centre of the AGC control curve. The control voltage applied to Pin 1 can be varied between 0.5 Volts (maximum gain) and V_{CC}-0.5Volts (minimum gain).

I & Q OUTPUTS

The I and Q output stages of the SL1710 are sensitive to the loads connected to them. To avoid degrading the output signals resistive loads connected to these Pins should always be 1KΩ or greater with a parallel capacitance of 15pF or less.

For evaluation purpose this makes the output unsuitable for connection to test equipment via normal coaxial cables. To alleviate this problem the application board is fitted with emitter follower buffer amplifiers which allow the connection of loads as low as 50Ω via coaxial cables without loading the output stages of the SL1710.

This technique may also be used in a real application where the SL1710 is used to drive an ADC via an anti-alias filter. Great care must be taken to ensure that the loading conditions stated above are not exceeded when designing the anti-alias filter section. Use of an emitter follower buffer is the easiest way to alleviate this constraint.

With the AGC voltage adjusted to 2.5 Volts apply an input signal to the IF IN (Pin 5) and monitor the Base Band output level at the I and Q outputs. Adjust the RF input level until an output level of 760mV pk-pk is achieved. For best performance this level should not be exceeded.

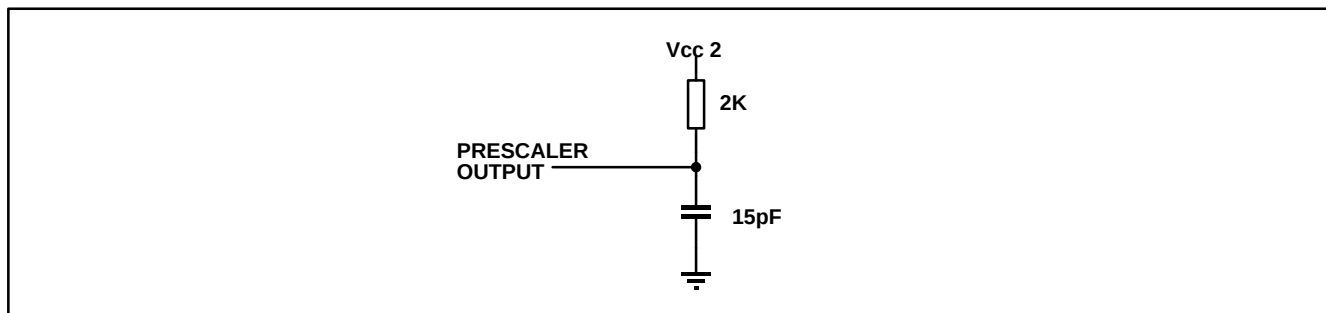
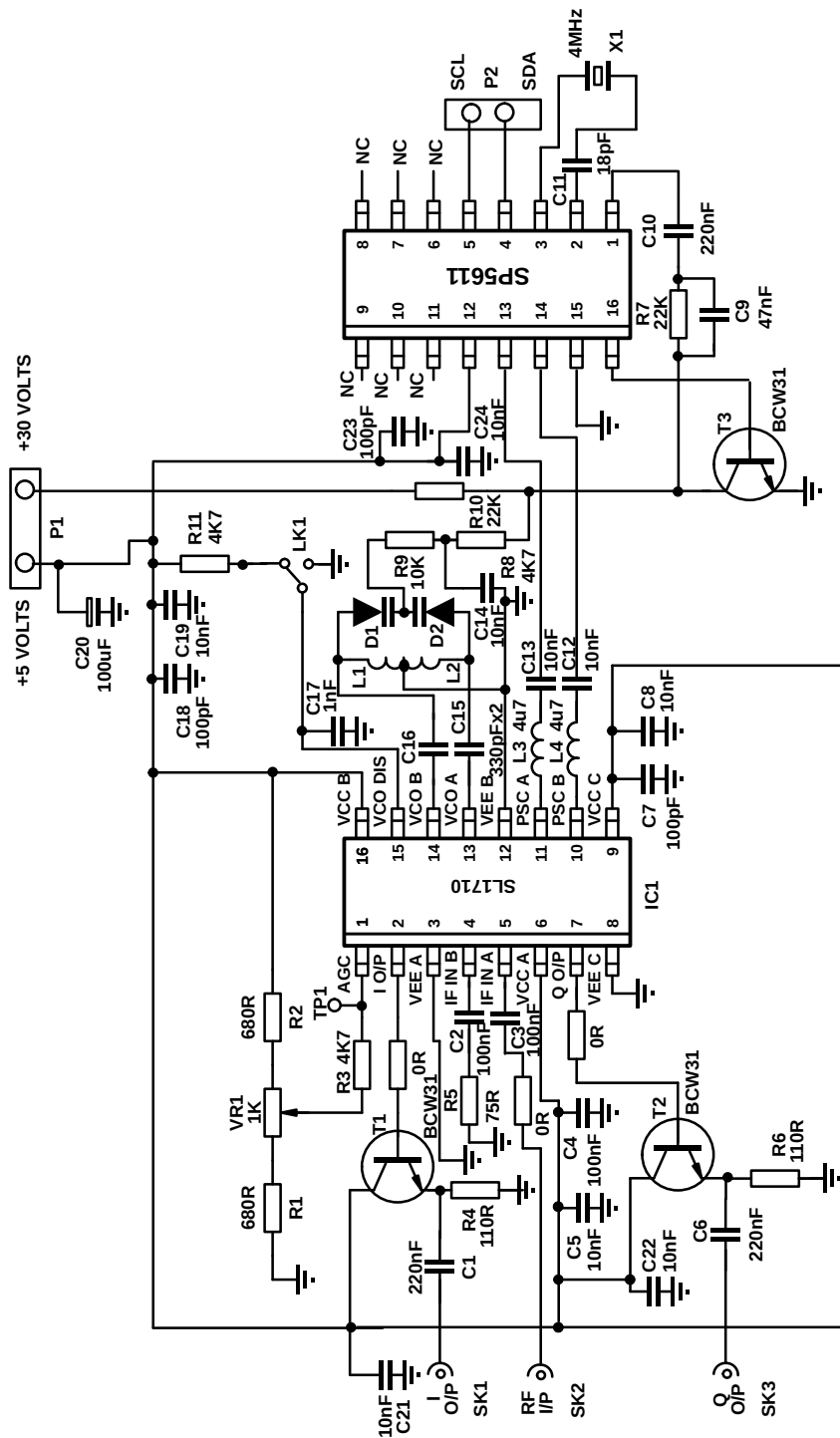


Fig. 5 Maximum prescaler output load.



NOTE:
 D1 - D2 = BB515
 L1 - L2 1.5 TURNS OF 24SWG
 ENAMELLED COPPER WIRE
 2.5mm DIAMETER.

Fig. 3 Demonstration board circuit diagram

ELECTRICAL CHARACTERISTICS (cont.)

$T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC} = +4.75$ to 5.25 volt. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Prescaler sidebands	2, 7		-50	-47	dBV	Measured in IQ outputs
Power supply rejection	2, 7	25	30		dB	Attenuation V_{CC} to IQ outputs, over 0–500kHz

Notes:

1. The choice of L will have an effect on phase noise of the VCO
2. Target value at $f_0=500\text{MHz}$, L (tank)=10nH, Q (tank, unloaded)=50, SSB

DESCRIPTION

The SL1710 is a quadrature downconverter, intended for high linearity, low noise digital satellite applications. It contains all the elements necessary, with the exception of the VCO tuning components, to extract baseband I and Q signal from a QPSK or QAM IF input signal.

A block diagram for the SL1710 is shown in Fig. 2.

In normal consumer digital satellite applications, the device is fed via a SAW filter, centred at the standard IF of 479.5MHz. A filtered single channel is therefore presented to the device, at a typical level of -51dBV. An AGC is included with 18dB of gain control, which is guaranteed to provide an overall conversion gain between 30 and 45dB from the RF input to the I and Q outputs.

The quadrature mixers are fed from an on-chip oscillator

which is centred on the incoming IF. The oscillator external tuning network should be fully symmetric, to ensure optimum gain and phase match.

Single ended I and Q amplifiers are provided, which output a 760mV (p/p) signal, assuming a nominal -51dBV input signal and 40dB gain, suitable for driving a dual channel ADC such as the PCA 869, PCA 913 & PCA 916 via an anti-alias filter (see application notes). The ADC is normally AC coupled via two capacitors (typically 4.7 μF).

The SL1710 also includes divide by 32 prescaler output. These may be fed to an external PLL circuit which can be used to drive the on-chip oscillator, thus forming a complete control loop.

The VCO can be disabled by applying 0V to pin 15.

ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC} = +4.75$ to 5.25 volt. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply voltage	6,9,16	4.75		5.25	V	
Supply current	6,9,16		94	110	mA	
RF Input						
RF freq range	4, 5	350		500	MHz	
Impedance	4, 5		75		ohm	@ 480 MHz. Fig. 4.
VSWR	4, 5			1.7		@ 480 MHz. Fig. 4.
Noise Figure	4, 5			19	dB	AGC at maximum gain
Noise Figure variation with gain	4, 5		0.5	1	dB/dB	
VCO						
V_{CO} freq (fo) control range	13, 14	350		500	MHz	External tank circuit with varicap
Phase noise	13, 14			-85	dBc/Hz	@10kHz from fo. but measured in I or Q output. Note (1, 2)
Fo sensitivity to V_{CC}	13, 14			2	MHz/Volt	Fixed external components and no control loop.
Fo sensitivity to temperature	13, 14			40	KHz/ $^{\circ}\text{C}$	Uncompensated.
Prescaler output, VOH	10, 11	$V_{CC}-0.96$			Volt	At 25°C
VOL	10, 11			$V_{CC}-1.65$	Volt	
Prescaler output duty cycle	10, 11	40		60	%	Under maximum load conditions Fig. 5
AGC						
Gain, Vagc= +2.5V			40		dB	
Temp stability of gain	1			± 2	dB	For any gain setting 0V TO 5V
Gain, Vagc= +0.5V	1	44			dB	See Fig. 6
Gain, Vagc= $+V_{CC}-0.5V$	1			32	dB	See Fig. 6
AGC range			18		dB	
I Q outputs						
						480MHz local oscillator, 481 to 495MHz RF input @-51dBV. Gain set to give -11dBV, 1-15MHz baseband output into maximum load. Fig. 7
Output impedance	2, 7			8	ohm	Fig.8
Output clipping level	2, 7	1.5			V p-p	
I phase lag with respect to Q	2, 7	88	90	92	degs	1-15MHz
IQ crosstalk				20	dB	
Output amplitude match	2, 7			1	dB	I relative to Q, 1-15MHz
Baseband flatness	2, 7			± 1	dB	1-15MHz, 1k Ω 15pF load
Two tone 3rd order intercept point	2, 7	+3			dBV	Referred to output. @ 1MHz Output load 1kohm, 15pF, all AGC settings, 0.7V pk-pk output.
Im3	2, 7	28			dBc	
LO, and Spurii in IQ outputs	2, 7			-30	dBV	1-100MHz

SL1710

QUADRATURE DOWNCONVERTER

(Supersedes version in October 1995 Media IC Handbook, HB3120-3)

The SL1710 is a quadrature downconverter intended for use with both Professional and Consumer Digital Satellite Applications.

The device contains high linearity, low noise amplifiers, quadrature mixers, plus an on-chip oscillator, operating between 350MHz and 500MHz, which may be synthesised via the differential prescaler outputs.

An AGC with 18dB gain control is provided to cope with a wide range of input signal levels.

I and Q outputs are via low impedance single ended amplifiers. These may be connected to a dual channel analog to digital converter such as the PCA869, 913 and 916 via a suitable anti-alias filter.

FEATURES

- Wide input frequency range (350–500MHz)
- On-chip VCO with quadrature generation, Phase match better than $\pm 2^\circ$, gain match better than 1dB
- Nominal 40dB conversion gain from IF input to I and Q outputs
- AGC amplifier with 18dB gain control range
- Low impedance I and Q single ended outputs, with 15MHz ± 1 dB BW
- Divide by 32 prescaler outputs
- Suitable for QPSK and up to 64QAM systems

APPLICATIONS

- Consumer digital satellite decoders
- Professional digital satellite decoders
- Communication systems

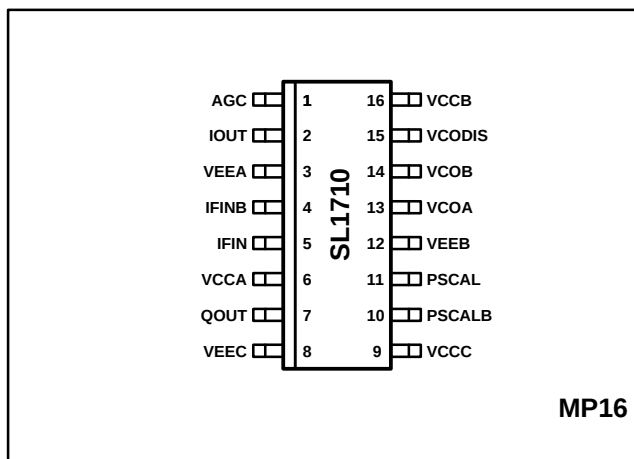


Fig. 1 pin connections top view

ORDERING INFORMATION

SL1710/KG/MPAS
SL1710/KG/MPAD (Tape & Reel)

ABSOLUTE MAXIMUM RATINGS

Storage temperature	–55°C to +150°C
Junction temperature	–20°C to +150°C
Supply voltage	–0.3 to +7.0V
Voltage at any other pin	–0.3 to +7.0V

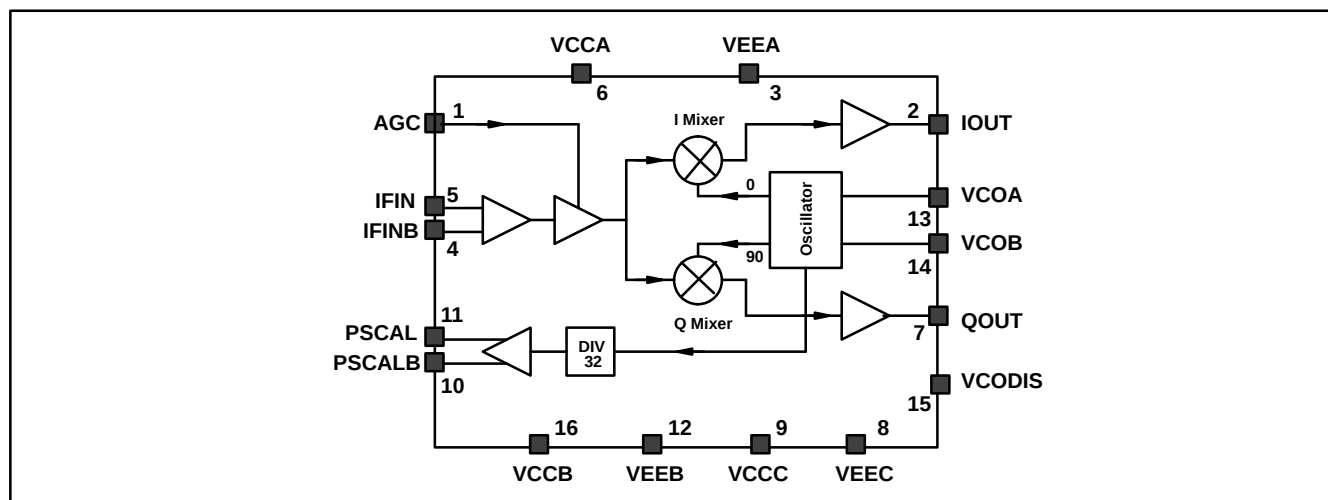


Fig. 2 SL1710 block schematic