PRELIMINARY DATA SHEET

SDA 9389X PIP III Plus Digital Picture-in-Picture Processor

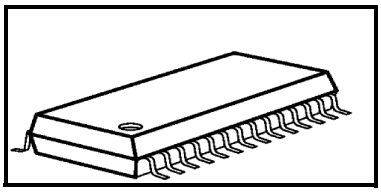
Edition March 23, 2001
6251-550-1PD

MICRONAS

Digital Picture-in-Picture (PIP) Processor SDA 9389X
PIP IIIplus

Version 1.04 **CMOS**

General Description:



P-DSO-28-1

SDA 9389X is a single chip Picture-in-Picture Processor which generates a picture of reduced size from a video signal (inset channel) for the purpose of combining it with another video signal (parent channel). The easy implementation of the IC into an existing system needs only a few additional external components. At Micronas, the fundamental idea behind developing a new generation of PIP ICs was to create a single-chip solution with integrated digital color decoder and data-slicer for violence blocking capability. Due to the NTSC-M and PAL-M color decoder the SDA 9389X 'PIP IIIplus' is especially suited for the american, korean and japanese market. PAL-N signals can also be processed to a certain extent. On a single chip, the 'PIP IIIplus' integrates analog functions (A/D converter, D/A converter, clock generation) with a 72 kbit memory and digital signal processing logic (color decoding, horizontal and vertical filtering, signal processing after storage).

Figure 0-1 Picture-in-Picture

A picture reduction to 1/9, 1/16 and 1/36 of original size is possible. The transfer functions of the decimation filters are optimally matched to the selected picture size reduction and can furthermore be adjusted to the viewer's requirements by a selectable peaking. A maximum of 112 luminance and 2x28 chrominance pixels per line are stored in the memory

Type	Ordering Code	Package
SDA 9389X(Tape and Reel)	Q67107-H5218	P-DSO-28-1

Content

1 Features:

- **Single chip solution:**
  - CVBS-Clamping, AD-conversion, AGC, chroma decoding, sync separation, filtering, field memory, RGB-matrix, DA-Conversion, RGB-switch and clock generation integrated on one chip
- **Analog inputs:**
  - 3 x CVBS; selectable via I^2C bus
  - 7 bit analog-digital conversion
  - Automatic Gain Control (AGC) or adjustment of input amplitude range via I^2C bus alternatively
- **Chroma Decoder**
  - NTSC M, PAL M, PAL N
  - Automatic standard detection
  - Automatic Chroma Control (-24dB ... +6 dB)
  - Adjustable Chroma Saturation and Hue Control
  - Only one crystal necessary for all color standards
- **Data slicing**
  - To achieve a violence blocking capability Closed Caption data is sliced
  - XDS type and class filter may be adjusted
- **Decimation**
  - 3 picture sizes: 1/9, 1/16 or 1/36 of normal size
  - Horizontal and vertical filtering
- **Display:**
  - Resolution up to 112 luminance and 28 chrominance pixels per inset line for picture size 1/9 and 1/36
  - 6-bit amplitude resolution
  - Digital interpolation for anti imaging
  - Field and frame-mode display
  - Adjustable transient improvement (peaking)
  - Contrast, brightness and pedestal level adjustable
  - Offset correction (blacklevel vs. blanking level)
  - POP display (3 pictures live or still, all pictures of one source only)
  - 16:9 compatibility: Operation in 4:3 and 16:9 sets
  - Colored background
  - Line doubling mode for progressive scan applications
  - Freeze picture
- **Analog outputs:**
  - YUV mode:Y, +(B-Y), +(R-Y) or Y, -(B-Y), -(R-Y)
  - Two RGB matrices: NTSC (Japan, USA)
  - Insertion of external RGB source possible
  - Programmable position of inset picture:
  - Coarse positioning at 4 corners of the parent picture

Features:

  - Fine positioning at steps of 4 pixels and 2 lines
- **Programmable framing:**
  - 64 frame colors
  - Variable frame width
  - Variable frame height
  - Frame giving a three dimensional impression
- **I^2C-Bus control**
- **High stability clock generation**
- **PDSO 28-1 package (SMD)**
- **fully SDA 9388X compatible**
- **SDA 9488X and SDA9489X compatible**
- **5 V supply voltage**

2 Application Environment

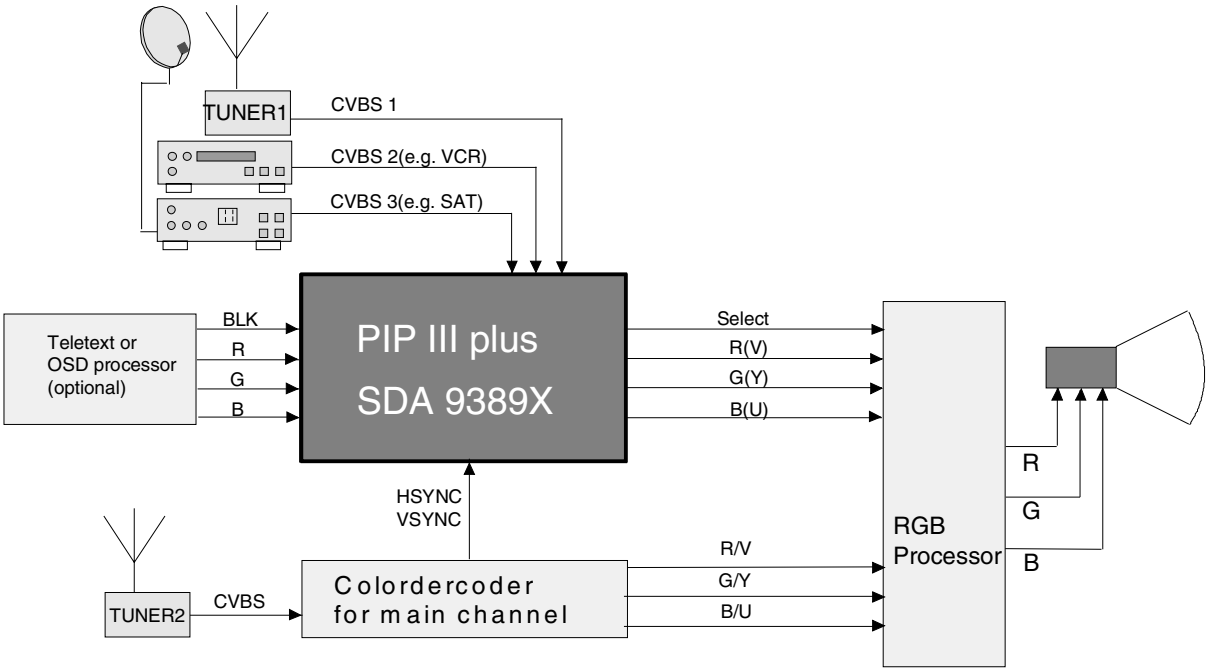


Figure 2-1 Application overview

3 Pin Configuration

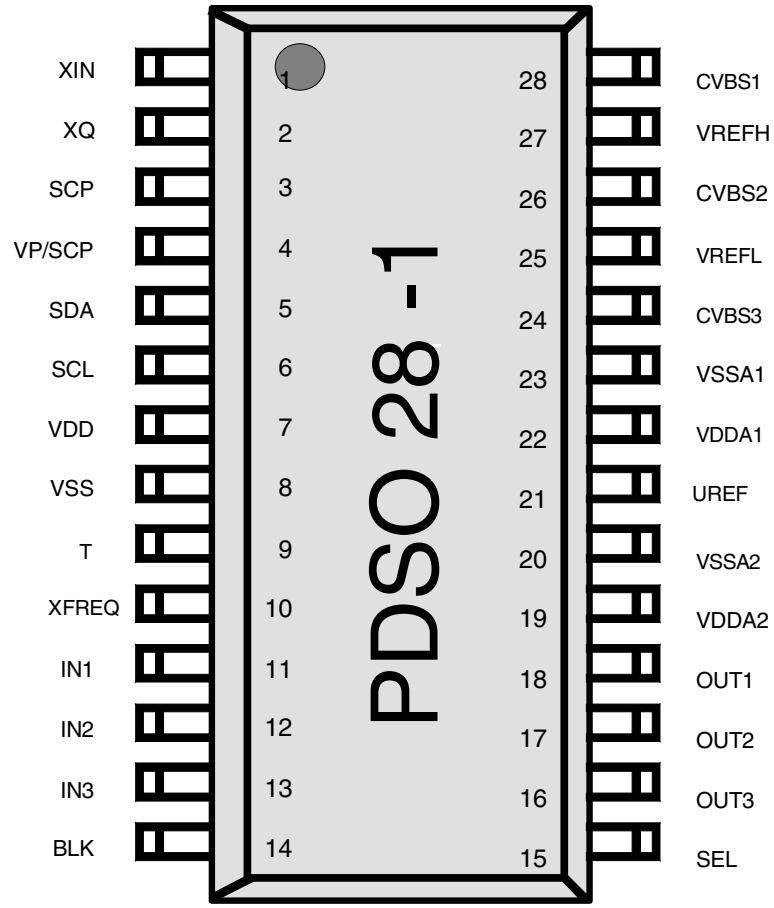


Figure 3-1 Pinout

3.1 Pin Description

Pin No.	Symbol	Type	Description
1	XIN	I	crystal oscillator (input) or crystal clock (from another IC)
2	XQ	Q	crystal oscillator (output)
3	SCP	I_{3-L}	horizontal sync for parent channel or sandcastle including V-sync
4	VP/SCP	I_{3-L}	vertical sync for parent channel or sandcastle including V-sync
5	SDA	I/Q	I^2C-bus data
6	SCL	I	I^2C-bus clock
7	VDD	S	digital supply voltage
8	VSS	S	digital ground
9	T	I	connect to VSS
10	XFREQ	I/Q	crystal frequency
11	IN1	I/ana	R Input for external RGB source
12	IN2	I/ana	G Input for external RGB source
13	IN3	I/ana	B Input for external RGB source
14	BLK	I	fast blanking input for RGB switch, DAC outputs switched off if BLK is high
15	SEL	Q	fast blanking output for PIP / RGB mode (Tristate), if BLK is high also SEL output is high
16	OUT3	Q/ana	analog output: chrominance signal +(B-Y) or -(B-Y) or B
17	OUT2	Q/ana	analog output: luminance signal Y or G
18	OUT1	Q/ana	analog output: chrominance signal +(R-Y) or -(R-Y) or R
19	VDDA2	S	analog supply voltage (V_{DDA}) for DAC
20	VSSA2	S	analog ground (V_{SSA}) for DAC
21	UREF	I/ana	reference voltage for DA-converters
22	VDDA1	S	analog supply voltage (V_{DDA}) for ADC
23	VSSA1	S	analog ground (V_{SSA}) for ADC
24	CVBS3	I/ana	CVBS Input 3 (selectable via I^2C-bus)
25	VREFL	I/Q	reference voltage (low) for ADC
26	CVBS2	I/ana	CVBS Input 2 (selectable via I^2C-bus)
27	VREFH	I/Q	reference voltage (high) for ADC
28	CVBS1	I/ana	CVBS Input 1 (selectable via I^2C-bus)
			I= Input / ana=analog / $_{3-L}$=3 level / Q= Output / TTL=Digital (TTL) S=Supply voltage

Table 3-1 Pinout description

4 Block Diagram

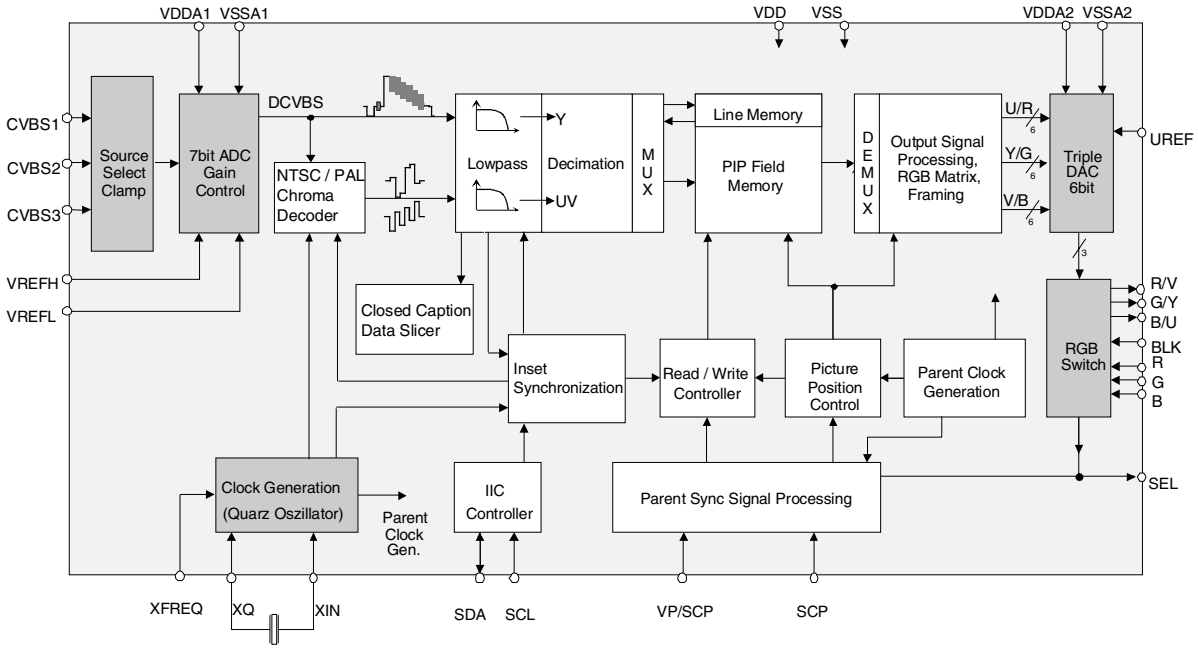


Figure 4-1 Block Diagram

5 System Description

5.1 AD-Conversion, Clock Generation

The analog inset CVBS signal can be fed to the inputs CVBS1-3 of SDA 9389X (amplitude 0.7-2 V_{pp}). Each of these input signals can be selected via I^2C bus (CVBSEL). After clamping to the sync bottom the signal is AD-converted with an amplitude resolution of 7bit. The conversion is done by using a 27 MHz clock which is not related to the incoming CVBS signal.

The clamp timing for the analog input is generated from the CVBS signal. No external sync signals are required for the inset channel. Three different types of crystals can be chosen:

- 13.5 MHz fundamental mode, or
- 27 MHz fundamental mode, or
- 27 MHz third overtone mode.

The crystal can be chosen via pin XFREQ. When XFREQ is connected to V_{dd} the PIP is initialized for a 13.5 MHz crystal. When using a 27 MHz crystal, XFREQ must be connected to V_{ss}.

For crystal specifications, please refer to section 8 and 12.

5.2 Automatic Gain Control

To accommodate different CVBS input voltages an automatic gain control has been implemented. To avoid control oscillation, the adjustment is carried out only after power on or resynchronisation of the video source. The chip works correctly for input voltages in the range from 0.7 to 2 V_{pp}. For best signal-to-noise ratio, the maximum amplitude is recommended when available. Alternatively the fixed adjustment of input range via I^2C bus is possible (AGC[3:0]; AGCFIX=1). The characteristic for U_{ref}=5V is shown in the picture below.

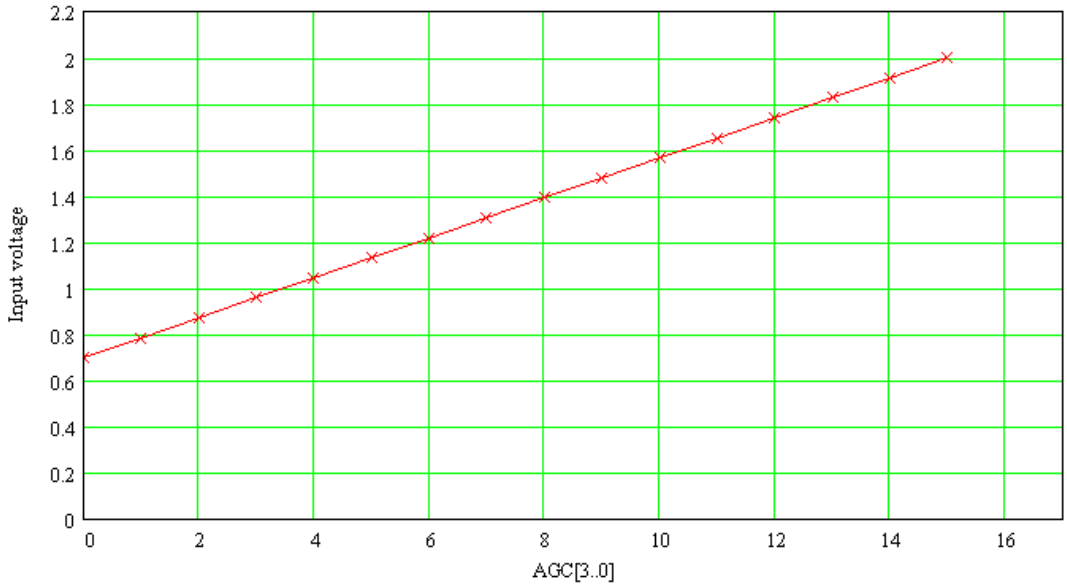


Figure 5-1 Expected input voltage by using the AGC adjustment via I^2C

The correct setting for $1V_{pp}$ input signals is AGC[3:0]= ’0101’ and AGCFIX=’1’.

5.3 Inset Synchronization

Horizontal and vertical sync pulses are separated after elimination of the high frequency components of the CVBS signal by a low pass filter. Horizontal sync pulses are generated by a digital phase-locked-loop. The time constant can be adjusted between fast and slow behavior in four steps (PLLITC[1:0]) to accommodate different input sources (e.g. VCR).

5.4 Chroma Decoding

In order to obtain the chrominance information the digitized video signal has to be multiplied with the re-generated color subcarrier once in-phase and once phase-shifted by 90°. After lowpass filtering digital UV is available. The subcarrier is regenerated by a digital PLL.

Reference for the subcarrier generation is a crystal stable clock of 27.000 MHz. In order to avoid color standard detection problems, the maximum deviation of this frequency should not exceed 100ppm and should be as low as possible. A small frequency adjustment (-50 ... +110 ppm) is possible when using a crystal with small frequency deviations (INCRA[4:0]).

The system is able to decode NTSC M and PAL M/N signals with a subcarrier frequency of about 3.58 MHz. Phase of the demodulation can be influenced by the Hue Control (HUE[5:0]) between -44.8° and 43.4° in steps of 1.4°(NTSC only).

For variations in the chroma signal upto 30dB, a stable output amplitude after chroma decoding is achieved due to the ACC (Automatic Chroma Control). When the chroma signal (color burst) is below a selectable threshold (CKILL: -24 dB, -18 dB or -12 dB), the color will be switched off. Alternatively the color-killer can be bypassed and the color can be switched on or off under all conditions.

Color killer theshold[1)]			
	NTSC	**PAL-M**	**CKILL**
color on	-9.3 dB	-9 dB	00
color off	-13 dB	-12.5 dB	
color on	-15.8 dB	-16.7 dB	01
color off	-19.3 dB	-20.5 dB	
color on	-21.2 dB	-21.9 dB	10
color off	-26.8 dB	-27.9 dB	
	color off	color off	11

1) typical values, assuming standard signals according to ITU-R BT.470-3 and recommended operating range

An automatic norm detection or preset mode can be chosen (CSTAND[1:0]).

5.5 Filtering and Scaling

Luminance and chrominance signals are filtered in horizontal and vertical direction.

The horizontal and vertical picture size is freely programmable (SIZEHOR, SIZEVER). The transfer functions of the decimation filters are optimally matched according the selected reduction of picture size. A small reduction of horizontal picture size is accessible with PICSZE.

			PICSZE=0				PICSZE=1		
SIZEHOR1	SIZEHOR0	horizontal scaling	Y	(B-Y)	(R-Y)		Y	(B-Y)	(R-Y)
0	0	3:1	108	27	27		112	28	28
0	1	4:1	82	20.5	20.5		84	21	21
1	1	6:1	108	27	27		112	28	28
1	0	(reserved)							

Table 5-1 Number of stored pixel

SIZEVER1	SIZEVER0	vertical scaling	PIP lines
0	0	3:1	70
0	1	4:1	53
1	1	6:1	35
1	0	(reserved)	

Table 5-2 Number of stored lines

5.6 Luminance Peaking-Filter

To improve picture sharpness, a peaking filter is provided, which amplifies higher frequencies of the input signal. The amount of peaking can be varied in seven steps from ’000’ to ’111’. The setting ’000’ switches the peaking off; ’100’ is the recommended value. The characteristic for all possible settings is shown in Table 5-3 and its characteristic in Figure 5-2.

YPEAK2	YPEAK1	YPEAK0	peaking
0	0	0	**0** (= off)
0	0	1	weak
0	1	0	
0	1	1	
1	0	0	nominal (recommended)
1	0	1	
1	1	0	
1	1	1	strong

Table 5-3 Peaking values

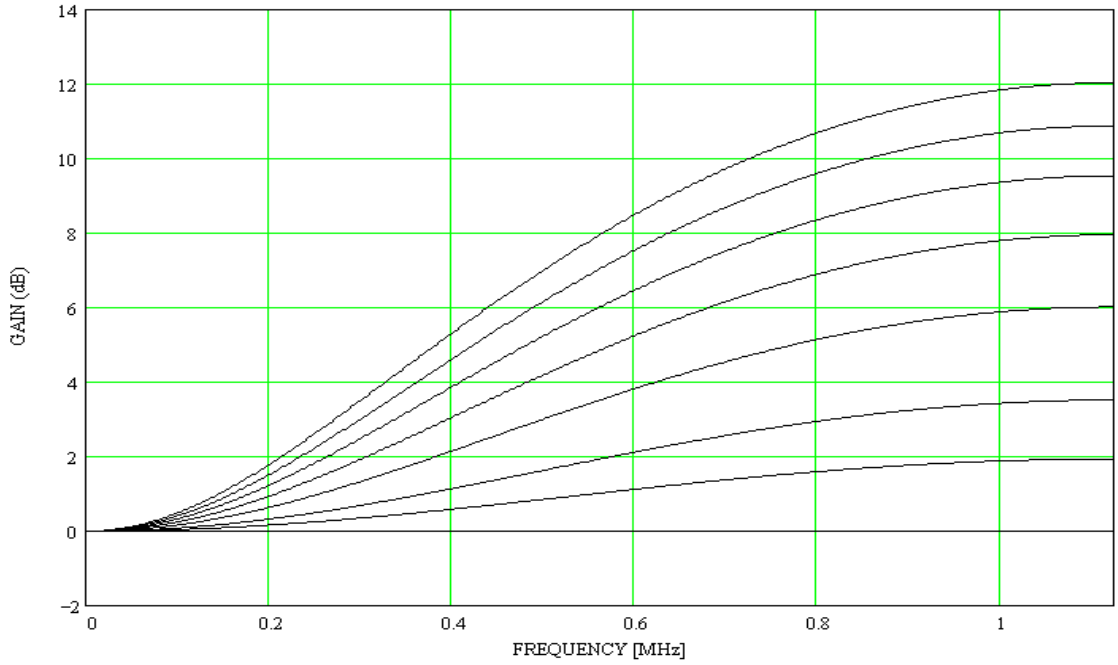


Figure 5-2 Characteristic of various peaking factors

Coring should be switched on (YCOR) to reduce noise, which is also amplified when peaking is chosen. As the coring stage is in front of the peaking filter, 1LSB noise will not be peaked.

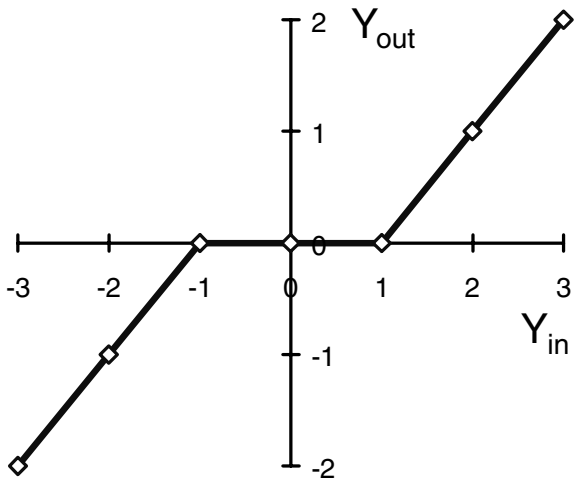


Figure 5-3 Coring Characteristic

With YDEL the phase between luma and chroma can be adjusted by +/- 1 pixel.

5.7 Offset correction

According to ITU-R BT.470-3 a 7.5 IRE difference between black and blanking level occurs for NTSC and PAL M signals. When necessary, this offset can be reduced by LMOFST. For adjustment to the offset correction of the decoder of the main channel, three settings are available (approximately 6, 7.5 or 9 IRE resp.)

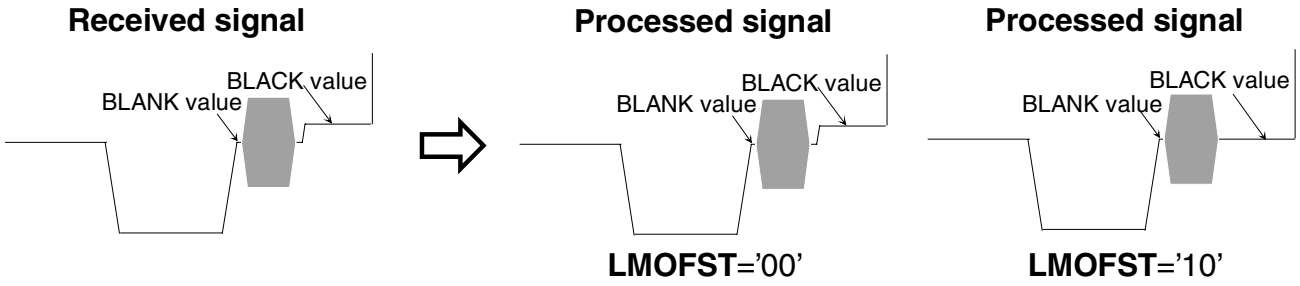


Figure 5-4 Without and with offset correction

PAL N signals (Argentina) do not include this offset.

5.8 Closed Caption Data Slicer

Closed Caption data (’Line 21’) is sliced by the digital data slicer and is readable from I^2C. Raw CC as well as prefiltered data is provided. With a built in programmable XDS-Filter, the program-rating information (’V-chip’) can be filtered out.

The linenumber of the sliced data is selectable with SELLNR between line 21 and line 20. The Closed Caption data is assumed to be conform to the ITU standards EIA-608 and EIA-744.

5.9 Class and Type Filter

Raw CC as well as prefiltered data is provided alternatively. With a built in programmable XDS-Filter, the program-rating information as well as others can be filtered out. The XDS extensions of Closed Caption are sent only in second field of Line 21.

In the following table all selectable Class filter are shown.They can be used to reduce traffic on the I²C bus and to reduce calculation power of the main controller. When no Class is selected, all incoming data (both fields) is sliced and fed to the I²C output. When one or more class filter are chosen, only data in field 2 is sliced. Any combination of class filter is allowed.

XDSCLS4	XDSCLS3	XDSCLS2	XDSCLS1	XDSCLS0	selcted Class
0	0	0	0	0	no Class selected (transparent mode)
1	X	X	X	X	’Current Class’
X	1	X	X	X	’Future Class’
X	X	1	X	X	’Channel Class’
X	X	X	1	X	’Misc. Class’
X	X	X	X	1	’Public Class’

Table 5-4 selectable CLASS filter

Each ’CLASS’ is divided into ’TYPES’ which can be sorted out by the XDS-secondary filter(XDSTPE[2..0]). Any combination of type filter is allowed. Type filter often make sense only with the appropriate class filter.

XDSTPE2	XDSTPE1	XDSTPE0	Type number (according EIA 608)	selcted Type (examples)
0	0	0		no data is filtered out.
0	0	1	05h	program rating (PR) only
0	1	0	01h,04h	Time information only
0	1	1	40h	out of band only
1	0	0	01h,02h,03h, 04h,0Dh,40h	VCR information
1	0	1	01h, 04h,05h	Time information only and PR
1	1	0	05h,40h	out of band only and PR
1	1	1	01h,02h,03h, 04h,05h,0Dh,40h	VCR information and PR

Table 5-5 selectable TYPE filter

5.10 Indication of new data

The sliced and filtered data is available in DATAA[7..0] and DATAB[7..0]. Every time new data arrives, DATAV becomes 1. Every time both databytes are read DATAV becomes 0 until new data arrives. It must be ensured that the data polling is activated once per field (16.7 or 20 ms) or every second field (33.3 or 40 ms), depending on the slicer configuration and program field frequency. When ACQNEW equals ’0’, one data line is buffered to allow one later polling access.

5.11 Memory Control

The embedded memory stores one decimated field of the inset picture. Its capacity is 70560 bits.

In field-mode display just every second inset field is written into the memory whereas in frame-mode display the memory is continuously written with every incoming field. Data is processed with the lower memory clock frequency depending on the horizontal decimation factor. For progressive scan conversion systems and HDTV / VGA displays a line doubling mode is available (LINEDBL). Every line of the inset picture is read twice.

At scan conversion modes only 3:1 and 4:1 horizontal scaling and field-mode can be used. Memory writing is stopped by FREEZE register; an unchanged field is permanently read out of the memory.

Frame-mode display is possible for standard 60 Hz (NTSC / PAL M) video sources at inset and parent channel (or both 50 Hz (PAL N) respectively). The result is a higher vertical and time resolution as every incoming field is displayed.

For this purpose the inset and parent channel are internally analyzed and activation of frame-mode display is blocked automatically when at least one of the following conditions is not fulfilled:

- inset and parent channel have equal field frequencies
- the number of lines is between 260 - 265 (310 - 315 resp.) (standard signals according to ITU)
- interlace is detected for inset and parent

Depending on the phase between inset and parent signals a correction of the display raster for the read out data is performed. Synchronization of memory reading with the parent channel is achieved by processing the parent horizontal and vertical synchronization signals. Either separated horizontal and vertical pulses or sandcastle pulse are possible. The signals are fed to the IC at pin SCP for horizontal synchronization and pin VP/SCP for vertical synchronization. The sandcastle pulse can be used at pins SCP or VP/SCP if it fulfills the specification of the input pin (PARSYN).

PARSYN	
00	parent sync. TTL signals read via pins VP/SCP and SCP
01	parent sync. sandcastle for double frequency read via pin VP/SCP
10	parent sync. TTL signals read via pins VP/SCP and SCP (burstgate)
11	parent sync. sandcastle via pin SCP

Table 5-6 Parent Synchronization

The setting ’10’ is used for a burstgate pulse from color decoder of main channel. All other settings are timed for using the horizontal pulse as timing information. From these external signals HSP (horizontal sync pulse) and VSP (vertical sync pulse) are derived. The timing between HSP and VSP is used to obtain the parent field number. As the external VSP and HSP signals can come from different devices with different delay paths, the phase between both can be adjusted for correct field identification (VSPDEL).

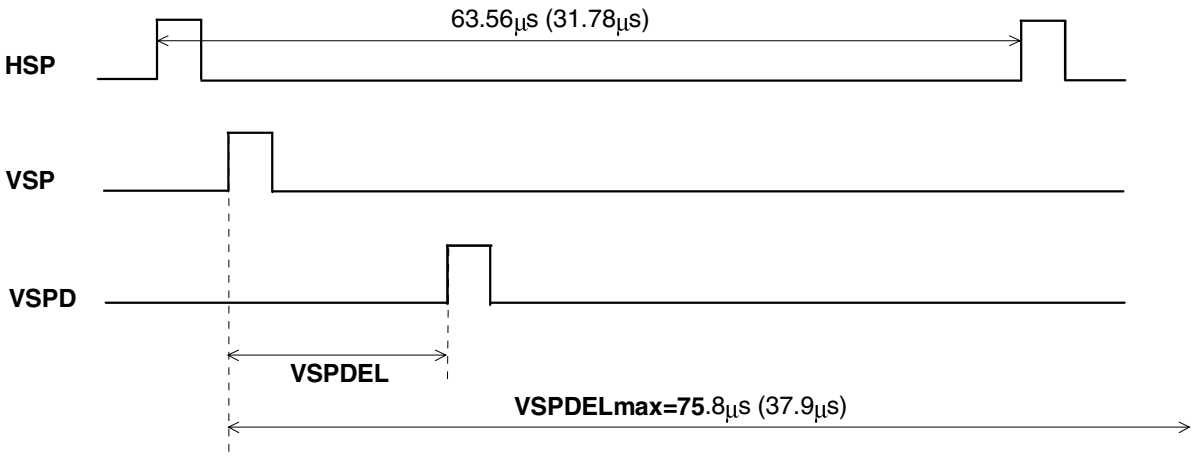


Figure 5-5 Phase adjustment of vertical pulse

Usually a noise reduction of the incoming parent vertical pulse is performed. With this function a missing vertical pulse is inserted. It can be disabled with VSPISQ.

A great variety of combinations of inset and parent settings are possible. The following table shows all usual and unusual constellations

Inset Frequency	Parent Frequency	frame-mode possible	field-mode possible	correct aspect ratio	picture size 1/9, 1/16	picture size 1/36	READD	LINEDBL
50	50	√	√	√	√	√		
50	60		√		√	√		
60	50		√		√	√		
60	60	√	√	√	√	√		
50	50 (progr.)		√	√	√		1	1
50	60 (progr.)		√		√		1	1
60	50 (progr.)		√		√		1	1
60	60 (progr.)		√	√	√		1	1
50	100[1)]	√	√	√	√	√		
50	120[1]		√		√	√		
60	100[1]		√		√	√		
60	120[1]	√	√	√	√	√		
50	100[2)]		√	√	√		1	
50	120[2]		√		√		1	
60	100[2]		√		√		1	
60	120[2]		√	√	√		1	

[1)]combination before upconversion

[2)]combination after upconversion (upconversion done by PIP)

Table 5-7 Combinations of inset and parent vertical frequency

5.12 Picture Positioning

The display position of the inset picture is programmable to the 4 corners of the parent picture (CPOS[1:0]). From there PIP can be moved to the middle of the TV Picture with POSHOR[7:0] and POSVER[6:0]. If standard signals are used for synchronization the values for POSHOR and POSVER are the same for each coarse position. The frame elements are always placed outside the Inset Picture, except for the inner shade of three dimensional frame. There is no shift of the inset picture position if the inset frame width is modified. Depending on coarse position, one PIP corner remains stable when changing the picture size

CPOS[1:0]	POSITION	REFERENCE CORNER of Inset Picture	increasing POSVER= moving direction	increasing POSHOR = moving direction
00	upper left	upper left	down	right
01	upper right	upper right	down	left
10	lower left	lower left	up	right
11	lower right	lower right	up	left

Table 5-8 PIP coarse positioning

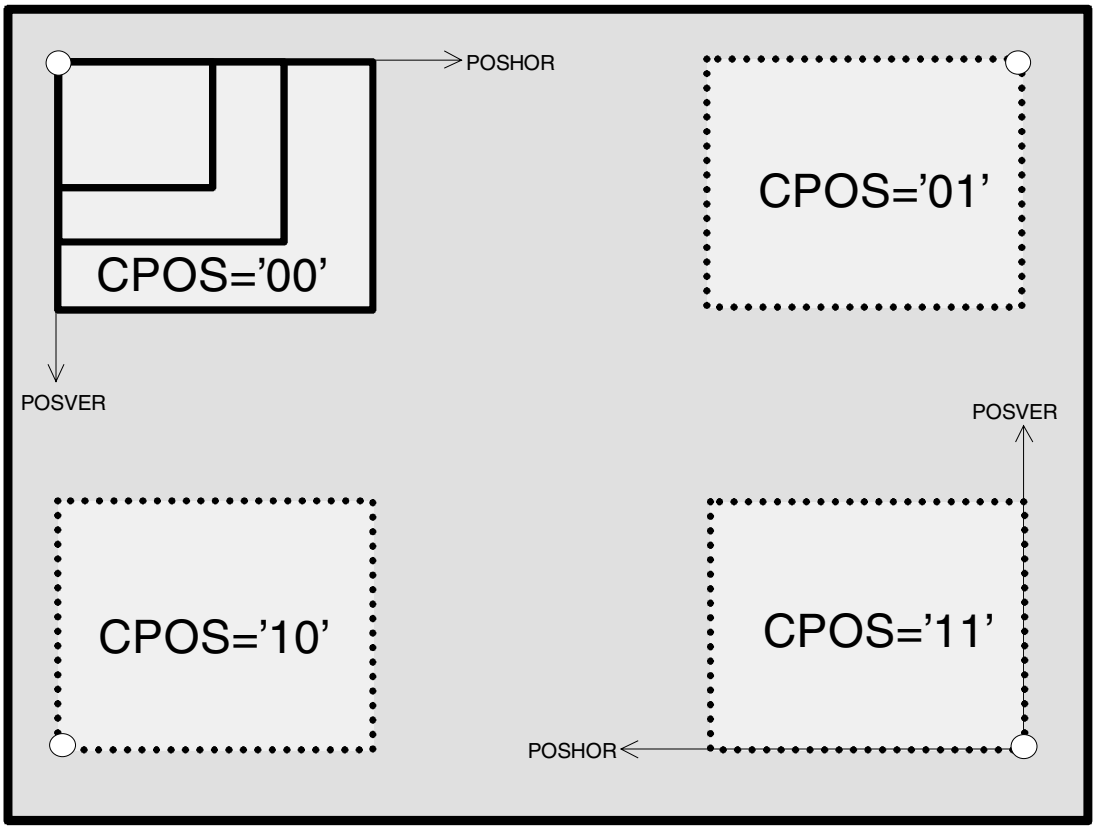


Figure 5-6 PIP Positioning

Starting at every coarse position, the picture can be moved to 256 horizontal locations (4 pixel increments) and 128 vertical locations (2 line increments). Even POP-positions (Picture Outside Picture) in 16:9 applications are possible.

5.13 Postprocessing

The postprocessing improves the transient behavior of the YUV signals. The multiplier in the UV signal path adjusts the color saturation depending on SAT register in 16 steps between 0 and 1.875 (SAT[3:0]). The read frequencies of the YUV signals are changing with the picture size. A double line frequency for 100/120 Hz applications is possible for all picture sizes except 1/36.This can be done by setting READD to '1'. Doubling of the horizontal size is possible using PIXDBL.

5.14 RGB Matrix

The chip contains two different matrices, one for Japan and one for USA, which are selectable via I^2C-signal MAT. The matrices differ in the magnitudes and angles of the color-difference signals and are derived from the original matrix defined by television

standards. This modification should give a better reproduction of skin color and adjusts the color reproduction to the used colorimetry for transmission and the chromaticity of the picture tube.

NTSC-USA (MAT=0)**:**

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} Y \\ U \\ V \end{bmatrix} \cdot \begin{bmatrix} 1 & -0{,}5312 & 1{,}9687 \\ 1 & -0{,}1875 & -0{,}5625 \\ 1 & 2 & 0 \end{bmatrix}$$

NTSC-Japan (MAT=1)**:**

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} Y \\ U \\ V \end{bmatrix} \cdot \begin{bmatrix} 1 & -0{,}125 & 1{,}5625 \\ 1 & -0{,}3125 & -0{,}5312 \\ 1 & 2 & 0 \end{bmatrix}$$

5.15 Framing and colored Background

A colored frame can be added to the inset picture. The chip can display two different types of frames: one simple monochrome frame and a more sophisticated three dimensional frame (FRSEL)

.

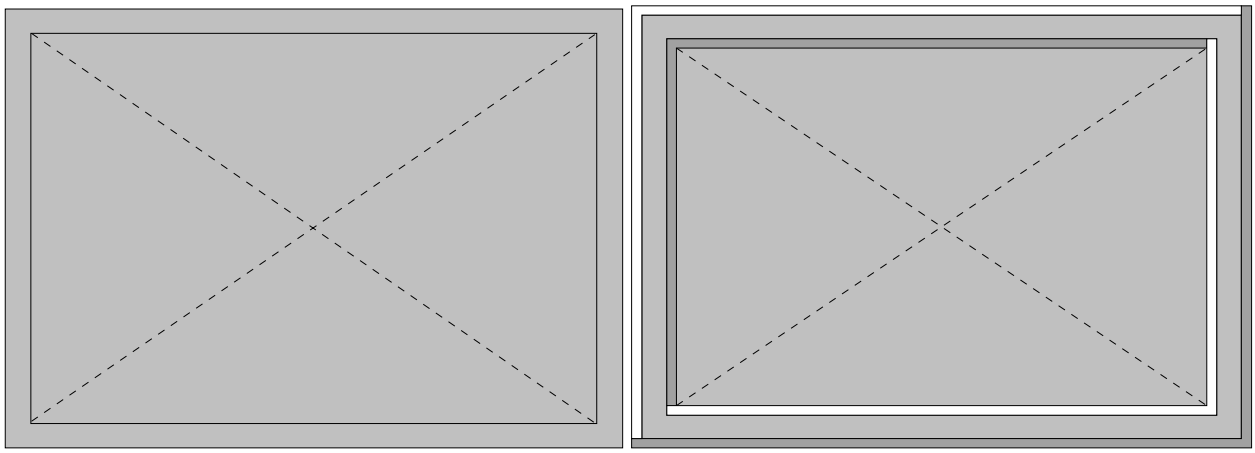


Figure 5-7 Normal frame (left) and frame with three dimensional impression (right)

64 frame colors are programmable, 2 bits for each component Y, (B-Y), (R-Y) through FRY[1:0], FRU[1:0] and FRV[1:0].

Frame Color	FRY	FRU	FRV
blue	01	01	11
green	01	11	11
white	11	00	00
yellow	11	10	01
cyan	11	00	11
magenta	10	01	01
black	00	00	00

Table 5-9 Examples for frame color

The horizontal and vertical width of the frame are independently programmable (FRMWIDV[1:0] and FRMWIDH[2:0]). For 100/120 Hz applications the frame width can only be changed in steps of 2 pixel. Frame color can be displayed over the whole PIP

size or whole picture size of the main channel. Alternatively a colored background can be displayed with visible PIP on it (PBGRD[1:0]). The colored background and the PIP can be blanked vertically for 16 lines (VERBLK). The horizontal blanking is adjustable.

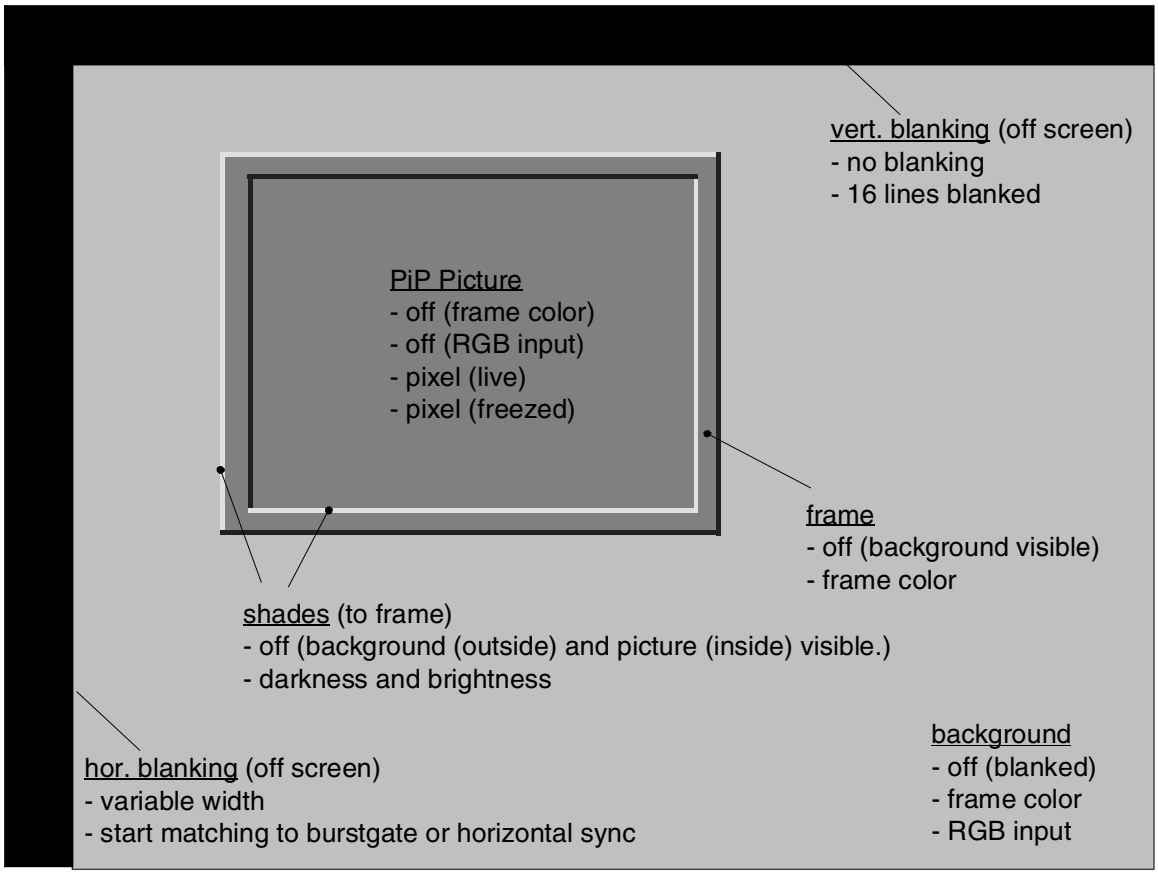


Figure 5-8 Framing and blanking of PIP

5.16 Blanking

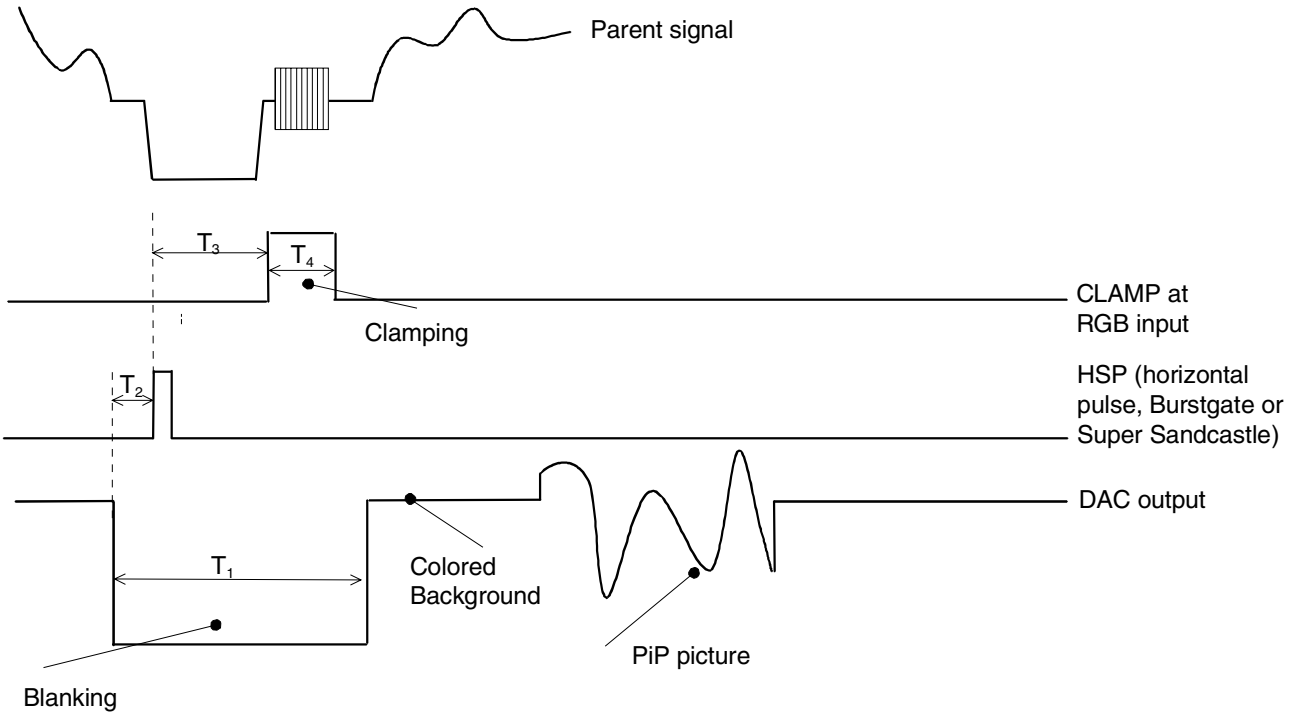


Figure 5-9 PIP horizontal blanking timing

HZOOM	READD	CLPDEL [2..0]	PARSYN [1..0]	T_1 (µs) (Blanking Duration)	T_2 (µs) (Blanking Start, negative value before HSP)	T_3 (µs) (Clamping Start, negative value before HSP)	T_4 (µs) (Clamping Duration)
0	0	000	00	10.4	-2	3.2	5.1
0	0	111	00	10.4	0.07	5.3	5.1
1	0	000	00	10.4	-2.8	2.3	5.2
1	0	111	00	10.4	0.01	5.3	5.2
0	1	000	00	5.2	-0.88	3.6	2.5
1	1	000	00	5.2	-1.3	1.6	2.5
0	0	000	10	10.4	-8.7	-3.5	5.1
0	0	111	10	10.4	-6.6	-1.4	5.1

Table 5-10 PIP horizontal blanking timing

5.17 DA-Conversion and external RGB-insertion

The SDA 9389X includes three 6-bit DA-converters. Brightness (BRIGTH[3:0]), Contrast(CON[3:0]) and Pedestal Level of the output signal can be controlled via I^2C bus. The output amplitude can be controlled by YAMP, UAMP, VAMP. For controlling an external RGB or YUV switch a select signal is provided. The delay of this select signal compared to RGB/YUV output is programmable for adaptation to different external output signal processing (SELDEL[3:0]).

The U and V oversampling stage inverts the sign of the U and V signals if UVPOLAR is active. The signals can be bypassed internally depending on OUTFOR to yield YUV or Y-U-V instead of RGB signals.

External RGB signals can be fed to the inputs IN1-3. By forcing the BLK input to high level these signals are switched to the RGB outputs OUT1-3 while the internal signals are switched off. The BLK input signal is passed through to the SEL output. This feature is only available, if PiP output signal is in RGB mode.

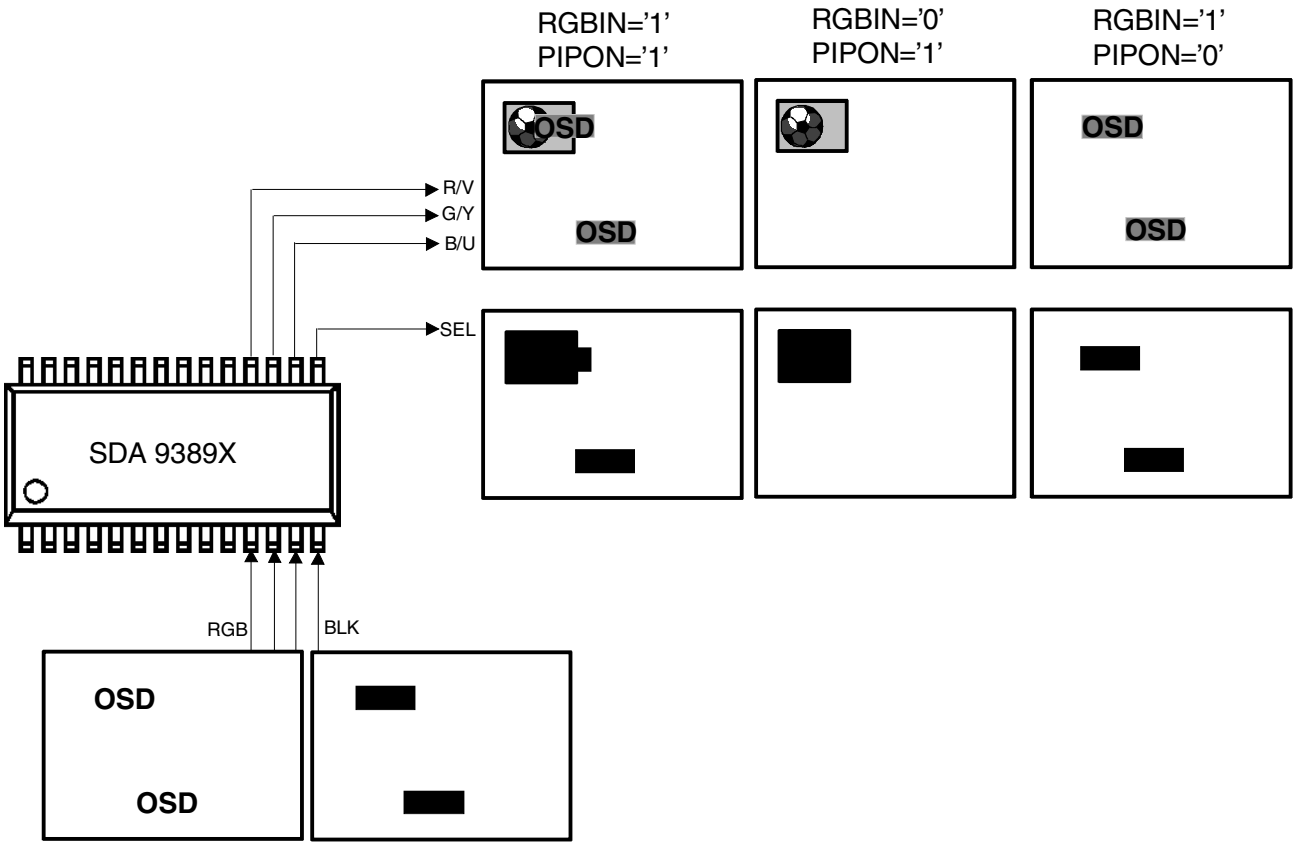


Figure 5-10 Insertion of external RGB

When IN1-3 are not used, they must be left open or connected to ground by a capacitor.

5.18 Pedestal Level adjustment

The pedestal level adjustment controlled by I^2C signals BLKLR, BLKLG, BLKLB enables the correction of small offset errors. This adjustment has an effect on the setup level during the active line interval of each channel like the brightness adjustment but has an enhanced resolution of 0.5 LSB. The maximum possible offset amounts to 7.5 LSBs. In YUV mode the action depends on the setting of BLKINVR and BLKINVB. If BLKINVR (BLKINVB) is active the offset applies to the blank level of the RV (BU) channel during the clamping interval for shifting the setup level to the negative direction. In RGB mode BLKINVR and BLKINVB are not necessary.

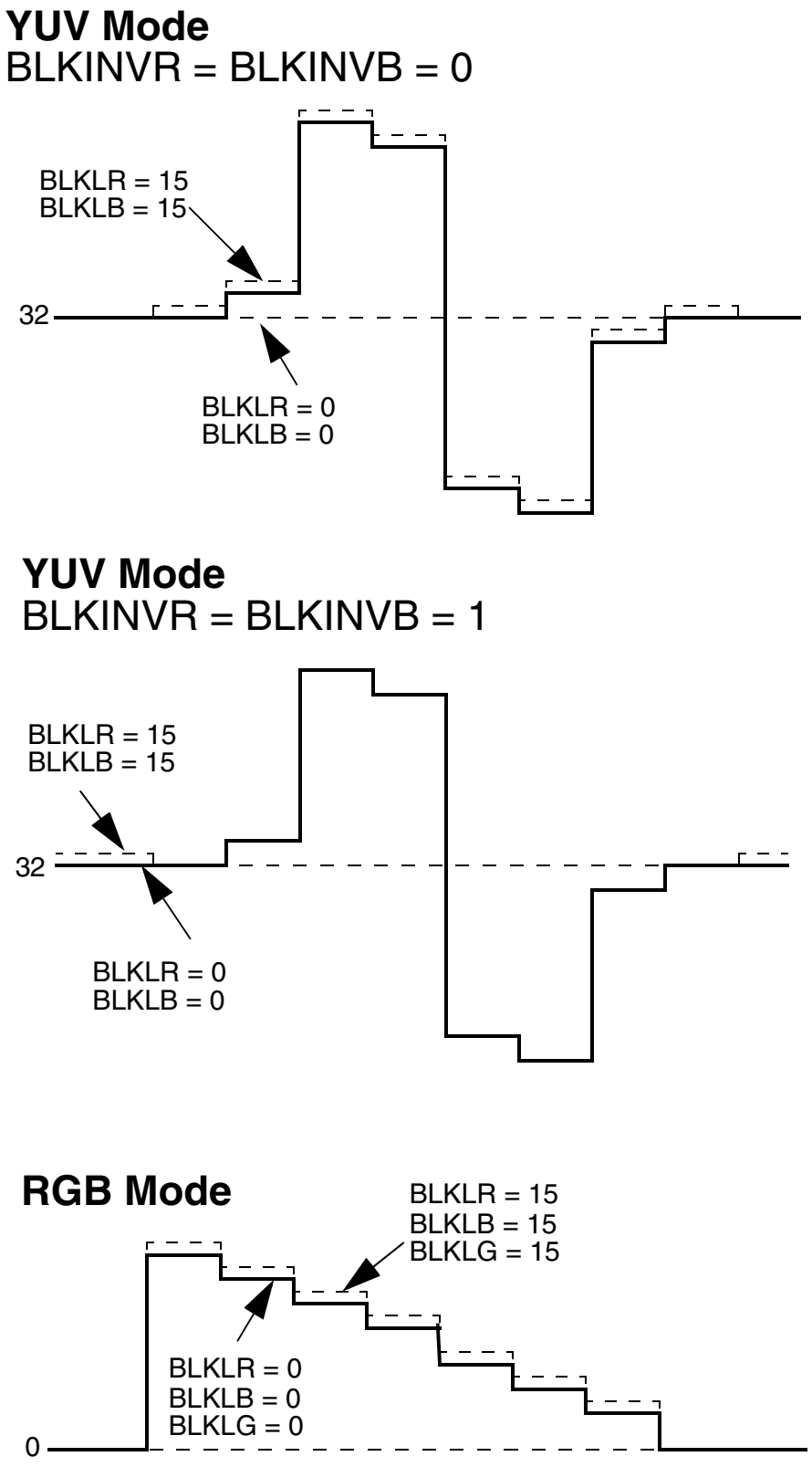


Figure 5-11 Pedestal level adjustment

5.19 Parent Clock Generation

The phase of the output signals is locked to the rising edge of the horizontal parent sync pulse.

The nominal internal read data frequency is 13.5 MHz. With respect to different displays, this can be changed to the values shown in the following table.

HZOOM	READD	XFREQF	Frequency	remark
0	0	0	13.5	
0	0	1	13.8	(can be used with 27 MHz crystal only)
0	1	0	27.0	
0	1	1	28.6	(can be used with 27 MHz crystal only)
1	0	0	9.45	
1	0	1	9.75	(can be used with 27 MHz crystal only)
1	1	0	18.9	
1	1	1	19.5	(can be used with 27 MHz crystal only)

Table 5-11 Memory-read-out frequency

5.20 Display Features

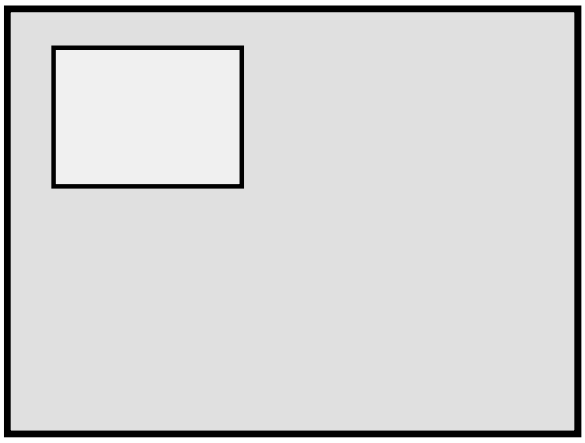


Figure 5-12 Picture size 1/9

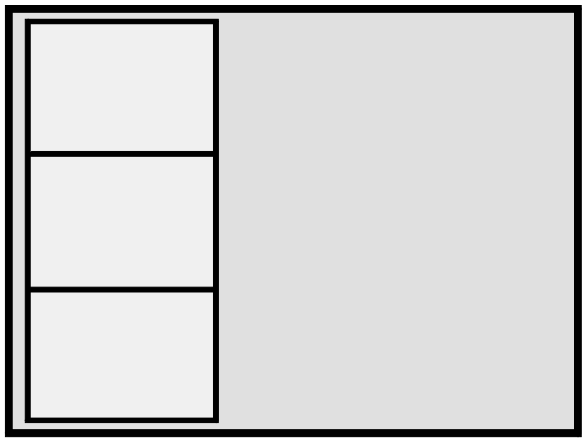


Figure 5-13 Picture size 1/9 and POP active

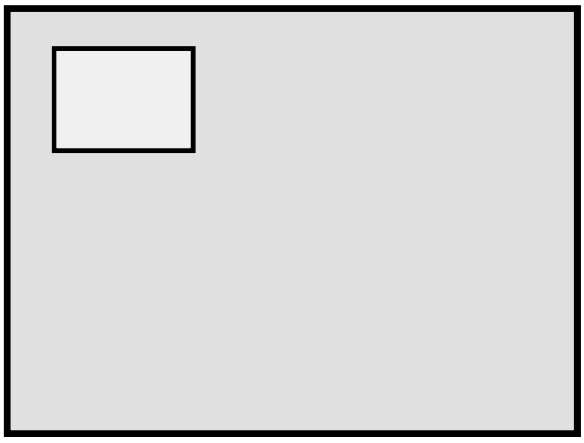


Figure 5-14 Picture size 1/16

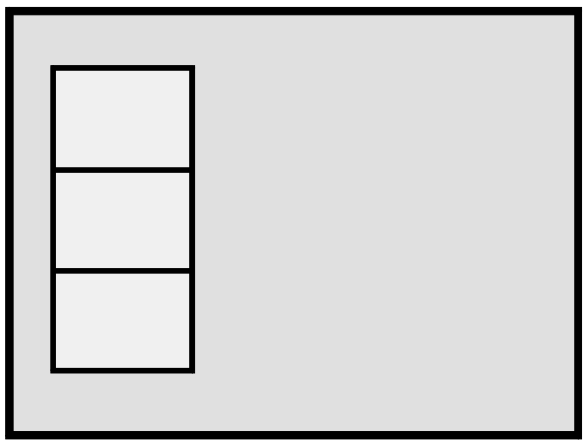


Figure 5-15 Picture size 1/16 and POP active

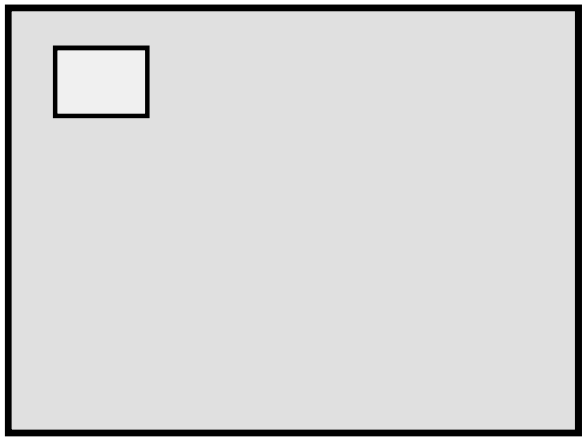


Figure 5-16 Picture size 1/36

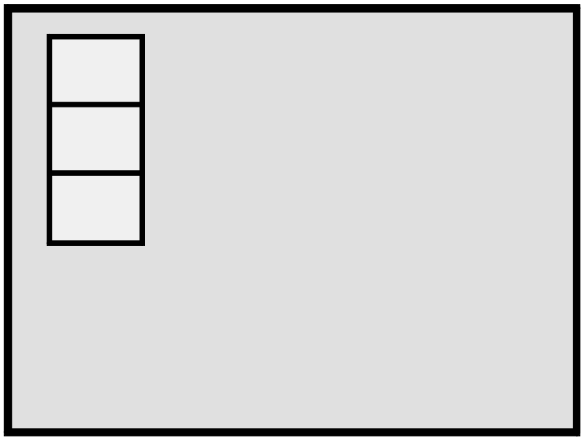


Figure 5-17 Picture size 1/36 and POP active

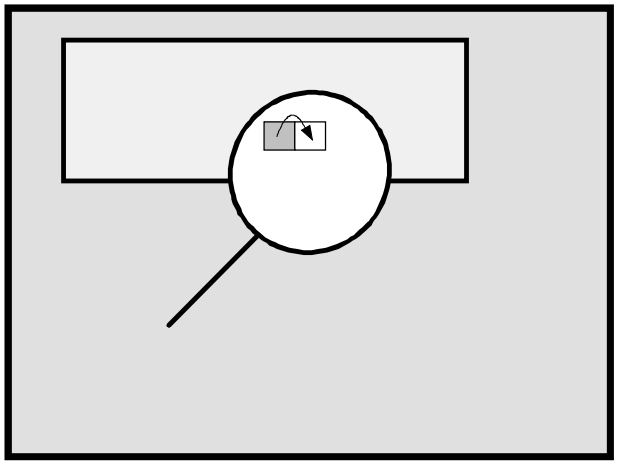


Figure 5-18 Picture size 1/9 and PIXDBL='1'

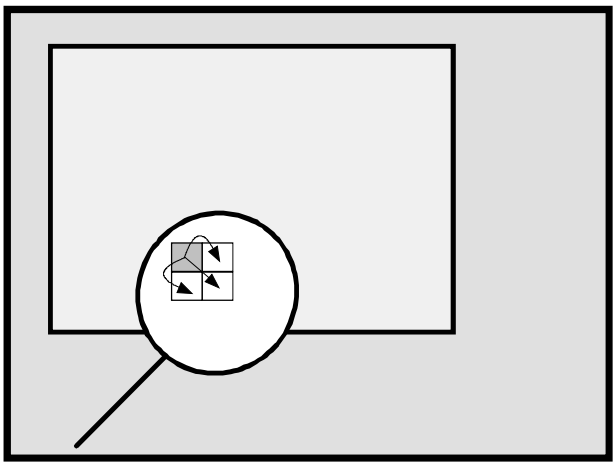


Figure 5-19 Picture size 1/9 and PIXDBL='1' and LINEDBL='1'

The decimation and memory circuits of PIPIIIplus are optimized for NTSC and PAL M signals. As the colordecoder is also able to handle PAL N signals, the additional lines are omitted. To share the omitted lines over the upper and lower part of the picture, the visible picture section can be centered vertically.

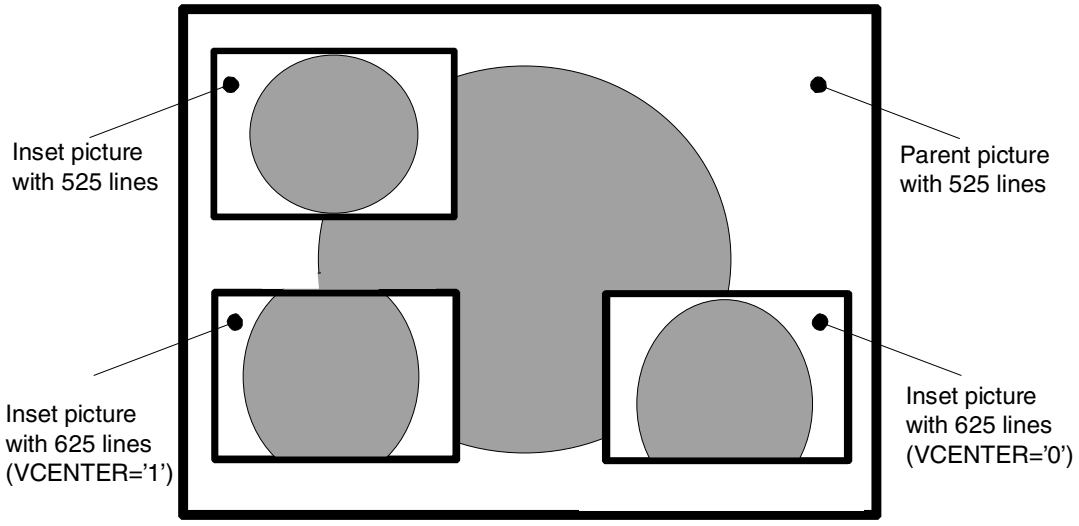


Figure 5-20 Display of 525 and 625 line inset signals

6 I²C-bus

6.1 I²C bus Address

w Write Address: 11011100 (DCh)

w Read Address: 11011101 (DDh)

6.2 I²C-bus Format:

S: Start condition

A: Acknowledge

P: Stop condition

NA: No Acknowledge

WRITE

S	11011100	A	Subaddress	A	Data Byte	A	****	A	P

READ

S	11011100	A	16h	S	11011101	A	Data Byte n	NA	P

Only write operation is possible at registers 00h-15h and 1Bh-1Dh, only read operation at registers 16h-1Ah. An automatic address increment function is implemented. Register 17h is left blank.

6.3 I²C-Bus Commands:

Sub-Addr	Data Bytes							
Hex.	D7	D6	D5	D4	D3	D2	D1	D0
00_H	FIESEL1	FIESEL0	FREEZE	PIXDBL	READD	LINEDBL	HZOOM	PIPON
01_H	SELDOWN	SELDEL3	SELDEL2	SELDEL1	SELDEL0		CPOS1	CPOS0
02_H	POSHOR7	POSHOR6	POSHOR5	POSHOR4	POSHOR3	POSHOR2	POSHOR1	POSHOR0
03_H	POP	POSVER6	POSVER5	POSVER4	POSVER3	POSVER2	POSVER1	POSVER0
04_H	CVBSEL1	CVBSEL0	AGC3	AGC2	AGC1	AGC0	AGCADST	AGCFIX
05_H	SELLNR	ACQNEW	SIZEVER1	SIZEVER0	LMOFST1	LMOFST0	SIZEHOR1	SIZEHOR0
06_H			BLKINVR	BLKINVB	BLKLR3	BLKLR2	BLKLR1	BLKLR0
07_H	BLKLG3	BLKLG2	BLKLG1	BLKLG0	BLKLB3	BLKLB2	BLKLB1	BLKLB0
08_H	PARSYN1	PARSYN0				CLPDEL2	CLPDEL1	CLPDEL0
09_H	STDP	STATPQ	VSPISQ	VSPDEL4	VSPDEL3	VSPDEL2	VSPDEL1	VSPDEL0
$0A_H$	CON3	CON2	CON1	CON0	BRIGHT3	BRIGHT2	BRIGHT1	BRIGHT0
$0B_H$	RGBIN	VERBLK	FRY5	FRY4	FRV5	FRV4	FRU5	FRU4
$0C_H$	FRSEL	PBGRD1	PBGRD0	FRWIDV1	FRWIDV0	FRWIDH2	FRWIDH1	FRWIDH0
$0D_H$	SAT3	SAT2	SAT1	SAT0		MAT	UVPOLAR	OUTFOR
$0E_H$	ACCFIX	COLON	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0
$0F_H$	PLLITC1	PLLITC0	STATIQ			CSTAND1	CSTAND0	
10_H	CKILL1	CKILL0	CPLLOF	INCRA4	INCRA3	INCRA2	INCRA1	INCRA0
11_H					YCOR	YPEAK2	YPEAK1	YPEAK0
12_H	VCENTER	XFREQF	WTCHDG	PICSIZE			YDEL1	YDEL0
13_H	YAMP7	YAMP6	YAMP5	YAMP4	YAMP3	YAMP2	YAMP1	YAMP0
14_H	UAMP7	UAMP6	UAMP5	UAMP4	UAMP3	UAMP2	UAMP1	UAMP0
15_H	VAMP7	VAMP6	VAMP5	VAMP4	VAMP3	VAMP2	VAMP1	VAMP0
16_H	DEVICE	DATAV	LINESTD	STDET1	STDET0	DISPSTAT	SCSTAT	SYNCSTAT
17_H								

18_H	DATAA7	DATAA6	DATAA5	DATAA4	DATAA3	DATAA2	DATAA1	DATAA0
19_H	DATAB7	DATAB6	DATAB5	DATAB4	DATAB3	DATAB2	DATAB1	DATAB0
$1A_H$								SLFIELD
$1B_H$	XDSCLS4	XDSCLS3	XDSCLS2	XDSCLS1	XDSCLS0	XDSTPE2	XDSTPE1	XDSTPE0
$1C_H$	NONSED	NOCRID	FCBEOK	CRIBEOK	0	DSTDET		
$1D_H$	0	0	0	HFP4	HFP3	HFP2	HFP1	HFP0

After power on of the IC grey marked data bits are set to '1', all other to ‘0‘.

Not used and reserved bits must be set to ‘0‘ by software if the register is written.

Subaddress 00:

Bit	Name	Function
D0	PIPON	**PIP insertion** **’0’**: PIP insertion off ’1’: PIP insertion on
D1	HZOOM	**Horizontal Zooming** ’**0**’: horizontal Scaling Factor 1 ’1’: horizontal Scaling Factor 1.43
D2	LINEDBL	**Lindedouble mode** ’**0**’: each line of the PIP memory is read once (normal operation) ’1’: each line of the PIP memory is read twice (progressive scan conversion systems in parent channel)
D3	READD	**Readdouble mode** ’**0**’: PIP display with single read frequency ’1’: PIP display with double read frequency ***Note: When enabled, PIP should be set to ’frame-mode’ (FIESEL=’00’) for progressive scan or to ’field mode’ (FIESEL=’01’ or ’10’) for 100/120 Hz applications***
D4	PIXDBL	Pixdouble mode ’**0**’: normal display ’1’: each pixel read twice ***Note: Peaking is automatically set to ’000’ (no peaking) when enabled***
D5	FREEZE	Picture freezing ’**0**’: live picture ’1’: freeze picture

D7-D6	FIESEL	**Field selection** '**00**': display of both fields (frame-mode) '01': display of field 1 '10': display of field 2 '11': (reserved)

Subaddress 01:

Bit	Name	Function
D1-D0	CPOS	**Coarse positioning of PIP picture** '**00':** upper left '01': upper right '10': lower left '11': lower right
D2	(reserved)	
D6-D3	SELDEL	**Delay of output signal SELECT at pin SEL** '1000':-8 periods of read frequency clock ... '**0000**': 0 periods of read frequency clock ... '1111': 7 periods of read frequency clock
D7	SELDOWN	**SEL (select) output condition** '**0**': open source output at pin SEL '1': TTL output at pins SEL

Subaddress 02:

Bit	Name	Function
D7-D0	POSHOR	**Horizontal position of PIP picture (raster: 4 pixel)** '**00000000**': PIP at coarse position ... '11111111': PIP opposite coarse position ***Note: Positioning of PIP outside visible picture area is not allowed***

Subaddress 03:

Bit	Name	Function

D6-D0	POSVER	**Vertical position of PIP picture (raster: 2 lines);** '**00000000**': PIP at coarse position ... '11111111': PIP opposite coarse position ***Note: Positioning of PIP outside visible picture area is not allowed***
D7	POP	**Pip mode** '**0**': single PIP mode '1': three identical pictures lined up vertically with same content

Subaddress 04:

Bit	Name	Function
D0	AGCFIX	**Automatic Gain Control of ADC** '**0**': automatic Gain Control on '1': automatic Gain Control off (manual mode)
D1	AGCADST	**Automatic Gain Control restart** '**0**'-> '1': manual start of automatic adjustment of ADC input amplitude range
D5-D2	AGC	**Automatic Gain Control setting for manual mode** **'0000'** :maximum input amplitude of the CVBS signal 0.7V_{pp} ... '1111': maximum input amplitude of the CVBS signal 2V_{pp}
D7-D6	CVBSEL	**CVBS input selection** '**00**': Input CVBS1 active '01': Input CVBS2 active '10': (reserved) '11': Input CVBS3 active

Subaddress 05:

Bit	Name	Function
D1-D0	SIZEHOR	**Horizontal size reduction** '**00**': horizontal size reduction 3 to 1 '01': horizontal size reduction 4 to 1 '10': (reserved) '11': horizontal size reduction 6 to 1

D3-D2	LMOFST	**Luminance offset** '**00**': no offset '01': offset of -6 IRE '10': offset of -7.5 IRE '11': offset of -9 IRE
D5-D4	SIZEVER	**Vertical size reduction** '**00**': vertical size reduction 3 to 1 '01': vertical size reduction 4 to 1 '10': (reserved) '11': vertical size reduction 6 to 1
D6	ACQNEW	**Acquisition new** '**0**': one new data packet is saved '1': new data overwrites current data
D7	SELLNR	**Select linenumber** '**0**': data slicer at line 21 '1': data slicer at line 20

Subaddress 06:

Bit	Name	Function
D3-D0	BLKLR	**Adjustment of blanking level of DAC output 1 (steps of 0.5 LSB)** '0000': ... '1111':
D4	BLKINVB	**Pedestal adjustment for output 3** '**0**': offset current at OUT3 output is added during active picture '1': offset current at OUT3 output is added during blanking
D5	BLKINVR	**Pedestal adjustment for output 1** '**0**': offset current at OUT1 output is added during active picture '1': offset current at OUT1 output is added during blanking
D7-D6	(reserved)	

Subaddress 07:

Bit	**Name**	**Function**

D3-D0	BLKLB	**Adjustment of blanking level of DAC output 3 (steps of 0.5 LSB)** '0000': ... '1111':
D7-D4	BLKLG	**Adjustment of blanking level of DAC output 2 (steps of 0.5 LSB)** '0000': ... '1111':

Subaddress 08:

Bit	Name	Function
D2-D0	CLPDEL	**Delay of clamping pulse at RGB inputs** '**000**': 0 (no delay) '001': 148 ns (100/120 Hz) resp. 296ns (50/60 Hz) '111': 1036 ns (100/120 Hz) resp. 2072 ns (50/60 Hz)
D5-D3	(reserved)	
D7-D6	PARSYN	**Parent synchronization input pin and way** '**00**': parent sync. TTL signals read via pins SCP and VP/SCP '01': parent sync. sandcastle via pin SCP '10': parent sync. TTL signals read via pins SCP and VP/SCP '11': parent sync. sandcastle at pin VP/SCP ***Note: '10' must be used for burstgate input , '00' for horizontal sync pulse***

Subaddress 09:

Bit	Name	Function
D4-D0	VSPDEL	**delay of vertical synchronization pulse (parent signal)** '**00000**':in steps of 2.37µs / 1.68µs (50 / 100Hz) .... '11111':
D5	VSPISQ	**Noise reduction of the VSP pulse** '**0**': on '1': off

D6	STATPQ	**Frame-mode activation for non-standard parent sources** '**0**': Frame-mode only active for standard NTSC, PAL M sources '1': Frame-mode active also for non-standard sources, (disturbances possible)
D7	STDP	**Parent standard** '**0**': 60Hz (resp. 120 Hz) '1': 50Hz (resp. 100 Hz)

Subaddress 0A:

Bit	Name	Function
D3-D0	BRIGHT	**Brightness adjustment of PIP picture** '**0000**': nominal brightness '0001': 1 LSB added ... '1111': 15 LSB added
D7-D4	CON	**Contrast adjustment of PIP picture** '**0000**': nominal contrast ... '1111': max. contrast increase

Subaddress 0B:

Bit	Name	Function
D1-D0	FRU	**Chrominance component (B-Y) of frame color**
D3-D2	FRV	**Chrominance component (R-Y) of frame color**
D5-D4	FRY	**Luminance component of frame color** ***NOTE:*** FRY='00' is not suited for three dimensional frame
D6	VERBLK	**Vertical Blanking of DAC outputs** '**0**': clamping level only during line-blanking intervals '1': clamping level during line-blanking intervals and field-blanking intervals (16 complete lines following the vertical synchronization pulse of the parent channel)no external RGB insertion posssible, BLK signal ineffective external RGB insertion posssible during high periode of the BLK signal

D7	RGBIN	**RGB insertion permission** '**0**': no external RGB insertion posssible, BLK signal ineffective '1': external RGB insertion posssible during high period of the BLK signal

Subaddress 0C:

Bit	Name	Function
D2-D0	FRWIDH	**Horizontal width of PIP frame** '**000**': horizontal frame width 0 pixel ... '111': horizontal frame width 7pixel ***Note: Even with FRWIDH='0000' a shade remains for three dimensional frame***
D4-D3	FRWIDV	**Vertical width of PIP frame** '**00**': vertical frame hight 0 line ... '11': vertical frame hight 3 lines ***Note: Even with FRWIDV='00' a shade remains for three dimensional frame***
D6-D5	PBGRD	**Picture background** '**00**': background color off '01': PIP picture invisible, PIP background display same as frame color '10': background display with frame color instead of main picture, PIP visible '11': background and PIP display with frame color instead of picture
D7	FRSEL	**Frame selection** '**0**': standard frame '1': three dimensional frame

Subaddress 0D:

Bit	Name	Function
D0	OUTFOR	**Output format** '**0**': format of output signals: R G B '1': format of output signals: Y, (B-Y), (R-Y)

I2C-bus

D1	UVPOLAR	**Polarity of UV** '**0**': chrominance output signals: +(B-Y), +(R-Y) '1': inverted chrominance output signals: -(B-Y), -(R-Y)
D2	MAT	**RGB Matrix** '**0**': RGB Matrix USA '1': RGB Matrix Japan
D3	(reserved)	
D7-D4	SAT	**Saturation Control of chroma signal** '0000': 0 (color off) '0001': Saturation 1/8 of nominal value ... '**1000**': nominal value ... '1111': Saturation 15/8 of nominal value

Subaddress 0E

Bit	Name	Function
D5-D0	HUE	**Hue Control of chroma signal** Demodulation phase angle for NTSC color adjustment '100000':-44.8º .... '**000000**': 0º '000001': 1.4º ... '011111': 43.4º
D6	COLON	**Color killer** '**0**': chroma killer active '1': chroma always on
D7	ACCFIX	**Automatic Chroma Control disabling** '**0**': ACC active '1': ACC fixed to nominal value

Subaddress 0F:

Bit	Name	Function
D0	(reserved)	

D2-D1	CSTAND	**Chroma standard selection** '**00**': Automatic standard detection '01': NTSC M fixed '10': PAL N fixed '11': PAL M fixed
D4-D3	(reserved)	
D5	STATIQ	**Frame-mode activation for non-standard inset sources** '**0**': Frame-Mode possible in case of proper input signals '1': Frame-Mode always active
D7-D6	PLLITC	**Time constant of inset synchronization PLL** '00': fast time constant of sync separation (e.g. for VCR) ... '**11**': slow time constant of sync separation (e.g. for TV)

Subaddress 10:

Bit	Name	Function
D4-D0	INCRA	**Adjustment of regenerated color carrier frequency** '00000': adjustment -50 ppm ... '**00111**': nominal value ... '11100': adjustment +110 ppm ***Note: the maximum input allowed is '11100'***
D5	CPLLOF	**Opening of Chroma PLL** '**0**': Chroma PLL active '1': Loop of chroma PLL opened
D7-D6	CKILL	**Color killer threshold** '**00**': color killer threshold at -12db amplitude '01': color killer threshold at -18db amplitude '10': color killer threshold at -24db amplitude '11': color off ***Note: values are approximative***

Subaddress 11:

Bit	**Name**	**Function**

D2-D0	YPEAK	**Luminance Peaking** '**000**': peaking off ... '111': maximum peaking ***NOTE:*** a peaking greater than 4 ('100') is not recommended
D3	YCOR	**Coring** '**0**': coring off '1': coring active, no peaking for small luminance steps
D7-D4	(reserved)	

Subaddress 12:

Bit	Name	Function
D1-D0	YDEL	**Luminance delay** '**00**': Y signal not delayed '01': -1 pixel '10': +1 pixel '11': (reserved)
D3-D2	(reserved)	
D4	PICSZE	**Picture size** '**0**': 216/164/108 pixel visible '1': 224/168/112 pixel visible
D5	WTCHDG	**Watchdog control** '**0**': slow response '1': fast response ***Note: should be set to 0 for normal operation***
D6	XFREQF	**Read frequency Offset** '**0**': display clock frequency without offset '1': display clock frequency with offset of +2.5% ***Note: horizontal picture position varies with this setting*** ***Note: function only available when using a 27 MHz crystal***

D7	VCENTER	**Vertical centering of 625 lines inset signals** '**0**': additional lines omitted at lower picture (suited for NTSC and PAL-M) '1': additional lines omitted half at upper and lower picture ***Note: When enabled, display of 525 line signals can be disturbed***

Subaddress 13:

Bit	Name	Function
D7-D0	YAMP	**Amplitude of Y/G output signal (OUT2)** '00000000': min ... '**10000000**':default ... '11111111':max

Subaddress 14:

Bit	Name	Function
D7-D0	UAMP	**Amplitude of U/B output signal (OUT3)** '00000000':min ... '**10000000**':default ... '11111111':max

Subaddress 15:

Bit	Name	Function
D7-D0	VAMP	**Amplitude of V/R output signal (OUT1)** '00000000':min ... '**10000000**':default ... '11111111':max

Subaddress 16 (Read)

Bit	Name	Function

D0	SYNCSTAT	**Inset synchronisation status** '0': Internally generated sync not locked to CVBS signal '1': Internally generated sync locked to CVBS signal
D1	SCSTAT	**Choma display** '0': chroma off '1': chroma on
D2	DISPSTAT	**Display status** '0': Field mode '1': Frame mode
D4-D3	STDET	**Detected chroma standard** '00': non-standard '01': NTSC M '10': PAL N '11': PAL M ***Note: if SYNCSTAT equals '0' STDET is invalid***
D5	LINESTD	**Linestandard** '0': Internal generated sync locked to 60 Hz CVBS signal '1': Internal generated sync locked to 50 Hz CVBS signal ***Note: if SYNCSTAT equals '0' LINESTD is invalid***
D6	DATAV	**Data valid** '0': Data read by µC or Data invalid '1': new Data available at DATA output
D7	DEVICE	**Device identification** '0': SDA 9388X (PIP III) '1': SDA 9389X (PIP IIIplus)

Subaddress 17

Bit	Name	Function
D7-D0	(reserved)	

Subaddress 18 (Read)

Bit	Name	Function
D7-D0	DATAA	**First Data Byte of Closed Caption Data**

Subaddress 19(Read)

Bit	Name	Function
D7-D0	DATAB	**Second Data Byte of Closed Caption Data**

Subaddress 1A:

Bit	Name	Function
D0	SLFIELD	**Field Number of sliced data** Field fits to content of DATAA and DATAB '0': First Field '1': Second Field
D7-D1	(reserved)	

Subaddress 1B:

Bit	Name	Function
D2-D0	XDSTPE	**XDS Type Select** XDS-Secondary Filter (Type) '**000**':ALL (no filtering) '001': 05h (program rating) '010': 01h, 04h (Time information only) '011': 40h (out of band only) '100': 01h,02h,03h,04h,0Dh,40h (VCR information) '101': 01h, 04h,05h (Time information only and PR) '110': 05h,40h (out of band only and PR) '111': 01h,02h,03h,04h,05h,0Dh,40h (VCR information and PR)
D7-D3	XDSCLS	**XDS Class Select** Closed Caption XDS-Primary Filter (Class) '**00000**': Transparent (all sliced data, both fields) '1xxxx' :'Current' Selected (only second field) 'x1xxx' :'Future' Selected (only second field) 'xx1xx' :'Channel' Selected (only second field) 'xxx1x' :'Miscellenious' Selected (only second field) 'xxxx1' :'Public Services' Selected (only second field)

Subaddress 1C:

Bit	Name	Function

D1-D0	(reserved)	
D2	DSTDET	**Data start Detection** '**0**': additional data plausibility checking disabled '1': additional data plausibility checking enabled
D3	(reserved)	**set to '0' for normal operation**
D4	CRIBEOK	**Clock-run-in bit error** '**0**': check for correct clock-run-in '1': allow one deviation in clock-run-in
D5	FCBEOK	**Framing code bit error behaviour** '**0**':check for correct framing code '1':allow one deviation in framing code
D6	NOCRID	**No clock-run-in detection** '**0**': check clock-run-in according to bit **CRIBEOK** '1':do not check clock-run-in
D7	NONSED	**No Noise data** '**0**': only one data change allowed per closed caption cycle '1': all data allowed

Subaddress 1D:

Bit	Name	Function
D4-D0	HFP	**Horizontal Fine Positioning** '10000': max shift right (2.2 us) ... '00000': no shifting ... '01111': max. shift left (-2.2 us)
D7-D5	(reserved)	set to 0

7 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Unit
		min.	max.		
Ambient Temperature	T_A	0	70	°C	
Storage Temperature	T_{stg}	-55	125	°C	
Junction Temperature	T_j		125	°C	
Soldering Temperature	T_{sold}		260	°C	duration <10s
Input Voltage	V_i	-0.3V	V_{DD}+ 0.3V	1	CVBS1..3,IN1..3, SCP, VP/SCP
	V_i	-0.3	6.5	V	all other pins
Output Voltage	V_Q	-0.3V	V_{DD}+ 0.3V	1	pins OUT1, OUT2, OUT3, XQ
	V_Q	-0.3	6.5	V	all other pins
Supply Voltages	V_{DD}	-0.3	6.5	V	
Supply Voltage Differentials		-0.25	0.25	V	
Total Power Dissipation	P_{tot}		0.720	W	
Latch-Up Protection		-100	100	mA	
ESD robustness HBM: 1.5kΩ, 100pF	V_{ESD}	-2000	2000	V	

All voltages listed are referenced to ground (0V, V_{SS}) except where noted.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

8 Recommended Operating Range

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Supply Voltages	V_{DDxx}	4.75	5	5.25	V	
Ambient Temperature	T_A	0	25	70	°C	
All TTL Inputs						
Low-Level Input Voltage	V_{IL}	-0.25		0.8	V	
High-Level Input Voltage	V_{IH}	2.0		VDD +0.2	V	
Parent horizontal / vertical Sync Inputs: VP/SCP, SCP						
Sync H-Frequency In Single Frequency Display Mode	f_{PH}	14.9	15.734	16.6	kHz	
Sync H-Frequency In Double Frequency Display Mode	f_{P2H}	29.8	31.468	33.2	kHz	
Signal Rise Time				100	ns	noisefree transition
Signal High Time (horizontal)		200			ns	
Signal Low Time (horizontal)		900			ns	
Sync V-Frequency In Single Frequency Display Mode	f_{PV}	48	60	70	Hz	STDP dependent
Sync V-Frequency In Double Frequency Display Mode	f_{PV}	tbf	tbf	tbf	Hz	STDP dependent
Signal High Time (vertical)		200			ns	
Signal Low Time (vertical)		200			ns	
Fast I²C Bus (All values are referred to min(V_{IH}) and max(V_{IL})) This specification of the bus lines need not be identical with the I/O stages specification because of optional series resistors between bus lines and I/O pins.						
SCL Clock Frequency	f_{SCL}	0		400	kHz	
Inactive Time Before Start Of Transmission	t_{BUF}	1.3			µs	
Set-Up Time Start Condition	$t_{SU;STA}$	0.6			µs	
Hold Time Start Condition	$t_{HD;STA}$	0.6			µs	

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
SCL Low Time	t_{LOW}	1.3			µs	
SCL High Time	t_{HIGH}	0.6			µs	
Set-Up Time DATA	$t_{SU;DAT}$	100			ns	
Hold Time DATA	$t_{HD;DAT}$	0		0.9	µs	
SDA/SCL Rise/Fall Times	t_R, t_F	20+$		300	ns	$=0.1C_b/pF
Set-Up Time Stop Condition	$t_{SU;STO}$	0.6			µs	
Capacitive Load/Bus Line	C_b			400	pF	
I²C Bus Inputs/Output: SDA, SCL						
High-Level Input Voltage	V_{IH}	3V		V_{DD}+ 0.5V	1	also for SDA/SCL input stages
Low-Level Input Voltage	V_{IL}	-0.25V		1.5	V	
Spike Duration At Inputs		0	0	50	ns	
Low-Level Output Current	I_{OL}			6	mA	
Analog To digital converter (7 bit)						
Input Coupling Capacitors		10		100	nF	necessary for proper clamping
CVBS Source Resistance			0.1		kΩ	dependent on PCB layout
Reference Voltage Low	V_{REFL}	tbf	tbf	tbf	V	min and max values only with optional external resistors or if gain control is active
Reference Voltage High	V_{REFH}	tbf	tbf	tbf	V	
Input Voltage Range at inputs CVBS1-3	Vi	0.7	1.0	2	V	
Digital To Analog Converters (6-bit)						
Full Range Output Voltage	V_{OFR}	0.3	1	2.2	V	peak to peak
Load resistance	R_L	10			kΩ	

Recommended Operating Range

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Crystal Specification						
Maximum Permissible Frequency Deviation	$\Delta f_{max}/f_{xtal}$	-100		100	10^{-6}	deviation outside this range will cause color decoding failures
Frequency (27.0 MHz crystal)	f_{xtal27}	26.9973	27	27.0027	MHz	deviation outside this range will cause color decoding failures
Frequency (13.5 MHz crystal)	f_{xtal13}	13.4987	13.5	13.5013	MHz	deviation outside this range will cause color decoding failures
Permissible Frequency Deviation	$\Delta f/f_{xtal}$	-50	0	50	10^{-6}	recommended
Permissible Frequency Deviation with Temperature	$\Delta f_T/f_{xtal}$	-20	0	20	10^{-6}	recommended
13.5 MHz (fundamental mode)						
Load Capacitance	C_L		15		pF	
Series resonance resistance	R_S		4.7	25	Ω	
Motional capacitance	C_1		20.5		fF	
Parallel capacitance	C_0		4.7		pF	
27.0 MHz (fundamental mode)						
Load Capacitance	C_L		15		pF	
Series resonance resistance	R_S		4	25	Ω	
Motional capacitance	C_1		20		fF	
Parallel capacitance	C_0		4.7		pF	
27.0 MHz (third overtone mode)						
Load Capacitance	C_L	8			pF	
Series Resonance Resistance	R_S		13.5	40	Ω	
Motional Capacitance	C_1		1.6		fF	
Parallel Capacitance	C_0		3.8		pF	

Note: In the operating range the functions given in the circuit description are fulfilled.

9 Characteristics

(Assuming Recommended Operating Conditions)

All

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Average total supply current	I_{DDtot}			137	mA	
All Digital Inputs (TTL, I²C)						
Input Capacitance	C_I		7		pF	not tested
Input Leakage Current		-10		10	µA	including leakage current of SDA output stage
Three Level Input (3-L) SCP, VP/SCP						
Input Capacitance	C_I		7		pF	not tested
Low-Level Input Voltage	V_{IL}	-0.25		1	V	$V_{DD(min)}< V_{DD}< V_{DD(max)}$
Medium-Level Input Voltage	V_{IM}	2.0		3.0	V	$V_{DD(min)}< V_{DD}< V_{DD(max)}$
High-Level Input Voltage	V_{IH}	4		V_{DD} +0.5	V	$V_{DD(min)}< V_{DD}< V_{DD(max)}$
Hysteresis	V_{IMH}, V_{ILM}	0.2		0.5		Threshold difference between rising and falling edge
SEL						
High-Level Output Voltage	V_{OH}	2.4 V		V_{DD}	V	I_{OH}=-200µA
High-Level Output Voltage	V_{OH}	1.5V		V_{DD}	V	I_{OH}=-4.5mA
Low-Level Output Voltage	V_{OL}			0.4	V	I_{OL}=1.6mA, only valid if bit SELDOWN=1
Leakage Current		-10			µA	V_O=0V...V_{DD}
Output Capacitance				7	pF	not tested

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
BLK						
Low-Level Input Voltage	V_{IL}	-0.25		0.4	V	$V_{DD(min)}<V_{DD}<V_{DD(max)}$
High-Level Input Voltage	V_{IH}	0.9		V_{DD}+ 0.5	V	$V_{DD(min)}<V_{DD}<V_{DD(max)}$
Delay BLK in -> SEL out			tbf			ns
I²C Inputs: SDA/SCL						
Schmitt Trigger Hysteresis	V_{hys}			0.2	V	not tested
I²C Input / Output: SDA (Referenced to SCL; Open Drain Output)						
Low-Level Output Voltage	V_{OL}			0.4	V	I_{OL}=3mA
Low-Level Output Voltage	V_{OL}			0.6	V	I_{OL}=max
Output Fall Time from min(V_{IH}) to max(V_{IL})	t_{OF}	20+0.1*C_b / pF		250	ns	10pF≤Cb≤400pF
Analog Inputs CVBS1..3 *Note:* V_{DDA}=nom, T_A=nom						
CVBS Input Leakage Current		-100		100	nA	clamping inactive
CVBS Input Capacitance	C_I		7		pF	not tested
Input Clamping Error		-1		1	LSB	settled state
Input Clamping Current	$\lvert\bar{I}_{CLP}\rvert$	43		326	µA	dependent on clamping error
max. Input Clamping Current deviation	$\lvert I_{CLPx}\rvert / \lvert I_{CLP}\rvert$	-40		40	%	
Reference Voltage Difference	V_{REFH}-V_{REFL}	0.7		2	V	VDDA1=5V
D.C. Differential Nonlinearity			+/- 0.5		LSB	V_{REFH}-V_{REFL} = max

Characteristics

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Crosstalk between CVBS Inputs			-50		dB	
Digital To Analog Converters (6-bit): Outputs OUT1, OUT2, OUT3 *Note:* V_{DDA}=nom, T_A=nom						
D.C. Differential Nonlinearity	DNLE		+/-0.5		LSB	
Full Range Output Voltage	U_{OL}	0.3			V	CON, UAMP, VAMP, YAMP = 0
Full Range Output Voltage	U_{OH}			2	V	CON, UAMP, VAMP, YAMP = max
Output Voltage	U_O	0.9		1.1	V	CON, UAMP, VAMP, YAMP = default, VREF = const.
Deviation of OUT1-3 (matching)		-3		3	%	
Contrast Increase			30		%	please refer to figure 10-3
Output Amplitude Ratio $(U_{OH}-U_{OL})/U_{OL}$			400		%	please refer to figure 10-3
Brightness Increase				15	LSB	please refer to figure 10.3
Pedestal Level variation				+/- 7.5	LSB	
Reference Voltage Dependence of DAC Output Voltage						please refer to figure 10-2
Temperature Dependence of DAC Output Voltage						please refer to figure 10-1
RGB switch						
Input Voltage Range				1.2	Vpp	
Bandwith (-3dB)			10		MHz	R_L>10kΩ; C_L=20pF
Gain		0.9		1.1		

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Gain Difference RGB				3	%	f<4MHz
Crosstalk Between Inputs				-35	dB	f=5MHz,
Isolation (off state)		42			dB	f=5MHz
Clamping Level Difference at Output				15	mV	between external and internal source
Clamping Capacitor		10		100	nF	
Colordecoder						
Horizontal PLL Permissible Static Deviation	$\Delta f_{Hf}/f_H$		+/- 7		%	VCR1 or VCR2 (PLLITC='00' or '01')
Horizontal PLL Permissible Static Deviation	$\Delta f_{Hf}/f_H$		+/- 3.5		%	TV1 or TV2 (PLLITC='10' or '11')
Chroma PLL pull-in-range	Δf_{SC}		+/- 500		Hz	nominal crystal frequency
Color Killer						
			-12		dB	CKILL='00'
			-10		dB	
			-18		dB	CKILL='01'
			-16		dB	
			-24		dB	CKILL='10'
			-22		dB	

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25 \times C$ and the given supply voltage.

10 Diagrams

10.1 Output Voltage of DA Converters

Nominal values: V_{DDA}=5V; T_A=25°C

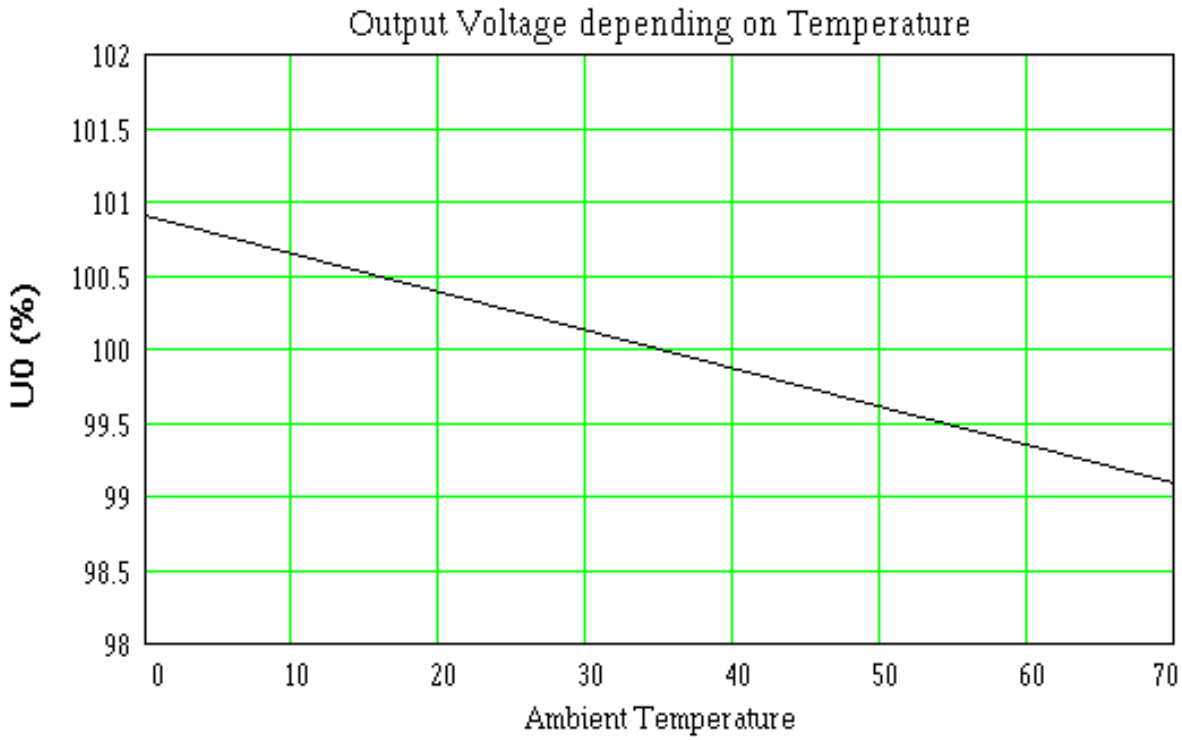


Figure 10-1 Output voltage dependency on temperature

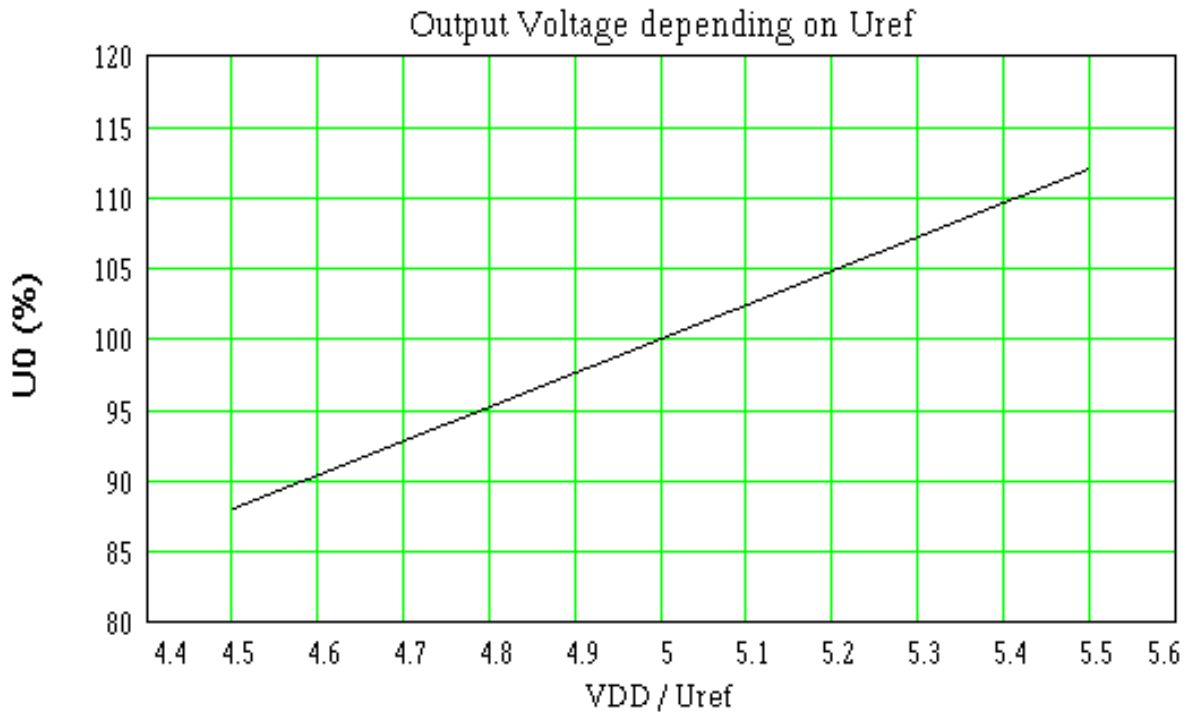


Figure 10-2 Output voltage dependency on U_{ref}

Diagrams

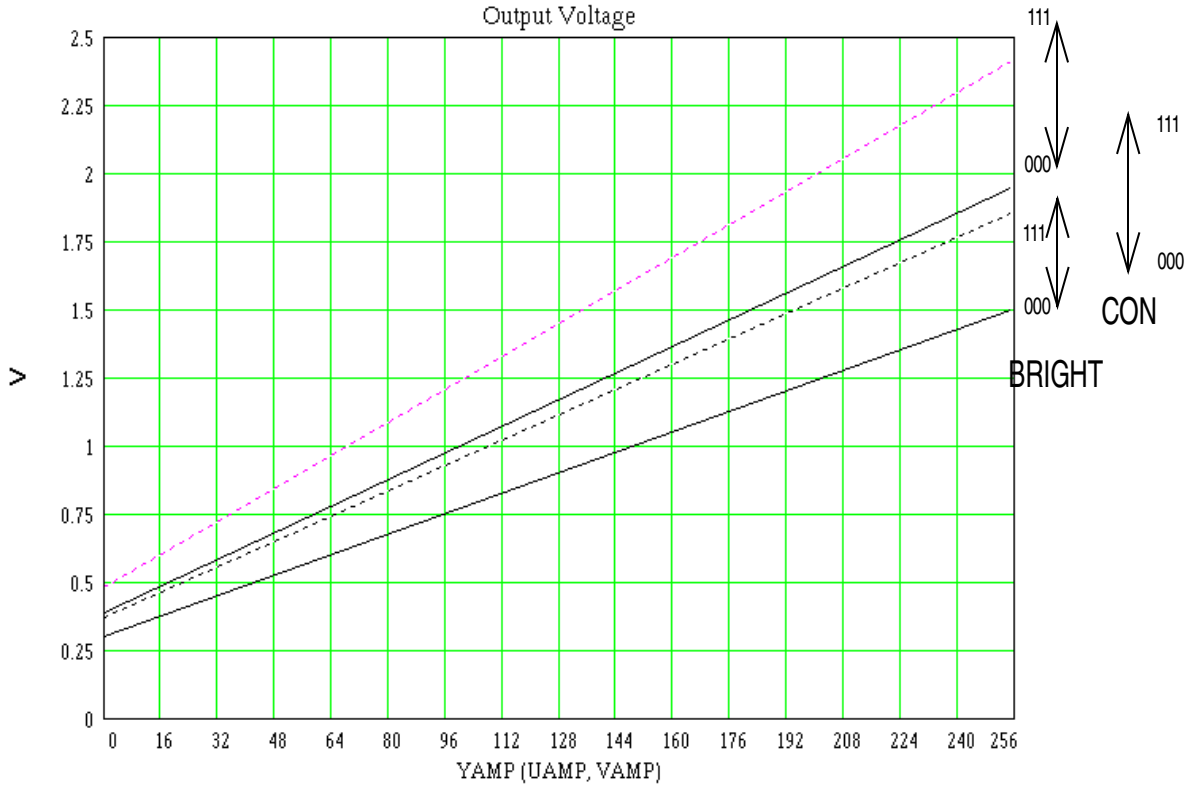


Figure 10-3 Output voltage dependency on YAMP, BRIGHT and CON

10.2 Three level input characteristic (SCP, VP/SCP)

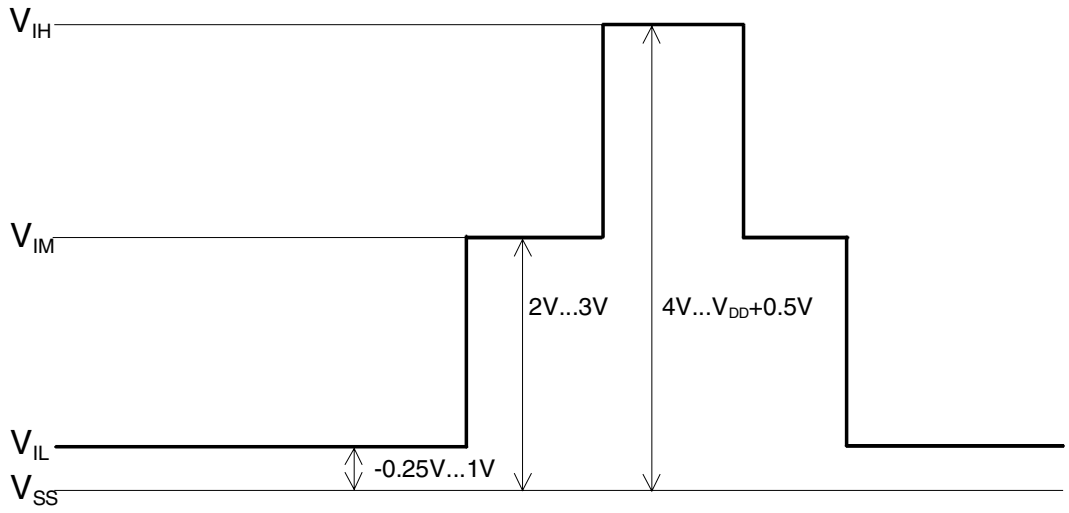
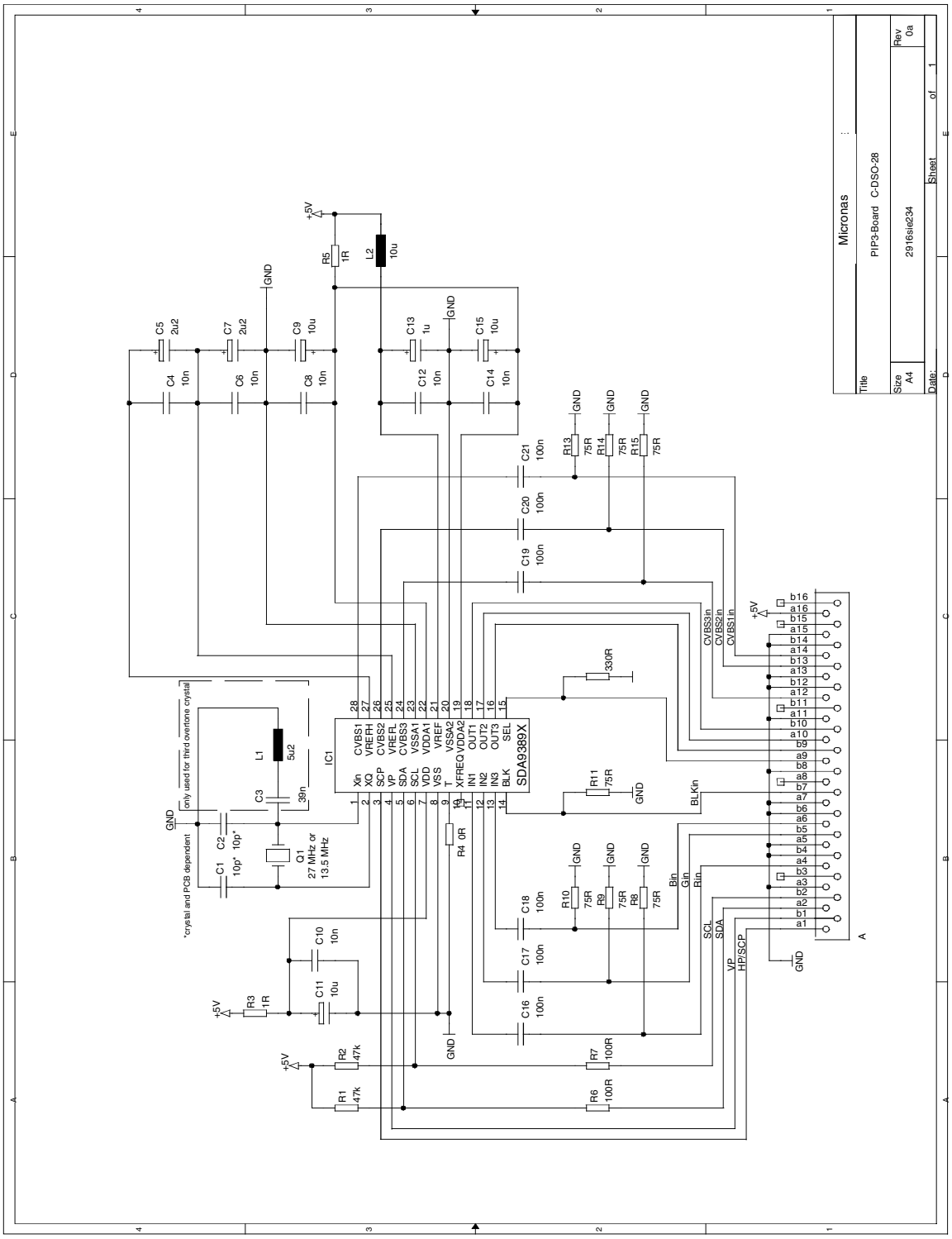


Figure 10-4 input voltages at SCP or VP/SCP for

11 Application Circuit



12 Clock Circuitry Diagram

For more details, please refer to chapter 5.1.

a) 27 MHz crystal (third overtone mode)

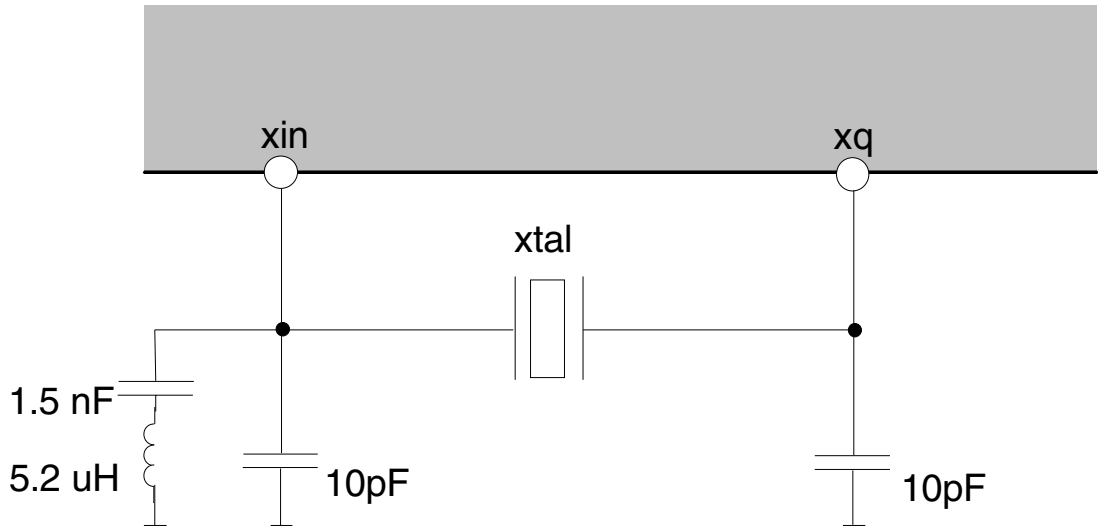


Figure 12-1 27 MHz crystal (third overtone mode)

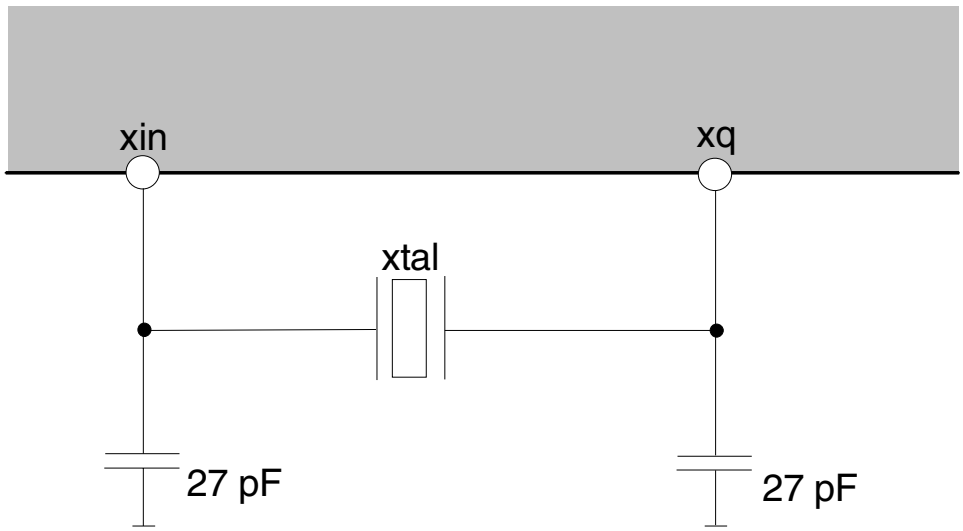
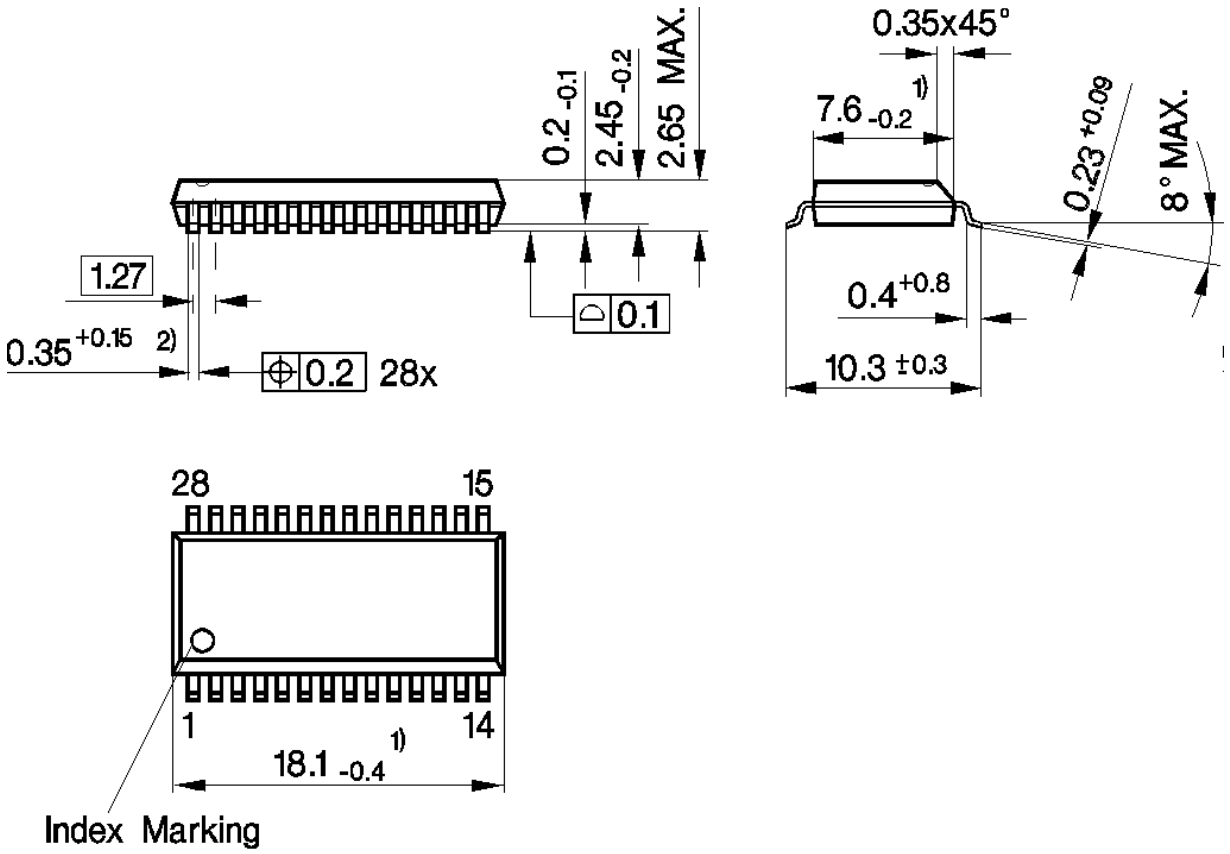


Figure 12-2 13.5 MHz / 27 MHz crystal (fundamental mode)

13 Package

P-DSO-28-1



1) Does not include plastic or metal protrusion of 0.15 max. per side

2) Does not include dambar protrusion of 0.05 max. per side

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