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ICs for Consumer Electronics

SRC-Scan Rate Converter
SDA 9255

Data Sheet 1998-02-01

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Scan Rate Converter

SDA 9255

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SDA 9255 Revision History:		Current Version: 1998-02-01
Previous Version:		1997-07-01
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
		Definition of N.C. pins

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Recommended Operating Conditions

Under this conditions the functions given in the circuit description are fulfilled. Nominal conditions specify mean values expected over the production spread and are the proposed values for interface and application. If not stated otherwise, nominal values will apply at T_A = 25°C and the nominal supply voltage.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit.

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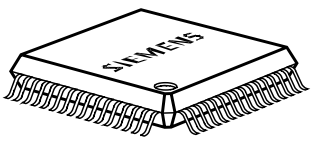
SRC-Scan Rate Converter **SDA 9255**

CMOS

1 Overview



P-MQFP-64-1

1.1 Features

- 100/120 Hz interlaced scan conversion
- Data format 4:1:1
- On chip field memory
- Digital vertical zooming
- Digital vertical panning
- Motion adaptive temporal noise reduction, field based
- Still field
- Color difference input data representation 2's complement or unsigned
- Color difference output data representation 2's complement or unsigned
- Sync Generation for backend IC
- I^2C-Bus control (400 kHz)
- P-MQFP-64 package
- 5 V ± 5 % supply voltage

1.2 General Description

The SDA 9255 is a new component of the Siemens MEGAVISION® IC set. The SDA 9255 comprises some of the functionalities of the MEGAVISION® IC's SDA 9220 (Memory Sync Controller) and SDA 9254 (Triple TV-SAM plus Noise Reduction) and can therefore be used as a low cost digital featurebox.

Type	Ordering Code	Package
SDA 9255	Q67101-H5190	P-MQFP-64-1

1.3 Pin Configuration

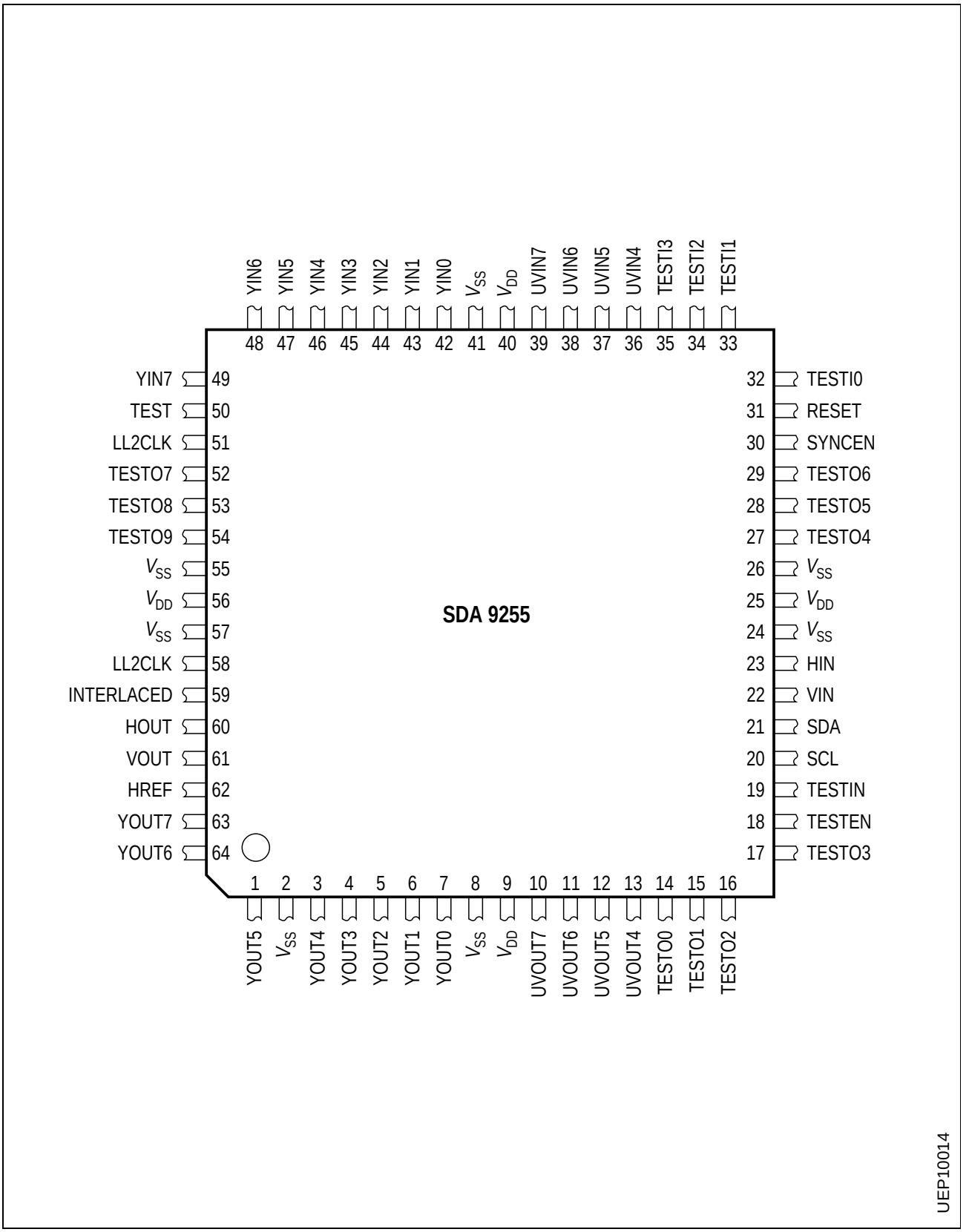


Figure 1

1.4 Pin Description

Pin No.	Name	Type	Description
2,8,24,26,41,55, 57	V_{SS}	S	Supply voltage (V_{SS} = 0 V)
9,25,40,56	V_{DD}	S	Supply voltage (V_{DD} = 5 V)
42,...,49	YIN0 ... 7	I/TTL	Data input Y (**see data format**)
36,...,39	UVIN4 ... 7	I/TTL	Data input UV (**see data format**)
30	SYNCEN	I/TTL	Synchronization enable input
31	RESET	I/TTL	System reset. The RESET input is low active. In order to ensure correct operation a **"**Power On Reset**"** must be performed. The RESET pulse must have a minimum duration of two clock periods of the system clock (LL2CLK).
23	HIN	I/TTL	H-Sync input
22	VIN	I/TTL	V-Sync input
21	SDA	I/O	I^2C-Bus data line
20	SCL	I	I^2C-Bus clock line
19	TESTIN	I/TTL	Test input, connect to V_{SS} for normal operation
18	TESTEN	I/TTL	Test enable input, connect to V_{SS} for normal operation
13,...,10	UVOUT4 ... 7	O/TTL	Data output UV (**see data format**)
7,...,3,1,64,63	YOUT0 ... 7	O/TTL	Data output Y (**see data format**)
62	HREF	O/TTL	Horizontal active video output
61	VOUT	O/TTL	V-Sync output
60	HOUT	O/TTL	H-Sync output
59	INTERLACED	O/TTL	Interlace signal for AC coupled vertical deflection
58,51	LL2CLK	I/TTL	System clock
50	TEST	I/TTL	Test input, connect to V_{SS} for normal operation
27,28,29, 52,53,54	TESTO 4...9	O	Do not connect, Pins have to be left open
14,15,16,17	TESTO 0...3	O	Not used output stages, do not connect to any other driver, V_{SS} or V_{DD} ; Pins can be left open
32,33,34,35	TESTI 0...3	I	Input stages (internal pull-down); Pins can be left open

S: supply, I: input, O: output, TTL: digital (TTL)

1.5 Block Diagram

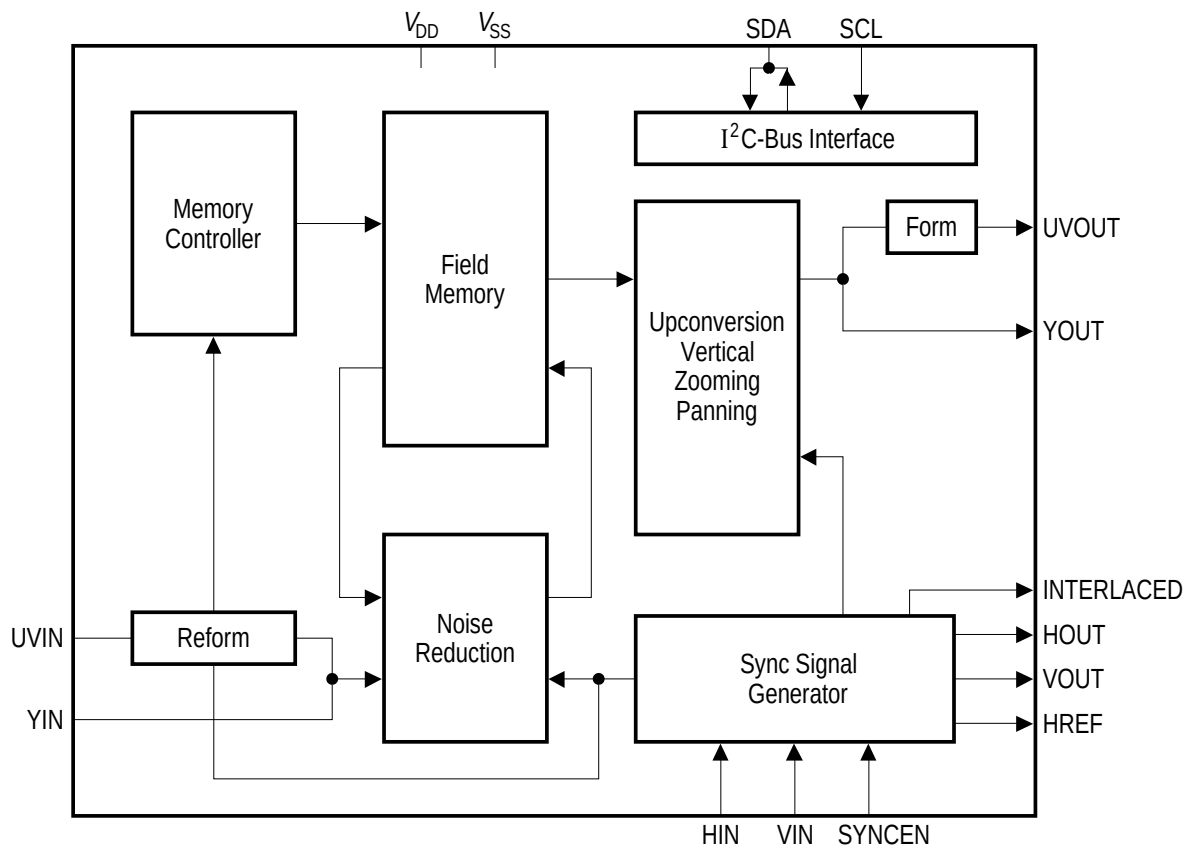


Figure 2

2 System Description

The device generates at its output an opportune sequence of 100/120 Hz fields ($\alpha\alpha\beta\beta$) [50/60 Hz frames ($\alpha\beta$)] derived by processing the field A or B which is stored in one internal field memory. The fields can be noise reduced and vertically zoomed.

Additionally the device generates a vertical sync pulse, a horizontal sync pulse and a horizontal reference signal (horizontal active video output) in phase with the output data. Furthermore an interlace signal for AC coupled vertical deflection is available.

2.1 Input Data Formats

The SDA 9255 accepts at the input side the following input format (relations of Y : (B-Y) : (R-Y) : 4 : 1 : 1). The representation of the samples of the chrominance signal is programmable as positive dual code (unsigned) or two's complement code (TWOIN, TWOOUT, subaddress 00_H, **see description of I^2C Bus**).

Data Pin	**SDA 9255**			
YIN7	Y_{07}	Y_{17}	Y_{27}	Y_{37}
YIN6	Y_{06}	Y_{16}	Y_{26}	Y_{36}
YIN5	Y_{05}	Y_{15}	Y_{25}	Y_{35}
YIN4	Y_{04}	Y_{14}	Y_{24}	Y_{34}
YIN3	Y_{03}	Y_{13}	Y_{23}	Y_{33}
YIN2	Y_{02}	Y_{12}	Y_{22}	Y_{32}
YIN1	Y_{01}	Y_{11}	Y_{21}	Y_{31}
YIN0	Y_{00}	Y_{10}	Y_{20}	Y_{30}
UVIN7	U_{07}	U_{05}	U_{03}	U_{01}
UVIN6	U_{06}	U_{04}	U_{02}	U_{00}
UVIN5	V_{07}	V_{05}	V_{03}	V_{01}
UVIN4	V_{06}	V_{04}	V_{02}	V_{00}

X_{AB}: X: signal component, A: sample number, B: bit number

The amplitude resolution for each input signal component is 8 Bit, the maximum clock frequency is 27 MHz.

2.2 Output Data Formats

Data Pin				
YOUT7	Y_{07}	Y_{17}	Y_{27}	Y_{37}
YOUT6	Y_{06}	Y_{16}	Y_{26}	Y_{36}
YOUT5	Y_{05}	Y_{15}	Y_{25}	Y_{35}
YOUT4	Y_{04}	Y_{14}	Y_{24}	Y_{34}
YOUT3	Y_{03}	Y_{13}	Y_{23}	Y_{33}
YOUT2	Y_{02}	Y_{12}	Y_{22}	Y_{32}
YOUT1	Y_{01}	Y_{11}	Y_{21}	Y_{31}
YOUT0	Y_{00}	Y_{10}	Y_{20}	Y_{30}
UVOUT7	U_{07}	U_{05}	U_{03}	U_{01}
UVOUT6	U_{06}	U_{04}	U_{02}	U_{00}
UVOUT5	V_{07}	V_{05}	V_{03}	V_{01}
UVOUT4	V_{06}	V_{04}	V_{02}	V_{00}

X_{AB}: X: signal component, A: sample number, B: bit number

2.3 Input Timing and Parameter

The SDA 9255 has five input signals:

HIN	Pin 23	Horizontal synchronization signal - low or high active
VIN	Pin 22	Vertical synchronization signal - low or high active
SYNCEN	Pin 30	Enable signal for HIN and VIN signal, low active
YIN0 ... 7	Pin 42, 43, 44, 45, 46, 47 ,48, 49	Luminance input
UVIN4 ... 7	Pin 36, 37, 38, 39	Chrominance input

The SDA 9255 includes a V-Sync delay block.This is implemented to make sure that the field identification is working correctly. This is briefly described below.

The phase relation of the incoming horizontal synchronization signal (HIN) and the incoming data for HSINP = 0 and VSINP = 0 is shown in figure 7 (**see chapter 5.1, Input Timing of the SDA 9255 (HSINP = 0)**). The SDA 9255 needs the synchronization enable input (SYNCEN) which is used to gate HIN and VIN. This is implemented for frontends which are working with 13.5 MHz and a large output delay time for H-Sync and

V-Sync (e.g. Intermetall VPC3200A, output delay: 35 ns). For this application the half system clock (13.5 MHz) from the frontend should be provided at this pin. In case the frontend is working at 27.0 MHz with sync signals whose delay time are smaller than 25 ns, this input can be set to low level (SYNCEN = V_{SS}) (e.g. Siemens SDA 9257, SDA 9206, output delay: 25 ns).

Thus the falling edge of HIN signal is detected when the SYNCEN input is low. The incoming HIN (and VIN) is sampled with the system clock (LL2CLK = 27.0 MHz). The register value HSDLY and MCNAPIP (subaddress $0B_H$ and $0C_H$, **see description of I²C Bus**) have to be adjusted in the way that the distance from the falling edge of the HIN to the first active pixel is correct. The half, quarter and eighth system clock is also shown in this diagram. They are generated inside the SDA 9255. The half system clock (LL_CLK = 13.5 MHz) is used to sample the incoming YUV data and run some blocks inside the SDA 9255. The quarter system clock (LH_CLK = 6.75 MHz) is used to run some blocks inside the SDA 9255. The eighth system clock (LQ_CLK = 3.375 MHz) is used to synchronize the 4:1:1 input data stream. The setting of the register HSDLY and MCNAPIP is explained in **chapter 1**.

The SDA 9255 has a fixed number of active pixels per input line. It is fixed to 720 luminance pixels and 180 chrominance pixels.

2.3.1 Delay of Vertical Input Synchronization Signal

In order to have always the same raster of the vertical and horizontal synchronization signal inside the SDA 9255 it is possible to shift the V-Sync signal. The subaddress 09_H of the SDA 9255 (VSDLY, **see description of I²C Bus**) controls the shift of the V-Sync. The user has to know the input sync raster and then the user can adjust the VSDLY register value in the way that the field identify circuit inside the SDA 9255 can work properly. The adjustment of the V-Sync can be done in steps of 32 clock periods (LL2CLK). Thus the delay is also dependent on the system clock frequency. The formula to calculate the delay is shown below.

$$\text{DELAY (VIN to VS\_int)} = (\text{VSDLY} * 32 + 7 \ldots 11) * T_{LL2CLK}$$

where:

VIN: Incoming V-Sync at pin 22; VSDLY: is the register value
VS_int: Internal V-Sync
T_{LL2CLK} : System clock period (e.g 1/27.0 MHz = 37.04 ns)

The initial delay (7 ... 11 system clocks) is caused by flip-flops at the input. This delay is not a fixed number, because a quarter of the system clock (LH_CLK) is used to set the delay. The phase of the LH_CLK is dependent on the RESET and the SYNCEN (**see figure 7**).

An example shows figure 9 (**see chapter 5.3, Internal Vertical Synchronization Signal (VSINP = 0)**). In this example the falling edge of the VIN signal of field A is at 35 µs and the falling edge of the VS_int signal is at 16 µs (both signals are related to the falling

edge of the previous HS_int, compare **chapter 1**). Thus the sampling points of the field identify circuit (marked in the diagram with „a“ and „b“) have uniform distances to the falling edge of the VS_int.

The falling edge of the VIN signal of field B is at 3 µs and the falling edge of the VS_int signal is at 48 µs (related to the falling edge of the previous HIN). Here the sampling points have also uniform distances to the falling edge of the VS_int signal. The user should adjust this value carefully. Dependent on the input mode of the frontend circuit the integration time of the V-Sync can change. For non-standard signals, for instance, a shorter integration time may be chosen. The internal V-Sync (VS_int) must have the falling edge at line 2 for field A. All the other settings (NALIP ...) are dependent on this internal V-Sync. The default setting of the VSDLY is $3A_H$. This corresponds to a delay of about 69 µs (58 (= $3A_H$) ∗ 32 ∗ 37 ns), which suits for the clock sync generator SDA 9257 and SDA 9206.

2.3.2 Number of Active Lines of an Input Field

The subaddress $0A_H$ (AL, **see description of I²C Bus**) is used to adjust the number of active lines per input and output field. It is independent of the MODE10050 in subaddress 00_H. The register value AL has to be chosen in the following way:

$$AL = \frac{\text{Number of lines per field} - 2}{2}; \text{ e.g. } \left(\frac{288 - 2}{2} = 143\right)$$

2.3.3 Number of Not Active Lines of an Input Field

Due to the fact that the SDA 9255 stores only the active field in the field memory, it requires the information of the start of the active field and the active line. A not-active-line counter (NALIP, subaddress $0B_H$, **see description of I²C Bus**) starts counting the incoming H-Syncs when it detects a falling edge of the VS_int signal. If VS_int is adjusted as recommended in the explanation of subaddress 09_H then the calculation of the NALIP value can be done in the following way:

NALIP = first active line of field A – 5 (e.g. 23 – 5 = 18)

In figure 10 (**see chapter 5.4, Example for Not Active Input Register**) an example for NALIP = 18 is shown. As you can see for field A 21 H-Syncs are counted and for field B 22 H-Syncs are counted. If NALIP is set to '0' line 5 is the first active line of field A and line 318 the first active line of field B (318 – 5 = 313). The difference between first active line of field B and field A should be:

δ = (No.lines per frame DIV 2) + 1; e.g. δ = 625 DIV 2 + 1 = 313

2.3.4 Not Active Pixels of Input Field

In the SDA 9255 an H-Sync delay circuit is implemented. The output of this block is the HS_int. The distance of the incoming H-Sync (HIN, falling edge for HSINP = 0) and the active data is adjustable by the HSDLY register value and the MCNAPIP register value (subaddress $0B_H$ and $0C_H$, **see description of I²C Bus**). With the HSDLY register the delay of the external (HIN) to the internal H-Sync (HS_int) is adjustable.

$$\text{DELAY (HIN to HS\_int)} = (\text{HSDLY} * 64 + 4) * T_{LL2CLK}$$

This internal H-Sync (HS_int) is fed to the memory control unit. The MCNAPIP (memory controller not active pixel at input) is used to adjust the distance to the active line in steps of one system clock period. So the MCNAPIP is used to set the phase of the internal generated clocks LL_CLK, LH_CLK and LQ_CLK.

$$\text{DELAY (HS\_int to active data)} = (\text{MCNAPIP} + 61) * T_{LL2CLK}$$

The total distance of the falling edge of the incoming H-Sync (HIN, falling edge for HSINP = 0) to the active data of the line is:

$$\text{DELAY (HIN to active data)} = (\text{HSDLY} * 64 + \text{MCNAPIP} + 65) * T_{LL2CLK}$$

In the formula above you can see that the first active pixel occurs 65 system clocks after the falling edge of the HIN signal, if HSDLY and MCNAPIP are set to zero.

In the figure 7 (**see chapter 5.1, Input Timing of the SDA 9255 (HSINP = 0)**) the input timing of the SDA 9255 is shown. The luminance and chrominance data are coming with half the system clock speed (e.g. 13.5 MHz). The SDA 9255 accepts the YIN data every second edge of the LL2CLK clock; in the SDA 9255 the luminance and chrominance data are sampled with the rising edge of the internal LL_CLK, which is half the system clock (e.g. 13.5 MHz). At the position of the first active pixel the phase of the half system clock (LL_CLK = 13.5 MHz), the quarter system clock (LH_CLK = 6.75 MHz) and the eighth system clock (LH_CLK = 3.375 MHz) is always as shown in the diagram. The LL_CLK is used for sampling the incoming data. The LQ_CLK is used to synchronize the 4:1:1 data stream.

2.4 Output Timing and Parameter

The SDA 9255 has six output signals:

HOUT	Pin 60	Horizontal synchronization signal - high active
VOUT	Pin 61	Vertical synchronization signal - high active
HREF	Pin 62	Horizontal active video output
INTERLACED	Pin 59	Interlace signal
YOUT0 ... 7	Pin 7, 6, 5, 4, 3, 1, 64, 63	Luminance output
UVOUT4 ... 7	Pin 13, 12, 11, 10	Chrominance output

There are different modes of output synchronization raster possible. The data output signal of the SDA 9255 (YOUT, UVOUT and HREF) are fed to the digital-to-analog converter. The timing of the output signals is given in figure 8 (**see chapter 5.2, Output Timing of the SDA 9255**).

2.4.1 Number of Not Active Lines of Output Field

The register values NALOP and NAPOP are used to set the position of the active output field on the screen. To do this the register value to align the not active lines (NALOP, subaddress $0D_H$, **see description of I^2C Bus**) and the register value to align the not active pixels (NAPOP, subaddress $0E_H$, **see description of I^2C Bus**) for the output signal are available.

To change the vertical position of the picture on the screen the NALOP register can be utilized. The NALOP register (not active lines for output) is used to adjust the number of not active output lines in steps of two lines in case of 100/120 Hz interlaced and in steps of four lines in case of 50/60 Hz proscan. To calculate the first active output line the following formula can be used:

for MODE10050 = 0 ==> 100/120 Hz interlaced:

FAOPL = NALOP * 2 + 3

for MODE10050 = 1 ==> 50/60 Hz proscan:

FAOPL = NALOP * 4 + 5

where

FAOPL: The first active output line
NAL_OP: Register value

The maximum value for the first active line is 65 for 100/120 Hz and 129 for 50/60 Hz.

In figure 11 (**see chapter 5.5, Example for Not Active Output Register**) an example for the setting of the NALOP register is shown. The synchronization output (HOUT,

VOUT, HREF) signals are high active. In the example the register value is 10 and the mode is '0' (100/120 Hz/interlaced).

$$FAOPL = NALOP * 2 + 3 = 10 * 2 + 3 = 23$$

So line 23 is the first active output line.

For proper operation the number of not active lines at output side plus the number of active lines have to be smaller than the total number of lines. The following formula should be true.

$$NALOP * 2 + AL * 2 + 3 \leq \text{(No. of lines per frame) DIV 2 (e.g. 312)}$$

where

AL: Register value
NALOP: Register value

2.4.2 Number of Not Active Pixels of Output Field

To change the horizontal position of the picture on the screen the NAPOP register value can be utilized. The not active pixels for output register (NAPOP) is used to adjust the number of not active output pixels of a line. The register value is multiplied by '4' and has an initial value of 9 ... 12 (HSODLY = 0), depending on the MCNAPIP setting (subaddress $0B_H$ and $0C_H$, **see description of I²C Bus**).

$$FAOPP = NAPOP * 4 + 9 \ldots 12 - HSODLY = 0$$

$$FAOPP = NAPOP * 4 + (-163) \ldots (-160) ; HSODLY = 1$$

is equal to : $FAOPP = NAPOP * 4 + 9 \ldots 12 - 172 * HSODLY$

where

FAOPP: The first active output pixel after rising edge of HOUT
NAPOP: Register value
HSODLY: Register value

The time from the rising edge of the HOUT signal to the first active output pixel can be calculated in the following way:

$$t_{NAPOP} = (NAPOP * 4 + 9 \ldots 12) * t_{LL2CLK} ; HSODLY = 0$$

$$t_{NAPOP} = (NAPOP * 4 + (-163) \ldots (-160)) * t_{LL2CLK} ; HSODLY = 1$$

where

t_{NAPOP} : Time from rising edge of HOUT to first active output pixel

t_{LL2CLK} : System clock period (e.g. 1/27 MHz)

figure 12 (**see chapter 5.6, Example for Not Active Output Pixels**) shows the effect of the register NAPOP.

2.4.3 VOUT, HOUT and HREF Signal Length

The length of the output synchronization signals (HOUT, VOUT) is fixed. The HOUT signal is active high with a length of 32 system clocks (27.0 MHz) which corresponds to a length of 1.185 µs. The VOUT signal is also active high with a length of 2 output lines. So in case of PAL B/G the active high period of the VOUT lasts for 64 µs (**see figure 13, Timing for HOUT Signal and figure 14, Timing for VOUT Signal**).

The HOUT signal of the SDA 9255 can be delayed by a fixed value of 172 system clocks (27.0 MHz) by setting the HSODLY bit of subaddress $0F_H$ to '1'(**see description of I^2C Bus**). The number of active pixels per line is constant 720 pixels. The HREF output signal (pin 62) indicates the active part of the output lines. The length is also constant (720 system clocks). During the vertical and horizontal blanking period this signal is low. The timing is shown in figure 15 (**see chapter 5.9, Timing for HREF Signal**). The chrominance output format is like the output format as described in **chapter 1**.

2.4.4 Output Synchronization Raster and Interlaced Output Signal

The output synchronization and data raster in 100/120 Hz mode can be set by the MODESYNC register value (subaddress 01_H, **see description of I^2C Bus**). In case of MODE10050 = 1 (50/60 Hz pro-scan mode) this register value has no effect.

The interlaced signal INTERLACED (pin 59) is a control signal which may be used to control an AC coupled vertical deflection unit. If the MODESYNC register value (subaddress 01_H, **see description of I^2C Bus**) is set to AABB mode, where field 2 and 3 have to be shifted down (MODESYNC = 10). For this the interlaced register INTL (subaddress $0D_H$ and $0E_H$, **see description of I^2C Bus**) must be set to 0110. In figure 16 (**see chapter 5.10, Example for INTERLACED Signal**) an example for the INTL register value is shown. Bit zero defines the output for the first field (field A); bit one defines the output for the second field (field A); bit two defines the output of the third field (field B); bit three defines the output of the fourth field (field B). So if the bit is set to zero then the output is low and if the bit is set to one then the output is high. For DC coupled vertical deflection the INTERLACED signal is not required.

2.5 Motion Adaptive Temporal Noise Reduction

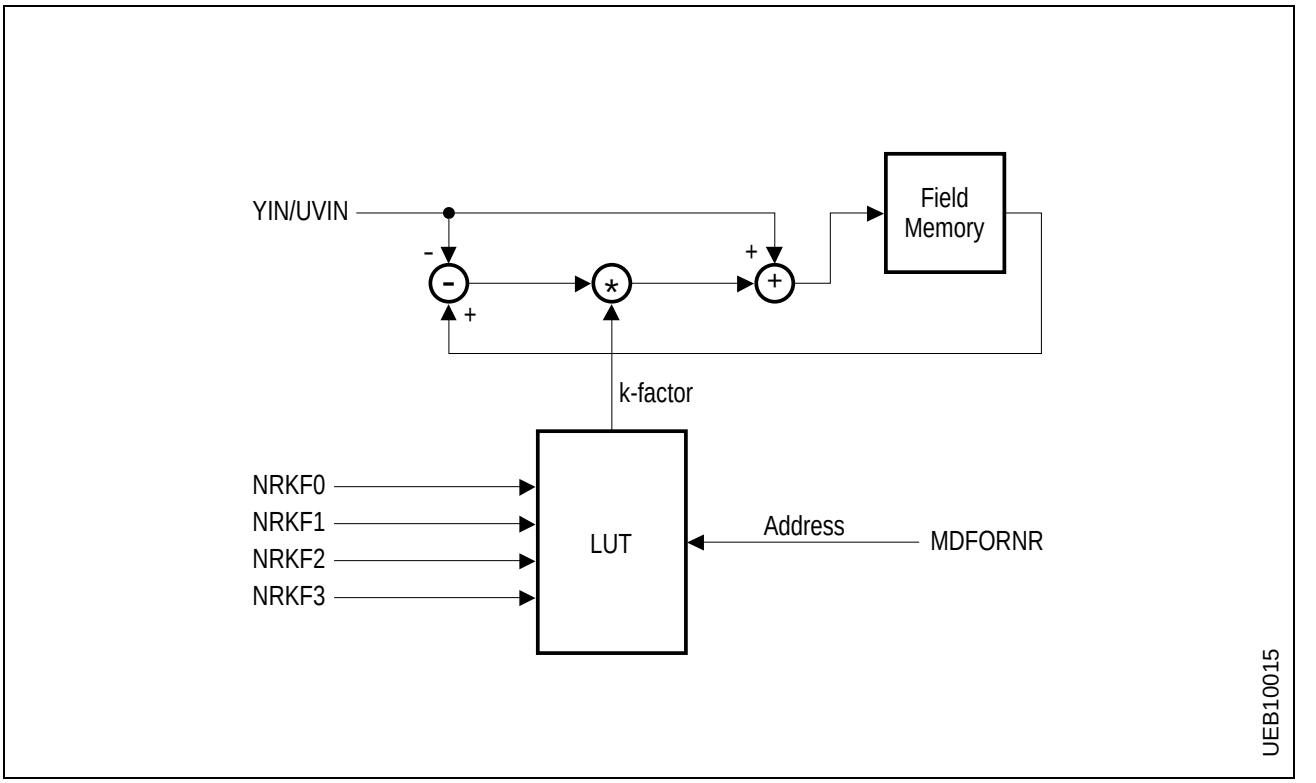


Figure 3
Block Diagram of Noise Reduction

The diagram above shows a block diagram of the motion adaptive noise reduction. The noise reduction in the luminance path has the same structure as the noise reduction in the chrominance path. Subaddresses 02_H and 03_H (NRKF0, NRKF1, NRKF2, NRKF3, **see description of I^2C Bus**) are used to align the filter coefficients of the noise reduction IIR filter. Four different k-factors NRKF0 ... 3 can be modified which are fed to the multiplier of the IIR filter. Depending on the output of the motion detection for noise reduction (MDFORNR) the corresponding k-factor NRKF0 ... 3 is used for the IIR filter (**see the table below**).

Table 1
MDFORNR and Corresponding k-Factor

MDFORNR	k-Factor	Mode
0	NRKF0	Still
1	NRKF1	Quasi still
2	NRKF2	Quasi motion
3	NRKF3	Motion

For NRKF0 ... 3 values between 0 and 7 can be chosen. The following table shows the theoretical amount of noise reduction dependent on the applied k-factor.

Table 2
Filter Coefficients Dependent on the k-Factor

k-Factor	Amount of NR
0	0 dB
1	1.1 dB
2	2.2 dB
3	3.4 dB
4	4.8 dB
5	6.4 dB
6	8.5 dB
7	11.8 dB

The subaddresses 04_H, 05_H and 06_H (MDNRTH0, MDNRTH1, MDNRTH2, **see description of I^2C Bus**) are used to align the motion detection for noise reduction (MDFORNR). The sensitivity of the motion detection is influenced by changing the threshold levels of the motion values. A rough block diagram of the motion detection for noise reduction is shown below.

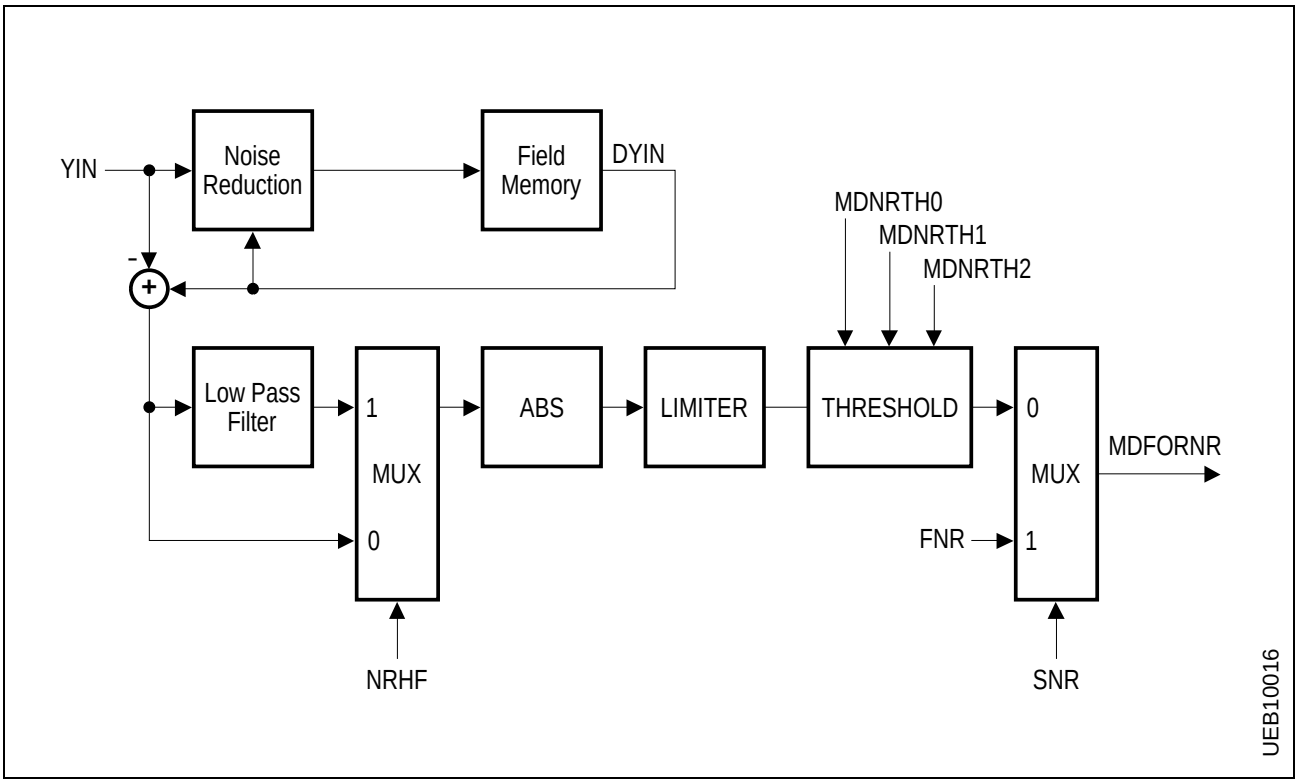


Figure 4
Block Diagram of Motion Detection for Noise Reduction

The input signals for the motion detection for noise reduction are the just incoming luminance signal (YIN) and the already noise reduced luminance signal on one field delay (DYIN). Both signals are fed to a subtractor, followed by a low pass filter. This filter can be bypassed by setting the NRHF bit (**see description subaddress 08_H, Bit 0**) to '0'. The absolute value is calculated and given to a limiter block. The output signal is fed to the threshold block, where the value is quantized by using the 3 threshold values MDNRTH0, MDNRTH1 and MDNRTH2. The quantization characteristic of the threshold block is shown by the following table and diagram.

Table 3
Quantization Table of MDFORNR

Input Value	Output	Mode
0 ... (TH0 – 1)	0	Still
TH0 ... (TH1 – 1)	1	Quasi still
TH1 ... (TH2 – 1)	2	Quasi motion
TH2 ... 31	3	Motion

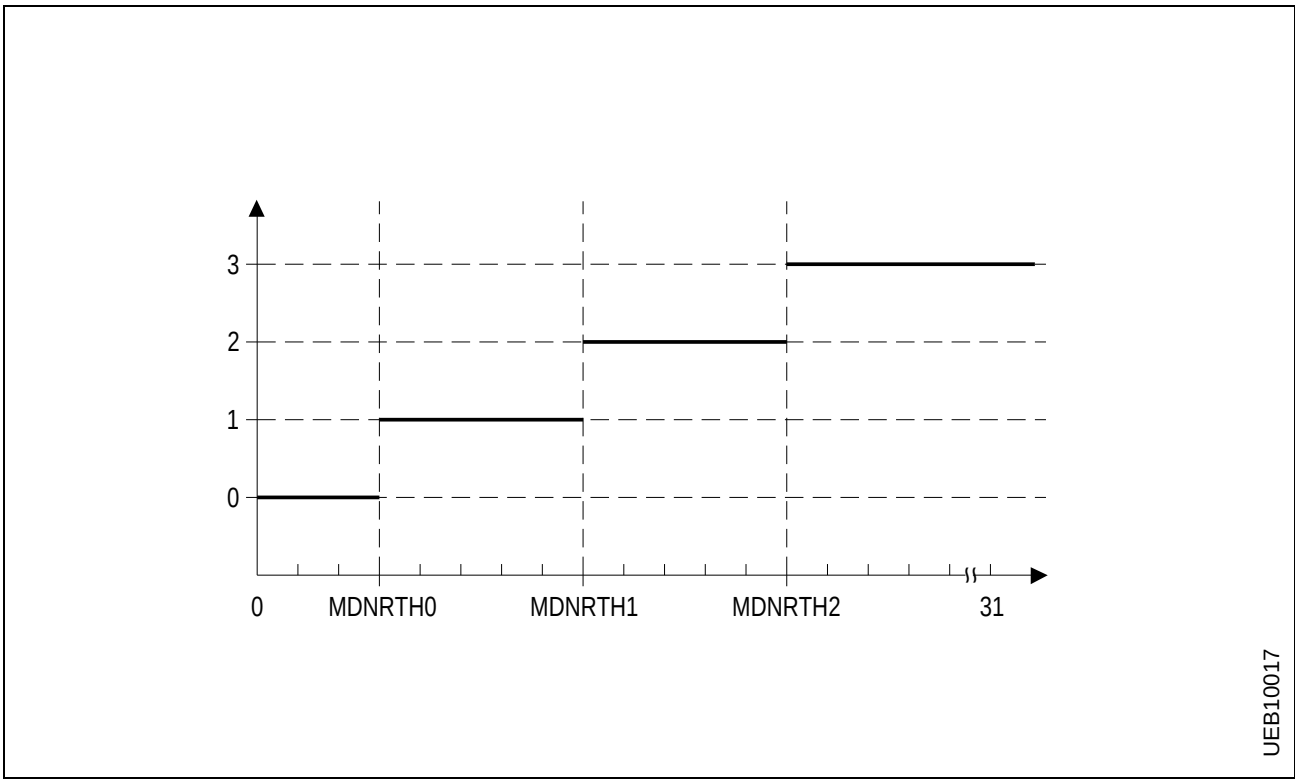


Figure 5
Quantization Characteristic of MDFORNR

The following table shows an example for noise reduction settings. These five settings could be implemented and the customer can choose, which he prefers. For example, to have a subjective impression of medium noise reduction of the picture, you have to set the k-factors: NRKF0 = 4, NRKF1 = 3, NRKF2 = 2, NRKF3 = 0 and MDNRTH0 = 4, MDNRTH1 = 8 and MDNRTH2 = 12.

Table 4
Example for Noise Reduction Settings

	Amount of Noise Reduction				
Parameter	**No**	**Slightly**	**Medium**	**Strong**	**Heavy**
NRKF0	0	3	4	7	7
NRKF1	0	2	3	4	5
NRKF2	0	1	2	2	3
NRKF3	0	0	0	0	1
MDNRTH0	don’t care	2	4	4	4
MDNRTH1	don’t care	6	8	10	10
MDNRTH2	don’t care	10	12	14	16

2.6 Digital Vertical Zooming and Panning

The user can choose 17 different zoom factors and 37 pan factors. Every zoom factor can be used without considering other register values, but on the other hand the pan factor is very much dependent on the zoom factor. So be careful in choosing the pan factor. In the following table the zoom factor (subaddress $0F_H$, **see description of I^2C Bus**) and the corresponding visual zoom of the input field is shown. In the third column the required number of input lines is shown, when the number of displayed output lines is 288. The fourth column shows the allowed value PAN value (subaddress 10_H, **see description of I^2C Bus**) and the last column the PAN register value for vertical centre position.

Table 5
Table of Zoom Factors and Panning Factors

Zoom	Visual Zoom	NoIPL (NoOPL = 288)	Panning Range PAN	Centre Panning PAN
16	1	288	0	0
15	1.03	279	0 ... 2	1
14	1.06	270	0 ... 4	2
13	1.10	261	0 ... 6	3
12	1.14	252	0 ... 9	4
11	1.18	243	0 ... 11	5
10	1.23	234	0 ... 13	6
9	1.28	225	0 ... 15	7
8	1.33	216	0 ... 18	8
7	1.39	207	0 ... 20	10
6	1.45	198	0 ... 22	11
5	1.52	189	0 ... 24	12
4	1.6	180	0 ... 27	13
3	1.68	171	0 ... 29	14
2	1.77	162	0 ... 31	15
1	1.88	153	0 ... 33	17
0	2.0	144	0 ... 36	18

Dependent on the zoom factor the SDA 9255 requires a certain number of input lines of a field.

$$NoIPL = NoOPL \times \frac{ZOOM \times 2 + 32}{64}$$

where

NoIPL: Number of required input lines
NoOPL: Number of generated output lines (AL * 2) + 2
ZOOM: Register value (0 ... 16)

In the third column of the table above the required number of input lines is shown, if the generated number of output lines is 288 (AL = 143). In the last row you can see that for the visual zoom factor of 2 half the number of input lines is necessary, which is of course obvious.

As mentioned before, only zoom factors between '0' and '16' are allowed. If factors bigger than 16 are chosen, they are set to '16'.

Panning is possible in steps of 4 input lines. So the first active input line which is used to generate the first active output line can be calculated in the following way:

$$FAIPL = PAN * 4 + 1$$

where

FAIPL: First active input line to generate the first active output line
PAN: Register value

With PAN = 0 the first active input line is line 1, as expected. In case of PAN = 1 the first active input line is line 5, etc.

So the allowed register value for pan can be calculated from the last column of the table above. In this example with 288 active lines and, for instance, zoom factor of '15', the maximum pan factor is '2'. Pan = '3' is permitted which can be seen by this calculation: $3 * 4 + 279 = 291$. The required number of input lines plus the panning lines is larger than the actual number of input lines (288). A formula to calculate the maximum pan factor is shown below.

$$PAN \leq int\left(\frac{NoOPL - NoIPL}{4}\right)$$

After some rearranging of the formula we get this simple formula to calculate the maximum register value of the pan factor.

$$PAN \leq int\left(\frac{NoOPL}{8} \times \frac{16 - ZOOM}{16}\right)$$

where

NoIPL: Number of required input lines
NoOPL: Number of generated output lines (AL * 2) + 2

ZOOM: Register value (0 ... 16)
PAN: Register value (0 ... 63)

In the fourth column of table 5 the panning range is shown for NoOPL = 288.

If the pan factor is larger than specified in the previous equation, the last input line is used for interpolation of the remaining lines. On the screen the last line is repeated.

2.7 I²C Bus

2.7.1 I²C-Bus Slave Address

1	0	1	1	1	1	0

Write Address: BC_H
Read Address: BD_H

2.7.2 I²C-Bus Format

The SDA 9255 I²C-Bus interface acts as a slave receiver and a slave transmitter and provides three different access modes (write, read, continuous read). All modes run with a subaddress auto increment. The interface supports the normal 100 kHz transmission speed as well as the high speed 400 kHz transmission.

Write:

S	1	0	1	1	1	1	0	0	A	Subaddress	A	Data Byte	A	*****	A	P

S: Start condition
A: Acknowledge
P: Stop condition
NA: Not Acknowledge

Read:

S	1	0	1	1	1	1	0	0	A	Subaddress	A	S	1	0	1	1	1	1	0	1	A	Data Byte	A

*****	Data Byte	NA	P

Continuous Read:

S	1	0	1	1	1	1	0	1	A	Data Byte	A	*****	Data Byte	NA	P

The transmitted data are internally stored in registers. The master has to write a don't care byte to the subaddress FF_H (store command) to make the register values available for the SDA 9255. To have a defined time step, where the data will be available, the data are made valid with the incoming V-Sync or with the next SYNC_ST pulse, which is an internal signal and indicates the start of a new output cycle of either four fields in 100/120 Hz interlaced mode or two frames in 50/60 Hz proscan mode. The subaddresses, where the data are made valid with the V-Sync (every 20 ms) are indicated in the overview of the subaddresses with „V“, where the data are made valid with the

SYNC_ST (every 40 ms) are indicated with „S“. The I^2C-Bus status bits of the SDA 9255 ($sub19_H$, Bit 7; $sub1E_H$, Bit 7) reflect the state of the register values. If these bits are read as ’0’ then the store command was sent, but the data aren’t made available yet. If these bits are ’1’ then the data were made valid and a new write or read cycle can start. The I^2C-Bus status bits have to be checked before writing or reading new data, otherwise data can be lost by overwriting.

After switching on the IC, all bits of the SDA 9255 are set to defined states. In particular:

Subaddress	**Default Value**	**R/W**	**Take Over**	**Subaddress**	**Default Value**	**R/W**	**Take Over**
00_H	$6F_H$	R/W	S	$0C_H$	$A2_H$	R/W	V
01_H	56_H	R/W	S	$0D_H$	50_H	R/W	S
02_H	68_H	R/W	V	$0E_H$	$2C_H$	R/W	S
03_H	23_H	R/W	V	$0F_H$	81_H	R/W	S
04_H	10_H	R/W	V	10_H	00_H	R/W	S
05_H	30_H	R/W	V	11_H ... 18_H	not used	R/W	
06_H	50_H	R/W	V	19_H		R	
07_H	not used	R/W		$1A_H$ ... $1D_H$	not used	R/W	
08_H	61_H	R/W	V	$1E_H$		R	
09_H	74_H	R/W	V	$1F_H$ ... FE_H	not used	R/W	
$0A_H$	$8F_H$	R/W	V	FF_H		W	
$0B_H$	94_H	R/W	V				

R/W: R-Read Register, W-Write Register, R/W-Read and Write Register,
Take over: V-take over with V-Sync, S-take over with SYNC_ST

2.7.3 I²C-Bus Commands

Subadd. (Hex.)	Data Byte							
	D7	D6	D5	D4	D3	D2	D1	D0
00_H	MODE10050	1	1	FREEZE	TWOIN	TWOOUT	TVMODE1	TVMODE0
01_H	0	1	0	1	0	MODESYNC1	MODESYNC0	0
02_H	NRKF02	NRKF01	NRKF00	NRKF12	NRKF11	NRKF10	x	x
03_H	NRKF22	NRKF21	NRKF20	NRKF32	NRKF31	NRKF30	HSINP	VSINP
04_H	MDNRTH04	MDNRTH03	MDNRTH02	MDNRTH01	MDNRTH00	x	x	x
05_H	MDNRTH14	MDNRTH13	MDNRTH12	MDNRTH11	MDNRTH10	x	x	x
06_H	MDNRTH24	MDNRTH23	MDNRTH22	MDNRTH21	MDNRTH20	x	x	x
08_H	SNR	FNR1	FNR0	x	x	x	x	NRHF
09_H	VSDLY6	VSDLY5	VSDLY4	VSDLY3	VSDLY2	VSDLY1	VSDLY0	x
$0A_H$	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
$0B_H$	NALIP4	NALIP3	NALIP2	NALIP1	NALIP0	MCNAPIP6	MCNAPIP5	MCNAPIP4
$0C_H$	MCNAPIP3	MCNAPIP2	MCNAPIP1	MCNAPIP0	HSDLY3	HSDLY2	HSDLY1	HSDLY0
$0D_H$	NALOP4	NALOP3	NALOP2	NALOP1	NALOP0	INTL3	INTL2	INTL1
$0E_H$	NAPOP6	NAPOP5	NAPOP4	NAPOP3	NAPOP2	NAPOP1	NAPOP0	INTL0
$0F_H$	ZOOM4	ZOOM3	ZOOM2	ZOOM1	ZOOM0	x	x	HSODLY
10_H	PAN5	PAN4	PAN3	PAN2	PAN1	PAN0	x	x
19_H	VSTATUS	x	x	x	x	x	x	x
$1E_H$	SSTATUS	x	x	x	x	x	x	x
FF_H	x	x	x	x	x	x	x	x

x = don’t care

2.7.4 Detailed Description

Subaddress 00_H

Bit	Name	Function
D7	MODE10050	Output mode switch: 0: 100/120 Hz (default value) 1: 50/60 Hz
D6		1: Should be set to 1
D5		1: Should be set to 1
D4	FREEZE	Still picture: 0: Off (default value) 1: On
D3	TWOIN	Chrominance input format: 0: Unsigned input (0 ... 255) 1: 2's complement input (-128 ... 127) (default value) Inside the SDA 9255 the data are always processed as unsigned data
D2	TWOOUT	Chrominance output format: 0: Unsigned output (0 ... 255) 1: 2's complement output (-128 ... 127) (default value)
D1 ... D0	TVMODE	Television system: 00: NTSC (1716) 01: Automatic PAL (n ∗ 32) 10: Automatic NTSC (n ∗ 32 + 20) 11: PAL (1728) (default value) The SDA 9255 is designed for a line-locked system. Therefore the number of system clock periods between two H-Sync (HIN) must be constant. In PAL (1728) mode the number of system clocks (~27.0 MHz) per input line is assumed to be constant 1728. In case of NTSC (1716) mode the number of system clock periods is assumed to be constant 1716. In automatic mode (01 and 10) the number of system clock periods (~27.0 MHz) per incoming line is measured and used to calculate the outgoing line length. In automatic PAL mode the number of system clock periods between two H-Syncs must be n ∗ 32 (n = 1, 2, ..., 54, ...). In automatic NTSC mode the number of system clock periods between two H-Syncs must be n ∗ 32 + 20 (n = 1, 2, ..., 53, ...).

Subaddress 01_H

Bit	Name	Function
D7 ... D3		Should be set to 01010
D2 ... D1	MODESYNC	Output synchronization mode: 00: Reserved 01: AABB mode for AC coupled vertical deflection, no data shift 10: AABB mode for AC coupled vertical deflection, field 2 and 3 shift down 11: AABB mode for DC coupled vertical deflection (default value)
D0		0: Should be set to 0

Subaddress 02_H

Bit	Name	Function
D7 ... D5	NRKF0	Noise Reduction k-factor KF 0: 011: (default value)
D4 ... D2	NRKF1	Noise Reduction k-factor KF 1: 010: (default value)
D1 ... D0		xx

Subaddress 03_H

Bit	Name	Function
D7 ... D5	NRKF2	Noise Reduction k-factor KF 2: 001: (default value)
D4 ... D2	NRKF3	Noise Reduction k-factor KF 3: 000: (default value)
D1	HSINP	H-Sync input polarity: 0: Low active 1: High active (default value)
D0	VSINP	V-Sync input polarity: 0: Low active 1: High active (default value)

Subaddress 04_H

Bit	Name	Function
D7 ... D3	MDNRTH0	Noise Reduction threshold 0: 00010: (default value)
D2 ... D0		xxx

Subaddress 05_H

Bit	Name	Function
D7 ... D3	MDNRTH1	Noise Reduction threshold 1: 00110: (default value)
D2 ... D0		xxx

Subaddress 06_H

Bit	Name	Function
D7 ... D3	MDNRTH2	Noise Reduction threshold 2: 01010: (default value)
D2 ... D0		xxx

Subaddress 08_H

Bit	Name	Function
D7	SNR	Switch for fixed value for motion detection for noise reduction 0: Off (default value) 1: On
D6 ... D5	FNR	Fixed value for motion detection for noise reduction 11: (default value)
D4 ... D1		xxxx
D0	NRHF	Switch for low pass filter for motion detection for noise reduction 0: Off 1: On (default value)

Subaddress 09_H

Bit	Name	Function
D7 ... D1	VSDLY	V-Sync input delay (default value $3A_H$)
D0		x

Subaddress $0A_H$

Bit	Name	Function
D7 ... D0	AL	(Number of active input lines per field – 2) / 2 (default value $8F_H$)

Subaddress $0B_H$

Bit	Name	Function
D7 ... D3	NALIP	Number of not active lines of input data (default value 12_H)
D2 ... D0	MCNAPIP6 ... 4	Number of system clocks from internal HS_int to active input data, Bit 6 to 4 (default value 4_H)

Subaddress $0C_H$

Bit	Name	Function
D7 ... D4	MCNAPIP3 ... 0	Number of system clocks from internal HS_int to active input data, bit 3 to 0 (default value A_H)
D3 ... D0	HSDLY	H-Sync input delay (default value 2_H)

Subaddress $0D_H$

Bit	Name	Function
D7 ... D3	NALOP	Number of active lines at output (default value A_H)
D2 ... D0	INTL3 ... 1	Interlace output for field Bit 3 to 1 (default value 0_H)

Subaddress $0E_H$

Bit	Name	Function
D7 ... D1	NAPOP	Number of not active pixels at output (default value 16_H)
D0	INTL0	Interlace output for field bit 0 (default value 0_H)

Subaddress $0F_H$

Bit	Name	Function
D7 ... D3	ZOOM	Zooming factor (default value 10_H)
D2 ... D1		xx
D0	HSODLY	Delay of H-Sync output (default value 1_H)

Subaddress 10_H

Bit	Name	Function
D7 ... D2	PAN	Panning of the output picture (default value 0_H)
D1 ... D0		xx

Subaddress 19_H

Bit	Name	Function
D7	VSTATUS	Status bit for subaddresses, which will be made valid by V-Sync
D6 ... D0		xxxxxxx

Subaddress $1E_H$

Bit	Name	Function
D7	SSTATUS	Status bit for subaddresses, which will be made valid by SYNC_ST
D6 ... D0		xxxxxxx

Subaddress FF_H

Bit	Name	Function
D7 ... D0		Store command for all subaddresses, xxxxxxxx

3 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remark
		min.	max.		
Operating temperature	T_A	0	70	°C	
Storage temperature		-65	125	°C	
Junction temperature			125	°C	
Soldering temperature			260	°C	
Soldering time			10	s	
Input voltage		-0.3	V_{DD} + 0.3	V	
Output voltage		-0.3	V_{DD} + 0.3	V	
Supply voltages	V_{DD}	-0.3	6	V	
Total power dissipation			1.2	W	
ESD protection		-2	2	kV	MIL STD 883C method 3015.6, 100 pF, 1500 Ω
Latch-up protection		-100	100	mA	All inputs/outputs

All voltages listed are referenced to ground (0 V, V_{SS}) except where noted.

Note: *Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the operational sections of this specification is not implied.*

3.1 Recommended Operating Conditions

Parameter	Symbol	Limit Values			Unit	Remark
		min.	nom.	max.		
Supply voltages	V_{DD}	4.75	5	5.25	V	
Ambient temperature	T_A	0	25	70	°C	
All TTL Inputs						
H-input voltage	V_{IH}	2.0		V_{DD}	V	
L-input voltage	V_{IL}	0		0.8	V	
All TTL Outputs						
H-output voltage	V_{QH}	2.4			V	I_{QH} = -2.0 mA
L-output voltage	V_{QL}			0.4	V	I_{QL} = 3.0 mA
INPUT/OUTPUT: SDA						
L-output voltage	V_{QL}			0.5	V	at I_{QL} = max
Clock TTL Input LL2CLK						
Clock frequency	1/T		27		MHz	**see figure 19**
Low time	t_{WL}	12			ns	
High time	t_{WH}	12			ns	
Rise time	t_{TLH}			5	ns	
Fall time	t_{THL}			5	ns	
I²C Bus (All values are referred to min (V_{IH}) and max (V_{IL})), f_{SCL} = 400 KHz						
H-input voltage	V_{IH}	3		V_{DD}	V	**see figure 17**
L-input voltage	V_{IL}	0		1.5	V	**see figure 18**
SCL clock frequency	f_{SCL}	0		400	kHz	
Inactive time before start of transmission	t_{BUF}	1.3			µs	
Set-up time start condition	$t_{SU;\,STA}$	0.6			µs	
Hold time start condition	$t_{HD;\,STA}$	0.6			µs	
SCL low time	t_{LOW}	1.3			µs	
SCL high time	t_{HIGH}	0.6			µs	
Set-up time DATA	$t_{SU;\,DAT}$	100			ns	
Hold time DATA	$t_{HD;\,DAT}$	0			µs	

3.1 Recommended Operating Conditions (cont'd)

Parameter	Symbol	Limit Values			Unit	Remark
		min.	nom.	max.		
SDA/SCL rise times	t_R			300	ns	
SDA/SCL fall times	t_F			300	ns	
Set-up time stop condition	$t_{SU;\,STO}$	0.6			µs	
Output valid from clock	t_{AA}			900	ns	
Input filter spike suppression (SDA and SCL pins)	t_{SP}			50	ns	
L-output current	I_{QL}			3	mA	

3.2 Characteristics (Assuming Recommended Operating Conditions)

Parameter	Symbol	Limit Values		Unit	Remark
		min.	max.		
Average supply current	I_{CC}		200	mA	All V_{DD} pins, typ. 170 mA
All Digital Inputs (Including I/O Inputs)					
Input capacitance	C_I		10	pF	
Input leakage current	$I_{I(L)}$	-10	10	µA	
TTL Inputs: YIN, UVIN (Referred to LL2CLK)					
Set-up time	t_{SU}	0		ns	
Input hold time	t_{IH}	25		ns	
TTL Inputs: HIN, VIN, SYNCEN (Referred to LL2CLK)					
Set-up time	t_{SU}	7		ns	
Input hold time	t_{IH}	6		ns	
TTL Outputs: YOUT, UVOUT, HOUT, VOUT, HREF, INTERLACED (Referred to LL2CLK)					
Hold time	t_{QH}	6		ns	
Delay time	t_{QD}	25		ns	C_L = 30 pF

4 Application Information

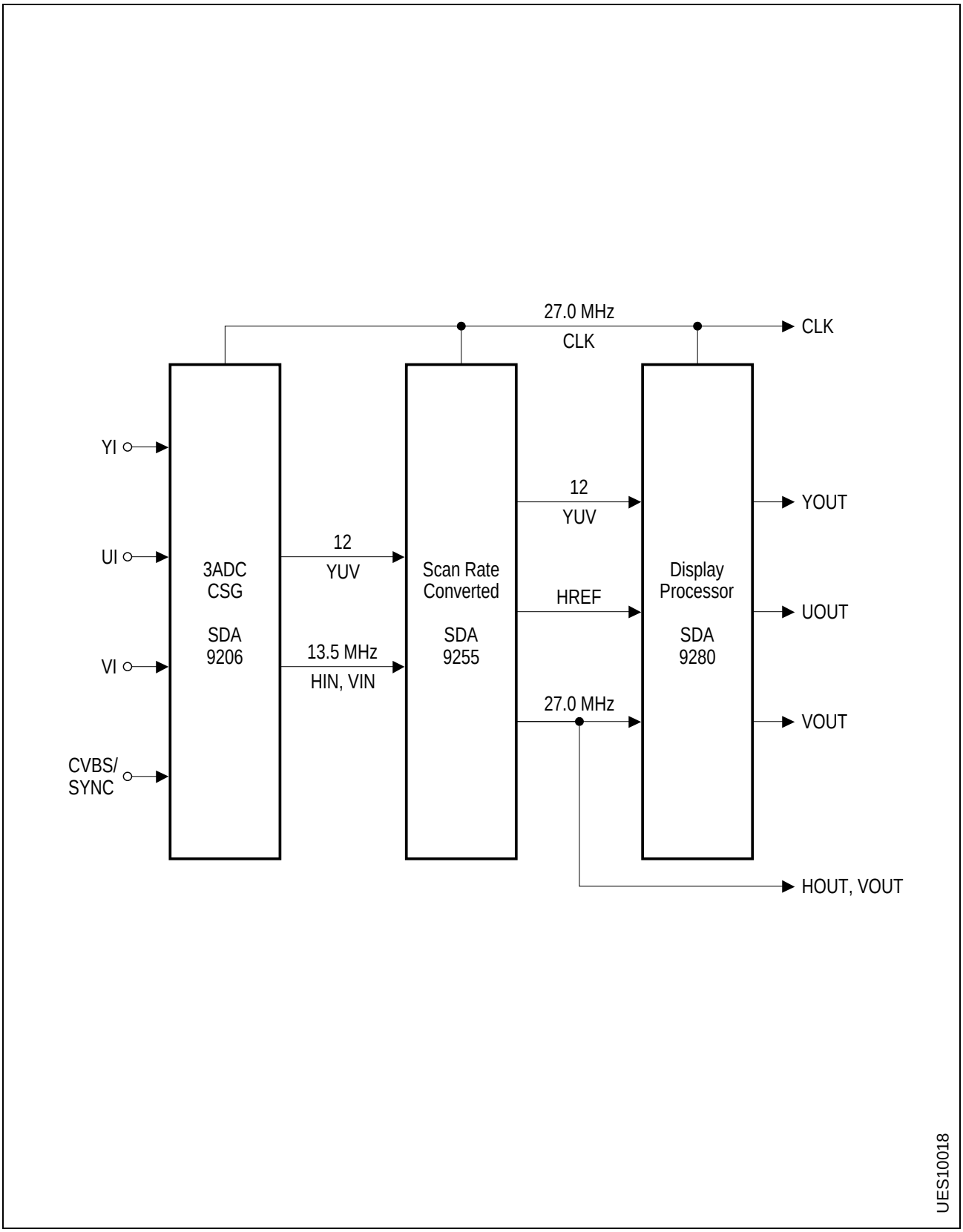


Figure 6

5 Waveforms

5.1 Input Timing of the SDA 9255 (HSINP = 0)

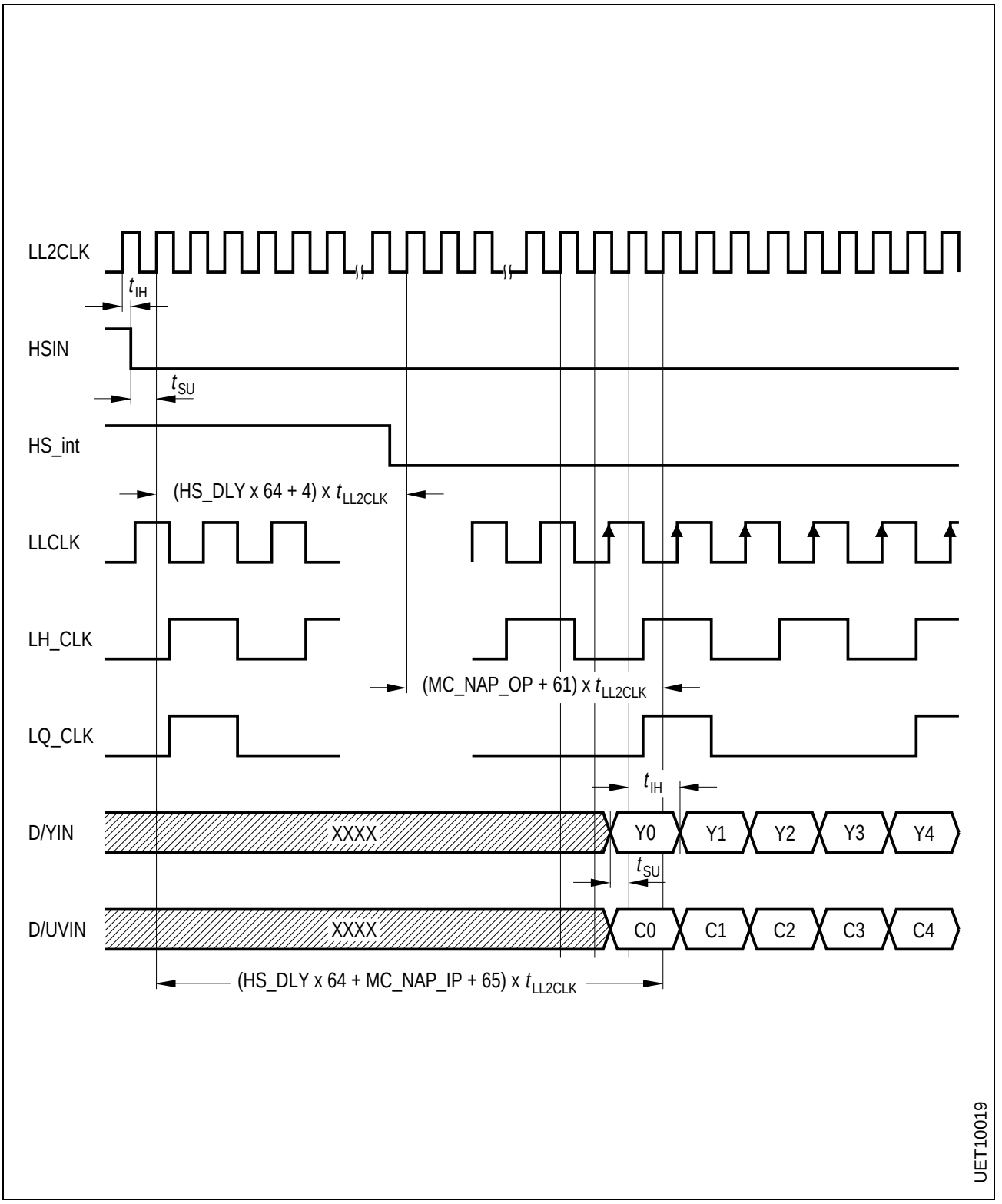


Figure 7

5.2 Output Timing of the SDA 9255

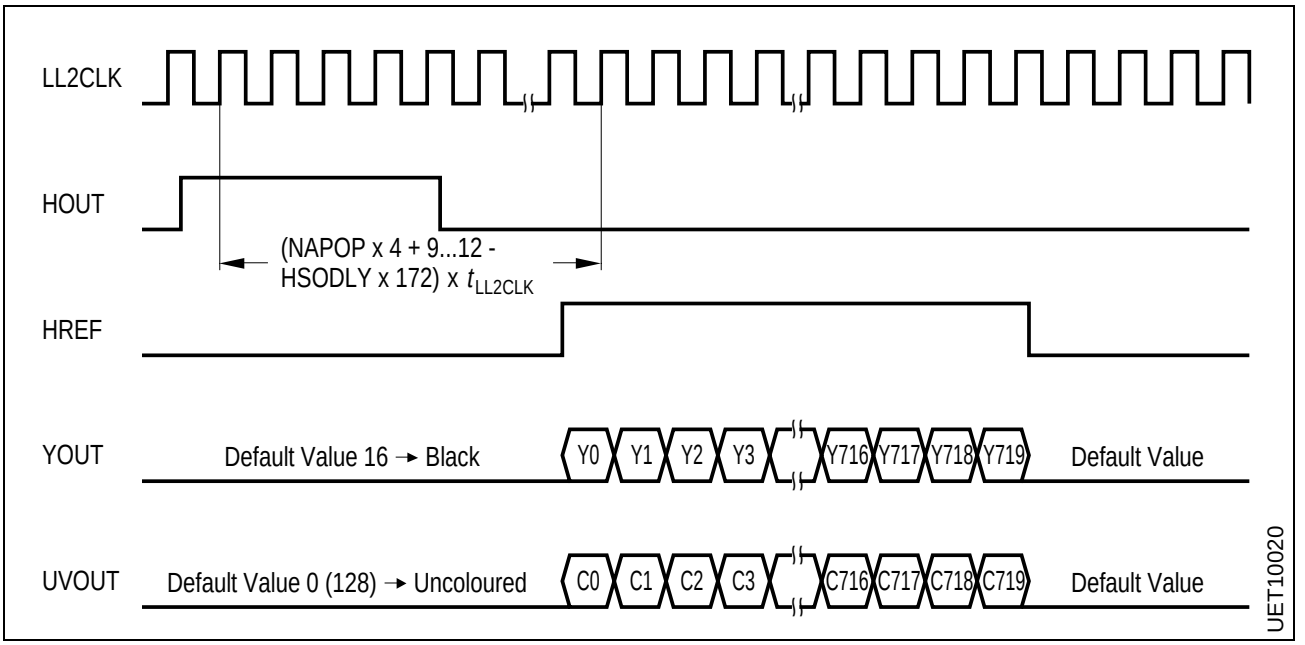


Figure 8

5.3 Internal Vertical Synchronization Signal (VSINP = 0)

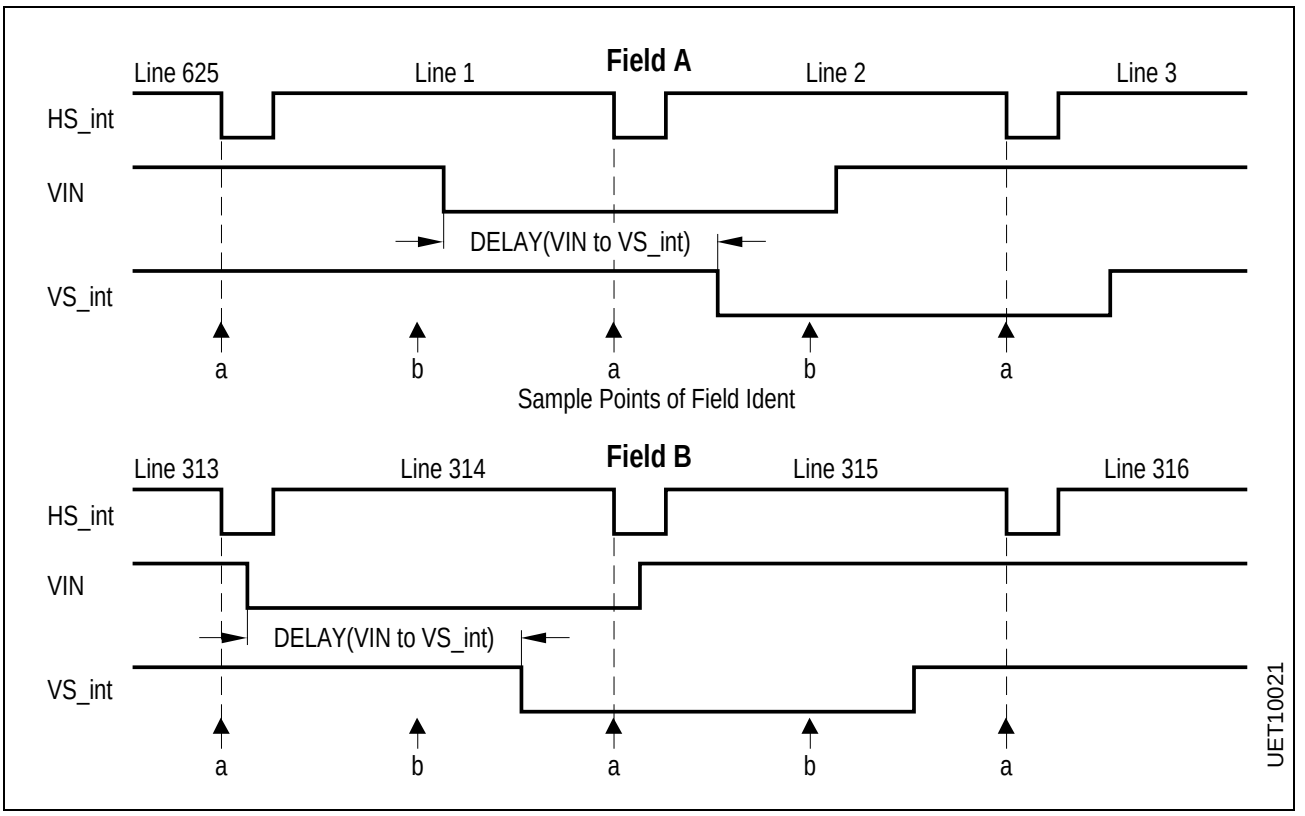


Figure 9

5.4 Example for Not Active Input Register

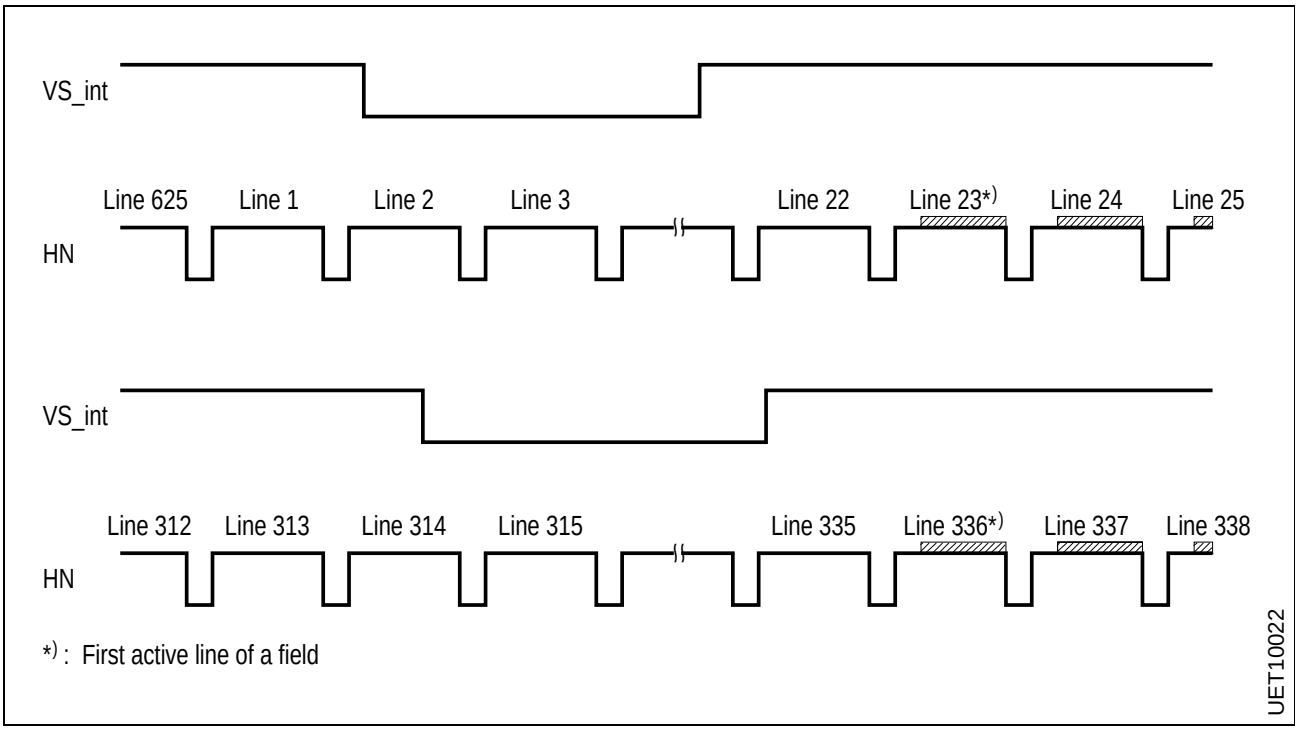


Figure 10

5.5 Example for Not Active Output Register

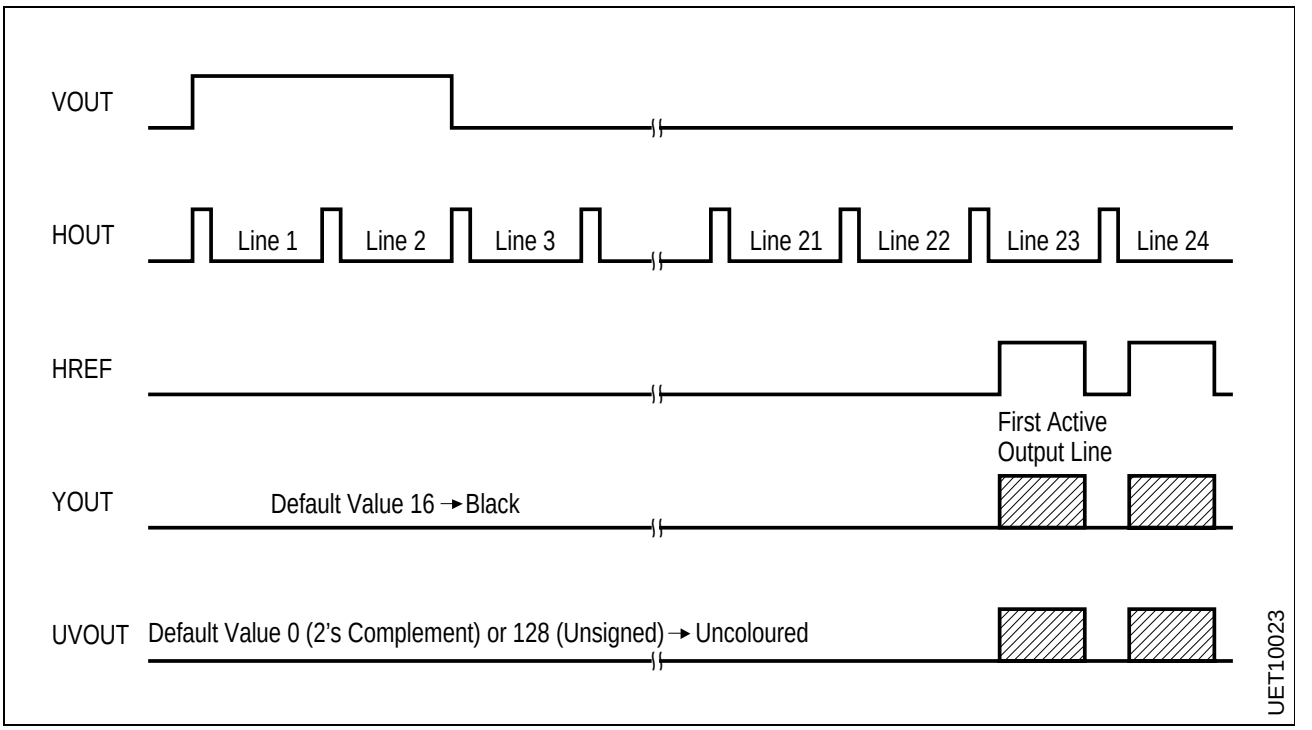


Figure 11

5.6 Example for Not Active Output Pixels

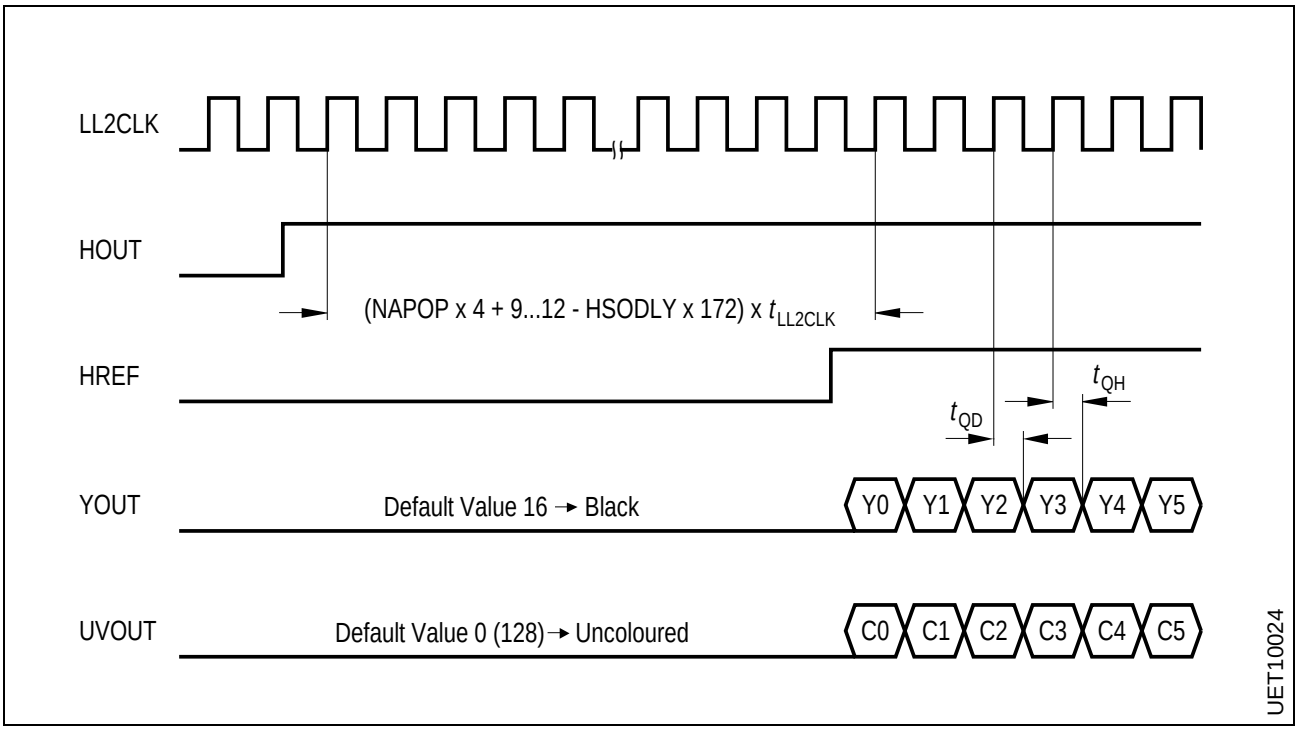


Figure 12

5.7 Timing for HOUT Signal

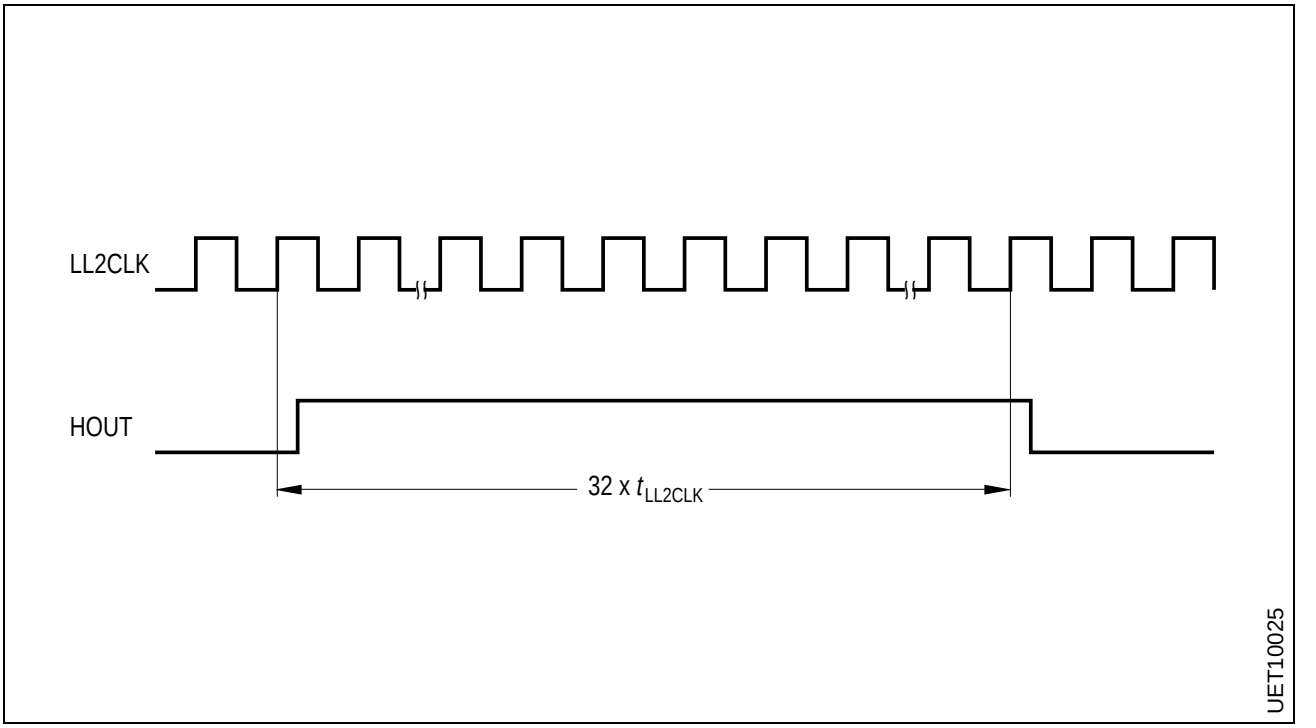


Figure 13

5.8 Timing for VOUT Signal

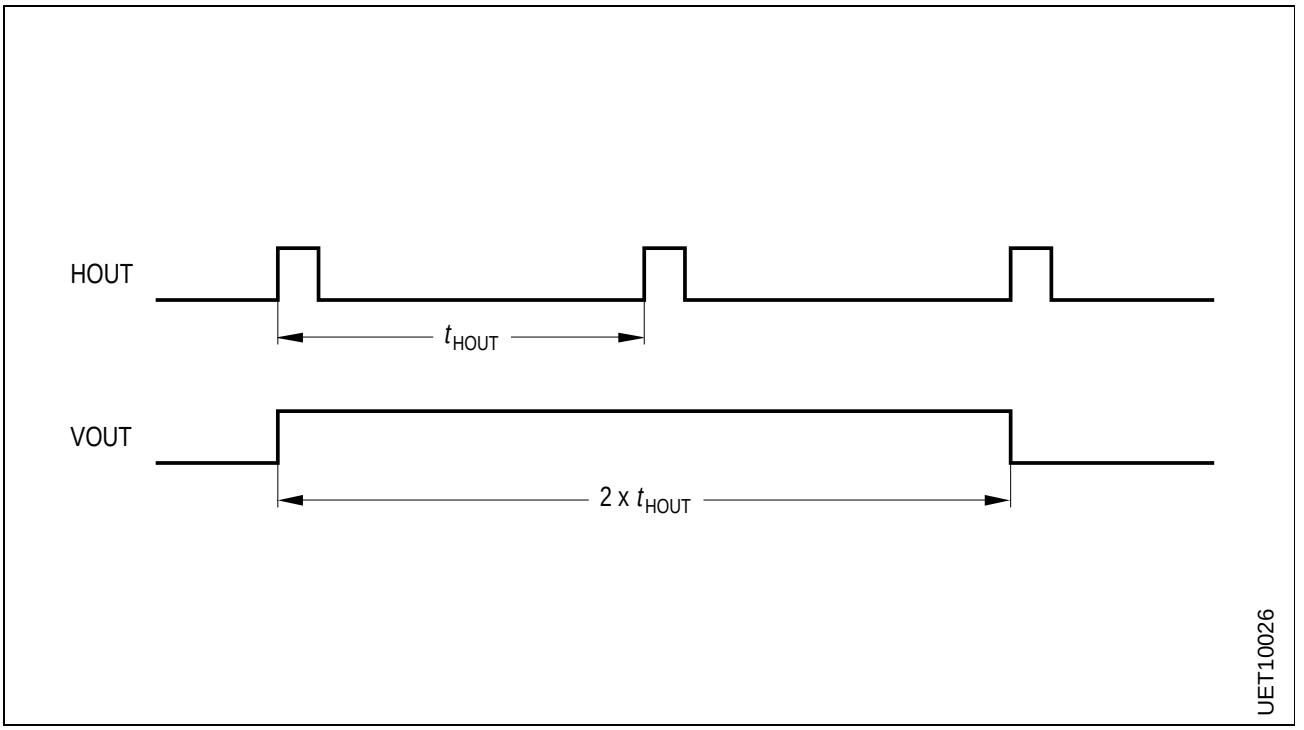


Figure 14

5.9 Timing for HREF Signal

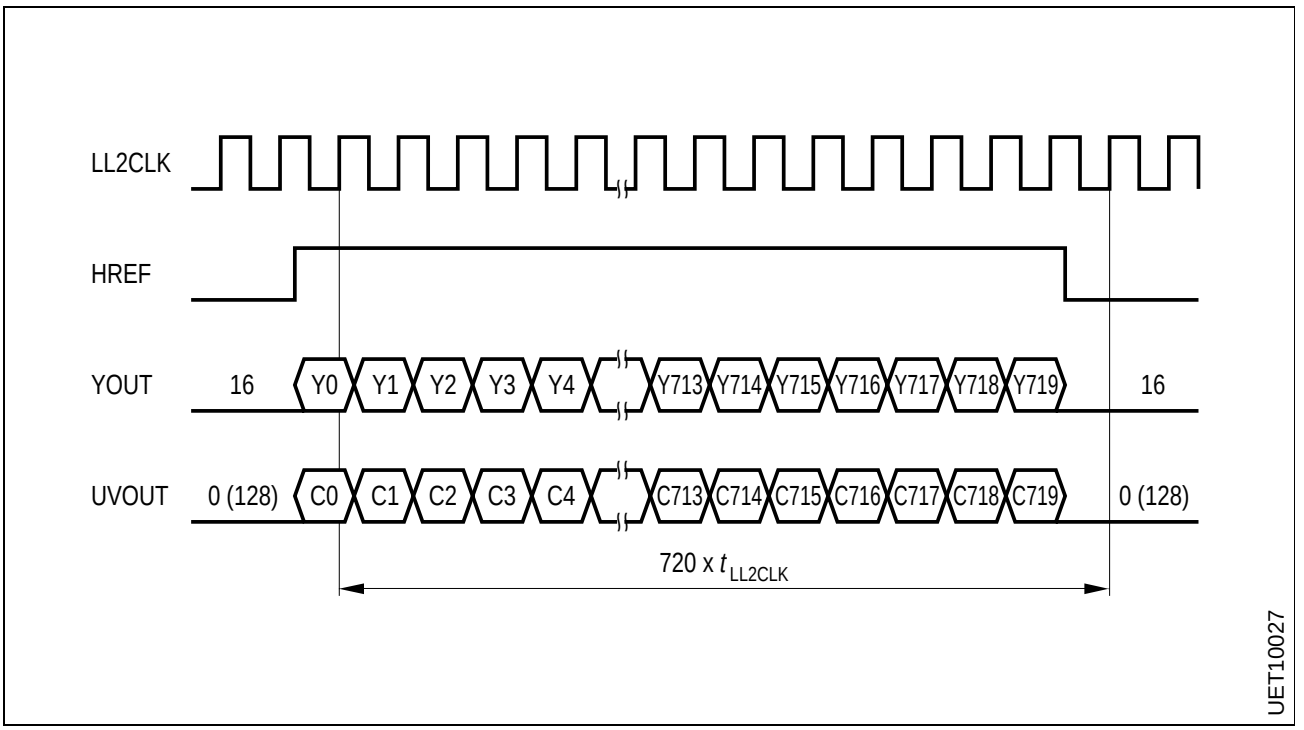


Figure 15

5.10 Example for INTERLACED Signal

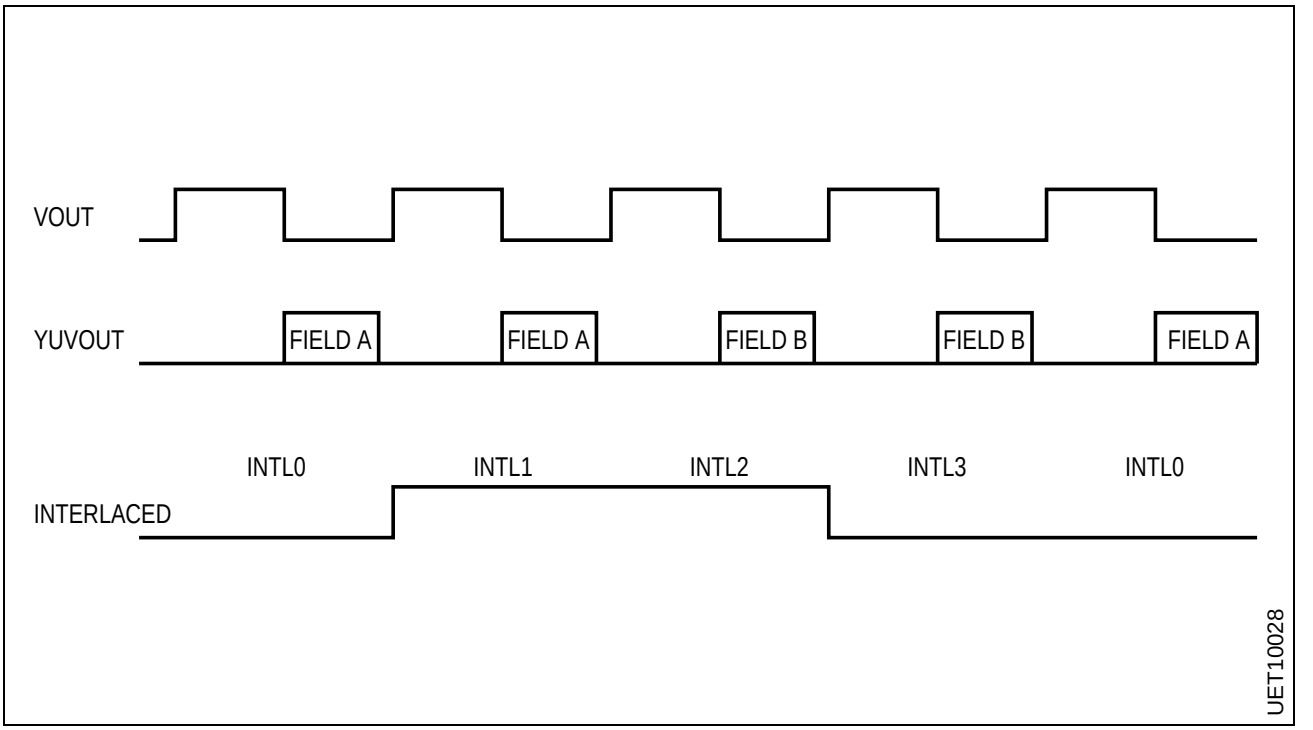


Figure 16

5.11 I²C-Bus Timing START/STOP

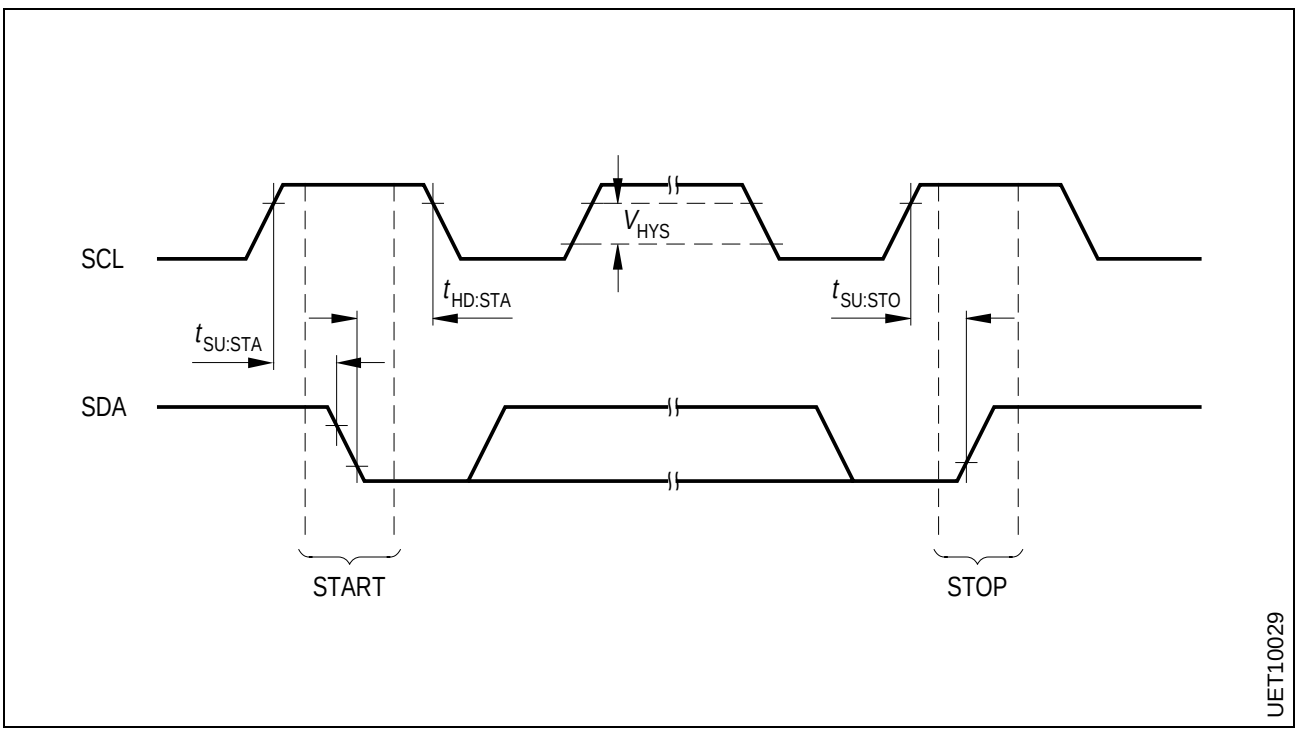


Figure 17

5.12 I²C-Bus Timing DATA

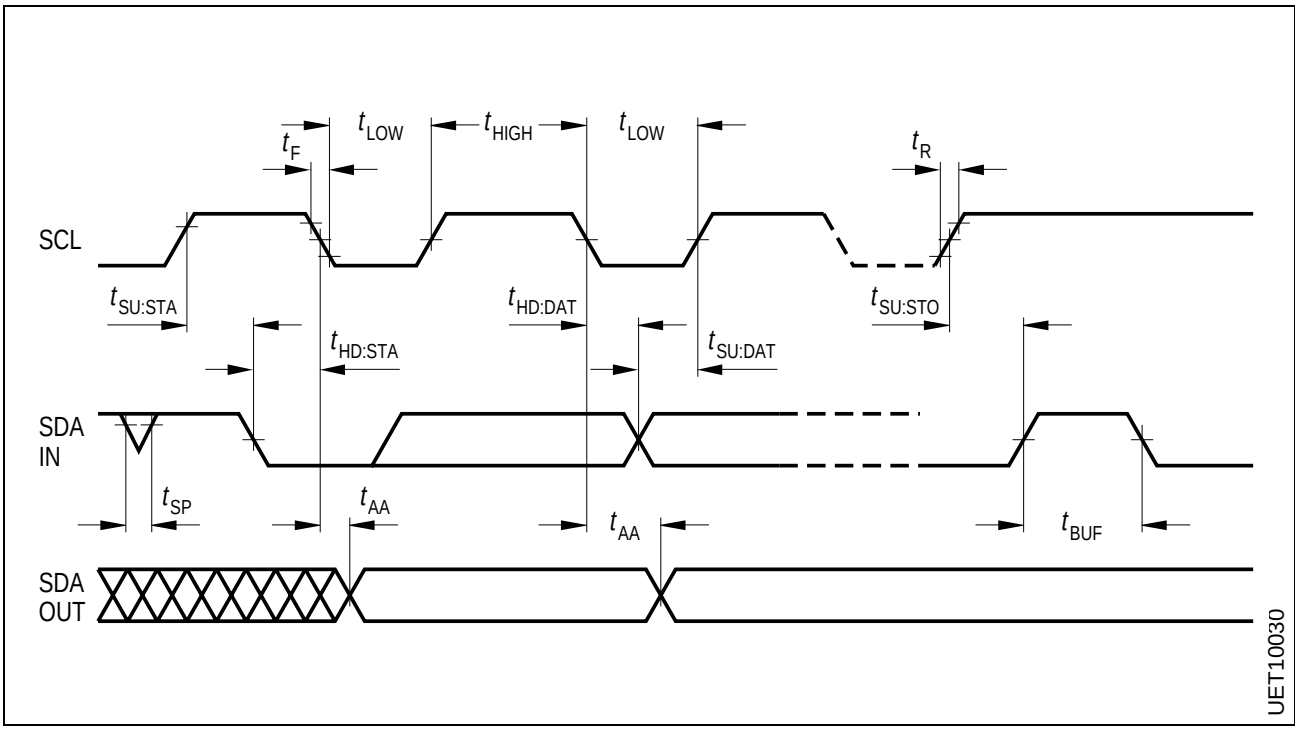


Figure 18

5.13 Timing Diagram Clock

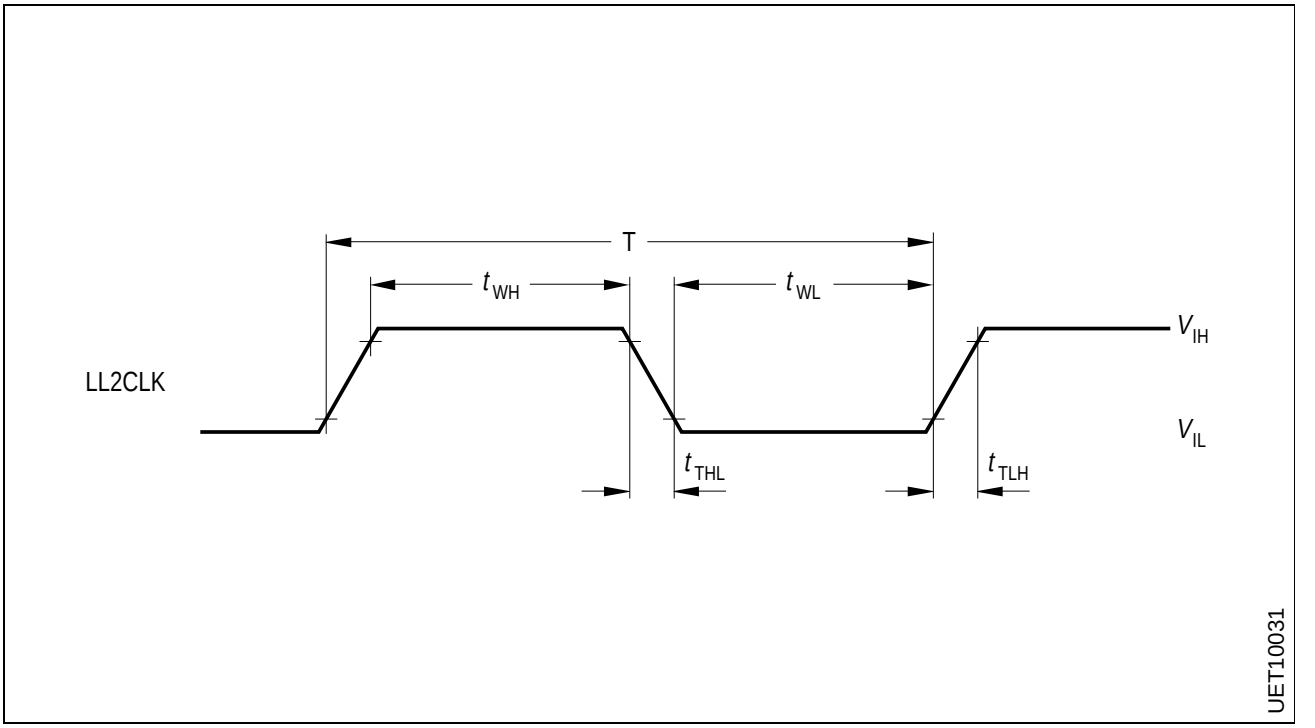


Figure 19

6 Package Outlines

P-MQFP-64-1
(Plastic Metric Quad Flat Package)

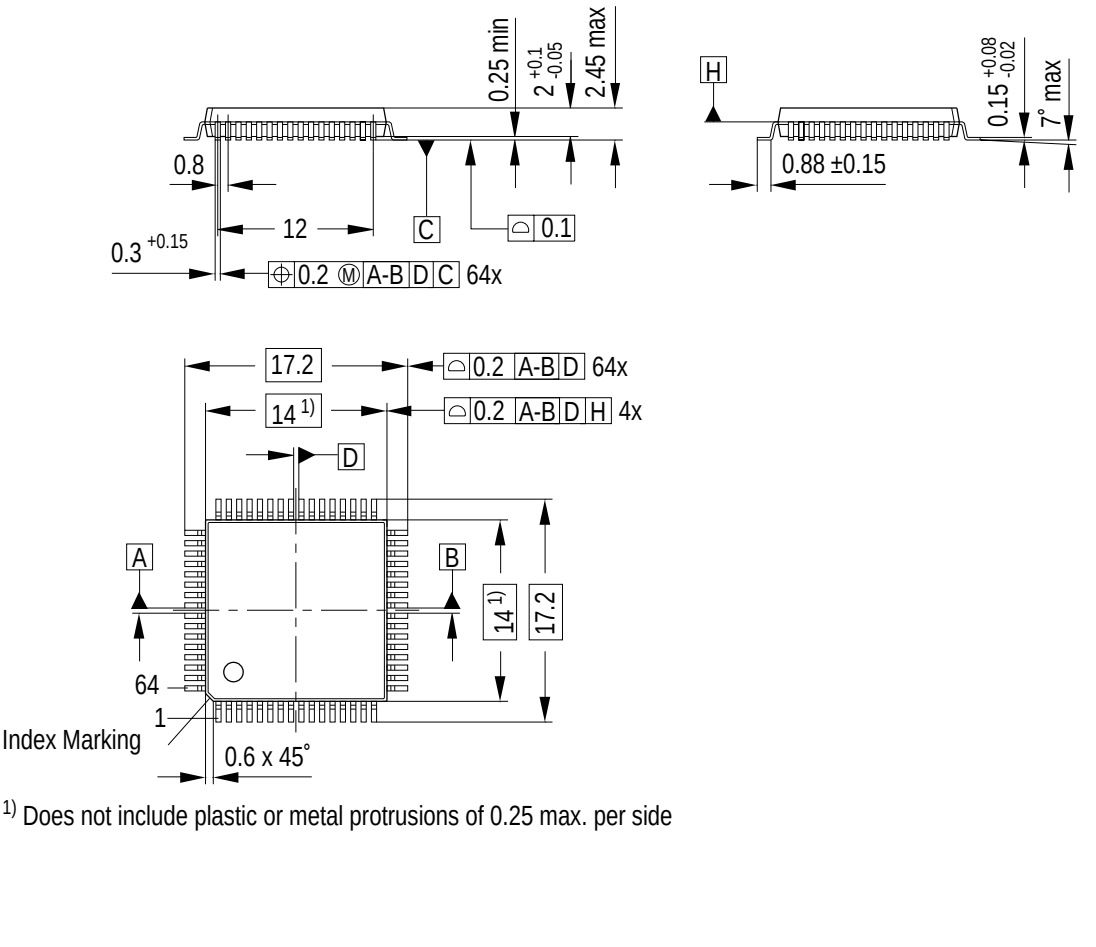


Figure 20

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm