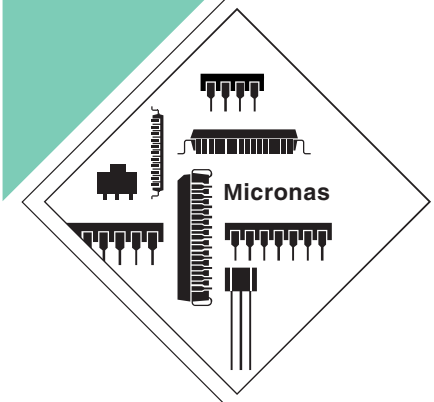


APPLICATION NOTE KITS/BOARDS

SDA 6000
M2 Evaluation Board

Edition Oct. 22, 2001
6251-557-1AK

MICRONAS

SDA 6000, M2 EVALUATION BOARD

Revision History: **Current Version: V2.0 May 2001**

Previous Version: V1.2

Page	Subjects (major changes since last revision)
	Complete update of all chapters due to the requirements of the new version of the M2 Evaluation Board (B001-V006)

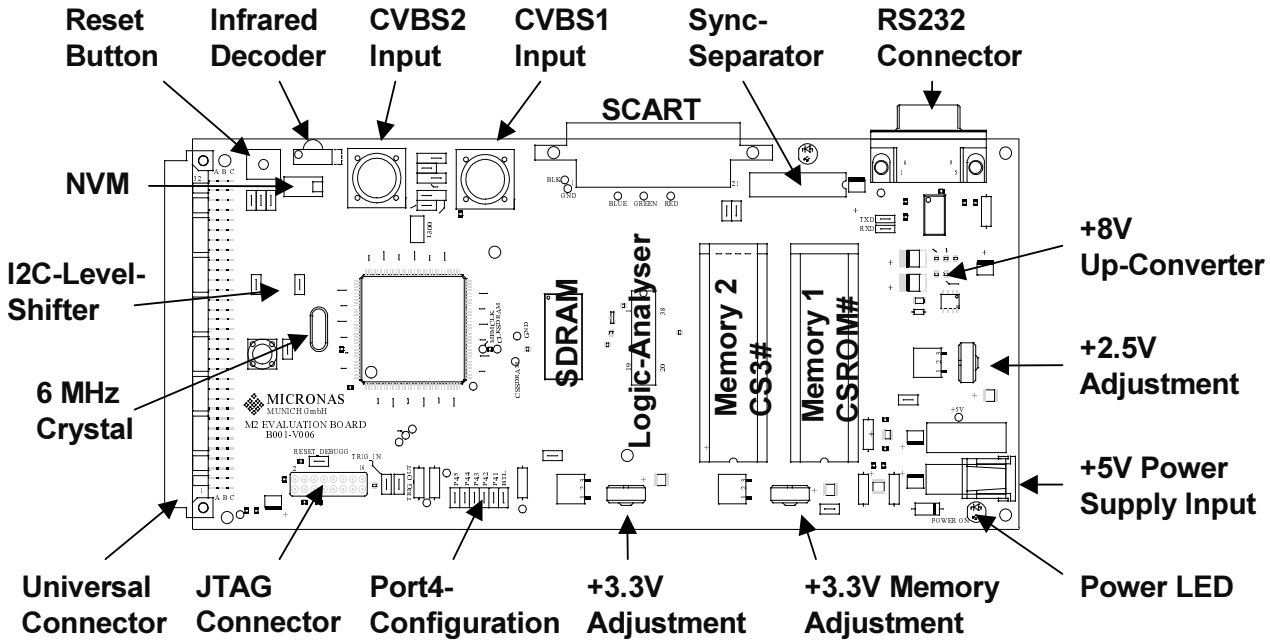
For questions on technology, delivery and prices please contact the Micronas Offices in Germany or the Micronas GmbH Companies and Representatives worldwide:
see our webpage at http://www.micronas.com

1 Introduction

The M2 Evaluation Board is a versatile tool, providing you quick access to the capabilities of M2's powerful architecture.

To enable applications to be developed quickly and easily the M2 Evaluation Board is fitted with a variety of peripherals for connections to the outside world. There is also an interface for the M2's On-Chip-Debugging-Features (OCDS), which is supported by the development tool chain of our tool partners.

This document is related to the M2 Evaluation Board version 6 or higher. The version number of the M2 Evaluation Board can clearly be seen on the board by the marking B001-**V006**.



2 Features of the M2 Evaluation Board

- CPU: - M2 in MQFP100 package soldered on PCB
- MEMORY: - SDRAM 8 MByte connected to CSSDRAM#
  - Memory Module Socket 1 connected to CSROM#
  - Memory Module Socket 2 connected to CS3#
  - NV-Memory (I2C controlled)
- CLOCK: - 6MHz crystal
- INTERFACES: - Serial Interface for RS232 (RS232 Connector, DB9)
  - Emulator Interface for OCDS (JTAG Connector)
  - TV Interface for Display (SCART Connector, SCART)
  - CVBS Input for Full Data Service Slicer (CVBS1 Connector, BNC)
  - CVBS Input for WSS Slicer (CVBS2 Connector, BNC)
  - Multifunctional Interface for extension (Universal Connector, 96pin)
  - Oscillator Interface for timing analyses (Oscillator Connector, SMB)
  - Memory Interface for logic analyses (LA Connector, MICTOR)
- POWER: - Only one external stabilized +5V power supply unit required
  - On-board generated +3.3V (adj.), +2.5V (adj.) and +8.0V
- MODULES: - Infrared Preamplifier for IR remote control
  - I2C-Level-Shifter for 5V and 3.3V I2C-Bus
  - Sync-Separator for generating H- and V-sync from an CVBS signal
- DIMENSIONS: - 110mm x 225mm, Height: 22mm

3 Differences to previous Versions

Version 6 of the M2 Evaluation Board differs in the following items from the previous version 4 which is not longer available:

Version 6 has no on-board soldered Flash device connected to CS3# (chip select 3) of the M2. Instead of the flash device version 6 provides an additional memory module socket. Version 6 has now 2 memory module sockets for flexible changing between EPROM, Flash module or SRAM module with up to 4 MByte memory size. The previous version had only one memory module socket.

Version 6 has no on-board "Wiggler" circuit. As it was not used the "Wiggler" circuit has been removed0. OCDS Debugger from pls and Lauterbach are still supported by the on-board JTAG connector.

The sync separator has been changed in version 6 because the previously used device is no longer available in the market. The new sync separator device needs +8V power supply instead of +12V.

Version 6 needs only one stabilized external +5V power supply unit instead of two external power supplies with +5V and +12V. The +8V power for the sync separator is generated on-board out of the +5V.

The possibility to take the ground reference for the CVBS1 signal from the source has been removed to reduce the number of jumpers.

The board of version 6 becomes 2cm shorter.

4 Getting Started

4.1 Jumper Settings

The following table gives an overview on all necessary jumpers of the M2 Evaluation Board for starting a demonstration software. The setting of all other jumpers not mentioned on this table are not important (don't care) for starting the demonstration software on the M2 Evaluation Board. The settings recommended in the last column 'SETTING' is used for running the demonstration software with a television connected via the SCART connector.

JUMPER	DESCRIPTION	SETTING
J300	Selection of CVBS source for the slicer of the M2: A: CVBS1 (BNC) or B: SCART	B
J301 J303	Selection of CVBS source for the sync separator	J301: open J303: B
J305 J306	Group Delay Filter for CVBS signal enable/disable	J305: A J306: open
J200	Connects / disconnects the +2.5V power to the board	set
J201	Connects / disconnects the +3.3V port power to the board	set
J202	Connects / disconnects the +3.3V memory power to the board	set
J307 (VSYCN)	Connects / disconnects the VSYNC signal to the M2	set
J308 (HSYNC)	Connects / disconnects the HSYNC signal to the M2	set
J402-406	Port 4 Configuration	J404: set others: open
J401 (BTL)	Bootstrap Loader Mode	open

4.2 How to start the Demonstration?

After setting the jumpers to the right position proceed through the following instructions to start the demonstration software:

- connect an antenna to a TV set and tune the TV (video picture on screen)
- connect the TV set via a SCART cable to the M2 Evaluation Board
- connect a stable +5V power supply unit (600mA) to the power supply input ('+5VIN') of the M2 Evaluation Board
- press the reset button on the M2 Evaluation Board
- if the M2 does not synchronize his OSD to the video, switch the TV set to AV mode.

5 Modules

5.1 Power Supply

The M2 Evaluation Board requires an external power supply unit, which should provide a stabilized +5V voltage (min. 600mA). The on-board voltage regulators generate the required other supply voltages +2.5V, +3.3V and +8V.

The following table gives an overview over all voltages used on the M2 Evaluation Board.

Voltage	Supplied Modules	Remark
2.5VCOR 2.5VANA	• Core of M2 (pin 21, 87) • Analogue part of M2 (pin 111, 116, 119, 123)	Voltage is generated out of 5.0V by on-board regulator and adjustable by potentiometer marked with "**ADJUST +2,5V**"
3.3VMEM	• Memory supply pins of M2 (pin 32, 42, 53, 61, 69) • Memory devices (Memory Socket 1/2, SDRAM)	Voltage is generated out of 5.0V by on-board regulator and adjustable by potentiometer marked with "**ADJUST +3,3V$_{MEM}$**"
3.3V	• Ports of M2 (pin 14,85,106) • I2C-Level-Shifter • RS232-Interface • JTAG-Interface • NVM • RGB-Amplifier • Sync-Separator	Voltage is generated out of 5.0V by on-board regulator and adjustable by potentiometer marked with "**ADJUST +3,3V**"
5.0V	• IR-Decoder • I2C-Level-Shifter • Universal –Connector	Must be applied externally with accuracy of 10%. Use jack marked with "**+5VIN**"
8.0V	• Sync-Separator	Voltage is generated out of 5.0V by an on-board up-converter

5.2 Sync Separator

The Sync Separator of the M2 Evaluation Board separates the H- and V-Sync signal from a CVBS signal. This Sync Separator is build with a TDA4691 and a few external

components. The CVBS input signal may be provided by different sources, with the selection being made by jumpers (see “Distribution of CVBS- and SYNC-Signals”). The generated H- and V-Sync signal are linked to the M2 (pin 102 and 103), the Universal-Connector (A18 and C18) and SCART socket. Jumpers allow to disconnect the connection between the Sync Separator and the M2. The jumpers can be open to avoid injection into M2 related analog circuits.

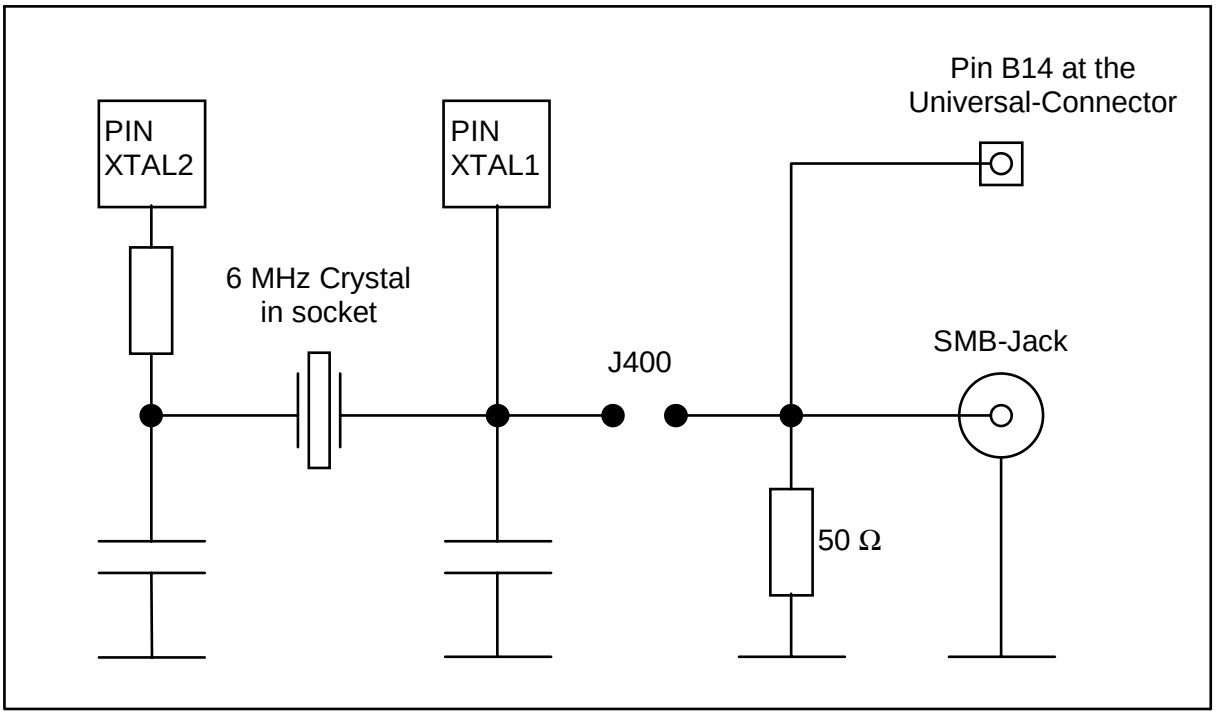
Sync Distribution	**J308 (HSYNC)**	**J307 (VSYNC)**
H- and V-Sync connected to M2 and Universal Connector	set	set
No H- and V-Sync available at M2 and Universal Connector	open	open

5.3 Clock Generation

There are three different possibilities to provide a 6 MHz clock for the M2.

Clock Generation	**Crystal Socket**	**J400**
internal oscillator of M2	6 MHz Crystal	open
external 6 MHz signal applied to universal connector B14 (source impedance = 50 Ω)	open	set
external 6 MHz signal applied to SMB-Jack (source impedance = 50 Ω)	open	set

The figure below shows the external circuit at the oscillator pins XTAL1 and XTAL2 of the M2.



5.4 Infrared Receiver

The M2 Evaluation Board provides an IR-Preamplifier with a carrier frequency of 33 kHz or 36 kHz. The demodulated IR signal is available at Port 3.2 (CAPIN) of the M2. This signal can be disconnected by opening the respective jumper:

Infrared Receiver	**J100 (IR)**
IR-Receiver connected to M2 (Pin P3.2) and Universal Connector (Pin A32)	set
IR-Receiver signal not available at M2 and Universal Connector	open

5.5 Reset

The M2 Evaluation Board provides three possibilities to generate a hardware reset signal for the M2:

- by pressing the reset button
- by forcing pin B30 of the Universal Connector to low
- by using an OSDC Debugging System at the JTAG Connector (J110 must be shorted)

5.6 Board-to-Board Interfaces (external connectors)

The M2 Evaluation Board provides many interfaces to allow software development on the M2 and to connect other applications to the M2 Evaluation Board. The table below gives you an overview over all external connectors:

Name of Connector	Function	Signals of M2
Universal Connector	General purpose connector for other application boards	nearly all signals of M2, except pins of the external bus interface (EBI)
RS232 Connector	Interface for ROM Monitor Debugger, In-System Flash-Programming via Bootstrap-Loader	P3.11/RxD0, P3.10/TxD0 converted by 3.3V ↔ 10V Level Shifter
JTAG Connector	Interface for OCDS (On-Chip-Debug-Support)	TCK, TMS,TDI, TDO, P6.0, P6.1, RST#
SCART Connector	SCART-Connection to TV-Set	buffered RGB- and Blank-Signal; CVBS1A
CVBS1 Connector	CVBS-Test-Signal Input for Full-Data-Service-Slicer	CVBS1A
CVBS2 Connector	CVBS-Test-Signal Input for WSS-Slicer	CVBS2
Oscillator Connector	Input for external CPU clock	XTAL1 pin
Logic Analyzer Connector	Monitoring of Memory Interface	all memory interface related signals (all EBI pins)

5.6.1 Universal Connector

The Universal Connector is a 96-pin connector comprising nearly all signals of the M2 except following signals: XTAL2, CVBS1A, CVBS1B, CVBS2, A0-A15, D0-D15, RD#, WR#, LDQM, UDQM, MEMCLK, CLKEN, CSROM#, CSSDRAM#. The table below shows the pinning of the Universal Connector.

	C	**B**	**A**	
PIN 1	P4.2/A18	P4.1/A17	P4.0/A16	**PIN 1**
PIN 2	P4.4/A20	P4.3/A19	P4.5/CS3#	**PIN 2**
PIN 3	P2.13	P2.14	P2.15	**PIN 3**
PIN 4	P2.10	P2.11	P2.12	**PIN 4**
PIN 5	TDO	P2.8	P2.9	**PIN 5**
PIN 6	TMS	TCK	TDI	**PIN 6**
PIN 7	-	TMODE	-	**PIN 7**
PIN 8	GND	GND	GND	**PIN 8**
PIN 9	P5.3	P5.0	P5.2	**PIN 9**
PIN 10	-	-	P5.1	**PIN 10**
PIN 11	GND	GND	GND	**PIN 11**
PIN 12	GOUT	ROUT	BOUT	**PIN 12**
PIN 13	GND	GND	GND	**PIN 13**
PIN 14	-	XTAL1	-	**PIN 14**
PIN 15	GND	GND	GND	**PIN 15**
PIN 16	BLANK	-	COR	**PIN 16**
PIN 17	GND	GND	GND	**PIN 17**
PIN 18	VSYNC	-	HSYNC	**PIN 18**
PIN 19	GND	GND	GND	**PIN 19**
PIN 20	P6.5	P6.4	P6.6	**PIN 20**
PIN 21	P6.3	P6.2	SCL_{5V}^{*}	**PIN 21**

PIN 22	P6.1	P6.0	SDA_{5V}*	**PIN 22**
PIN 23	-	P3.6	P3.5	**PIN 23**
PIN 24	-	-	-	**PIN 24**
PIN 25	P3.10/TxD0	P3.11/RxD0	P3.9	**PIN 25**
PIN 26	P3.15	P5.15	P3.13	**PIN 26**
PIN 27	P3.12	P3.7	P3.8	**PIN 27**
PIN 28	P3.3	P3.4	P5.14	**PIN 28**
PIN 29	P3.1/SDA0	P3.0/SCL0	P3.2	**PIN 29**
PIN 30	-	RST#	-	**PIN 30**
PIN 31	$+3.3V_{UNI}$	$+3.3V_{UNI}$	$+3.3V_{UNI}$	**PIN 31**
PIN 32	+5V	+5V	+5V	**PIN 32**
	C	**B**	**A**	

* pin is not connected directly to the M2

5.6.2 RS232 Connector

The RS232-Connector is used for directly connecting the serial port of a PC. A 1:1 cable with a female D-SUB-9 and male D-SUB-9 connector is needed. The maximum baud rate supported by the RS232 driver device MAX3237 is 1 Mbps (= 1 MBaud).

If the port pin P3.10 (TxD0) and/or P3.11 (RxD0) of the M2 are used for I/O purposes, jumper J108 and J109 can disconnect the on-board RS232 driver IC.

RS232 Driver IC	**J108 (RXD)**	**J109 (TXD)**
RS232 driver IC connected to M2 (enable RS232 Interface)	set	set
RS232 driver signals not available at M2	open	open

5.6.3 JTAG Connector

The M2 Evaluation Boards provides the possibility to access the OCDS-Interface of the M2 via the JTAG Connector. The JTAG Connector (16-pin) is used for connecting an external OSDS hardware provided by our tool-partners e.g. pls, Lauterbach. Jumper J110 must be shorted to connect the reset function of the debugger with the reset pin of the M2.

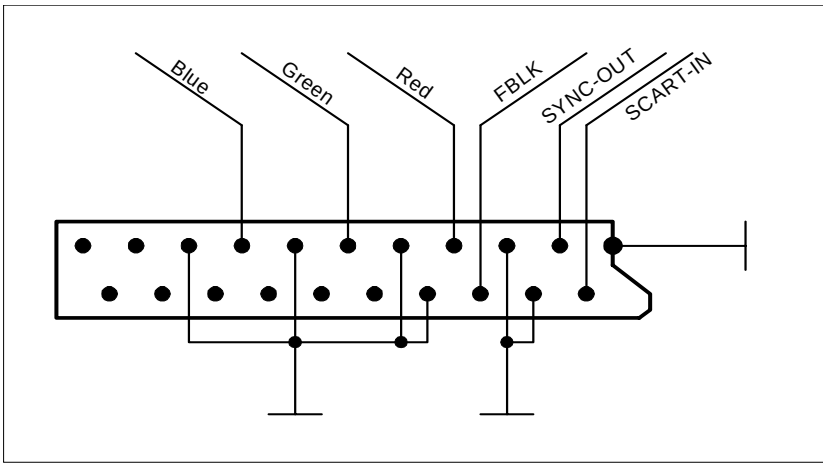
PINNING of JTAG Connector

TMS	1	2	VCC
TDO	3	4	GND
GND	5	6	GND
TDI	7	8	RESET#
NC	9	10	Brk_OUT#
TCLK	11	12	GND
Brk_IN#	13	14	NC
NC	15	16	key (no pin)

5.6.4 SCART Connector

Available signals at the SCART Connector:

- buffered RGB signal
- buffered Blanking signal
- CVBS-Input (SCART-IN)
- H/V-Sync-Signal generated by the Sync Separator (SYNC-OUT)



5.6.5 CVBS1 Connector

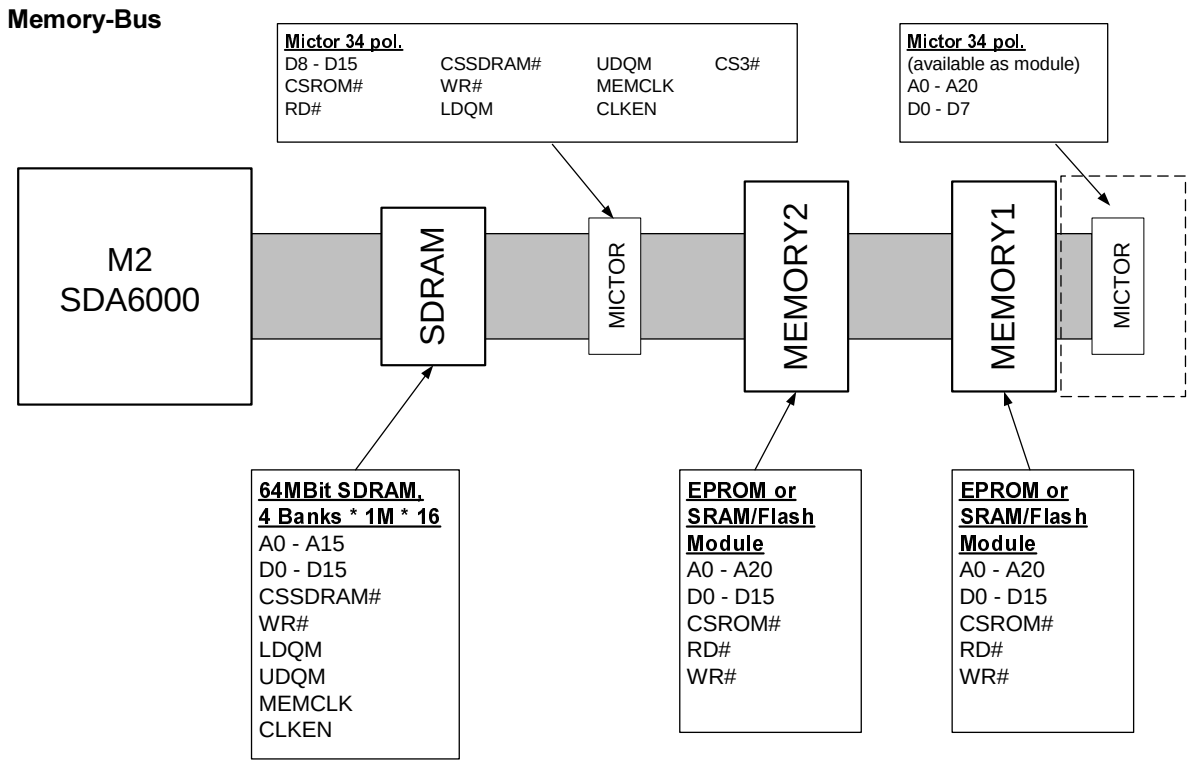
External CVBS-signal input for test purposes of the Full-Data-Service-Slicer of the M2 (see also chapter “Distribution of CVBS- and SYNC-Signals”).

5.6.6 CVBS2 Connector

External CVBS-signal input for test purposes of the WSS-Slicer of the M2 (see chapter “Distribution of CVBS- and SYNC-Signals”).

5.6.7 Logic Analyzer Interface

The whole External Bus Interface (EBI) of the M2 can be analyzed via two Mictor jacks (Mictor - Trademark of AMD). One Mictor jack is on the board, the other one is located on a separate PCB which can be plugged into the one of the memory sockets. The I/O port of the M2 and other signals are available at the Universal Connector. (See also chapter “Modules / Memory Interface”)



5.7 Memory Interface

The M2 Evaluation Board provides two memory sockets for EPROMs or memory modules with SRAM or Flash devices. A SRAM module is needed if you want to develop software on the M2 Evaluation Board. An EPROM or Flash module is needed to start programs directly after power-up of the board. The board has also an on-board 64 Mbit SDRAM.

Micronas provides SRAM modules with a maximum size of 2 Mbyte and Flash modules with a maximum size of 2 Mbyte. The EPROM type that fits to the M2 Evaluation Board is M27V160 from ST Microelectronics.

The external bus interface of the M2 is able to drive maximum three memory devices, because of the capacitive bus load. The maximum size of SRAM devices in the market is 1 MByte (8 Mbit). SRAM memory modules with more than 2 MByte can currently not be used. This is because of the limited number of memory devices which can be connected to the external memory bus of the M2 and the above mentioned market availability of large SRAM memory devices.

Type	Size	Device
SDRAM	64 Mbit (4 x 1 M x 16 bit)	Infineon HYB39S64160BT-8
EPROM	16 Mbit (1M x 16 bit)	ST Microelectronics M27V160
16M SRAM Module	2 x 8 Mbit	Samsung 2 x K6F8016V3M
16M Flash Module	16 Mbit	AMD AM29LV160DT-90

Programming of the Flash memory can by done in-system via the RS232 Interface. The tool FLASHit from our tool partner hse is such a tool for in-system programming of flash devices. For details please contact hse (www.hse-electronic.de).

5.8 CVBS Group Delay Filter

To test the slicer performance of the M2 a CVBS group delay filter has to be used in order to improve the slicer performance with CVBS signal with negative group delay of about 170ns. This group delay compensation filter must be used for design steps A22 and A23 only. To get an optimal slicer performance, the CVBS group delay filter must be enabled and the CVBS source must deliver an increased CVBS amplitude. To adjust the correct amplitude please refer to the "M2 Design Guide". The adjustment of the CVBS amplitude must be done externally (CVBS source).

Group Delay Filter	J305	J306
filter is enabled	B	set
filter is disabled	A	open

5.9 Port 4 Configuration

Most of the programmable features of the M2 are either selected during the initialization phase or repeatedly during program execution. There are however some features that must be selected earlier. These features are used for the first access of the program execution in the external RAM. These selections are made during a reset via some pins of Port 4, which are read at the end of the internal reset sequence. During reset internal pull-up devices are active on Port 4 lines, so their input level is high, if the respective pin is left open, or is low, if the respective pin is connected to an on-board pull-down device.

The M2 Evaluation Board supports the Port 4 configuration by on-board pull-down resistors, which can be connected to the respective port pins by jumpers. If the jumper is set the external pull-down resistor is active, otherwise the Port 4 is pulled high by the on-chip pull-up devices an additional on-board 220 kOhm resistors.

PORT4 Configuration - Bootstrap Loader Mode	**J401 (BTL)**
M2 in normal operation mode, external memory	open
M2 in Bootstrap Loader Mode	short

PORT4 Configuration - CS3# for 2nd Memory	**J406 (P4.1)**
P4.5 operates as output	open
P4.5 operates as CS3#	set

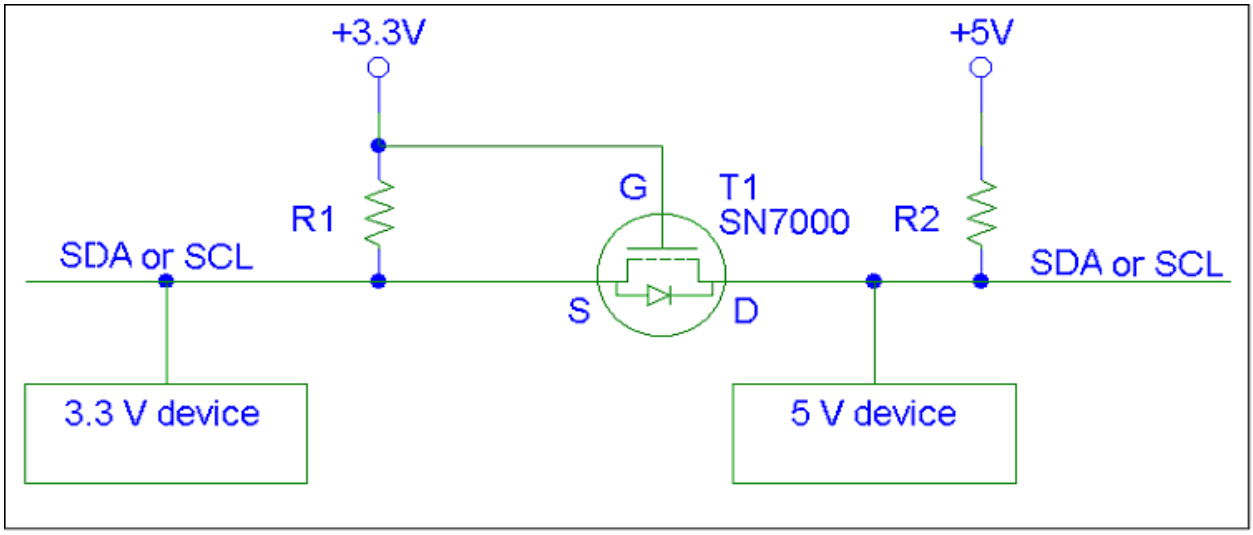
PORT4 Configuration - number of address lines	**J402 (P4.5)**	**J403 (P4.4)**	**J404 (P4.3)**
P4.0-4 operate as A16-A20	open	open	open
P4.0-3 operate as A16-A19, P4.4 operates as output	open	open	set
P4.0-2 operate as A16-A18, P4.3-4 operate as output	open	set	open
P4.0-1 operate as A16-A17, P4.2-4 operate as output	open	set	set
P4.0 operate as A16, P4.1-4 operate as output	set	open	open

5.10 I2C-Bus-Level-Shifter

The M2 is based on a modern technology with I/O pins capable to handle 3.3V. Devices based on older technologies still require 5.0V level signals. To work with both types of devices connected to the I^2C-Bus an interface is required, which can translate the voltage level in both directions.

The solution consists of an N-channel MOSFET that interconnects the two different supply voltages and logic level devices in a bi-directional way. The circuit can be found in the figure below. To avoid a latch-up of devices connected to the 5V section, the 5V power supply should be powered on simultaneously with the 3.3V power supply.

5V↔3.3V Level-Shifter-Circuit for I^2C Bus



6 Distribution of CVBS and SYNC Signals

6.1 CVBS1, CVBS2

The M2 has two slicers. One is a full data service slicer with a differential input (pin CVBS1A, CVBS1B), the other one is a WSS-only slicer connected to the CVBS2 input pin.

The CVBS1 input of the M2 can either be connected to the CVBS1 Connector or to the CVBS signal provided via the SCART Connector. The jumper J300 is used to select the source of the CVBS1 signal. The CVBS2 input of the M2 is always connected to the CVBS2 Connector.

CVBS1 Source Selection	**J300 (CVBS1A)**
Source is the CVBS1-Connector (BNC plug)	A
Source is the SCART-Connector (SCIN signal)	B

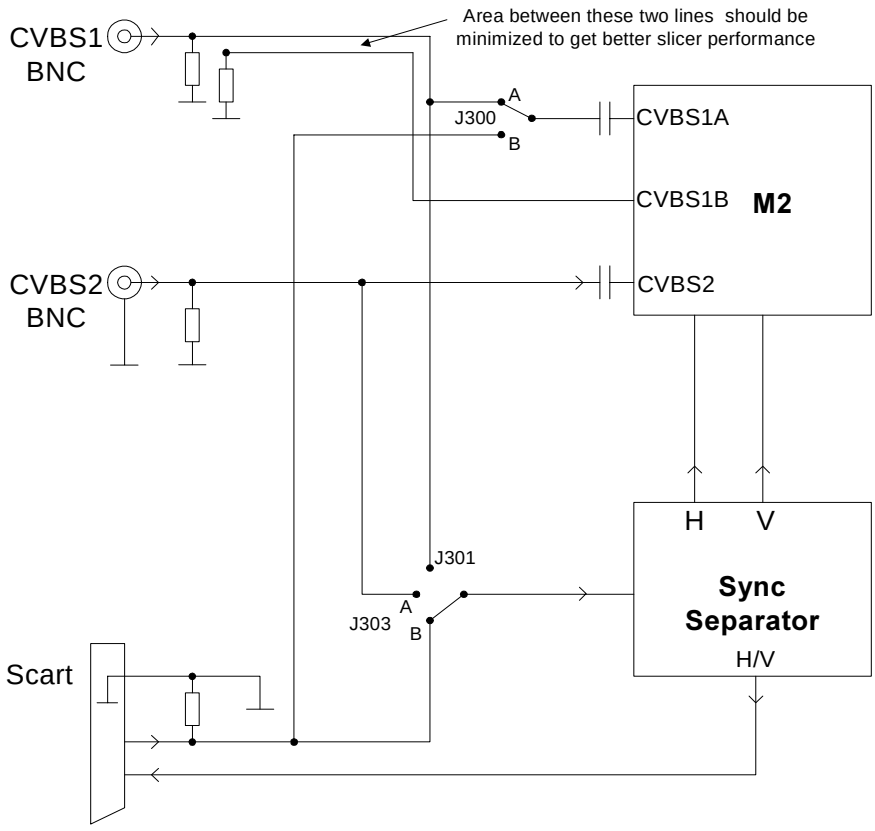
6.2 H-Sync and V-Sync

The synchronization signals (H- and V-Sync) for synchronizing the display generator of the M2 to a connected TV set are produced by the sync separator. The sync separator can produce the sync signals from a CVBS signal from one of the three different sources:

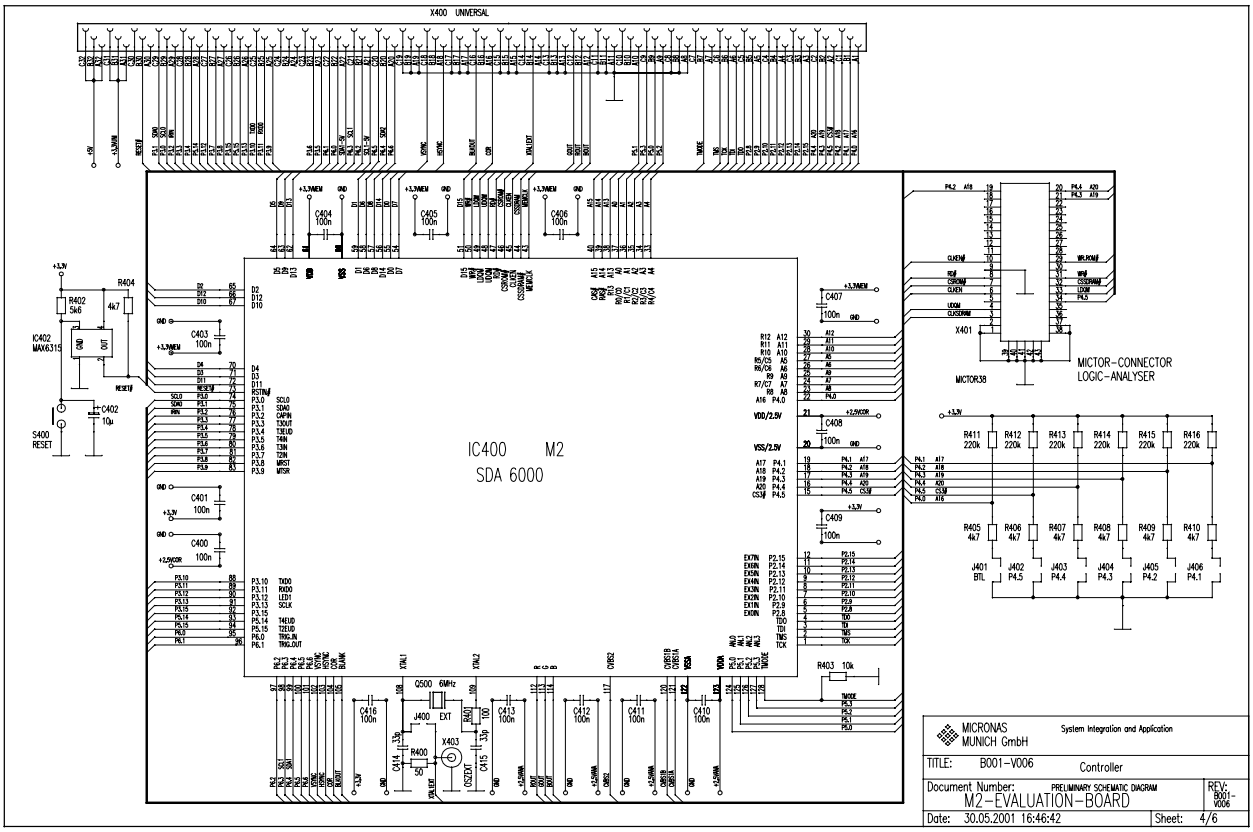
- SCART-Connector (SCART-IN Signal),
- CVBS1-Connector (BNC),CVBS2-Connector (BNC)

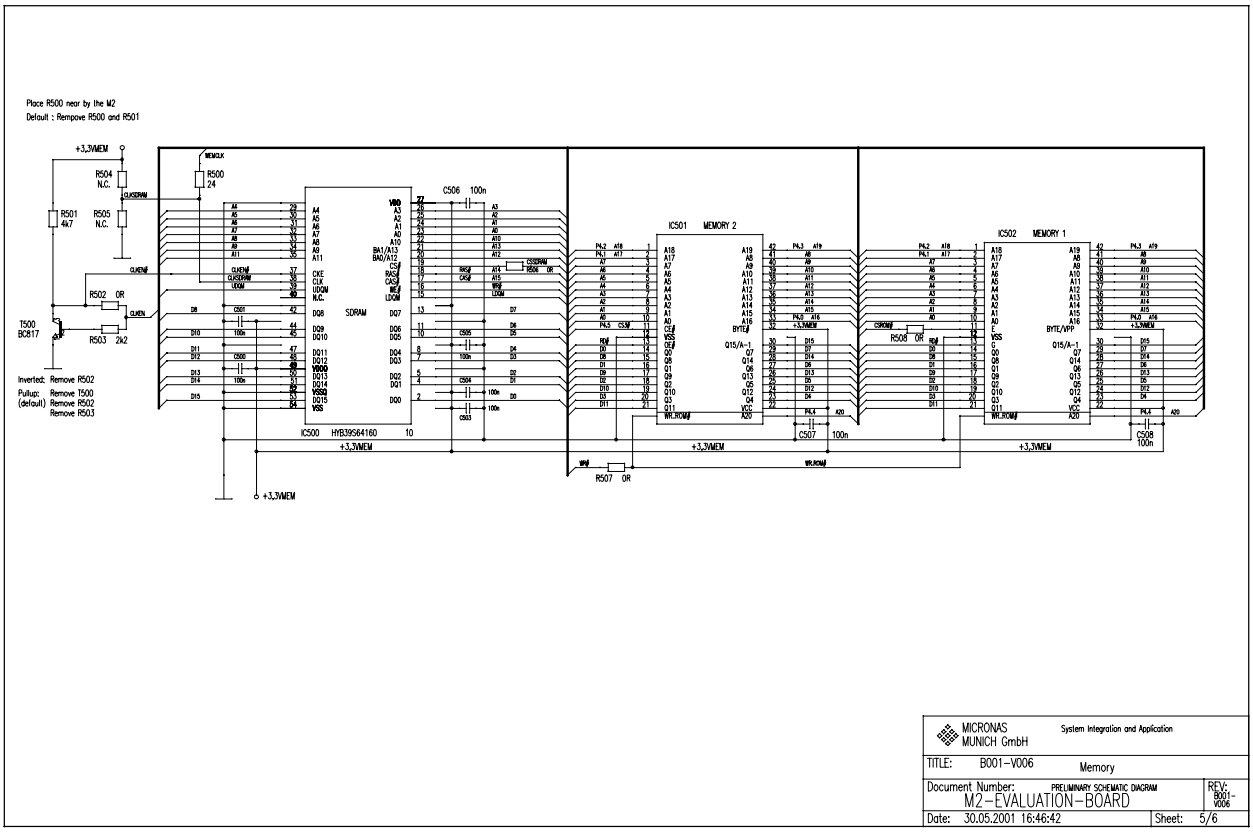
Source Selection for SYNC Separator	**J301**	**J303**
SCART-Connector	open	B
CVBS1-Connector	short	open
CVBS2-Connector	open	A

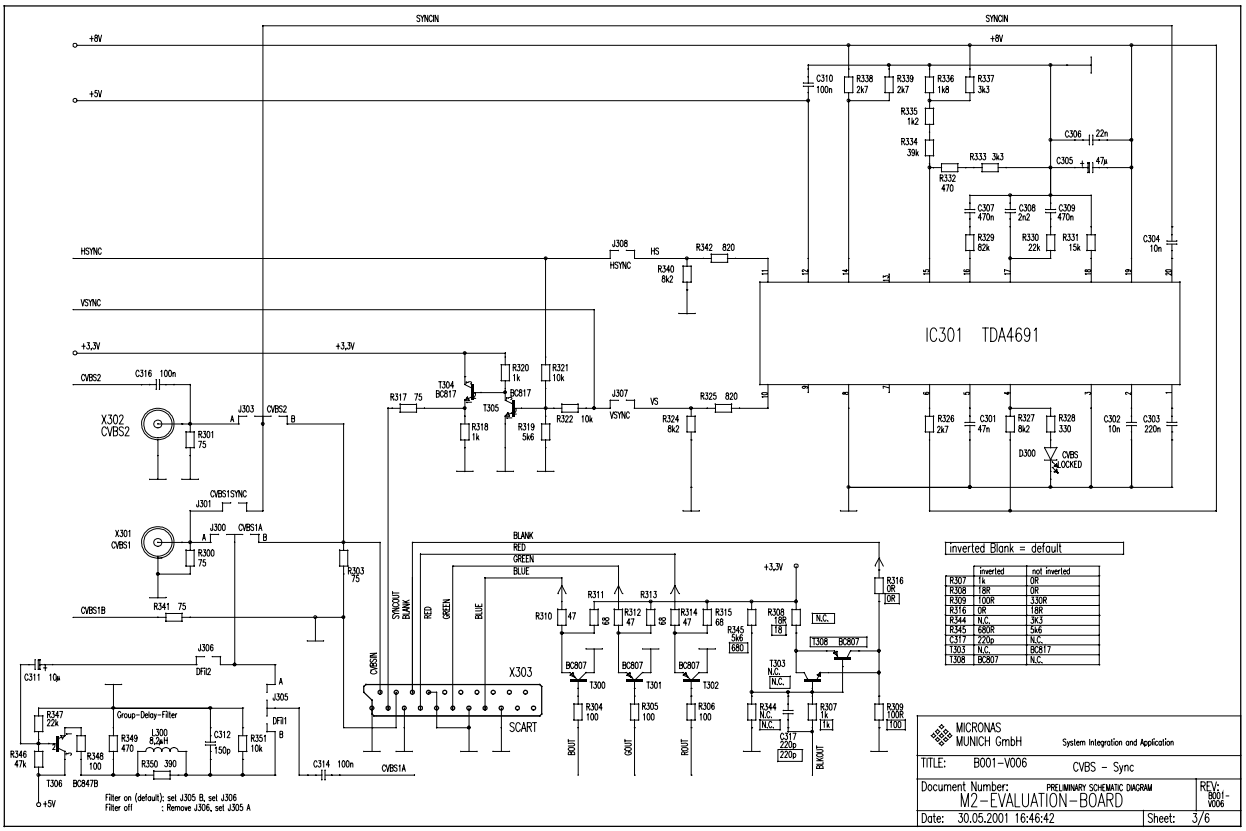
The figure below shows the distribution of the CVBS and SYNC signals on the board.



CVBS Signal and SYNC Signal Distribution


X400 UNIVERSAL
IC400 M2
SDA 6000
IC402
MAX6315
S400
RESET
X401
MICTOR38
MICTOR-CONNECTOR
LOGIC-ANALYSER
Q500 6MHz
EXT
X403
MICRONAS
MUNICH GmbH
System Integration and Application
TITLE: B001-V006
Controller
Document Number:
M2-EVALUATION-BOARD
PRELIMINARY SCHEMATIC DIAGRAM
REV: B001-V006
Date: 30.05.2001 16:46:42
Sheet: 4/6


Place R500 near by the M2
Default : Rempove R500 and R501
IC500 HYB39S64160
IC501 MEMORY 2
IC502 MEMORY 1
Inverted: Remove R502
Pullup: Remove R502
(default) Remove R503
MICRONAS
MUNICH GmbH
System Integration and Application
TITLE: B001-V006
Memory
Document Number:
M2-EVALUATION-BOARD
PRELIMINARY SCHEMATIC DIAGRAM
REV: B001-V006
Date: 30.05.2001 16:46:42
Sheet: 5/6


IC301 TDA4691
X302 CVBS2
X301 CVBS1
X303 SCART
inverted Blank = default
MICRONAS MUNICH GmbH
System Integration and Application
TITLE: B001-V006 CVBS - Sync
Document Number: M2-EVALUATION-BOARD
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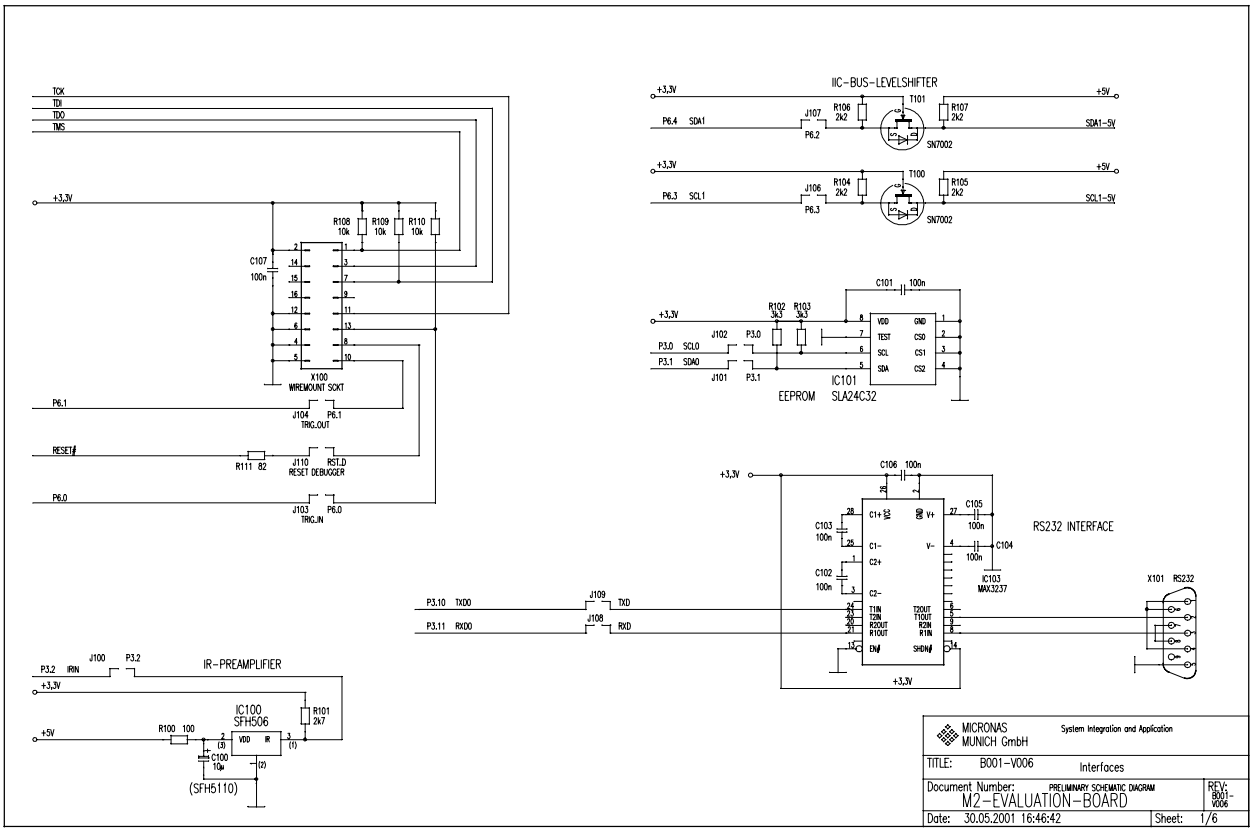
REV: B001-V006
Date: 30.05.2001 16:46:42
Sheet: 3/6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RS232 INTERFACE
IR-PREAMPLIFIER
IC101 SLA24C32
IC103 MAX3237
IC100 SFH506
X100 WIREMOUNT SOKT
MICRONAS MUNICH GmbH
System Integration and Application
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Document Number: M2-EVALUATION-BOARD
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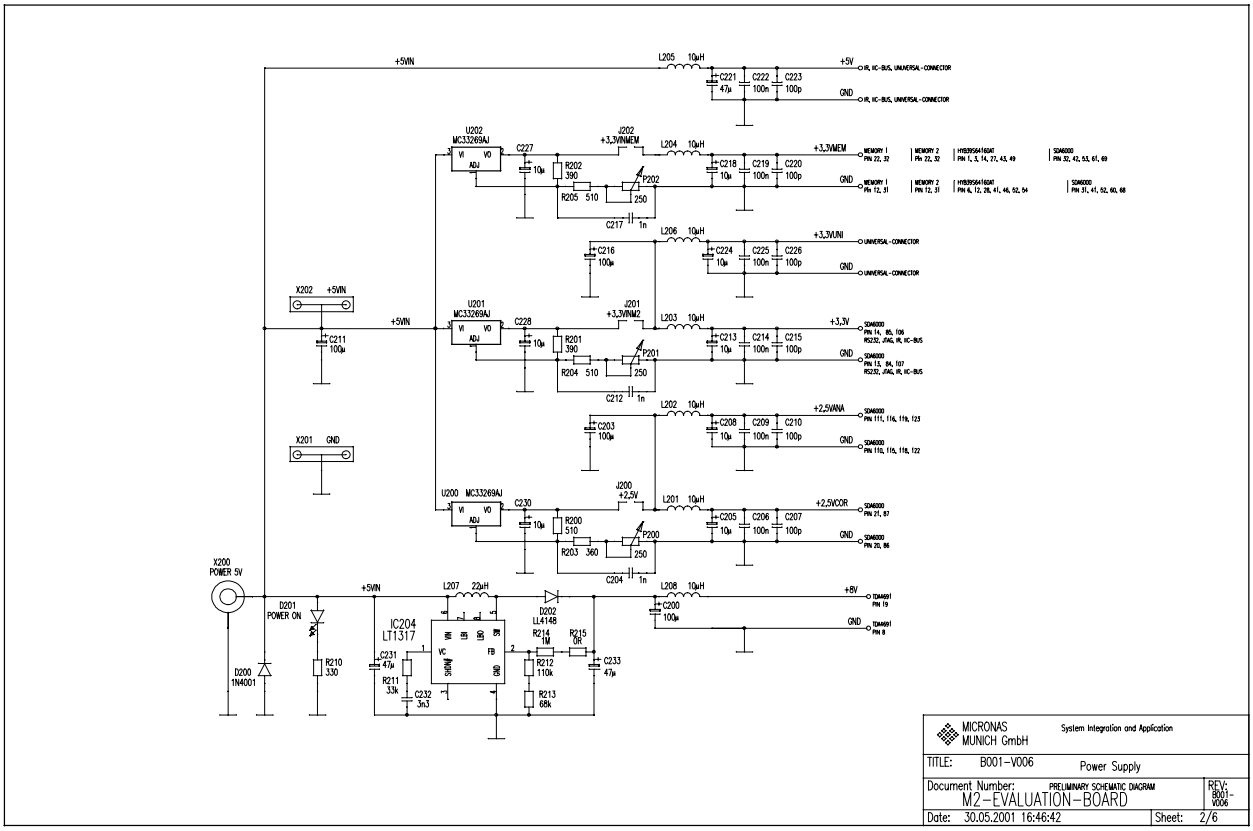
REV: B001-V006
Date: 30.05.2001 16:46:42
Sheet: 1/6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+5V
C221 47µ
C222 100n
C223 100p
GND
U202 MC33269AJ
J202 +3.3VMEM
C227 10µ
R202 390
R205 510
P202 250
C217 1n
L204 10µH
+3.3VMEM
C218 10µ
C219 100n
C220 100p
L206 10µH
+3.3VUNI
C216 100µ
C224 10µ
C225 100n
C226 100p
X202 +5VIN
C211 100µ
U201 MC33269AJ
J201 +3.3VMA2
C228 10µ
R201 390
R204 510
P201 250
C212 1n
L203 10µH
+3.3V
C213 10µ
C214 100n
C215 100p
L202 10µH
+2.5VMA
C203 100µ
C208 10µ
C209 100n
C210 100p
X201 GND
U200 MC33269AJ
J200 +2.5V
C230 10µ
R200 510
R203 360
P200 250
C204 1n
L201 10µH
+2.5VCOR
C205 10µ
C206 100n
C207 100p
X200 POWER 5V
D201 POWER ON
D200 1N4001
R210 330
IC204 LT1317
C231 47µ
R211 33k
C232 3n3
L207 22µH
D202 LL4148
R214 1M
R215 0R
R212 110k
R213 68k
C233 47µ
L208 10µH
+8V
C200 100µ
MICRONAS MUNICH GmbH
System Integration and Application
TITLE: B001-V006 Power Supply
Document Number: M2-EVALUATION-BOARD
PRELIMINARY SCHEMATIC DIAGRAM
REV: B001-V006
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Sheet: 2/6

2. Application Note History

1. Application Note Kits/Boards: “SDA 6000 M2 Evaluation Board”, Oct. 22, 2001, 6251-557-1AK. First release of the application note kits/boards.

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