SDA 5652-2X
VPS/PDCPro
VPS/PDC/OSD Device for VCRs

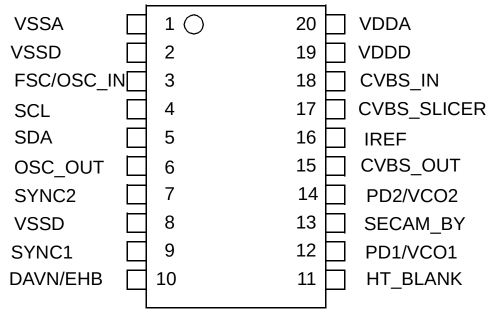
Edition Feb. 28, 2001
6251-559-1

MICRONAS

1. Features

General Features

- Low external component count
- No external crystal required
- Technology: CMOS
- P-DSO-20 -1 package



P - DSO 20 -1

PDC Features

- Reception of VPS data in line 16 of the vertical blanking interval
- Complete reception of BDSP packet 8/30/1 and packet 8/30/2
- Reception of the complete teletext header row
- 400KHz I²C-Bus interface
- Integrated OSD Module

OSD Features

- Display structure: 14 rows x 32 characters
  12 rows x 30 characters (27 characters in visible frame area)
- 128 ROM characters (12 Pixel * 18 Lines)
- Fringing
- Display start position programmable in horizontal and vertical direction
- Insertion of OSDs in the CVBS signal (Black and white)
- Colored full screen OSD mode
- Integrated Sync-Separator
- Integrated SECAM switch
- Analog CVBS Output
- 8 programmable background colors (via Look Up Table)
- Programmable flashing frequency (1.5Hz, 1 Hz or 0.5 Hz)
- Cursor
- Four size settings in vertical and horizontal directions

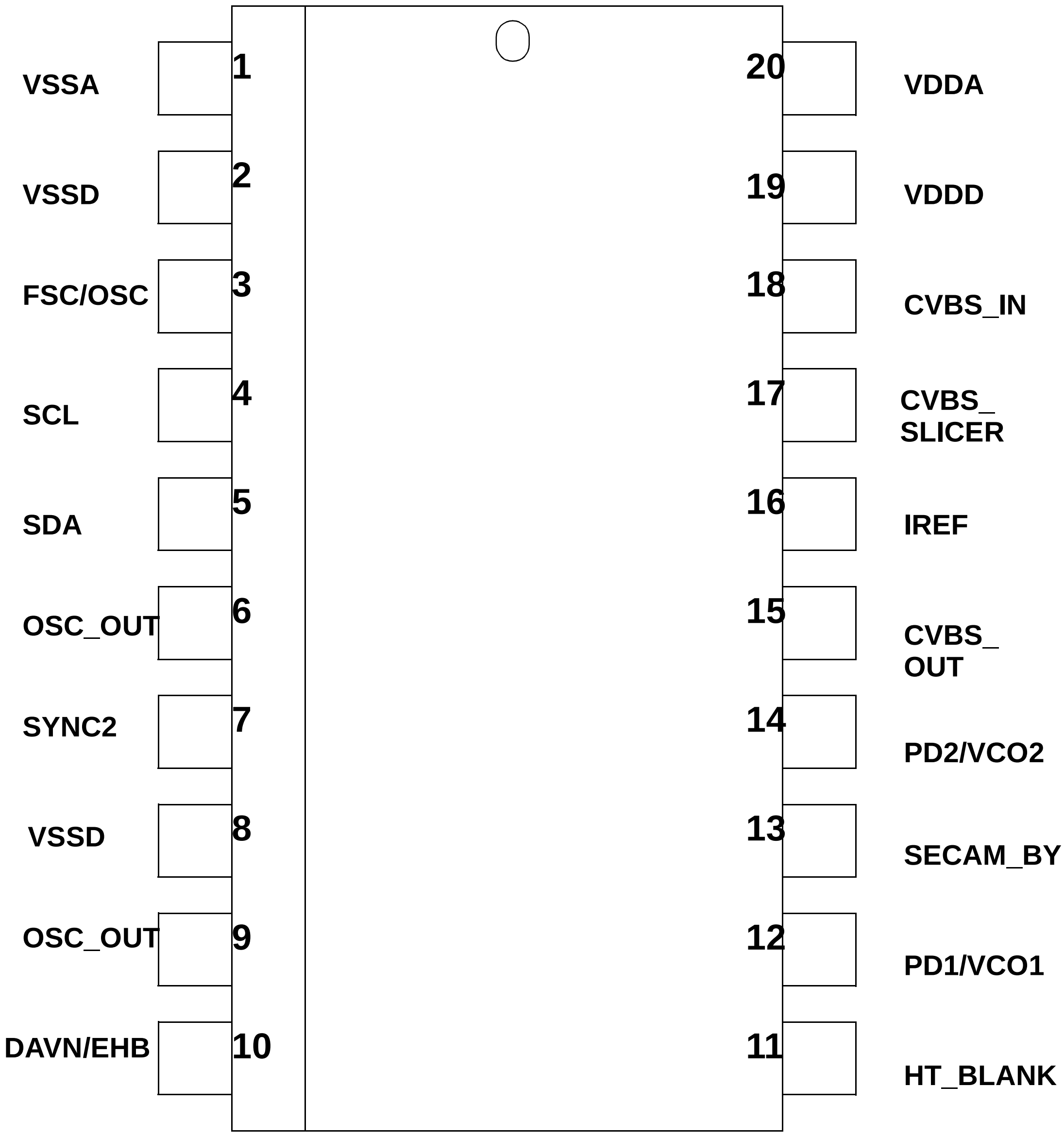
2. Order Information

Type	Package	Ordering Code
SDA 5652-2X	P - DSO - 20 - 1	

3. General Description

The PDC/OSD SDA 5652-2X decoder chip receives all VPS and 8/30 Format 1 and 2 data together with the teletext header information for easy identification of the broadcaster. In addition to the well known PDC/VPS decoder an OSD module with an YUV to CVBS encoder is integrated. The OSD can be synchronized to an CVBS signal or can generate a complete multistandard (PAL/NTSC, 50Hz/60Hz frame rate) CVBS signal with a full screen colored OSD.

4. Pin Configurations

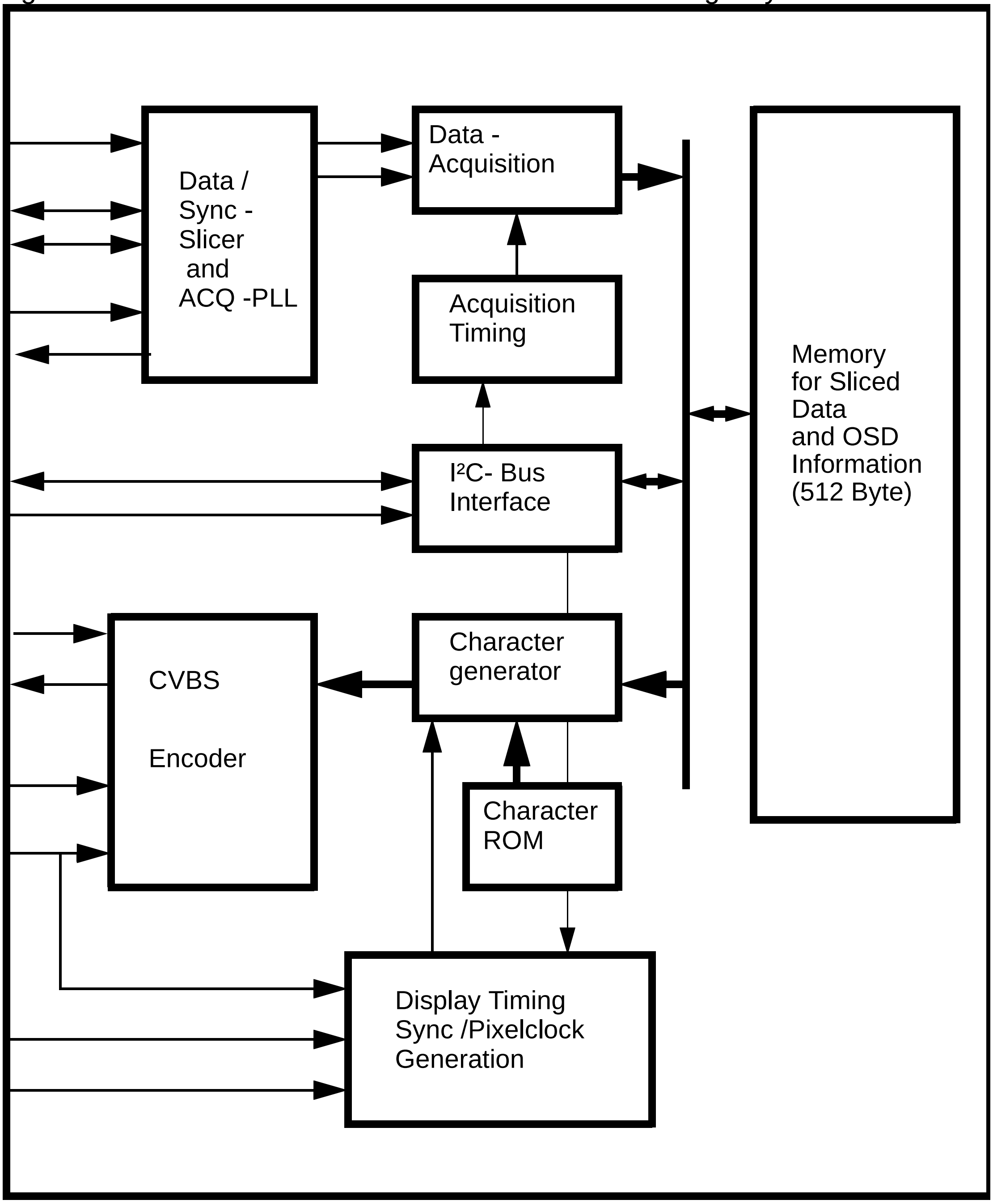


5. Pin Definitions and Functions

Pin. No. P-DSO-20	Symbol	Function
1	V_{SSA}	Analog ground (0 V)
2	V_{SSD}	Digital ground (0 V)
3	FSC/OSC_IN	Color Carrier Clock
4	SCL	Serial clock input of I^2C-Bus.
5	SDA	Serial data input of I^2C-Bus.
6	OSC_OUT	Optional oscillator for 2FSC
7	SYNC2	Vertical Sync/Vertical Composite Sync (Depending on I²C Bus definition it can be switched to either Input or Output. When it is switched as an input, analog or digital signals can be processed)
8	V_{SSD}	internal used; should be connected to GND
9	SYNC1	Vertical/Horizontal Sync (Depending on I²C Bus definition it can be switched to either digital input or output)
10	DAVN/EHB	output of the signals DAVN/EHB coming from the VPS/PDC-circuit.
11	HALFTONE_BLANK	Output-Pin for Halftone-Blanking. Goes to high for halftone-blanked video-areas, low for non-halftoneblanked areas
12	PD1/VCO1	Connector of the loop filter for the SYSPLL.
13	SECAM_BY	Input for Secam bypass.
14	PD2/VCO2	Connector of the loop filter for the DAPLL.
15	CVBS_OUT	Composite video signal output from the OSD path.
16	I_{REF}	Reference current input for the on-chip analog circuit.
17	CVBS _SLICER	Composite video signal input for the data slicer. The source of this signal must be the same as the source for signal at Pin 18.
18	CVBS_IN	Composite video signal input for the OSD path. The source of thsi signal must be the same as the source for signal at Pin 17.
19	V_{DDD}	Positive supply voltage for the digital circuits. (+ 5 V nom.).
20	V_{DDA}	Positive supply voltage for the analog circuits (+ 5 V nom.).

6.Block Diagram

The processing of the data in the SDA 5652-2X works in the following way:



7. Circuit Description

7.1 VPS/PDC Functions

Referring to the functional block diagram the composite video signal with negative going sync pulses is coupled to the pin CVBS through a capacitor which is used for clamping the bottom of the sync pulses to an internally fixed level. The signal is passed to the slicer, an analogue circuitry separating the sync and the data parts of the CVBS signal, thus yielding the digital composite sync signal VCS and a digital data signal for further processing by comparing those signals to internally generated slicing levels.

The output of this sync separator is forwarded to the acquisition clock generator and the acquisition timing block in which teletext / vps related data-valid-windows are generated.

The data slicer separates the data signal from the CVBS signal by comparing the video voltage to an internally generated slicing level which is found by averaging the data signal during TV line no. 16 in the VPS mode or by averaging the data signal during the clock run-in period of the teletext lines during the data entry window (DEW) in PDC mode.

The acquisition clock generator delivers the system clock needed for the basic timing as well as for the regeneration of the dataclock. It is based on two phase locked loops (PLL's) all parts of which are integrated on chip with the exception of the loop filter components. Each of the PLL's is composed of a voltage controlled relaxation oscillator (VCO), a phase/frequency detector (PFD), and a charge pump which converts the digital output signals of the PFD to an analogue current. That current is transformed to a control voltage for the VCO by the off-chip loop filter. The generated VCO frequencies are 10 MHz and 13.875 MHz for VPS mode and PDC mode, respectively.

All signals necessary for the control of sync and data slicing as well as for the data acquisition are generated by this timing block.

The SDA 5652-2X can be operated in three different modes: Depending on the selected operating mode, either teletext lines carrying 8/30 packages, the dedicated TV line no. 16(VPS) or the teletext header bytes are acquired.

In PDC mode, only teletext rows 8/30 containing Broadcast Data Service Package (BDSP) information are acquired. The relevant bytes of 8/30 format 1 (8/30/1) and 8/30 format 2 (8/30/2) are extracted. The 8/30/1-bytes are stored in the acquisition register in a transparent way without any bit manipulation, whereas the hamming coded bytes of packet 8/30/2 are hamming-checked and bytes with one bit error are corrected.

In TTX header mode all bytes of the headers are stored. Hamming protected bytes are corrected and need not to be processed by the external controller. For the order of the stored bytes see I²C bus register description.

A micro controller can read the stored bytes via the I²C bus interface at any time.

In order to achieve maximum system performance it is recommended to start the SDA 5652-2X in VPS mode (state after power on) and read the register to check whether line 16 is received. After reception of VPS data in line 16 the SDA 5652-2X can be switched to 8/30 mode and waiting for packet 8/30 data. Since VPS data in line 16 is transmitted every frame and PDC data in packet 8/30 is transmitted nearly every second the recognition of both VPS and 8/30 packets can be done within PDC-system constraints (about 1 sec).

To differ between older (SDA5649/5650) and future (SDA5652-2X/...) PDC versions a special method can be used for chip identification:

SDA5649/5650 PDC-versions are not writeable. First step is, the user chooses a pattern of bytes and writes them to the RAM. Second step is to read these bytes from the RAM. By comparing the written bytes and the read bytes there may be correspondence or not. If there's correspondence the present IC is a new version (SDA5652-2X/...) if there's no correspondence its a older version (SDA5650/5651). In addition further versions (SDA5652-2X/...) could be differed with a special I²C-Register.

Valid-Data-Recognition:

The PDC/VPS-registers could be read by the external controller.
There is no necessity for the controller reading the PDC/VPS-contents if the register-contents aren't made topical by a new reception. There are three methods to identify if the register-contents are made topical after a previous reading-operation:

1. Data-Set-Valid-Bit

After a new reception is fulfilled the data-set-valid-bit is set from low to high. If data-set-valid-bit is high and a I²C-read-operation for a subaddress between 4 and 40 is closed by a stop condition the data-set-valid bit is set from high to low, if during the IIC-Read-operation no new datas are received.

2. DAVN-signal

On Pin10 the signal DAVN (Data Valid active low) will be available. The behaviour of this signal is described as follows:

a) VPS-Mode:

H/L-Transition (set to low):	After VPS-data has been received.
L/H-Transition (set to high):	At the start of line 16.

b) PDC/HTA/HTB/HTC-Mode:

H/L-Transition (set to high):	In the line where valid data is carried.
L/H-Transition (set to low):	At the beginning of the next field

3. VPS/PDC-register-contents

If a stop-condition is send to the I²C-bus-interface after a read-operation has been accessed for the addresses between 4 and 40, all register-contents from 4 to 40 are set to 255 if during the IIC-Read-operation no new datas are received (falling edge of DAVN). A new reception of VPS/PDC-datas during or after the IIC-Read-operation, will overwrite these FFh-contents. As a result a new data-reception could be detected by the register-contents itself.

Format of register ACQ_CONTROL (default values in brackets)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACQ_CONTROL	(0)	(0)	DSV (0)	MABC_1 (0)	MABC_0 (0)	HDT (0)	PDC/ VPS (0)	FOR1/ FOR2 (0)

FOR1/FOR2: Determines which kind of data is stored in the decoder when PDC mode is active:
0: BDSP 8/30/2 accessible
1: BDSP 8/30/1 or header row data accessible (refer to description of bit PDC/VPS

PDC/VPS: **0**: VPS mode is active
1: PDC mode is active

ATTENTION: Please refer to Errata-Sheet Item-No. H5 relating to VPS-Mode/Byte13

HDT: Determines whether BDSP 8/30/1 data or header row data is stored.
0: BDSP 8/30/1 accessible
1: Teletext header mode is active. See also bit MAB

MABC_1...0: **00**: Mode A. Header bytes are accessed in order 38 - 45, 30 - 37.
01: Mode B. Header bytes are accessed in order 22 - 29, 14 - 21.
1X: Mode C. Header bytes are accessed in linear increasing order 4-45.

DSV: Data set valid
This bit is only read and not writeable. Write-operations have got no influence to this bit.
Declares when PDC/VPS-register-contents are renewed after a previous read-operation. It is not allowed to read the content of DSV-Bit (Subadr. 03h) and VPS/PDC-data (subadr. 04h - 27h) within one IIC-protocol. In this case DSV is not cleared and the data-registers are not set to FFh reliable.
0: Register-contents haven't been renewed up to the moment this bit is read.
1: Register-contents are renewed. The datas read out by a new IIC-read-operation from byte 4-40 are completly valid.

7.1.1 Format of stored data bytes

Bits are stored in the order of their reception, that means the first transmitted bit is stored in bit 7 of the appropriate I²c bus address. In format 2 of packet 8/30 the contents of two transmitted bytes is stored in one I²c bus register address. Hamming bits are not stored.

ATTENTION: Please refer to errata-sheet item-no. H5 relating to VPS-Mode/Byte13 (I²C-subaddress 6)

I²C- Subaddress	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
8/30 Format 1	15	16	17	18	19	20	21	13	14	22	23	24
8/30 Format 2	16,17	18,19	20,21	22,23	14,15	24,25	13,x	x	x	x	x	x
VPS	11	12	13	14	5	15	x	x	x	x	x	x
HTA	38	39	40	41	42	43	44	45	30	31	32	33
HTB	22	23	24	25	26	27	28	29	14	15	16	17
HTC	4,5	6,7	8,9	10,11	12,13	14	15	16	17	18	19	20

I²C- Subaddress	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**
8/30 Format 1	25	26	27	28	29	30	31	32	33	34	35	36
8/30 Format 2	x	26	27	28	29	30	31	32	33	34	35	36
VPS	x	x	x	x	x	x	x	x	x	x	x	x
HTA	34	35	36	37	x	x	x	x	x	x	x	x
HTB	18	19	20	21	x	x	x	x	x	x	x	x
HTC	21	22	23	24	25	26	27	28	29	30	31	32

I²C- Subaddress	**28**	**29**	**30**	**31**	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**
8/30 Format 1	37	38	39	40	41	42	43	44	45	x	x	x
8/30 Format 2	37	38	39	40	41	42	43	44	45	x	x	x
VPS	x	x	x	x	x	x	x	x	x	x	x	x
HTA	x	x	x	x	x	x	x	x	x	x	x	x
HTB	x	x	x	x	x	x	x	x	x	x	x	x
HTC	33	34	35	36	37	38	39	40	41	42	43	44

I²C- Subaddress	**40**

8/30 Format 1	x
8/30 Format 2	x
VPS	x
HTA	x
HTB	x
HTC	45

7.2. OSD Functions

The OSD block consists of a character generator unit which reads out character addresses from the internal RAM and transforms them by the help of a character ROM into pixel information. The OSD memory has a size of 448 Bytes. As a result the display is fixed to a format of 14 rows with 32 characters. For a 50Hz-system 14 rows are displayed, for a 60Hz-system 12 rows. The count of columns can be defined by the user to 30 or 32. For systems using a color-carrier of 4,43MHz 32 characters should be choosen, for systems using a 3,58MHz color-carrier 30 characters should be choosen. So if needed the display-memory-contents from the two columns on the right side or the contents from the two last rows are ignored. Bytes are processed in linear binary increasing order. The display memory is accessed via the dataport. Starting address is 0_d (see also 7.3.2. Dataport access). The character structure is 12 pixels in horizontal direction and 18 lines in vertical direction.

HORIZONTAL_SIZE (2Bit)	VERTICAL_SIZE (2Bit)	CHAR-attribute_2 (2Bit)	CHAR-attribute_1 (2Bit)		i = 0	.....	i = 31
	X X	XX	XX	0 + i			
	X X	XX	XX	32 + i			
	X X	XX	XX				
	...	...	...				
	...	...	...				
	...	...	...	...		Display Memory 14 rows with 32 characters	
				416 + i			

With the Bits 0 to 6 of the address 128 characters of the character ROM can be addressed. The addresses of the characters are orientated on the wellknown ASCII-table.

Bit 7 of the character address is used to switch between two attribute definitions. These two attribute definitions can be chosen for each row individual. For this choice each row has two character-attribute-registers, **CHAR_attribute_1** and **CHAR_attribute_2**.

CHAR-attribute_1 consists of two bit and **CHAR-attribute_2** consists of two bits. One out of four character-definitions can be selected by these two bits. These four character-definitions are made for **CHAR-attribute_1** in the four registers **CHAR-definition1_1...1_4**. For **CHAR-attribute_2** these four definitions are made in **CHAR-definition2_1...2_4**.

The format of the CHAR-definition-Registers and the CHAR-attribute-Registers see below.

Format of the registers CHAR-definition1_1...1_4 and CHAR-definition2_1...2_4: (default value in brackets):

	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
BYTE 1	HALF-TONE	BL_1	BL_0	HS_1	HS_0	BK_0	BK_1	INV
BYTE 2	FCOL_4	FCOL_3	FCOL_2	FCOL_1	FCOL_0	BCOL_2	BCOL_1	BCOL_0

HALFTONE:

Fullpage-Mode or if Display is turned off:
In Fullpage-Mode or if display is turned off this bit has got no influence. Pin11 is static switched to L-Level.
Mixed-Mode:
Switches between Halftone-Blanking on and off. Characters for which halftone-blanking is turned on, pin11 is switched to H-Level during these characters are displayed. Otherwise pin11 is switched to L-Level.

0: Switching Halftone-Blanking off
1: Switching Halftone-Blanking on

HS_1...0:

Horizontal size per dot as multiples of the pixel clocks. Only used if the row-attribute HORIZONTAL_SIZE_SELECT bits are set to 0.
00: 1 pixel clock per dot.
01: 2 pixel clocks per dot.
10: 3 pixel clocks per dot.
11: 4 pixel clocks per dot.

BL_1...0:

Defines the blanking mode of the characters in mixed mode. There’s a special fringing-mode. Fringing means, that the character is surrounded by a border. This border has the size of one pixel:

Settings for mixed mode:
00: Blanking is switched off. The complete character (border and background) is visible on the screen.
01: Background is blanked, only the foreground information

of the character is visible.
10: Background is blanked, only the foreground information of the character including the border (fringing) is visible.
11: The complete characters are blanked. (The character is not visible)

In full-page-mode no blanking is available. Fringing can be switched with bit BL_1.
Settings for full-page-mode:
0X: Fringing is switched off
1X: Fringing is switched on

BK_1...0: Defines the flashing mode and period for the appropriate row. When flashing is specified for reversed characters, the flashing will be between normal character and reversed display.
00: Flashing is switched off
01: Flashing is switched on. The period is approximately set to 0.5/s
10: Flashing is switched on. The period is approximately set to 1.0/s
11: Flashing is switched on. The period is approximately set to 1.5/s

BCOL_2...0: **In full-page-mode:** Defines the background color vector. The final color depends on the values of the look up table (see below).
In mixed-mode: Defines the background grey-value. The final grey-value depends on the luminancevalue described in the look up table (see below).

FCOL_4...0: Defines the foreground grey-value. Up to 23 values between 1,4V and 2,9V in steps of about 68mV can be selected in full-page-mode (The values from 0 to 8 are not allowed because there levels are in the sync-area). Up to 32 values between 1,4V and 2,9V in steps of about 48 mV can be selected in mixed-mode.

INV: 0: Inverting is switched off
1: Inverting is switched on

The characters can be zoomed in horizontal and vertical direction. Characters neighboured on the right or below of a zoomed character are overwritten and not shifted.

Each row has two **VERTICAL-SIZE-SELECT** bits in which the size of the characters are defined for the whole row. The size can be zoomed in vertical direction up to factor 4.

Each row has two **HORIZONTAL-SIZE-SELECT** bits in which the size of the characters can be defined for the whole row. The size can be zoomed in horizontal direction up to factor 4. If the **HORIZONTAL_SIZE_SELECT** bits are set to 0 each character can be zoomed individual by the char_attributes- and char_definition-registers.

The **HORIZONTAL_SIZE_SELECT** bits, **VERTICAL_SIZE_SELECT** bits and the **CHAR_attribute_1..2** bits are stored for each row in the register ROW_ATTRIBUTE:

Format of the register ROW_ATTRIBUTE:

	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
ROW 1	HORIZONTAL_SIZE/Bit1	HORIZONTAL_SIZE/Bit0	VERTICAL_SIZE/Bit1	VERTICAL_SIZE/Bit0	CHAR_ATTRIBUTE_2/Bit1	CHAR_ATTRIBUTE_2/Bit0	CHAR_ATTRIBUTE_1/Bit1	CHAR_ATTRIBUTE_1/Bit0
ROW 2	HORIZONTAL_SIZE/Bit1	HORIZONTAL_SIZE/Bit0	VERTICAL_SIZE/Bit1	VERTICAL_SIZE/Bit0	CHAR_ATTRIBUTE_2/Bit1	CHAR_ATTRIBUTE_2/Bit0	CHAR_ATTRIBUTE_1/Bit1	CHAR_ATTRIBUTE_1/Bit0
....	....	....	....	....	....	....	....	....
ROW 14	HORIZONTAL_SIZE/Bit1	HORIZONTAL_SIZE/Bit0	VERTICAL_SIZE/Bit1	VERTICAL_SIZE/Bit0	CHAR_ATTRIBUTE_2/Bit1	CHAR_ATTRIBUTE_2/Bit0	CHAR_ATTRIBUTE_1/Bit1	CHAR_ATTRIBUTE_1/Bit0

ATTENTION: Please refer to errata-sheet item-no. H1, H4 relating to vertical and horizontal zoom

Format of the registers VERTICAL_START_POSITION and HORIZONTAL_START_POSITION:

The position of the display can be adjusted in terms of pixels and lines referring to the horizontal and vertical edge of the picture. The position is programmed in the register vertical_start_position and horizontal_start_position. The line-counter for the vertical-start-position is set to 0 during the negative going flank of V-Sync. The pixel-counter for the horizontal-start-position is set to 0 after the positive going flank of H-Sync (negative flank of VCS).

	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
VERTICAL_START_POSITION	(0)	VSP_6	VSP_5	VSP_4	VSP_3	VSP_2	VSP_1	VSP_0
HORIZONTAL_START_POSITION	(0)	HSP_6	HSP_5	HSP_4	HSP_3	HSP_2	HSP_1	HSP_0

ATTENTION: Please refer to errata-sheet item-no. H1, H2, H3, H4, H6 relating to horizontal and vertical start-position.

VSP_6...0: Vertical start position of the screen. VSP_6...0 define the shift of the screen in vertical direction as multiples of horizontal lines.

HSP_6...0: Horizontal start position of the screen. HSP_6...0 define the shift of the screen in horizontal direction in pixel clocks.

Clock-Supply

The pixel clock (2FSC, FSC, 2FSC/3, FSC/2) is derived from the system-clock (4FSC) depending on the horizontal-zoom-factor.

The system-clock(4FSC) is derived from a external frequency. There are two methods to provide these external frequency. One method is to fed in a frequency of 1FSC or 2FSC or 4FSC at Pin3. The second method is to plug a 2FSC-crystal-oscillator to Pin3 and Pin6. Which of these methods is used is defined in the register SYNCHRONISATION.

The pixel clock is internally synchronized to the horizontal- sync information by a discrete phase shifter.

Synchronisation-modes

The sync information may be delivered as external V/H impulses, as a composite sync signal or is derived from the analog CVBS-signal. In free run mode the timing block can generate its composite sync signal so a stable display can be produced even if no external sync source is available. There are different synchronisation-modes for mixed-mode-OSD. For more information of these modes, see register **SYNCHRONISATION** and the figure on page 22.
For high-end-sync-performance in mixed-mode a internal HPLL can be used for synchronisation.
The HPLL consist of a digital DTO, a digital phase-detector and a loop-filter.

There are different settings for the loop-filter possible. For high-performance we recommend a universal loop-filter-setting. For advanced high-performance there is the possibility to adapt the loop-filter to each customer-specific-VCR in the different replay-modes (Fast-Forward/Fast-Backward-mode, Long-Play/Short-Play).

	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
HPLL	(0)	(0)	(0)	(0)	HPLL_3	HPLL_2	HPLL_1	HPLL_0

HPLL0: Register to justify the integral filter-component
0: 1/128
1: 0

HPLL1: Register to justify the proportional filter-component
0: 1
1: 4

HPLL2..3: Register to justify the proportional/integral filter-component
00: 1/32

01: 1/16
10: 1/8
11: 1/4

For universal VCR/Tuner-modes we recommend:

HPLL0: 0
HPLL1: 1
HPLL2: 1
HPLL3: 1

For high-performance noise-surpress we recommend:
HPLL0: 0
HPLL1: 0
HPLL2: 0
HPLL3: 0

In mixed mode display the signal processing is synchronized to the CVBSin-Signal. For this at Pin7 and Pin9 the H-synchronization and V-synchronization-signals can be fed to the IC. In full-page-mode both pins(Pin7 and Pin9) are working as a output. In this case they deliver H-sync and V-sync-signals. They also can be switched in a highly impedant state.

Format of register SYNCHRONISATION (default values in brackets):

	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
SYNCHRONISA-TION	(0)	SYNC_2 (1)	SYNC_1 (0)	SYNC_0 (0)	IIC_SWITCH(1)	DISPON (0)	OSC_SYS_1(0)	OSC_SYS_0(1)

DISPON: Switches the CVBS_in-signal (Pin18) to CVBS_out-signal(Pin15). This bit has highest priority. Switching it to low, the incoming CVBS-signal is fed through the IC to CVBS output.

0: CVBS_in=CVBS_out
1: The two states CVBS_in=CVBS_out and D/A=CVBS_out is controlled by the character-generator

IIC_SWITCH: After RELEASE-bit has been set from 1 to 0, a new IIC-bus-protocol should be started to switch IIC-switch from 1 to 0. By this, highest noise-surpression of the SDA/ SCL-signals is guaranteed.
(see also „10.1 After-Reset-Start-Sequence“)

OSC_SYS_1...0: Defines source for system-clock generation. The frequency of this source is internally multiplied to 4FSC.
This frequency is used for color-carrier-generation in full-

page-mode.
00: 1 FSC (Pin 3) with ext. feedback resistor
01: 2 FSC (Pin 3) with ext. feedback resistor
10: 4 FSC (Pin 3) with ext. feedback resistor
11: optional, external crystal-oscillator for system-clock-generation(Pin3/Pin6). This crystal-oscillator must have his resonance-frequency at 2FSC.
This mode also can be used as a alternative mode to 01: 2FSC (Pin3). In this mode the external feedback resistor is no longer necessary because in this mode a internal resistor is used.

The oscillator-mode can be installed by these bits as long as the bit RELEASE in the register LEVELS_AND_CHANGE is set to 1.

After setting bit RELEASE in register LEVELS_AND_CHANGE to 0, the oscillator-mode won't change anymore, anyway if the polarity of these bits are changed by the user.
Next to the oscillator-mode-settings, the bit OSC_SYS(0) can be used to switch a special VCS-spike-surpress-filter for the slicer on and off. We recommend to keep this filter switched on in all modes.

0: The VCS-spike-filter is switched on.
1: The VCS-spike-filter is switched off.

Next to the oscillator-mode-settings the bit OSC_SYS(1) can be used to switch a special algorithm to the slicer. This special algorithm allows high noise-surpress. The algorithm works for signals in which the CRI has the same length(8cycles) as it is described inside the ETSI-standard for teletext. If a CVBS-signal is processed in which the count of CRI-cycles is non-standard the special algorithm should be switched off. We recommend to start the data-slicing by switching the special algorithm on (for standard-signals and high-noise-performance). If this is not success-full we recommend to proceed the data-slicing by switching the special algorithm off. By this, non-standard-signals can be sliced with a little less noise-performance.

0: Special algorithm is switched on
1: Special algorithm is switched off

SYNC_2...0: Three MUXes inside the synchronisation-signal-pathes are controlled by these three bits as shown below in the figure. Pin9 and Pin7 are used as a input/output for external syn chronisation. If bit SYNC_2 is switched to 0 Pin7 is used as output, if SYNC_0 is switched to 1 Pin9 is used as output.

Next to SYNC_2...0 the synchronisation-signal-path is controlled by the bits SYNC_HIMP, HSYNC_HIGH/LOW_DETECT and VSYNC_HIGH/LOW_DETECT of the register LEVELS_AND_CHANGE (see also page 26/27). SYNC_HIMP is used to switch the outputs in high-impedant-state. HSYNC_HIGH/LOW_DETECT and VSYNC_HIGH/LOW_DETECT is used to invert the synchronisation-signals for enabling the detection of both edges synchronisation-edges.

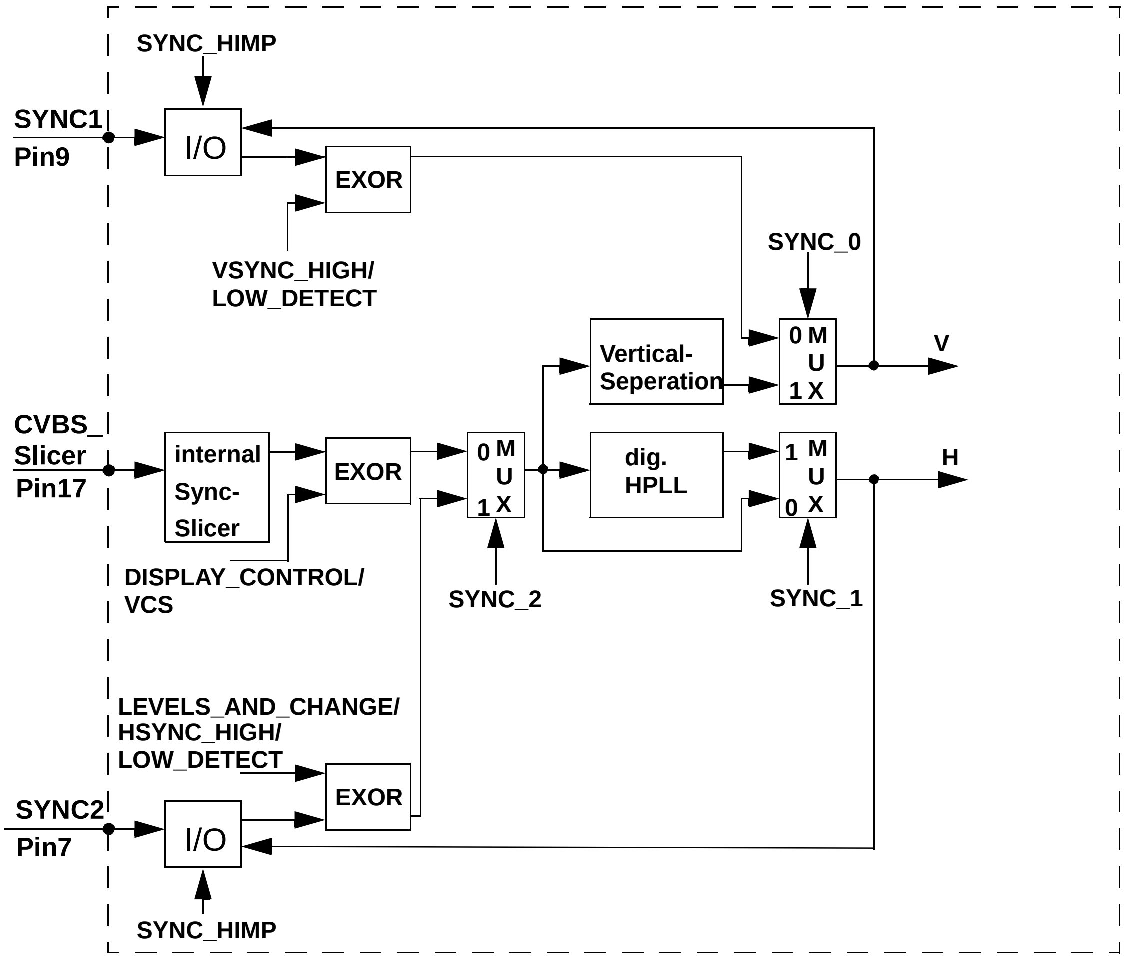


Figure: Signal-pathes of the sync-seperation-circuit

Summary of Sync-Modes (SYNC2...0):

SYNC_2	SYNC_1	SYNC_0	H	V	HPLL	Pin9	Pin7
0	0	0	intern	extern	out of use	input	output
0	0	1	intern	intern	out of use	output	output
0	1	0	intern	extern	in use	input	output
0	1	1	intern	intern	in use	output	output
1	0	0	extern	extern	out of use	input	input
1	0	1	extern	intern	out of use	output	input
1	1	0	extern	extern	in use	input	input
1	1	1	extern	intern	in use	output	input

Negative going **HSync**-pulses are expected by default. Using the register LEVELS_AND_CHANGE this can be switched to positive going syncpulses.

With VSYNC_EDGE_POLARITY in the register LEVELS_AND_CHANGE the user can choose level or edge-sensitive vertical synchronisation.

The polarity of the digital output-H-sync-signal are positive going sync-impulses.

The color look-up-table

The IC is capable to display eight different color values in one picture. These eight values can be defined by the user in the registers **color_value**:

On the assumption, that the color-values are given in voltage values which are related to a CVBS-Signal the corresponding register-contents could be derived as follows:

given color-value: phase
chromaamplitude (peak to peak in mV)
luminanceamplitude (in mV above porch-level)

corresponding register-contents:

luminance-register: INTEGER(63*(luminanceamplitude+300mV)/1000mV)

U-component-register: INTEGER(chromaamplitude*cos(phase)*63/2000mV)

V-component-register: -INTEGER(chromaamplitude*sin(phase)*63/2000mV)

For example these equations are solved for three color-values:

1. Blue

Phase: -38° Chromaphase
162mV Chromaamplitude (peak to peak in mV)
200mV Luminanceamplitude (above Porch-Level)

luminance-register: 32

U-component-register: +4

V-component-register: +3

2. Blue-Green

Phase: -90° Chromaphase
286mV Chromaamplitude (peak to peak in mV)
250mV Luminanceamplitude (above Porch-Level)

luminance-register: 35

U-component-register: 0

V-component-register: +9

3. Grey

Phase: indifferent Chromaphase
0mV Chromaamplitude
125mV Luminanceamplitude (above Porch-Level)

luminance-register: 27

U-component-register: 0

V-component-register: 0

The U/V-component-registers are programmed in two's-complement. This means:

01111b = +15
01110b = +14
01101b = +13
....
00000b = 0
11111b = -1
11110b = -2
11101b = -3
....
10001b = -15

The value 10000 b = -16d is not allowed.

Format of the eight registers color-value1...8:

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LUMINANCE	(0)	(0)	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
U-COMPONENTE	(0)	(0)	(0)	BIT4	BIT3	BIT2	BIT1	BIT0
V-COMPONENTE	(0)	(0)	(0)	BIT4	BIT3	BIT2	BIT1	BIT0

Format of border-color-register/Fringing-color-register:

There is a leftover of active video surrounding the field of characters. The colors of this border can be defined via the look-up-table described above.

Next to the border-color, the fringing color is defined in this register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BORDER_FRINGIN G	(0)	FRCO_2	FRCO_1	FRCO_0	BO_ON OFF	BORDE R_2	BORDE R_1	BORDE R_0

Border can be switched on and off.

Border off means for **fullpage-mode:** The left part of the border in each row is set to the same color as the first character in each row is set. The right part of the border in each row is set to the same color as the last character is set. The upper and lower part of the border is set to the color defined for the border.

Border on means for **fullpage-mode:** The whole border has the color which is defined for the border.

BO_ONOFF
0: Border on
1: Border off

BORDER2...0
Defines the color of the border via the color-look-up-table (see above).

FRCO_2..0:
If fringing is turned on one out of eight fringing grey-values can be selected. The levels for the grey-values in full-page mode are 1.4V and 1.9V in steps of about 67 mV. In mixed mode eight levels between 1.4V and 2.1V in steps of about 93mV can be selected in full-page-mode.

Format of register Display Control:

Switching between full-page-OSD and mixed-mode and turning display off, etc. ...
is handled with the Display-Control-Register. The IC has a multi standard video output. That means, NTSC/PAL-color-systems can be encoded and field-frequencies of 50/60Hz can be choosen.

In standard-mode the pixel-clock is derived from color-carrier (2FSC). The user is free to choose the color-carrier which is fed in at Pin3. For example PAL color-carrier is 4.43MHz and NTSC color-carrier is 3.58MHz. The pixel-clock is derived from this color-carrier. A suitable count of character in horizontal direction can be choosen by the bit NORM1.

For NTSC and some PAL-derivates a frame-rate of 60Hz (525 lines) is used. In this case in vertical direction 12 character-rows are produced. In standard-PAL a frame-rate of 50Hz (625 lines) is used. As a result in vertical direction 14 character-rows are produced.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DISPLAY CON-TROL	DAVN/ EHB	VCS	FULL-PAGE	SECAM_ SWITCH	SPACE	NORM_2	NORM_1	NORM_0

DAVN/EHB: The DAVN and EHB-signals can be made visible on the output-pin10. Which of these two signals is shown on the output-pin is defined in the bit DAVN/EHB.

1: EHB is shown at Pin10.
0: DAVN is shown at Pin10.

VCS:
0: Internal VCS is not inverted (front porch of H is used for synchronisation).
1: Internal VCS is inverted (back porch of H is used for synchronisation).

NORM0: This bit is only used in full-page-mode.
0: NTSC
1: PAL

NORM1: This bit is used in both modes (full-page and mixed-mode)
0: 30 characters in horizontal direction
1: 32 characters in horizontal direction

NORM2: This bit is used in both modes (full-page and mixed-mode)
0: 50Hz-system
1: 60Hz-system

Following standards can be choosen by NORM2 and NORM0:

NORM2	NORM0	standard	nominal color-carrier-frequency
0	0	NTSC(equivalent to mode “10”)	3,57954500 MHz
0	1	PAL BG	4,43361875 MHz
1	0	NTSC(equivalent to mode “00”)	3,57954500 MHz
1	1	PAL M	3.57561149 MHz

SPACE:
0: In this state the character-RAM is displayed.
1: In this state the contents of the character-RAM are ignored and space-characters are displayed all over the screen.

SECAM_SWITCH:
0:SECAM-Switch off for PAL/NTSC
1:SECAM-Switch on for SECAM-Signals. That means the current SECAM-color-frequency on CVBSin-side is added to the CVBS-out signal in the areas of characters in mixed mode.

FULLPAGE:
0:Full-Page-OSD-Mode.
1:Mixed-Mode.

Format of register LEVELS_AND_CHANGE:

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LEVELS_AND_CHANGE	(0)	(0)	VSYNC_EDGE_POLAR-ITY (1)	RELEASE (1)	SYNC_HIMP(1)	VSYNC_HIGH/LOW_DETECT (0)	HSYNC_HIGH/LOW_DETECT (0)	CHNG_MIXED_FULL (1)

CHNG_MIXED_FULL: Next to the Register-Bit FULLPAGE in DISPLAY_CONTROL-Register this bit has to be used for switching between fullpage-mode and mixed-mode.
0: For mixed-mode
1: For fullpage-mode

1. Switching from mixed-mode to fullpage-mode:
first step: DISPLAY_CONTROL/Bit5 set to 0
second step: CHNG_MIXED_FULL set to 1

2. Switching from fullpage-mode to mixed-mode:
first step: CHNG_MIXED_FULL set to 0
second step: DISPLAY_CONTROL/Bit5 set to 1

HSYNC_HIGH/LOW_DETECT: Defines which polarity of the Hsync should be used for OSD-synchronization.
0: Negative going sync-pulses are expected.
1: Positive going sync-pulses are expected.

VSYNC_HIGH/LOW_DETECT: Defines which edge of the Vsync should be used for OSD-synchronization.
0: Uses the rising edge
1: Uses the falling edge

SYNC_HIMP:
0: The output of the pins 7/9 are not switched to high-impedant-state in all the modes.
1: The output of the pins 7/9 are switched to high-impedant-state in all the modes.

RELEASE: After power-on-reset the contents of the synchronisation-register may not refer to the frequency which is fed in at Pin9/7. After setting the bits OSC_SYS1..0 in the Register SYNCHRONISATION to the contents which are referring to the input-frequency, the bit RELEASE has to be switched from 1 to 0. After switching to 0 the bit RELEASE cannot be changed anymore to 1 except by a IIC-bus- or power-on-reset.
After switching bit RELEASE to 0 the bits OSC_SYS1..0 in Register SYNCHRONISATION cannot be changed anymore without executing a IIC- or

power-on-reset..

VSYNC_EDGE_POLARITY: This bit is used, to choose the synchronisation-mode in mixed-mode for the VSync. If polarity is choosen the OSD is synchronized by the levels of the VSync. In this case the Vsync should have a minimum-length of 1line. If edge is choosen the OSD is synchronized by the edge of the VSync. In this case there are no special efforts to the Vsync-length.
In general it’s recommended to use the edges.

0: OSD is synchronized by VSync edges.

1: OSD is synchronized by VSYNC polarity.

7.3. I²C-Bus

Information is exchanged between an external controller and the SD 5652-2X on a fast asynchronous bidirectional data bus. The I²C-Bus uses two connections, the pins SDA (data) and SCL (clock), and operates according to the I²C-Bus specifications, which limits the maximum transfer rate at 400 kbit/s. The interface operates in the slave mode: either as receiver or transmitter. The chip address is fixed to **MSB 0010000X LSB**. The MSB is transmitted first. The LSB switches between reading-mode(1) and writing-mode(0).

The bus-system isn't blockaded if there is no power-supply switched to the SDA5652-2X

7.3.1 Protocols

The following protocols are supported (in read mode the subaddress must be defined by a previously access):

Write followed by a read:

START	SL_AD	WRITE	ACK_S	SU_AD	ACK_S	DATA	ACK_S	DATA	ACK_S	...	...	...	START	SL_AD	READ	ACK_S	DATA	ACK_M	DATA	ACK_M	DATA	ACK_M	...	...	...	STOP

Please notice: Before the stop-condition after the reading-operation, there is no ACK_M allowed!!!

Write followed by a read with stop condition:

START	SL_AD	WRITE	ACK_S	SU_AD	ACK_S	DATA	ACK_S	DATA	ACK_S	...	...	STOP	START	SL_AD	READ	ACK_S	DATA	ACK_M	DATA	ACK_M	DATA	ACK_M	...	...	...	STOP

Please notice: Before the stop-condition after the reading-operation, there is no ACK_M allowed!!!

with the following abbreviations:

START: Start condition (I²C: see technical bus description)

STOP: Stop condition (I²C: see technical bus description)

ACK_S: Acknowledge by slave (I²C: see technical bus description)

ACK_M: Acknowledge by master (I²C: see technical bus description)

SL_AD: 7- Bit chip select address

SU_AD: 8- Bit subaddress

7.3.2 Access modes

There are two possibilities to access SDA 5652-2X. One is addressing it direct by use of one of the 256 possible subaddresses of the I²C protocol. The other method is an indirect addressing method. This must be used if a byte from the display RAM should be read or written. In that case a dataport must be used for transfer (see below).

Autoincrement of Bus Registers

After any read or write access to a register the subaddress will be incremented automatically. There are only one exceptions: in read and write mode, subaddress „2“ is not incremented (see also dataport access).

7.3.3 Dataport access

The address pointer registers are used to address the internal memory to read or write data via the I²C Bus. A dataport (2) is an I²C-Bus register which can be read or written by addressing it with its subaddress. Independent from the transfer direction (read or write) the memory address is defined by the address pointer registers (0, 1) which must be defined before accessing the dataport. The display-RAM is accessed via the dataport. Its startaddress begins at address 0.

Autoincrement of the Dataport

The autoincrement for the dataport is always switched on. That means, each time after the dataport address (2) is accessed, the contents of the addresspointer registers is incremented. The following protocols are supported:

Writing the memory including initializing of addressport:

START	SL_AD	WRITE	ACK_S	SU_A0	ACK_S	ADR_0	ACK_S	ADR_1	ACK_S	DATA	ACK_S	DATA	ACK_S	DATA	ACK_S	DATA	ACK_S	...	...	...	...	...	...	...	ACK_S	STOP

Writing the memory using an previous defined addressport:

START	SL_AD	WRITE	ACK_S	SU_A2	ACK_S	DATA	ACK_S	DATA	ACK_S	DATA	ACK_S	DATA	ACK_S	DATA	ACK_S	DATA	ACK_S	DATA	ACK_S	...	...	...	...	...	ACK_S	STOP

Reading the memory using an previous defined addressport:

START	SL_AD	WRITE	ACK_S	SU_A2	ACK_S	STOP	START	SL_AD	READ	DATA	ACK_S	DATA	ACK_M	DATA	ACK_M	DATA	ACK_M	DATA	ACK_M	...	...	...	...	...	...	STOP

Please notice: Before the stop-condition after the reading-operation, there is no more a

ACK_M allowed!!!

with the following additional abbreviations:

SU_A0...2: Subaddress

ADR_1...0: Addresspointer

START: Start condition (I²C: see technical bus description, M3L Falling edge of I²CEN)

STOP: Stop condition (I²C: see technical bus description, M3L Rising edge of I²CEN)

ACK: Acknowledge (I²C: see technical bus description)

SL_AD: 7-Bit chip select address

Format of the register ADR_POINTER (default values in brackets):

	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
ADR_POINTER_1	(0)	(0)	(0)	(0)	(0)	(0)	ADR_9 (0)	ADR_8 (0)
ADR_POINTER_0	ADR_7 (0)	ADR_6 (0)	ADR_5 (0)	ADR_4 (0)	ADR_3 (0)	ADR_2 (0)	ADR_1 (0)	ADR_0 (0)
DATA_PORT	DAT_7 (0)	DAT_6 (0)	DAT_5 (0)	DAT_4 (0)	DAT_3 (0)	DAT_2 (0)	DAT_1 (0)	DAT_0 (0)

ADR_9...0 Addressport. Defines the internal memory address where data should be written or read from. Only address valid addresses defined in the memory map table are allowed.

Format of register DATA_PORT (default values in brackets):

	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DATA_PORT	DAT_7 (0)	DAT_6 (0)	DAT_5 (0)	DAT_4 (0)	DAT_3 (0)	DAT_2 (0)	DAT_1 (0)	DAT_0 (0)

DAT_7...0 Dataport. This register contains the data to be transferred. Each time when this register is read or written the contents of the addressport is autoincremented and not the internal subaddress.

Example for data port access (Beginning at address 292d (124h) the following data should be written: 11h, 12h, 13h, 14h

Protocol	Hex values	Comment
Chipadress,Write	20h	SDA 5652-2X chipaddress
Subaddress	00h	Subaddress is initialized
Data, Ack	24h	24h is transmitted to subaddress „0“ (Addresspointer). The internal subaddress is autoincremented.
Data, Ack	01h	01h is transmitted to subaddress „1“ (Addresspointer) Addresspointer is now set to 124h.
Data, Ack	11h	Subaddress is now „2“. Data is written to the dataport and then internally transferred to RAM address 124h. The addresspointer is autoincremented to 125h. The subaddress is not incremented
Data, Ack	12h	Data is written to the dataport and then internally transferred to RAM address 125h. The addresspointer is autoincremented to 126h.
Data, Ack	13h	Data is written to the dataport and then internally transferred to RAM address 126h.The addresspointer is autoincremented to 127h.
Data, Ack	14h	Data is written to the dataport and then internally transferred to RAM address 127h. The addresspointer is autoincremented to 128h.
Stop		

7.3.4 Subaddresses and commands of I²C-Bus

7.3.4.1 I²C-register-addresses:

The above described I²C-Registers can be handled with the subaddresses described below. A special function is implemented for the address 255. If this address is submitted to the IC a reset is released.

I²C-Address	Register-Name	read/write
0	ADR_POINTER_0	write
1	ADR_POINTER_1	write
2	DATA-PORT	read/write
3	ACQ-Control	read (only Bit5) / write(excluding Bit5)
4-40	VPS/PDC-datas	read
41	SYNCHRONISATION	read(only OSC_SYS1..0)/ write

42	LEVELS_AND_CHANGE	write
254	IC-IDENTIFICATION (content:02h)	read
255	RESET	write

7.3.4.2. I^{2}C-Commands

RESET-Command: 255d

This command resets the whole IC. The protocol which has to be used is defined as follows:

START	SL_AD	WRITE	ACK	255	ACK	DATA	ACK	STOP

START: Start condition (I^{2}C: see technical bus description, M3L Falling edge of I^{2}CEN)

STOP: Stop condition (I^{2}C: see technical bus description, M3L Rising edge of I^{2}CEN)

ACK: Acknowledge (I^{2}C: see technical bus description)

SL_AD: 7-Bit chip select address (Write-Mode)

255: Reset-Command

DATA: This data hasn't got any meaning. It's only used to keep the restrictions of a protocol.

7.3.4.3 RAM-registers

Some register-contents are stored in the RAM. These register-contents have to be accessed using the Data-Port of the I²C-bus:

from	to	content
0	447	display-RAM
448	484	used IC-internal
485		ROW_ATTRIBUTE/ROW1
486		ROW_ATTRIBUTE/ROW2
487		ROW_ATTRIBUTE/ROW3
488		ROW_ATTRIBUTE/ROW4
489		ROW_ATTRIBUTE/ROW5
490		ROW_ATTRIBUTE/ROW6
491		ROW_ATTRIBUTE/ROW7
492		ROW_ATTRIBUTE/ROW8
493		ROW_ATTRIBUTE/ROW9
494		ROW_ATTRIBUTE/ROW10
495		ROW_ATTRIBUTE/ROW11
496		ROW_ATTRIBUTE/ROW12
497		ROW_ATTRIBUTE/ROW13
498		ROW_ATTRIBUTE/ROW14
499		CHAR_definition1_1/BYTE1
500		CHAR_definition1_1/BYTE2
501		CHAR_definition1_2/BYTE1
502		CHAR_definition1_2/BYTE2
503		CHAR_definition1_3/BYTE1
....		....
507		CHAR_definition2_1/BYTE1
....		....
514		CHAR_definition2_4/BYTE2
515		VERTICAL_START_POSITION
516		HORIZONTAL_START_POSITION
517		DISPLAY_CONTROL
518		BORDER_color
519		COLOR_VALUE_1/LUMINANCE
520		COLOR_VALUE_1/V_COMPONENTE

from	to	content
521		COLOR_VALUE_1/U_COMPONENTE
522		COLOR_VALUE_2/LUMINANCE
523		COLOR_VALUE_2/V_COMPONENTE
524	....	....
525		COLOR_VALUE_4/LUMINANCE
....		COLOR_VALUE_4/V_COMPONENTE
530		COLOR_VALUE_4/U_COMPONENTE
....	....	....
....		COLOR_VALUE_8/LUMINANCE
....		COLOR_VALUE_8/V_COMPONENTE
542		COLOR_VALUE_8/U_COMPONENTE
543		HPLL
544	575	out of internal use
576	612	used internal

8. Electrical Characteristics

Power-on-reset:

After Power-on a so called Power-on-reset is executed. The condition for a power-on-reset is a rising VDDA from a voltage value of less than 0,8V to a voltage value of at least 4,5V.

Absolute Maximum Ratings

T_A = 25 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature	T_A	0	70	°C	in operation
Storage temperature	T_{stg}	– 40	125	°C	by storage
Total power dissipation	P_{tot}		tbd	mW	
Power dissipation per output	P_{DQ}		10	mW	
Supply voltage	V_{DDD} V_{DDA}	– 0.3 – 0.3	6 6	V V	
Thermal resistance	$R_{th\ SU}$		80	K/W	
Operating Range					
Supply voltage	V_{DDD} V_{DDA}	4.5 4.5	5.5 5.5	V V	
Supply current	I_{DD}	35	50	mA	
Ambient temperature range	T_A	0	70	°C	

Characteristics

T_A = 25 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input Signals SDA, SCL					
H-input voltage	V_{IH}	0.7xV_{DDD}	V_{DDD}	V	
L-input voltage	V_{IL}	0	0.3xV_{DDD}	V	
Input capacitance	C_I		10	pF	
Input current	I_{IM}		10	µA	
Input Signal TMODE					
H-input voltage	V_{IH}	0.9xV_{DDD}	V_{DDD}	V	
L-input voltage	V_{IL}	0	0.1xV_{DDD}	V	
Input capacitance	C_I		10	pF	
Input current	I_{IM}		10	µA	

Characteristics (cont'd)

T_A = 25 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input Signal CVBS/Output Signal mixed mode:					
synchron signal amplitude (bottom)	V_{SYNC}	0.7	0.9	V	
Black-Porch-Level	V_{PORCH}	1.3	1.5	V	

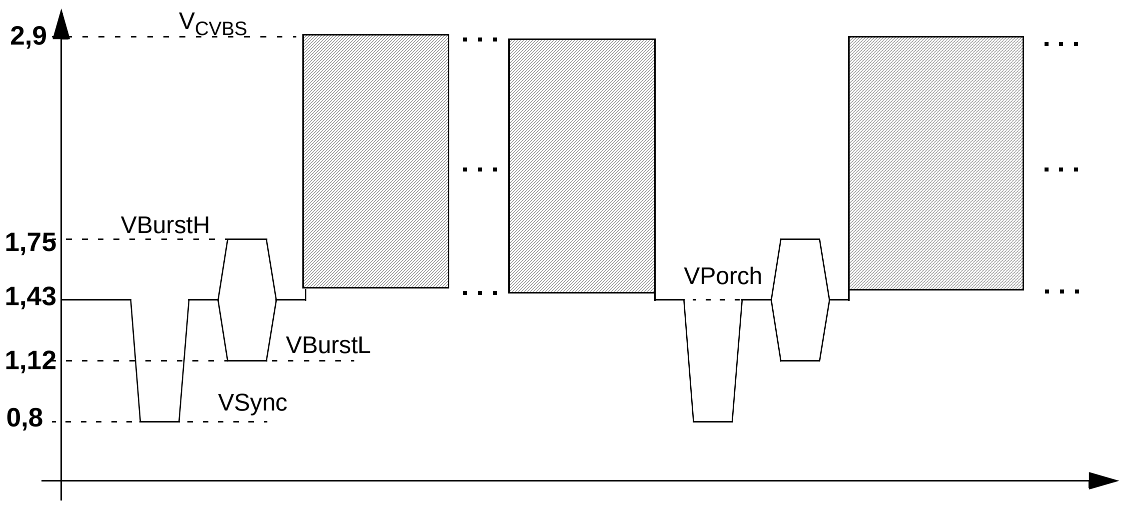
Resistance of the switch between input and output-signal in mixed mode: <50 Ohm

Output Signal CVBS in full page mode:
Supplyvoltage is used as reference for D/A-converter. So the stability of voltage-values for the output signal depend on the supplyvoltage stability. Min-values are related to a supplyvoltage of 4,5V and max-values are related to a supplyvoltage of 5,5V.

100% - white level	V_{CVBS}	2.6	3.2	V	
Synchron signal amplitude (bottom)	V_{SYNC}	0.7	0.9	V	
Color burst low	V_{BURSTL}	1.0(NTSC) 1.1(PAL)	1.2(NTSC) 1.3(PAL)	V	
Color burst high	V_{BURSTH}	1.6(NTSC) 1.5(PAL)	1.9(NTSC) 1.8(PAL)	V	
Black-Porch-Level	V_{PORCH}	1.3	1.6	V	
Input Signal CVBS_Slicer :					
Video input signal level peak to peak	V_{CVBS}	0.7	2.0	V	
Synchron signal amplitude peak to peak	V_{SYNC}	0.15	1.0	V	Vdat=450mV
Data amplitude peak to peak	V_{DAT}	0.25	1.0	V	VSync=300mV

T_A = 25 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		



Output Signals SDA (Open-Drain-Stage)

Parameter	Symbol	min.	max.	Unit	Test Condition
L-output voltage	V_{QL}		0.4	V	I_Q = 3.0 mA
Permissible output voltage			5.5	V	
Open-drain-resistance (SDA)	R_{SDA}	1.7	2.2	kΩ	max. 200pF load capacity
Open-drain-resistance (SCL)	R_{SCL}	1.7	2.2	kΩ	max. 200pF load capacity

PLL-Loop Filter Components

Parameter	Symbol	min.	max.	Unit	Test Condition
Resistance at PD1/VCO1	R	2.2	4.7	kΩ	
Resistance at PD2/VCO2	R	2.2	4.7	kΩ	
Capacitor at PD1/VCO1	C	68	220	nF	
Capacitor at PD2/VCO2	C	2,2	100	nF	

VCO – Frequence Range Adjustment

Parameter	Symbol	min.	max.	Unit	Test Condition
Resistance at IREF (for bias current adjustment)	R_4	68+/-5%		kΩ	

Input Signal Composite/Horizontal/Vertical-Sync

H-input voltage	V_{SyncH}	0.6xV_{DDD}	V_{DDD}	V	
L-input voltage	V_{SyncL}	0	0.2xV_{DDD}	V	

SECAM-bypass - bandpass filter

Coil at CVBS_OUT	L_1	10		uH	
Capacitor at SECAM-bypass	C_2	120		pF	

FSCin (1x/2x/4x)

Amplitude of FSCin-Signal peak to peak	$A(f_{SC})$	250	550	mV	
Coupling Capacitor	C	1	100	nF	

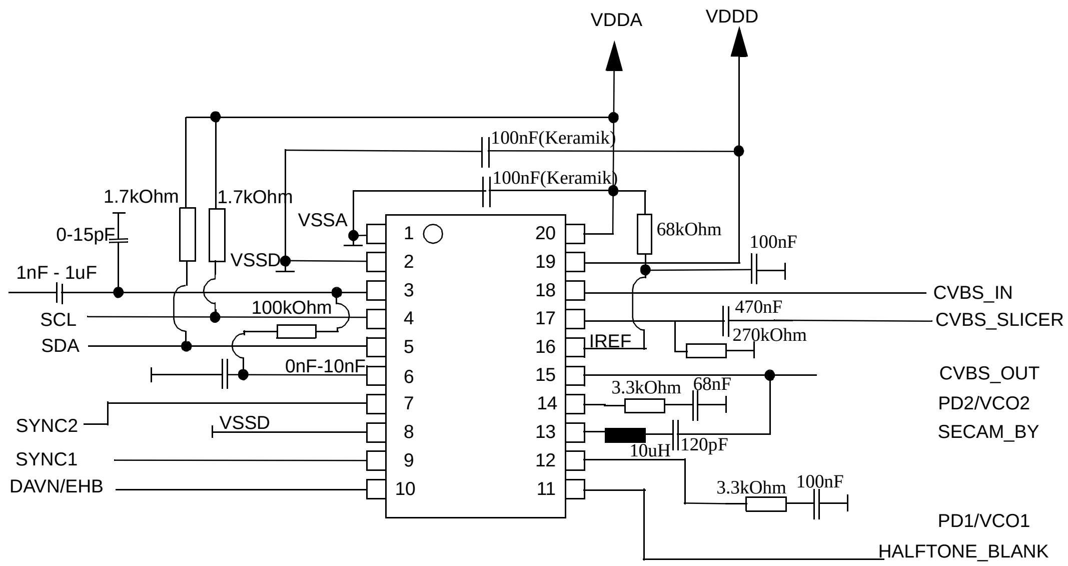
Clamp components on input CVBS-Slicer

Capacitor	C	330	1000	nF	
Resistance	R	220	270	kOhm	

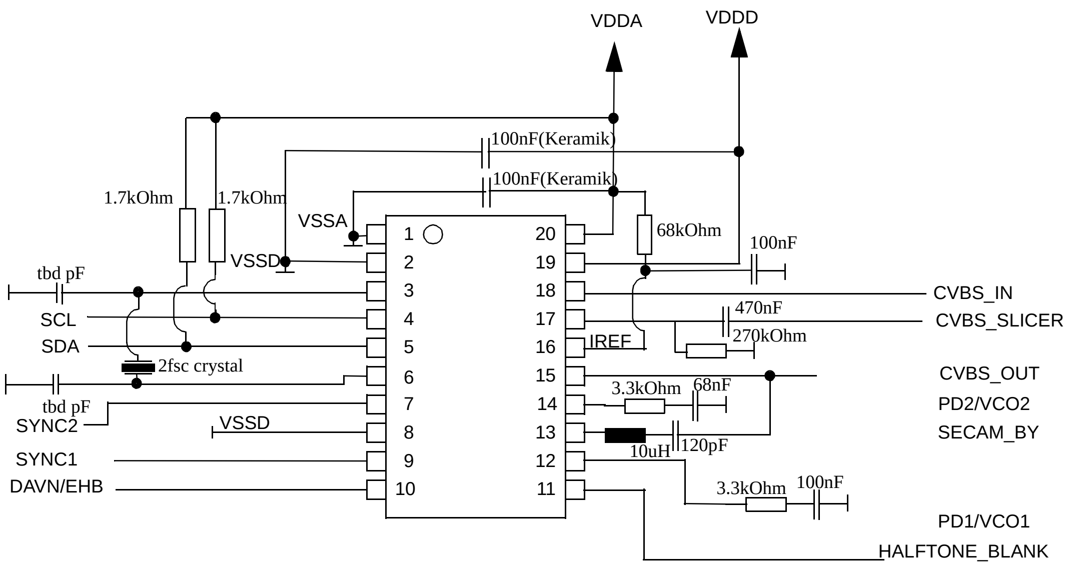
Crystal-Oscillator-Capacitances:

Capacitor	C	27		pF	
Crystal-impedance	R		30	Ohm	

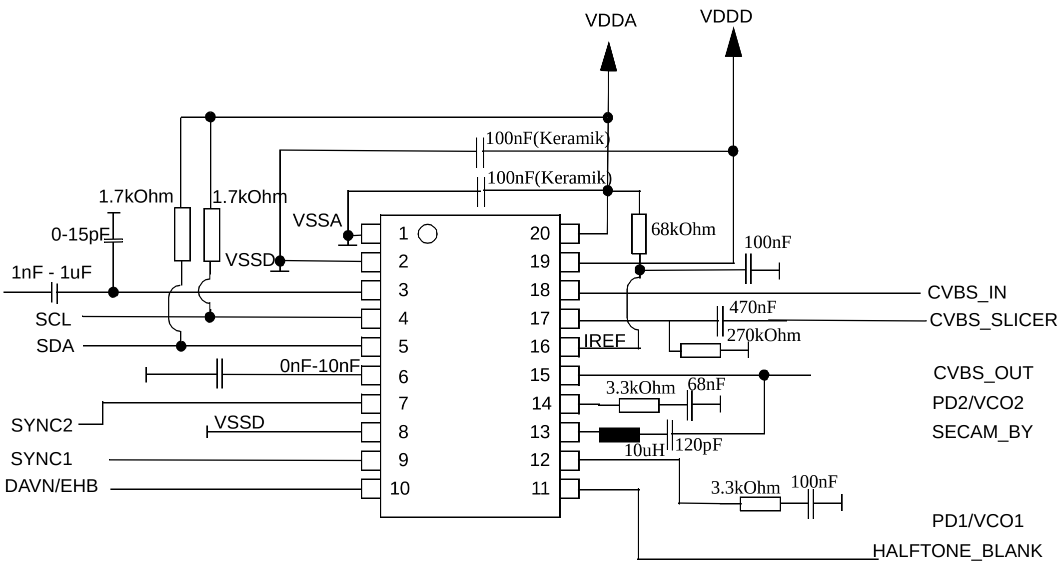
Environment for a system with 1fsc, 2fsc or 4fsc as external system-clock :



Environment for a system with a crystal-oscillator as system-clock:



Environment for a system with 2fsc as external system-clock in oscillator-mode 11:

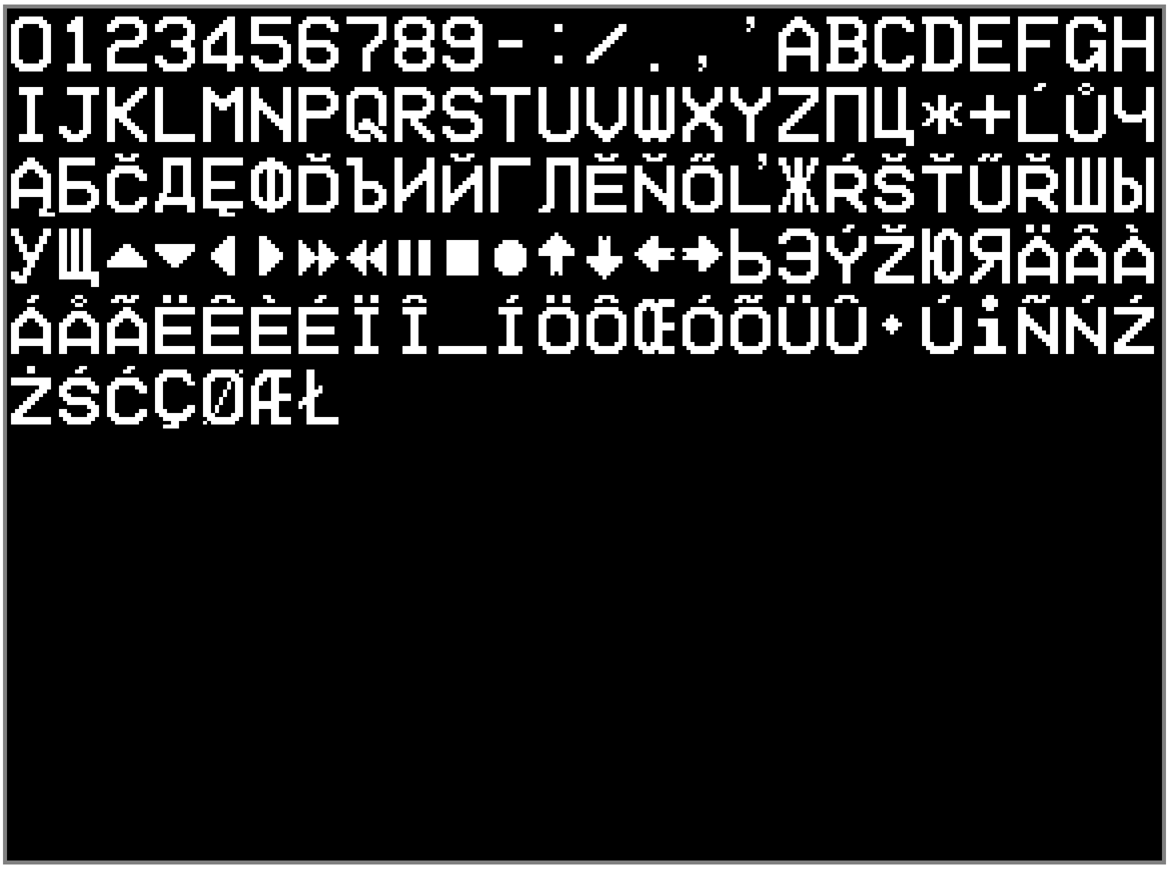


9. Character-ROM

In the character-ROM the shape of the characters is defined. 128 characters are stored in the ROM. Each character has got a structure ot 12columnsx18lines:

The pixel-structur of the characters shown in the figure above refer to character-adresses shown in the table below:

79	49	50	51	52	53	54	55	56	57	45	58	47	46	44	39	65	66	67	68	69	70	71	72
73	74	75	76	77	78	80	81	82	83	84	85	86	87	88	89	90	40	41	42	43	48	37	38
91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114
115	116	59	60	61	62	63	64	117	118	119	120	121	122	123	124	125	126	127	0	1	2	3	4
5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
29	30	31	33	34	35	36	32																



10. Application notes

10.1. After reset starting sequenz

After reset a maximum-time of 50us is needed in which the IC initializes itself. After this time, the following registers are set to their default-values:

ADR_POINTER_0,
ADR_POINTER_1,
DATA_PORT,
ACQ-Control
SYNCHRONISATION

and

LEVELS_AND_CHANGE.

All the other register-values are set to random-values and must be initialized with IIC-bus.

After the time of 50us, the first IIC-access can be executed.

Within the first IIC-bus-accesses the following procedure should be carried out:

Procedure 1:
The register-bits OSC_SYS0 and OSC_SYS1 of the register SYNCHRONISATION have to be set to the values according the used external clock-source (1FSC, 2FSC, 4FSC or crystal).

Procedure 2:

The bits OSC_SYS0 and OSC_SYS1 are read and compared to the expected values which have been written in procedure 1. By this it is assured, that there has been no transmission-error to the IC.

If there has been no transmission error please go on with procedure 3 otherwise please go back to procedure 1.

Procedure 3:

Setting bit RELEASE of register LEVELS_AND_CHANGE from high to low. This will initialize the internal clock-generation-circuits according to the settings of the bits OSC_SYS0 and OSC_SYS1. If once register-bit RELEASE ist set to 0 it cannot be set to 1 anymore.

Setting bit IIC_SWITCH of register SYNCHRONISATION from high to low. This will assure highest IIC-bus noise-surpressing.

11. Errata Sheet

Hardware Items

Item No.	Bug Designation	Description	Affected Version	Correction Schedule
H1	Wrong horizontal Start-Position of character-fields using zoom	The position of the characters of a row may be shifted to the left in dependency on: -horizontal zoom-factor of the 1st character in the zoomed row -k = modulo of the start-position of the character-field The dependencies are shown in the following table below (Clocks = Nr. of clocks by which the characters are moved to the left; pixel = Nr. of pixels by which the characters are moved to the left; pixel-frequency is half the clock-frequency):	B23	tbd

k / zoom	0		1		2		3	
	clocks	pixel	clocks	pixel	clocks	pixel	clocks	pixel
1	0	0	0	0	0	0	0	0
2	0	0	2	1	0	0	2	1
3	0	0	2	1	4	2	4	2
4	0	0	2	1	4	2	6	3

Item No.	Bug Designation	Description	Affected Version	Correction Schedule
H2	No display if horizontal start-position>118	If the horizontal start-position of the character-field is larger than 118, the character-field will vanish at all and there is an unexpected line at the beginning of the character-field. Uncritical for most applications, because such large horizontal start-positions aren't choosen in practise.	B23	tbd
H3	No display of row 14 at large vertical start-position	If the vertical start-position of the character-field is >100, row 14 will vanish. As for those large vertical start-positions row 14 shouldn't be visible on the screen of a normal TV-set at all, this should be uncritical for all applications.	B23	tbd

Item No.	Bug Designation	Description	Affected Version	Correction Schedule
H4	Row 8 at vertical zoom-factor “4”	If in row 8 zoom-factor “4” is used (and this row is visible on the screen), the next character-row will allready start at row 11 (instead of 12). Moreover row 14 will fail at all.	B23	tbd
H5	PDC-Format1 Byte 13	Byte 13 in PDC-mode Format 8-30-1 is falsely parity checked (e.g. the MSB is set to 1, if byte 13 hasn’t odd parity, else 0).	B23	tbd
H6	Forbidden vertical and horizontal start-positions of the character-field	The following vertical and horizontal start-positions are not allowed to use (due to different failures like an offset according to the expected start-position): 1. forbidden positions in fullpage-mode: VPOS = 0..16 HPOS = 0; HPOS != k*4; HPOS >=116 2. forbidden positions in mixed-mode: VPOS = 0.. 19; VPOS >100 HPOS = 0; HPOS != k*4; >=120	B23	tbd

Software/Firmware Items (optional)

Item No.	Bug Designation	Description	Affected Version	Correction Schedule

Software/Firmware Items (optional)

Item No.	Workaround Description
H5	Following algorithm can be used as a workaround for Item-No.H5: CASE MSB(byte13) IS 1: if byte13 (6:0) = even parity THEN MSB(byte13):=0; ELSE MSB(byte13):=1; end if; 0: if byte13 (6:0) = even parity THEN MSB(byte13):=1; ELSE MSB(byte13):=0; end if; END CASE;

Micronas GmbH
Hans-Bunte-Strasse 19
D-79108 Freiburg (Germany)
P.O. Box 840
D-79008 Freiburg (Germany)
Tel. +49-761-517-0
Fax +49-761-517-2174
E-mail: docservice@micronas.com
Internet: www.micronas.com

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