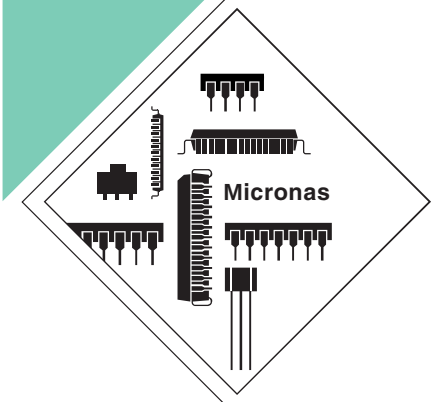

APPLICATION NOTE IC

SDA 55xx
TVText Pro
Design Guide

Edition Oct. 9, 2001
6251-556-1AN

MICRONAS

Contents

1. Introduction

The purpose of this application note is to give a brief overview of the most important hardware aspects of the TVText Pro, e.g. slicer performance, oscillator, and hardware design.

2. Device Overview

The following table gives an overview of all versions of the TVText Pro which are currently available.

Table 2–1: TVText Pro design step overview

Version	Type	Package	Design Steps
SDA 5550M	– ROMless version – 16 kByte RAM	PMQFP100	V0.1 (test chip) ES A11 (first silicon) ES A12 (1st redesign) ES A13 ES A14
SDA 5550	– ROMless version – 16 kByte RAM	PLCC84	ES A14
SDA 555XFL	– 128 kByte Flash memory on chip (re-programmable) – 16 kByte RAM	PSDIP52	V0.1 (test chip) ES A11 (first silicon) ES A12 ES A13 ES A14
		PMQFP64	ES A12 ES A14
SDA 555x x = 1...5	– 32-128 kByte user ROM – 8-16 kByte	PSDIP52	ES A14
SDA 5521	– OSD-only version – 32 kByte user ROM on chip – 6 kByte RAM	PSDIP52	ES A14
SDA 5522	– OSD-only version – 64 kByte user ROM on chip – 6 kByte RAM	PSDIP52	ES A14

3. Hardware Items

3.1. Filtering of Power Supply

The TVText Pro requires two different power supply voltages. The 3.3-V supply is used to drive all port pins and address/data lines. The 2.5 V is used for the CPU core and the analog units of the TVText Pro. It is important for the hardware designer to take special note of the stability and noise on the 2.5-V domain. To avoid interference on the power supply lines and improve the analog performance (e.g. slicer, ADC) of the TVText Pro, it is recommended to divide up the power supply into different sections, which are separated from each other by LC-filters. The number of power supply pins assigned to the different power supply sections depends on the package type of the TVText Pro. The tables below show pin assignments for the voltage domains in each of the four available package types.

Table 3–1: Power Sections (1)

Power Section	Supplied Module	PSDIP52		PMQFP64	
		VDD	VSS	VDD	VSS
2.5 V CORE	CPU, pad input stage	9, 42	10, 43	3, 44	4, 45
2.5 V ANALOG1	ADC, slicer, SC-Decoder	13	14	9	10
2.5 V ANALOG2	DAC (RGB), PLL, oscillator	37	36	37	36
3.3 V DIGITAL1	Port 0, Port 1, COR/BLANK	11, 44	10, 43	5, 46	4, 45
3.3 V DIGITAL2	VSYNC, Port 3, Port 4.2..3	30	29	29	28

Table 3–2: Power Sections (2)

Power Section	Supplied Module	PMQFP100		PLCC84	
		VDD	VSS	VDD	VSS
2.5 V CORE	CPU, pad input stage	6, 73	7, 74	14, 68	15, 69
2.5 V ANALOG1	ADC, slicer, SC-Decoder	22	23	26	27
2.5 V ANALOG2	DAC (RGB), PLL, oscillator	56	55	57	56
3.3 V DIGITAL1	Port 0, Address/Data, COR/BLANK, Port 1.7	8, 92, 75	7, 91, 74	1, 16, 70	84, 15, 69
3.3 V DIGITAL2	VSYNC, Port 3, Port 4.2..3, Port 1	40	39	43	42

3.2. Oscillator

In order to gain maximum slicer performance, a 6.000-MHz quartz crystal with a frequency tolerance of ±100 ppm (over all) should be used. This crystal is used to generate the CPU clock, screen pixel clock for OSD, sync. clock, and the clock frequency for the Teletext slicer. Resonator components (e.g. ceramic resonators) with higher tolerance may be used if the Teletext slicer is not used (e.g. in OSD-only application).

The recommended quartz crystal circuit is shown in Fig. 3–1. For quartz crystal applications, 33-pF capacitors should be used.

Important note: The connection to the analog GND (VSSA) should be as short as possible.

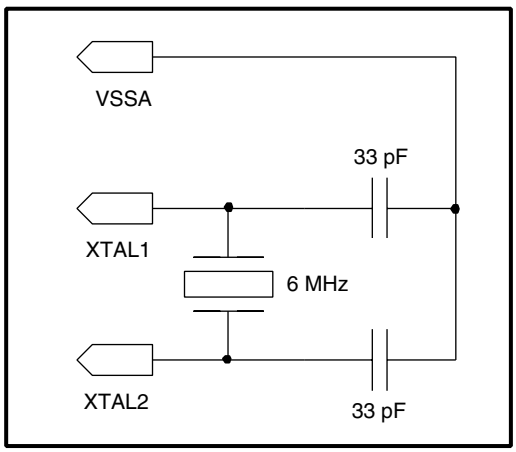

Fig. 3–1: Oscillator circuit

3.3. Slicer Performance

The performance of the Teletext slicer depends on several parameters. The performance of the slicer may be significantly improved if attention is paid to these parameters.

The digital slicer on the TVText Pro uses a fast analog-to-digital converter to digitize the CVBS signal. Noise and interference on the power supply to the slicer should be minimized by using filters and a large ground plane. In addition, analog signal lines should be shielded, for example by power lines.

- Place a ground plane under the TVText Pro device
- Note recommendations for filtering of power supply lines. In particular, the 2.5 V power supply voltage should be designed to be as stable and noise-free as possible
- Place a 100 nF capacitor (SMD) at each power supply pin pair, as close as possible to the device pins
- Note recommendations for the crystal oscillator design
- Keep fast switching signals (e.g. altering levels of port pins, address/data lines) away from CVBS signal and Port 2.
- The optimal CVBS amplitude is about 950 mV. The amplitude must be measured with a norm signal from H-Sync bottom to the maximum peak of the Clock-Run-In signal (CRI: first incoming pulses of a TEXTEXT signal).
- The maximum voltage level of the H-Sync or Sandcastle signal must not exceed 2.5 V
- To improve the slicer performance on signals which have a negative group delay component, an additional external group delay filter is recommended as described in the section "Group Delay Filter".

3.3.1. Group Delay Filter

The acquisition performance of the full data service slicer for CVBS signals with group delay ranging from 150 ns to 170 ns can be further improved by the addition of a filter in the CVBS signal path. This additional filter should add positive group delay compensation of approximately 60-80 ns; this will move the signal into a more optimal area for acquisition. Although the above is application-dependent (tuner & IF performance), the below circuit can be used to delay the CVBS signal by 60-80 ns in range from1 to 3.5 MHz.

The output of the filter must be connected by a serial 100-nF decoupling capacitor to the CVBS pin of the TVText Pro. The input of the filter must be from a CVBS source with an impedance less than 500 Ω. For fine adjustment of the filter output voltage, the resistor R1 may vary between 2.2 kΩ and 4.7 kΩ. This will also effect the group delay behavior slightly. A stable power supply voltage between 8 V and 9 V is recommended. The group delay response of the filter is shown in Fig. 3–3.

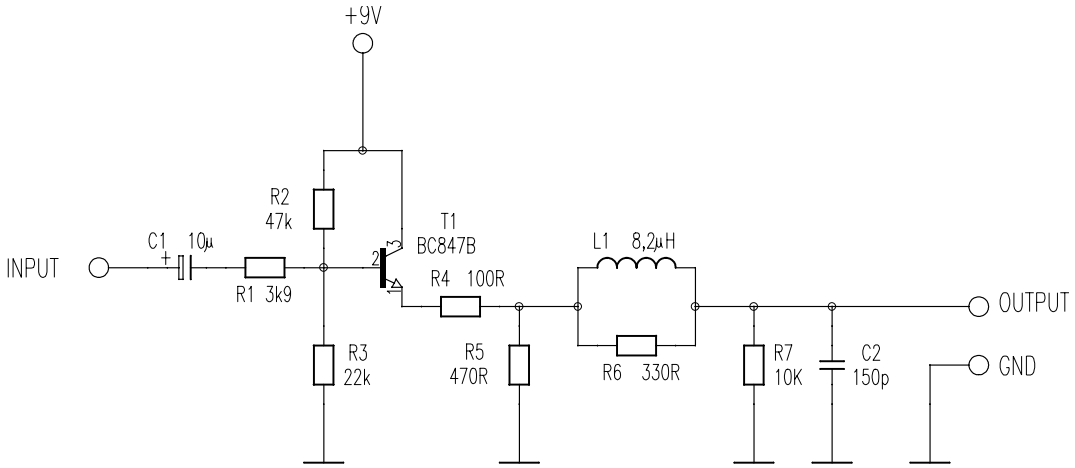

Fig. 3–2: Circuit diagram of a group delay compensation filter

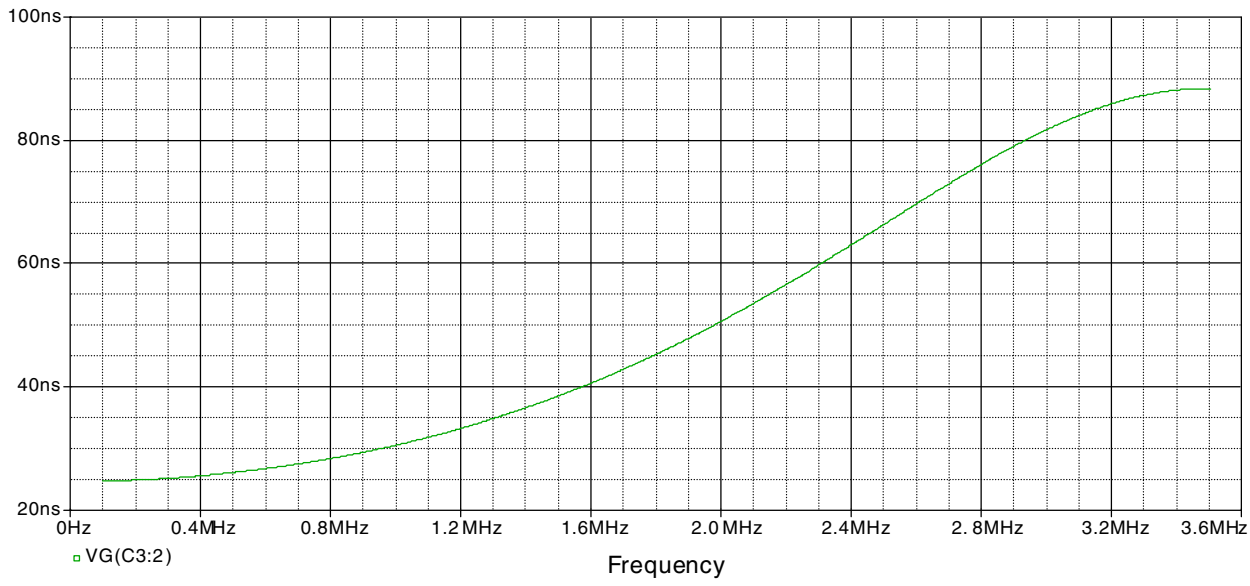

Fig. 3–3: Group delay response of the filter

How to adjust the correct CVBS amplitude

Fig. 3–4 shows a CVBS signal at the input of the group delay filter [1] and the signal at the output of the filter [2] resp. at the CVBS pin of the TVText Pro. The rear part of the H-sync, eight Clock-Run-In pulses, and the front part of the framing code of a TELETEXT line are visible. The signal amplitude at the filter input must be high enough (about 1.5 V) to enable an output voltage of 950 mV (as shown in Fig. 3–4) measured with CVBS signal from H-Sync bottom to the maximum peak of the Clock-Run-In signal (CRI: first incoming pulses of a TEXTEXT signal).

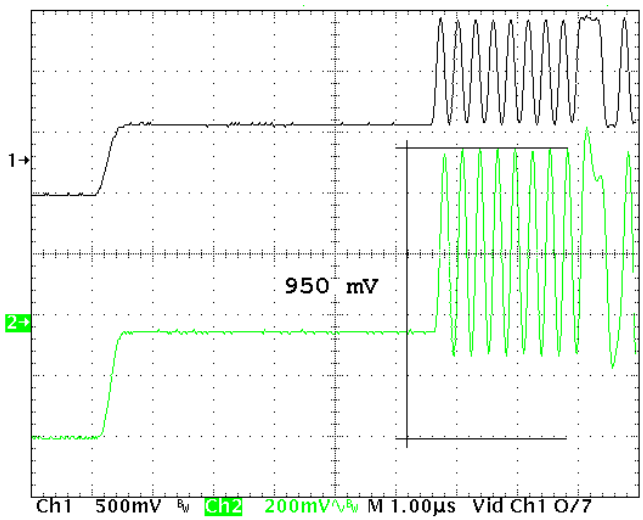

Fig. 3–4: Track 1: filter input signal /
Track 2: filter output signal (950 mV)

3.4. RGB Output

The RGB output of the TVText Pro can display 4096 color combinations. The maximum peak-to-peak amplitude (black-to-white level) can be set to 0.5 V, 0.7 V, 1.0 V, and 1.2 V. Because of a small non-linearity at the black level, 0.5 V and 0.7 V should not be used in high-end applications. For designs that require peak-to-peak amplitude of 0.5 V or 0.7 V, the output should be set to 1 V and a resistor voltage divider used. The load at each output must be greater than 5 kΩ.

3.5. Contrast Reduction

The TVText Pro has a three-level output pin for a combined BLANK and contrast reduction signal similar to the sandcastle signal, which also combines H-sync and V-sync together into one signal. This three-level COR-BLANK signal can be easily connected directly to Micronas' Deflection Controller with RGB Processor SDA 9380 (EDDC) to realize fast blanking and contrast reduction by using only one line.

After the TVText Pro is reset, the BLANK/COR pin is configured as BLANK output by default. The COR function is switched off. The COR-BLANK function must be switched on by software. If the application requires a separate BLANK and COR signal, an external decoder circuit is needed to separate the COR and the BLANK signal out of the three-level signal as shown in Fig. 3–6. An appropriate COR-BLANK decoder circuit is shown in Fig. 3–7.

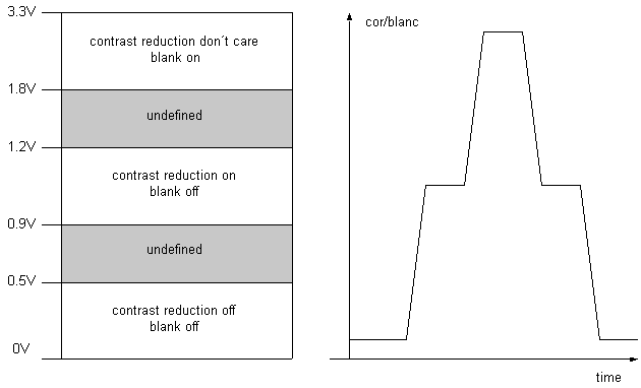

Fig. 3–5: Voltage level definition of COR-BLANK signal

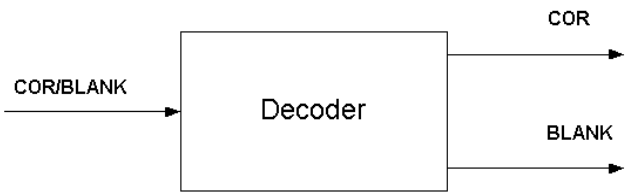

Fig. 3–6: COR-BLANK decoder

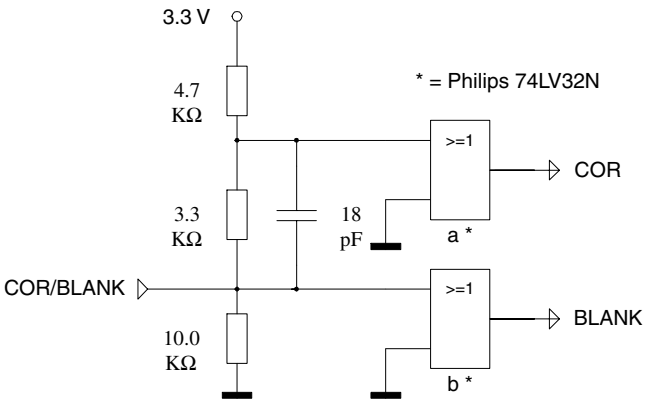

Fig. 3–7: Application circuit for COR-BLANK decoder

3.6. I²C Bus

The TVText Pro has no hardware I²C bus interface. The I²C bus protocol must be generated by software. The I²C bus output stages of the TVText Pro connected to the SCL and SDA lines must have an open-drain structure in order to perform the wired-AND function. Therefore, any pins of Port 0 of the TVText Pro may be used as I²C bus pins.

TVText Pro does not support I²C-specific I/O voltages, so care must be taken to ensure that the I²C bus voltage levels conform to the TVText Pro specification. Note especially that the input low voltage must be below 0.8 V.

To connect the I²C bus lines to I²C bus devices with 5-V interface, a voltage level shifter is needed. An example circuit for a level shifter using an SN7000/ SN7002 (Infineon) is shown in Fig. 3–8.

3.7. Application with 124 and 252 Pages Teletext

Fig. 3–9 and Fig. 3–10 are circuit diagrams for a 124 and 252 Teletext page application implemented using a ROMless TVText Pro in either a PLCC84 or a PMQFP100 package. Firmware for 1, 10, or 252-page Teletext acquisition can be obtained from Micronas. The 252-page Teletext acquisition firmware is scalable from 28 to 252 pages.

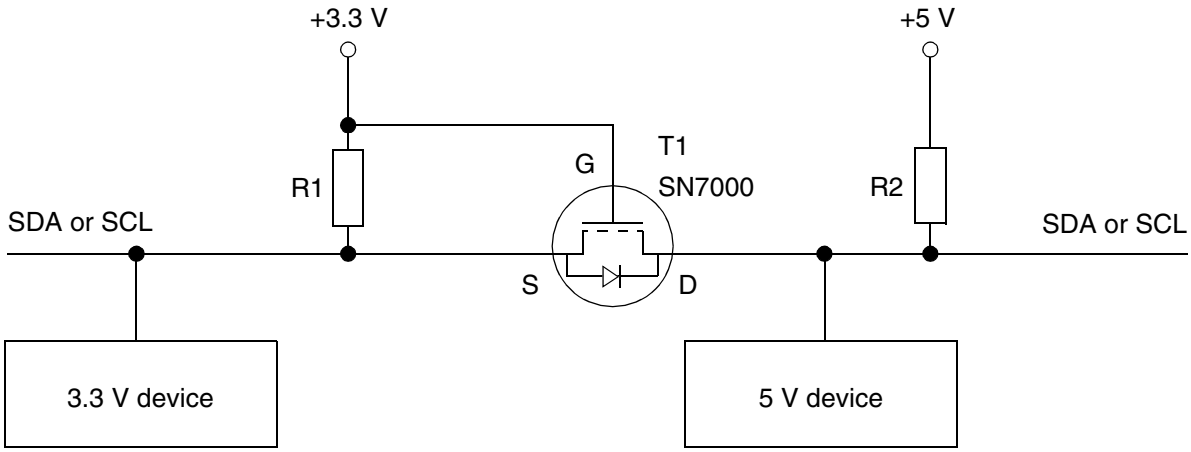

Fig. 3–8: I²C bus level shifter

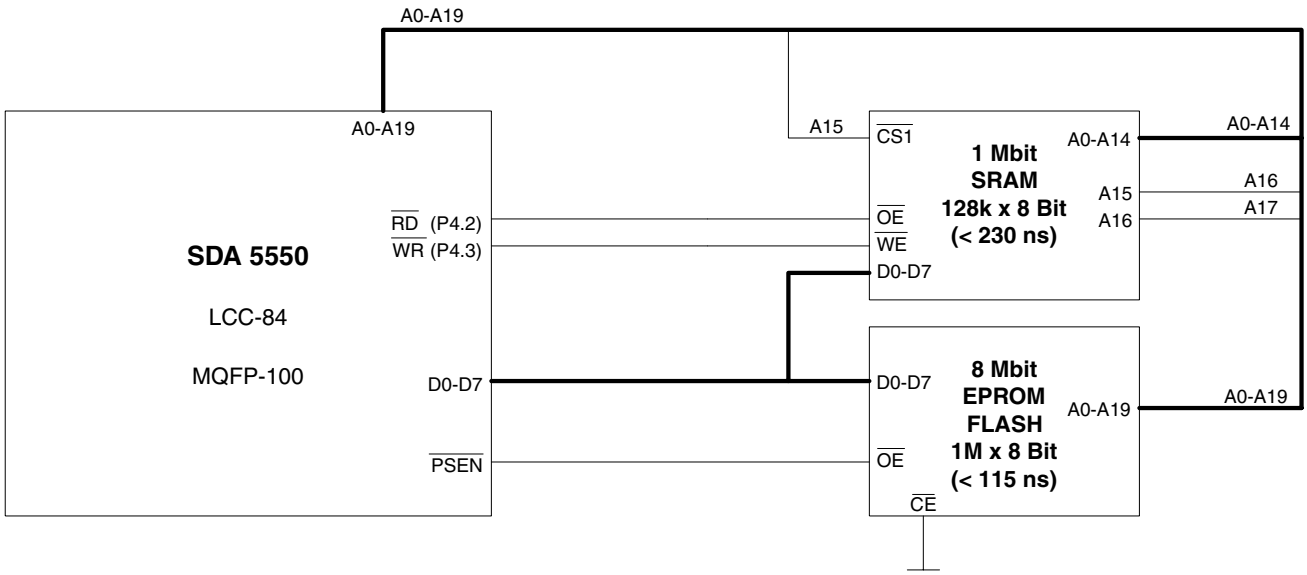

Fig. 3–9: 124-page Teletext application

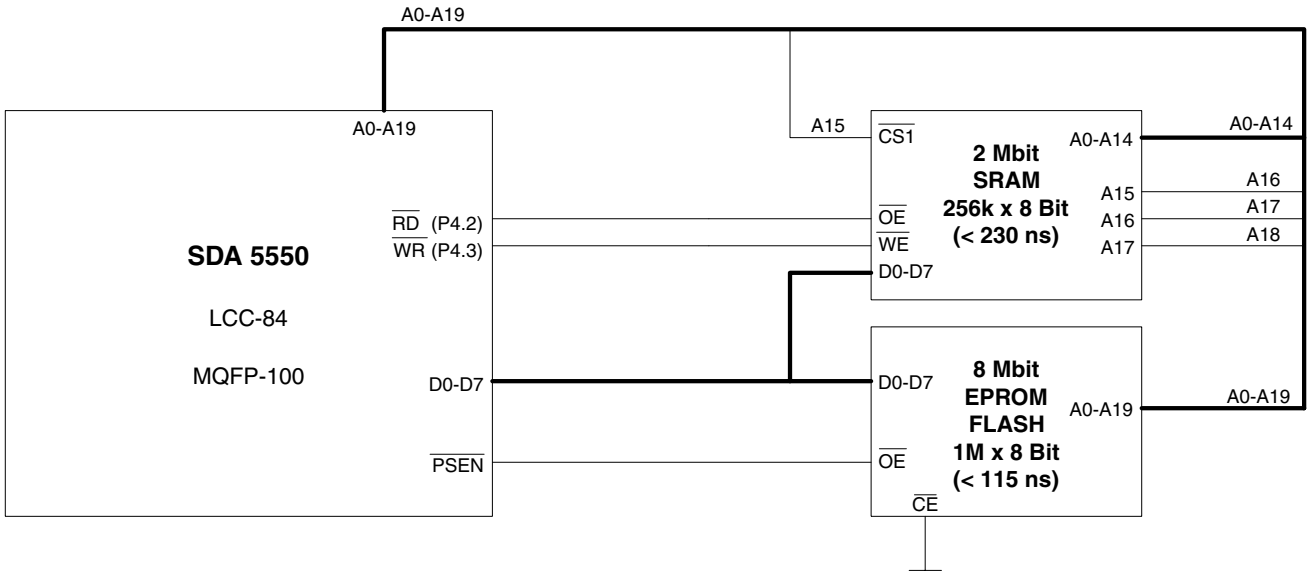

Fig. 3–10: 252-page Teletext application

3.8. Application Circuit

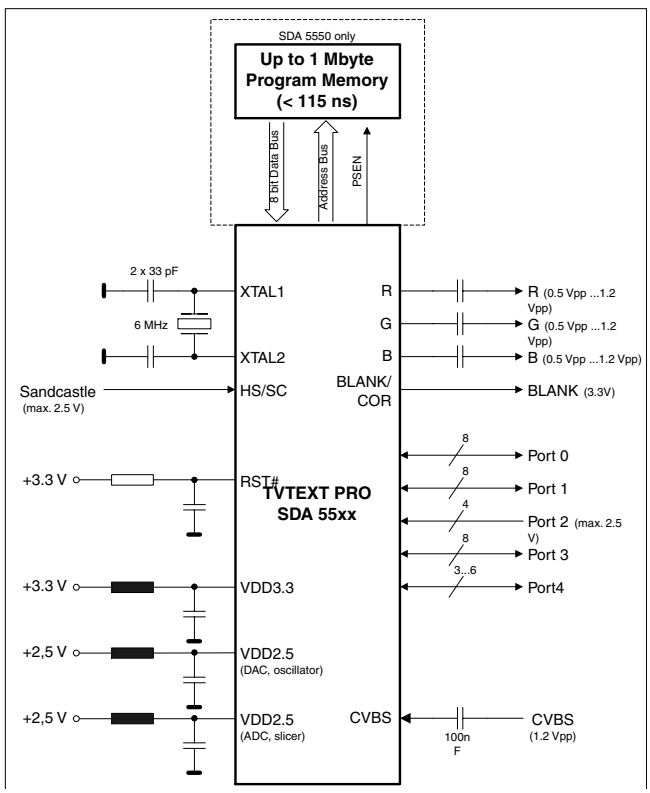

Fig. 3–11: Typical application

3.9. OSD-only Version (SDA 552x)

The OSD-only version of the TVText Pro provides the same features as the non OSD-only version with the below documented differences. The OSD-only has no

– Slicer and acquisition functionality

– Acquisition H-sync interrupt,

– Acquisition V-sync interrupt,

– Line23 interrupt,

– Channel change interrupt.

The functionality of your OSD-only software can be tested with a TVText Pro FLASH (SDA 555XFL) version by leaving the CVBS pin open. Of course, the test has to be done with the correct memory configuration, because the SDA 555XFL provides more memory than the OSD-only version.

3.10. Sync Master Mode

TVText Pro provides a sync master mode, where the H/V-sync signals are delivered by TVText Pro. These sync signals are not synchronized to any other signals like CVBS. The H/V sync master mode is enabled if the bit MAST in register SCR0 is set to “1”. The V-sync signal is delivered at the V-sync pin and the H-sync signal can be seen at P3.5 (instead of the H-sync pin). To enable the V-sync signal, the bits P4_7#_Alt and VS_OE# in register CSCR0 must also be set to “1”.

4. How to order 128-kByte ROM Mask

The BL51 code banking linker/locator takes the user-specified object files and library files and generates either an absolute object file or a banked object file. An absolute object file is generated for a none-code banking program. A banked object file is generated for a code banking program. The BL51 code banking linker/locator also generates a listing or map file.

Absolute object files may be converted into Intel HEX files by the OH51 Object-Hex Converter. Banked object files must be converted by the OC51 Banked Object File Converter into absolute object files (one for each bank) before they can be converted into Intel HEX files by the OH51 Object-Hex Converter (part of the KEIL Software Manual: 8051 Utilities).

Example of a none-code banking program (the code size is within 64 kByte):

Linking:
L51 @lk.dat (the linker output file is e.g. P073V180)

Object-Hex Converter:
OH51 p073V180

The ROM mask file is now: P073V180.hex

Example of a code banking program (code size is within 128 kByte or 2 banks):

Linking:
bl51 @blk.dat (the linker output file is e.g. P090V003)

Banked Object File Converter:
OC51 P090V003
The result is 2 files with the name P090V003.B00 and P090V003.B01

Object-Hex Converter Bank 0:
OH51 P090V003.B00
RENAME P090V003.hex P090V003.H00

Object-Hex Converter Bank 1:
OH51 P090V003.B01
RENAME P090V003.hex P090V003.H01

The ROM mask file0 for bank 0 (0-64kByte) is now: P090V003.H00
The ROM mask file1 for bank 1 (64-128kByte) is now: P090V003.H01

Please note:
The KEIL converters OH51 and OC51 from the compiler package 5 are DOS tools. Use Windows 3.11 directory and file naming conventions.

5. Development Tools

5.1. Flash Programming Tools for SDA 555XFL

There are two different programming systems for the flash version of TVText Pro: a single programming system and a gang programming system. The single programmer can be used for development purposes and pre-series with low quantities. The gang programmer is a modular programming system for production sites.

For further questions please contact ertec or refer to their Internet home page:

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Internet: http://www.ertec.com

5.2. OSD and Character Editor TEDI PRO

TEDI PRO is a software application for simulating the SDA 55xx display features and for editing SDA 55xx displays files on a PC running Microsoft Windows 95/98/NT. TEDI PRO is a powerful tool used to generate OSD-characters and OSD-menus, to export them, and to integrate them into the target application. Using the dual monitor feature, you can explore the features of the TVText Pro on a target system and evaluate the visual appearance of your OSD. Main focus is the easy handling of display objects such as fonts, colors, and register settings.

The current version of TEDI PRO is V1.02.1 (May 2000).

Required equipment for the Dual Monitor system together with SDA 55xx Evaluation Board:

– TEDI PRO software running on a PC under Microsoft Windows 95/98/NT
– LPT port of PC connected to target system e.g. TVText Pro Evaluation Board B010-V002 via parallel printer cable
– I2CSLAVE software running on TVText Pro

5.3. Emulation and Compiler

The same software tools (C51-Compiler, Linker/Locator and Assembler) used for TVText, TVText-2 or TVText Plus designs may be used for TVText Pro applications. The Teletext firmware object files provided by Micronas are compiled with tools from KEIL.

Other compilers are not supported.

The Kleinhenz emulator requires a KSC configurator (probe card) with TVText Pro, which can be used with a KSC X52 emulator. Suitable emulators are also available from HITEX (MX51-BH or AX51-H). The adapter probe is the modified type PVMUXCON.

Both emulators have been tested with up to two memory banks using the KEIL Compiler/Linker.

Table 5–1: Flash programming tools

System	No. of Devices	What is needed?	
Single Programming System PGS53	1	**PGS53A:** Base Set for DIP packages **AD555:** Adapter for SDA 555xFL in PSDIP52 package **AD555E:** Adapter for SDA 555XFL in PSDIP52 package and PMQFP64 package	
Gang Programming System PGS67	4-16	**PGS67001:** Base Set **PGS67673:** Module for 4 devices SDA 555xFL in PSDIP52 package	

6. Important Changes

6.1. Pin Configuration

The pin configuration of the PMQFP64 package has been modified from that shown in the SDA 55xx User's Manual Version 1.3 or older. The new pin configuration is shown in Fig. 6–1.

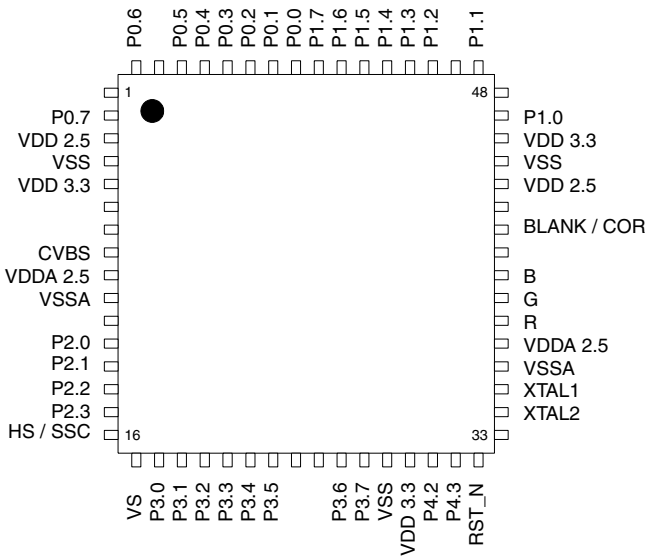

Fig. 6–1: Pin configuration of TVText Pro in PMQFP64

6.2. Memory Access Time

The access times for code and data memory have been changed from those shown in the SDA 55xx User's Manual Version 1.3 or older. The new timing values can be found in Table 6–1.

Table 6–1: Change of timing values

Page	Parameter	Old Value	New Value
226	t_{AVIV}	120 ns	115 ns
227	t_{AVDV}	240 ns	230 ns

This means, that the access times of the memory devices for the code memory (EPROM/Flash) must be less than 115 ns instead of 120 ns and for the data memory (SRAM) must be less than 230 ns instead of 240 ns.

7. Application Note History

1. Application Note “SDA 55xx TVText Pro Design Guide Version 1.0”, Edition June 7, 2000. First release of the application note.

2. Application Note IC: “SDA 55xx TVText Pro Design Guide”, Oct. 9, 2001, 6251-556-1AN. Second release of the application note IC. Major changes:

– In Table 2–1: OSD-only version added

– Section 3.3.: definition of "optimal CVBS amplitude" has been changed

– Section 3.3.1. Group Delay Filter added

– Section 3.9. OSD-only Version added

– Section 3.10. Sync Master Mode added

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