



POWER MANAGEMENT

Absolute Maximum Ratings

Parameter	Symbol	Maximum	Units
VCC to GND	V_{IN}	-0.3 to 7	V
PGNDH(L) to GND		± 1	V
BSTH(L) to PGNDH(L)		-0.3 to 15	V
Thermal Resistance Junction to Case	θ_{JC}	30	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	90	°C/W
Operating Junction Temperature Range	T_J	0 to 70	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C

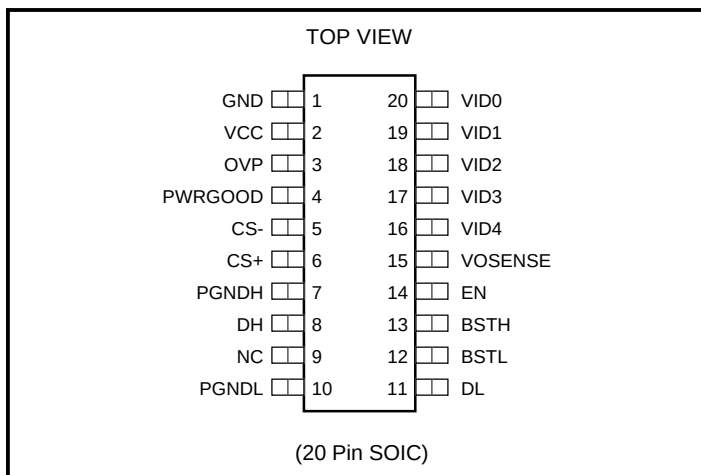
Electrical Characteristics

Unless specified: $V_{IN} = 4.75V$ to $5.25V$; GND = PGNDH = PGNDL = 0V; FB = V_O ; $0mV < (CS+ - CS-) < 60mV$; $T_J = 25^\circ C$

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	$I_O = 2A$	See Output Voltage Table			
Supply Voltage		4.2		7	V
Supply Current	$V_{IN} = 5.0V$		5		mA
Load Regulation	$I_O = 0.3A$ to $15A$		1		%
Line Regulation	All VID codes		0.5		%
Gain (A_{OL})	VOSENSE to VCCP		35		dB
Current Limit Voltage		60	70	80	mV
Oscillator Frequency		180	200	220	kHz
Oscillator Max Duty Cycle		90	95		%
DH Source/Sink Current	BSTH - DH = 4.5V, DH - PGNDH = 2V	1			A
DL Source/Sink Current	BSTL - DL = 4.5V, DL - PGNDL = 2V	1			A
OVP Threshold Voltage			120		.%
OVP Source Current	$V_{OVP} = 3V$	10			mA
Power Good Threshold Voltage		90		110	%
Dead Time		50	100		ns

Note:

(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

POWER MANAGEMENT
Pin Configuration

Ordering Information

Device ⁽¹⁾	Package	Temp Range (T _j)
SC1153CSW.TR	SO-20	0 to 125°C

Note:

(1) Only available in tape and reel packaging. A reel contains 1000 devices.

Pin Descriptions

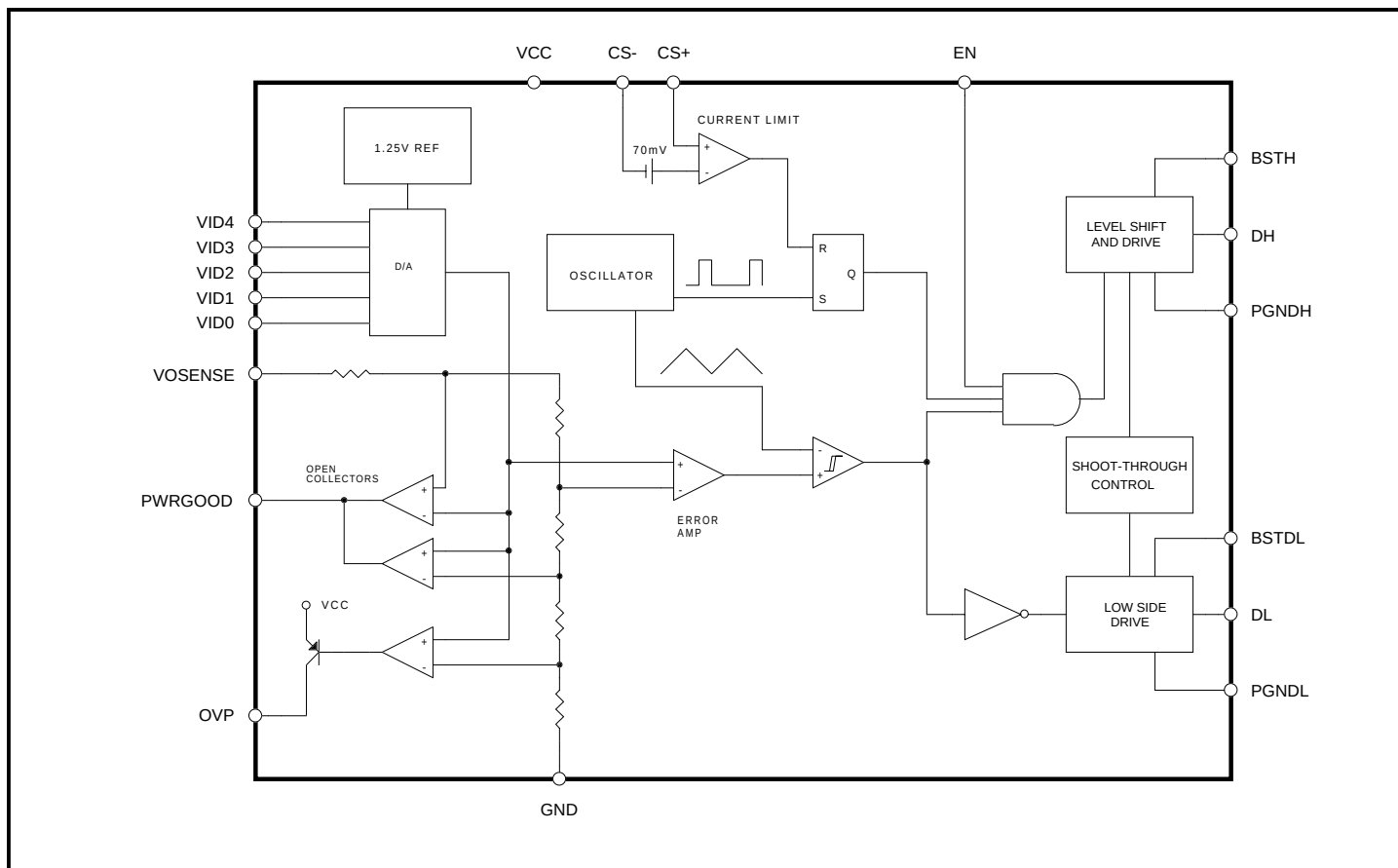
Pin #	Pin Name	Pin Function
1	GND	Small Signal Analog and Digital Ground
2	VCC	Chip Supply Voltage
3	OVP	High Signal out if V _o > setpoint + 20%
4	PWRGOOD ⁽¹⁾	Open collector logic output, high if V _o within 10% of setpoint
5	CS-	Current Sense Input (negative)
6	CS+	Current Sense Input (positive)
7	PGNDH	Power Ground for High Side Switch
8	DH	High Side Driver Output
9	NC	Not Connected
10	PGNDL	Power Ground for Low Side Switch
11	DL	Low Side Driver Output
12	BSTL	Supply for Low Side Driver (Boost)
13	BSTH	Supply for High Side Driver (Boost)
14	EN ⁽¹⁾	Enable, Logic low shuts down the converter
15	VOSENSE	Top end of internal feedback chain
16	VID4 ⁽¹⁾	Programming Input (MSB)
17	VID3 ⁽¹⁾	Programming Input
18	VID2 ⁽¹⁾	Programming Input
19	VID1 ⁽¹⁾	Programming Input
20	VID0 ⁽¹⁾	Programming Input (LSB)

NOTE:

(1) All logic level inputs and outputs are open collector TTL compatible.

POWER MANAGEMENT

Block Diagram



Applications Information - Theory of Operation

The voltage at the VOSENSE pin is applied, through the internal precision resistor feedback chain, to the inverting input of the error amplifier. The non-inverting input of the error amplifier is supplied with a DC voltage derived by the DAC from the internal trimmed bandgap voltage reference. The output of the error amplifier is compared to the triangular output of the internal oscillator to generate a fixed frequency, variable duty cycle pulse train. The internal oscillator uses an on-chip capacitor and precision trimmed current sources to set the frequency to 200 kHz.

The generated pulse train is gated with the output of the current limit latch and the inhibit signal to produce a drive

signal for the upper FET. It is also inverted to produce a drive signal for the lower FET. These FET drive signals are modified by the "shoot-through" control circuitry so that the top FET turn-on is delayed until the bottom FET has turned off, and visa-versa.

The current limit latch is set (ending the upper FET drive pulse early) if the current limit comparator indicates an overcurrent condition. The latch is reset at the start of each oscillator period.

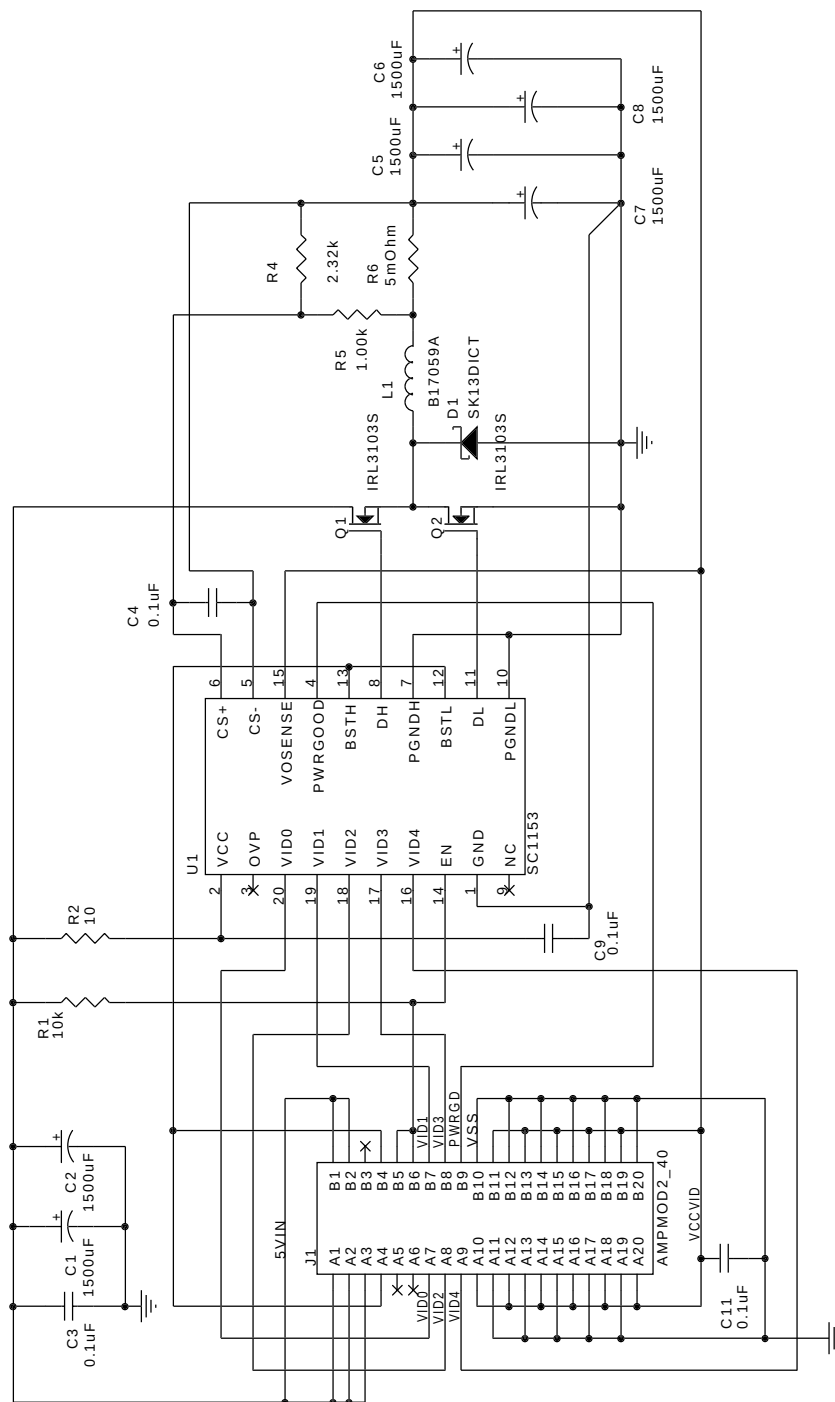
The PWRGOOD and OVP signals are derived from the voltage at the VOSENSE pin by comparators fed from the internal feedback chain.

POWER MANAGEMENT
Output Voltage Table

Unless specified: $V_{IN} = 4.75V$ to $5.25V$; $GND = PGNDH = PGNDL = 0V$; $FB = V_O$; $0mV < (CS+ - CS-) < 60mV$; $T_J = 25^\circ C$

Parameter	Conditions	VID 43210	Min	Typ	Max	Units
Output Voltage ⁽²⁾	$I_O = 2A$ in Application circuit	01111	1.287	1.300	1.313	V
		01110	1.336	1.350	1.364	
		01101	1.386	1.400	1.414	
		01100	1.435	1.450	1.465	
		01011	1.485	1.500	1.515	
		01010	1.534	1.550	1.566	
		01001	1.584	1.600	1.616	
		01000	1.633	1.650	1.667	
		00111	1.683	1.700	1.717	
		00110	1.732	1.750	1.768	
		00101	1.782	1.800	1.818	
		00100	1.832	1.850	1.868	
		00011	1.881	1.900	1.919	
		00010	1.931	1.950	1.969	
		00001	1.980	2.000	2.020	
		00000	2.030	2.050	2.070	
		11111	1.980	2.000	2.020	
		11110	2.079	2.100	2.121	
		11101	2.178	1.980	2.222	
		11100	2.277	2.300	2.323	
		11011	2.376	2.400	2.424	
		11010	2.475	2.500	2.525	
		11001	2.574	2.600	2.626	
		11000	2.673	2.700	2.727	
		10111	2.772	2.800	2.828	
		10110	2.871	2.900	2.929	
		10101	2.970	3.000	3.030	
		10100	3.069	3.100	3.131	
		10011	3.168	3.200	3.232	
		10010	3.267	3.300	3.333	
		10001	3.366	3.400	3.434	
		10000	3.465	3.500	3.535	

Evaluation Board Schematic (VRM)

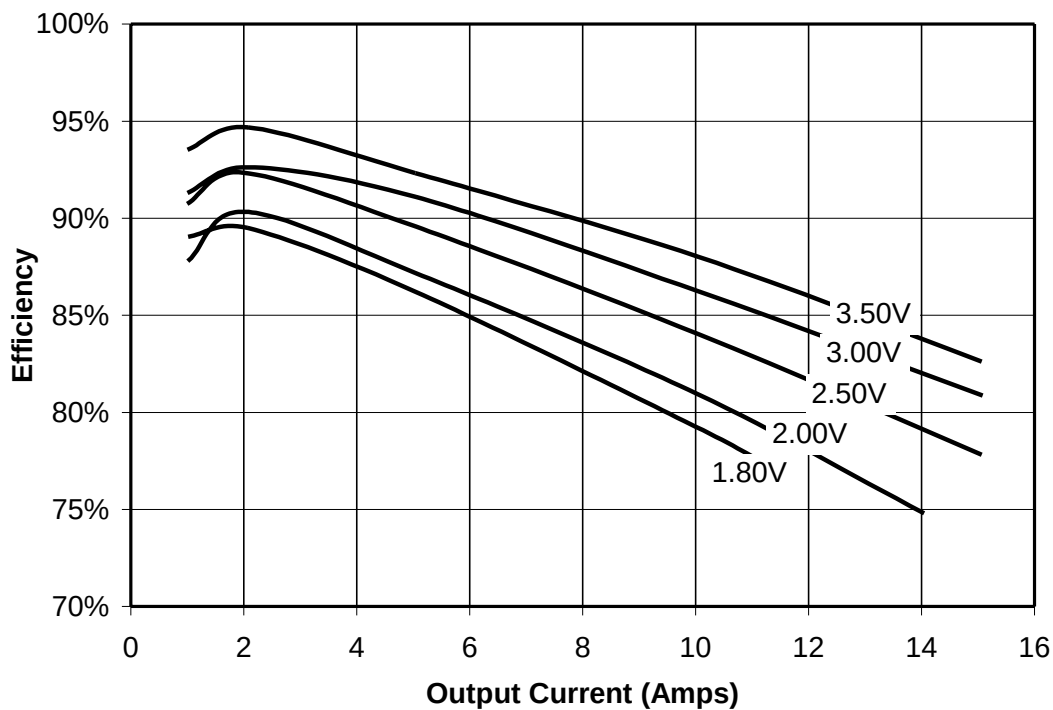


POWER MANAGEMENT
Evaluation Board Bill of Materials

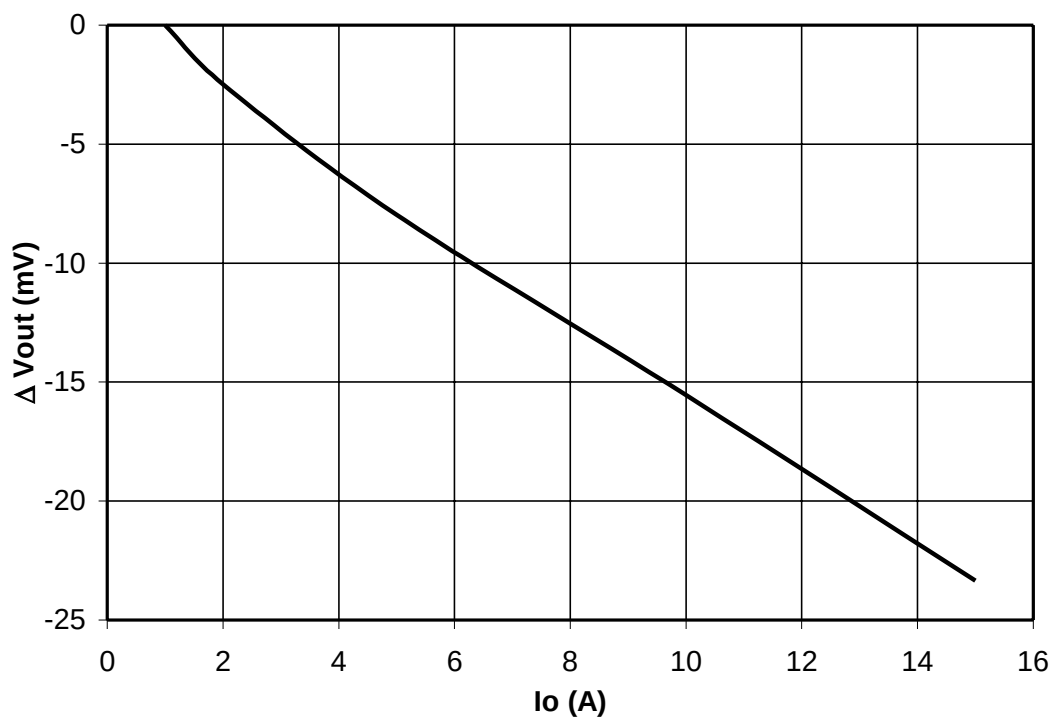
Item	Qty.	Reference	Value	Notes
1	6	C1,C2,C5,C6,C7,C8	1500uF	Low ESR Sanyo MV-GX or equivalent
2	4	C3,C4,C9,C11	0.1uF	
3	1	D1	SK13DICT	
4	1	J1	AMPMOD2_40	
5	1	L1	4uH	8 Turns 16AWG on MICROMETALS T50-52D core.
6	2	Q1,Q2	IRL3103S	
7	1	R1	10k	
8	1	R2	10	
9	1	R4	2.32k	1%
10	1	R5	1.00k	1%
11	1	R6	5mOhm	IRC OAR1
12	1	U1	SC1153	SEMTECH

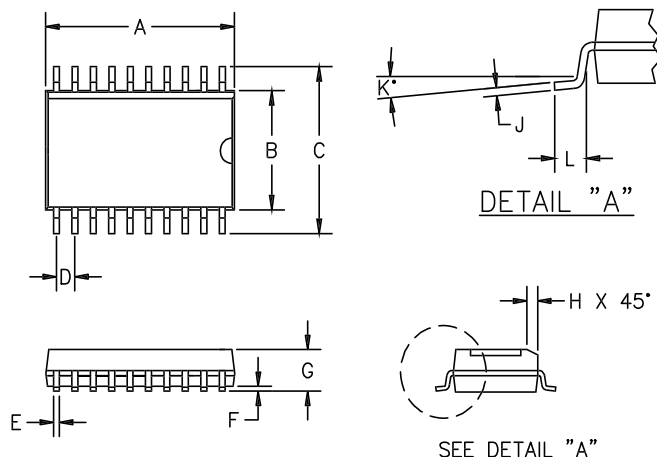
POWER MANAGEMENT
Typical Characteristic Curves

SC1153 Efficiency in Application Circuit



SC1153 Regulation in Application Circuit

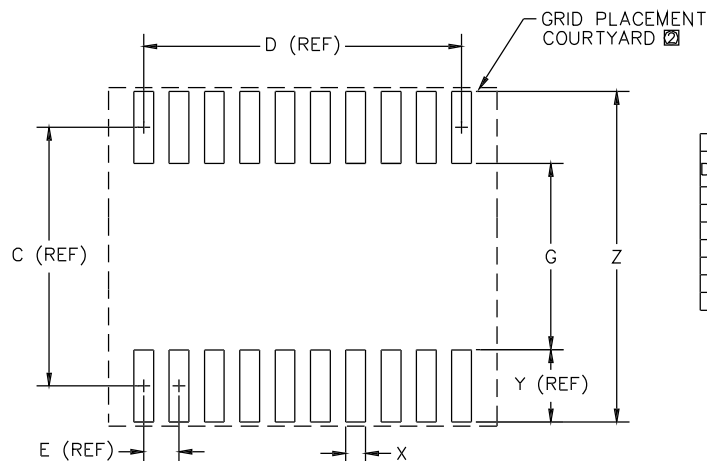


POWER MANAGEMENT
Outline Drawing - SO-20


DIMENSIONS ①					
DIM ^N	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.496	.512	12.6	13.0	②
B	.291	.299	7.40	7.60	②
C	.394	.419	10.0	10.65	—
D	.050	BSC	1.27	BSC	—
E	.013	.020	0.33	0.51	—
F	.004	.012	.10	.30	—
G	.092	.104	2.35	2.65	—
H	.010	.030	.25	.75	—
J	.009	.013	.23	.32	—
K	0°	8°	0°	8°	—
L	.016	.050	.40	1.27	—

② DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTUSIONS

① CONTROLLING DIMENSION : MILLIMETERS.

Land Pattern - SO-20


DIMENSIONS ①					
DIM ^N	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	—	.362	—	9.20	—
D	—	.45	—	11.43	—
E	—	.05	—	1.27	—
G	.260	.268	6.60	6.80	—
X	.02	.03	.60	.80	—
Y	—	.102	—	2.60	—
Z	.457	.465	11.60	11.80	—

② GRID PLACEMENT COURTYARD IS 28 X 24 ELEMENTS (14mm X 12mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

① CONTROLLING DIMENSION: MILLIMETERS.

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