Enhanced Serial Communication Controller (ESCC8)

SAB 82538

General Description

The Enhanced Serial Communication Controller ESCC8 (SAB 82538) is a data communication device with eight serial channels. It has been designed to implement high speed communication links and to reduce hardware and software overhead needed for serial synchronous/asynchronous communications.

The version 82538 H-10 of the ESCC8 opens a wide area for application which use time division multiplex methods (e.g. time-slot oriented PCM systems, systems designed for packet switching, ISDN applications).

General Features

Serial Interface

- Eight independent full-duplex serial channels
- On-chip clock generation or external clock source
- On-chip DPLL for clock recovery of each channel
- Eight independent baud rate generators
- Independent time-slot assignment for each channel with programmable time-slot length (1 - 256 bits)
- Async., sync. character oriented (MONOSYNC BISYNC) or HDLC/SDLC modes (including SDLC LOOP)
- Transparent receive/transmit of data bytes without framing
- NZR, NRZI, FM and Manchester encoding
- Modem control lines ($\overline{RTS}$, $\overline{CTS}$, CD)
- CRC support:
  – HDLC/SDLC: CRC-CCITT or CRC-32 (automatic handling for transmit/receive direction)
  – BISYNC: CRC-16 or CRC-CCITT (support for transmit direction)
- Support of bus configuration by collision detection and resolution
- Statistical multiplexing
- Continuous transmission of 1 to 32 bytes possible
- Programmable preamble (8 bit) with selectable repetition rate (HDLC/SDLC and BISYNC)
- Data rate up to 10 Mbit/s
- Master clock mode with data rate up to 4 Mbit/s

Applications

- Universal, multiprotocol communication board
- Asynchronous and synchronous terminal cluster controllers
- LAN gateways and bridges
- Multiplexers, cross-connect points, DMI boards
- Time-slotted packet networks
- Packet switches, packet assemblers/disassemblers

Type	Package	Max. Data Rate Clocked		Time-Slot Mode
		ext.	int. (DPLL)	
SAB 82538-H	P-MQFP-160-1	2 Mbit/s	2 Mbit/s	no
SAB 82538-H-10	P-MQFP-160-1	10 Mbit/s	2 Mbit/s	yes

Protocol Support (HDLC / SDLC)

- Various types of protocol support depending on operating mode
  – Auto-mode (automatic handling of S- and I-frames)
  – Non-auto mode
  – Transparent mode
- Handling of bit-oriented functions
- Support of LAPB / LAPD / SDLC / HDLC protocol in auto-mode (I- and S-frame handling)
- Modulo 8 or modulo 128 operation
- Programmable time-out and retry conditions
- Programmable maximum packet size checking

MP Interface and Ports

- 64-byte FIFOs per channel and direction (byte or word access)
- 8/16-bit microprocessor bus interface (Intel or Motorola type)
- All registers directly accessible (byte and word access)
- Efficient transfer of data blocks from/to system memory via DMA or interrupt request
- Support of Daisy Chaining and Slave Operation with Interrupt Vector generation
- 28-bit programmable universal I/Os

Block Diagram