SIEMENS

ICs for Communications

Enhanced Serial Communication Controller with 8 Channels ESCC8

SAB 82538

SAF 82538

Versions 3.1

Delta Sheet 02.97

T8253-8V31-L2-7600

SIEMENS

Enhanced Serial Communication Controller with 8 Channels
ESCC8

SAB 82538
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CMOS

This document describes the latest ESCC8 (Versions 3.1) in relation to the Version V2.2 and hence is a **"Delta Sheet"** which references the **ESCC8 User´s Manual 03.95**. The full data sheet will be developed in due course.

The **ESCC8 Versions 3.1** additionally offers:

1) Selectable enhanced resolution baud rate generator
2) Selectable out-of-band flow control for transmitter and receiver in ASYNC mode
3) In-band flow control transparency
4) Higher transfer rate of the HDLC controller

1 New Features

1.1 Selectable enhanced resolution baud rate generator

Two features are provided to allow the ESCC8 to work with higher XTAL rates and support higher transmission baud rates. The first is XTAL clock divide-by-4 logic and the second is the enhanced Baud Rate Generator (see also the BRG register description).

XTAL1-2 clock divide-by-4 function may optionally be selected (CCR4:MCK4) to feed the core logic and timer blocks. This allows the device to function with XTAL frequency up to 30 MHz. The baud rate generator is fed directly from the XTAL and can thus be used to provide clocks for baud rates in excess of 2 Mbaud (to be characterized) in ASYNC over-sampling mode. It also allows the timer block to operate at the highest resolution. See also description for CCR4 and TIMR registers.

The enhanced baud rate generator has two modes of operation for added flexibility. The **normal mode** is as in previous versions of the device. For the **enhanced mode**, the Baud Rate generator bits BR9-BR0 are re-assigned to provide two stages of division.

The first stage divides the clock by integer number up to 63, whereas the second stage allows further division by powers of 2 (1, 2, 4, 8, 16, 32, 64, .. 32768). See also description of the BRG register.

The Appendix shows baud rates derived from typical XTAL frequencies using the two modes of the baud rate generator.

1.2 Selectable out-of-band flow control for transmitter and receiver in ASYNC mode

Transmitter

The transmitter output is enabled if $\overline{CTS}$ signal is LOW OR the recognition of the XON characters (if MODE:FLON=1). If the MODE:FLON=0, then the transmitter is only enabled when the $\overline{CTS}$ signal is LOW. Setting the **MODE:FCTS=1 allows the transmitter to send data independent of the condition of the $\overline{CTS}$ signal,** the in-band flow control (XON-XOFF) method would still be operational if MODE:FLON=1.

Receiver

For some applications it is desirable to provide means of out-of-band flow control to indicate to the far end transmitter that the local receiver's buffer is getting full.

This flow control can be used between two DTEs as shown in figure 1 and between a DTE and a DCE (MODEM) as shown in figure 2 that supports this kind of bi-directional flow control.

Setting **MODE:FRTS=1** and MODE:RTS=0 invokes this out-of-band flow control for the receiver. When the shadow part of RFIFO has reached a set threshold of 28 bytes, the $\overline{RTS}$ signal is forced inactive (HIGH). When shadow part of the RFIFO is empty, the $\overline{RTS}$ is re-asserted (LOW). Note that the data is immediately transfered from the shadow RFIFO to the user accessible RFIFO (as long as there is space available). So when the shadow RFIFO reaches 28 bytes threshold, there is 4 more byte storage available before overflow can occur. This allows sufficient time for the far end transmitter to react to the change in the $\overline{RTS}$ signal and stop sending more data.

Figure 1 shows the connection between two ESCC8 Versions 3.1 devices as DTEs. The /RTS_A of DTE_A (ESCC8) feeds the /CTS_B input of the second DTE_B (another ESCC8). For example while DTE_A is receiving data and its receiver RFIFO threshold is reached, the /RTS_A signal goes inactive (HIGH) forcing the /CTS_B to become inactive indicating to DTE_B to stop transmitting. Both DTE devices should also be using the /CTS signal to flow control their transmitters. When the shadow RFIFO in DTE_A is cleared the /RTS_A goes active LOW and this signals the far end to resume transmission. Data flow control from DTE_B to DTE_A works in a similar way.

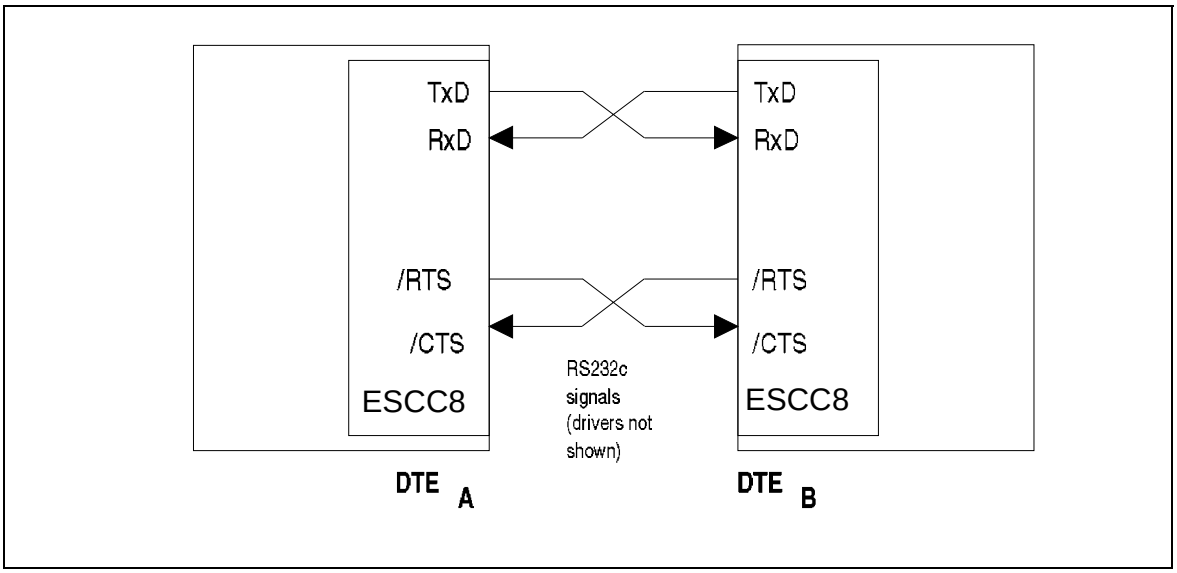

Figure 1
Out-of-Band DTE-DTE Bi-directional Flow Control

Figure 2 shows an ESCC8 as a DTE connected to a DCE (MODEM equipment). The /RTS_A feeds the /RTS_B input of the DCE (MODEM equipment) that supports bi-directional flow control. So when the DTE_A's receiver threshold is reached, the /RTS_A signal goes inactive HIGH which is sensed by the DCE and it stops transmitting. Similarly if the DCE's receiver threshold is reached, it deactivates the /CTS_B (HIGH) and causes the DTE to stop transmitting. These type of DCEs have fairly deep buffers to ensure that it can continue to receive data from the line even though it is unable to pass the data to the DTE for short periods of time. Note that a ESCC8 (Versions 3.1) can also be used in the DCE equipment as shown. Exchange of signals (e.g. /RTS to /CTS) is necessary inside the DCE equipment.

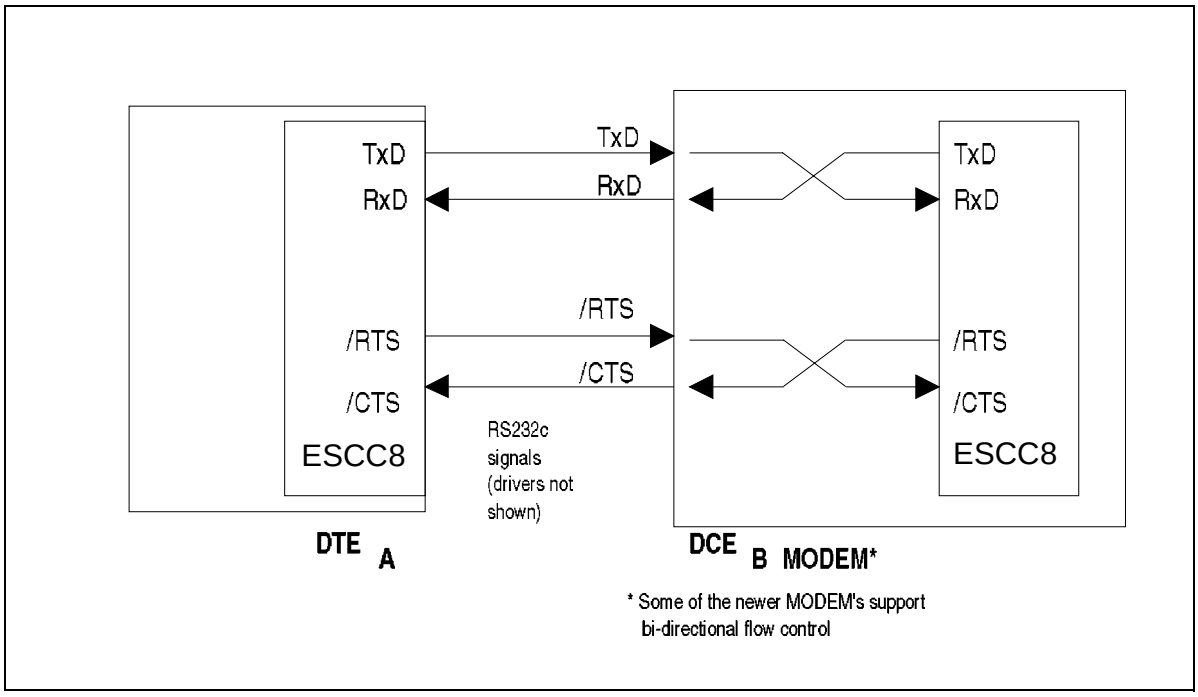

Figure 2
Out-of-Band DTE-DCE Bi-directional Flow Control

/RTS and /CTS are used to indicate when the local receiver's buffer is nearly full. This alerts the far end transmitter to stop transmitting.

The combination of transmitter and receiver out-of-band control features mentioned above enables data to be exchanged between two devices without software intervention for flow control.

1.3 In-band flow control transparency

In ASYNC mode optionally in-band flow control is provided with the XON/XOFF characters.
If MODE:FLON bit =1 then the transmitter output is controlled based on recognition of the XON/XOFF characters at the receiver.

A new optional function 'Disable XON/XOFF Storage' bit (DXS) in the RFC register is used to determine if the received in-band flow control characters (XON/XOFF) are to be stored in the RFIFO or to be removed from the incoming data stream. **Setting the control bit RFC:DXS=1 (in conjunction with MODE:FLON=1) causes the XON/ XOFF received characters to be discarded.** Normally with RFC:DXS=0 (and on RESET condition) the received XON/XOFF characters are stored in the RFIFO along with the data.

1.4 Higher transfer rate of the HDLC controller

All basic versions of the ESCC8, SAB 82538 and SAF 82538, support in HDLC mode the transfer rate of up to 2.048 Mbit/s.

2 Registers Description

Some register changes are available in ASYNC mode only. These are the features in the MODE & RFC registers. Other features in BRG, TIMR & CCR4 registers are available in HDLC, BISYNC & ASYNC modes.

MODE Mode Register (Read / Write) - ASYNC MODE only

This register has some new bits defined to access new features. These are indicated below.

Value after RESET: 00H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	**FRTS**	**FCTS**	FLON	RAC	RTS	TRS	TLP

FCTS... Flow control using /CTS

0.. (default) the transmitter is stopped if /CTS signal is HIGH. See section on out-of-band flow control.

1.. the transmitter is active continuously and disregards the condition of $\overline{\text{CTS}}$ signal. If MODE:FLON=1 then flow control is provided by using XON/XOFF characters.

FRTS.. Flow control using /RTS

This bit is used in combination with the RTS bit as follows:

FRTS	**RTS**	
0	0	The /RTS pin is controlled by the device autonomously and is activated (/RTS=LOW) when transmission starts and deactivated when transmission has been completed.
1	0	/RTS pin is controlled by the device autonomously for Bi-directional flow control and is forced active when shadow part of RFIFO is empty and forced in-active (/RTS=HIGH) when the RFIFO has reached a threshold. (See section on out-of-band flow control)
0	1	By setting this combination, the software can force the /RTS pin to active state (LOW).
1	1	By setting this combination, the software can force the /RTS pin to inactive state (HIGH).

TIMR Timer Register (Read / Write) - HDLC, ASYNC, BISYNC modes

TIMR Timer Register (Read/Write) is unchanged. However the input to the Timer function can be optionally selected to be XTAL/4 in Master clock mode by setting CCR0:MCE=1 and CCR4:MCK4=1.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CNT			VALUE				

VALUE.. (5 bits) sets the time period t1 as follows:

With CCR4:MCK4 = 0 & default condition, the timer value is given by the equation
t1 = k x (VALUE + 1) x TCP
where
- k is the timer resolution factor which is either 32768 (if MODE:TRS=0) or 512 (if MODE:TRS=1) clock cycles.
- TCP is the clock period of the Timer Clock Period.

Non Master Clock Mode (CCR0:MCE=0)

Timer Clock Period (TCP) = Transmit Clock Period

Master Clock Mode (CCR0:MCE=1)

if CCR4:MCK4 = 0 (Reset state)
Timer Clock Period (TCP) = XTAL Clock Period

if CCR4:MCK4=1
Timer Clock Period (TCP) = XTAL Clock Period / 4

With CCR4:MCK4 = 1 in master clock mode, XTAL clock divide-by-4 is fed to the Timer block. The XTAL clock feeds the baud rate generator which is used to select the transmit and received baud rate and generates the 16x over sampling clock. By this means, a XTAL clock of 30 MHz can be used while maintaining the Core logic’s clock operation limit of 10 MHz.

CNT.. (3 bits)

The CNT function is unchanged.

RFC, RFIFO Control Register - ASYNC mode only

This register has some new bits defined to access new features. These are indicated below.

Value after RESET: 00H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	DPS	**DXS**	RFDF	RFTH1	RFTH0	0	TCDE

DXS.... Disable storage of XON/XOFF characters

0... (default) All received characters, including XON, XOFF are stored in the RFIFO.
1... Any received XON/XOFF characters will not be stored in the RFIFO.

CCR4 Channel Configuration Register 4 - HDLC, ASYNC, BISYNC modes

Value after RESET: 00H,

a) **HDLC** Mode

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
MCK4	**EBRG**	**TST1**	**ICD**	0	0	RFT1	RFT0

b) **ASYNC, BISYNC** Mode

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
MCK4	**EBRG**	**TST1**	**ICD**	0	0	0	0

MCK4 - Master Clock divide-by-4

0... (default) XTAL 1-2 clock feeds the core logic and timer blocks. This causes the XTAL frequency to be restricted to 10 MHz, thus limiting the highest baud rate to about 600 Kbit/s, when transmission clock is derived from XTAL clock devided by 16.

1... XTAL 1-2 clock divide-by-4 feeds the core logic and timer blocks. This allows the device to function with XTAL frequency up to 30 MHz. The baud rate generator is fed directly from the XTAL. It also allows the timer block to operate at the highest resolution.

EBRG - Enhanced Baud Rate Generator Mode

0.. (default) selects standard baud rate generator operation. See description of BRG register.

1.. selects Enhanced baud rate generator. See description of BRG register.

TST1 Test Pin

Write 0 for normal operation.

ICD - Invert polarity of Carrier Detect signal

0..(default) selects the current polarity for Carrier Detect CD (Active HIGH)

1.. selects the invert polarity to be more consistent with other equipment, Carrier Detect $\overline{CD}$ (Active LOW).
As CD is a multifunctional pin, the ICD bit may only be set if CD functionality is being used.

RFT - RFIFO Threshold Level

Refer to the User's Manual 03.95, page 153.

VSTR Version Status Register (Read)

Value after RESET: x000vvvv

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CD	DPLA	0	0	VN3	VN2	VN1	VN0

VN3- VN0.. Version Number of Device Versions 3.1 will be 0010

BRG Baud Rate Generator Register. (Write) - HDLC, ASYNC, BISYNC modes

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0

BR7-BR0.... Baud Rate, bits 7-0

The Baud Rate generator divisor consist of bits BR7-0 from BRG register and bits BR9-8 from the CCR2 register.

The baud rate generator has two modes of operation giving added flexibility.

Standard Mode:
Bits BR9-0 contain a value N (N = 0 ... 1023) to give a XTAL clock division factor k:
k = (N + 1) x 2

Enhanced Mode:
This consists of a 2 stage divider. The first stage is divisor N is determined by bits BR5-BR0 (N = 0...63) while the second stage divisor M is determined by bit BR9-BR6 (M= 0 ..15). The first stage divides the clock by integer number up to 63, where the second stage allows further division by powers of 2 (1, 2, 4, 8, 16, 32, 64, 128... 32768).

Division by 1 using M=0 is restricted to frequencies below 10 MHz (to be characterized). The XTAL clock division factor k:

$k = (N + 1) \times 2^M$

The Baud Rate generator is typically used to derive clocks for DTE or DCE Asynchronous baud rates with 16x over sampling mode. Appendix A shows baud rates derived from typical XTAL frequencies using the two modes of the baud rate generator for ASYNC operation with 16x over sampling enabled.

3 Electrical Specification

In general the electrical Specifications for the ESCC8 Versions 3.1 are expected to be the same as that for the ESCC8 Version V2.2, however, they need to be characterized.

4 Appendix

Appendix A

Baud Rate Generator Tables

Table 1: Standard Baud Rate Generator Selections

Baud Rate	2.048 MHz	3.088 MHz	6.480 MHZ	8.000 MHZ	8.192 MHZ	9.126 MHZ	12.00 MHZ	15.36 MHZ	16.00 MHZ	16.384 MHZ	18.432 MHZ
300	300.5 (212)	299.7 (321)	300 (674)	300.5 (832)	300.1 (852)	300 (959)					
1200	1207.5 (52)	1206.3 (79)	1198 (168)	1201.9 (207)	1201.9 (212)	1200 (239)	1198.1 (312)	1200.0 (400)	1196.2 (417)	1196.3 (427)	1200 (479)
2400	2370.4 (26)	2412.5 (37)	2410.7 (83)	2403.8 (103)	2392.5 (106)	2400 (119)	2403.8 (155)	2400.0 (200)	2403.8 (207)	2392.5 (213)	2400 (239)
4800		4825 (19)	4821.7 (91)	4807.7 (51)		4800 (59)	4807.7 (77)	4800.0 (100)	4807.8 (103)	4785 (106)	4800 (119)
9600		9650 (9)	9642.9 (20)	9615.4 (25)	9481.5 (26)	9600 (29)	9615.4 (38)	9600.0 (50)	9615.9 (51)	9660.9 (52)	9600 (59)
19.2K		19.3K (4)		19.23K (12)		19.2K (14)	18.75K (19)	19.2K (25)	19.23K (25)	18.96K (26)	19.2K (26)
38.4K							37.5K (9)		38.46K (12)		35.4K (14)
48.0K		48.25K (1)				48K (5)	46.88K (7)	48.0 (10)			48K (11)
64.0K	64K (0)			62.5K (3)	64K (3)		62.5K (5)		62.5K (7)	64K (7)	64K (8)
96.0K		96.5K (0)				96K (2)	93.75 (3)	96.0 (5)			96K (5)
115.2K											115.2K (4)
144K						144K (1)					144K (3)
192K							187.5K (1)				192K (2)
288K						288K (0)					288K (1)
384K											
CK/16 Baud (max.)	128K	193K	405K	500K	512K	576K	750K *	960K *	1000K *	1024K *	1152K *

The value in brackets is (N), where N is programmed in BR9- BRO.
Maximum tolerance <2.5%
F baud = F XTAL / (16 x (N+1) x 2)

* to be characterized

Table 2: Enhanced Baud Rate Generator Selections

Baud Rate	2.048 MHZ	3.088 MHZ	6.480 MHZ	8.000 MHZ	8.192 MHZ	9.126 MHZ	12.00 MHZ	15.36 MHZ	16.00 MHZ	16.384 MHZ	18.432 MHZ	29.491 MHZ
300	301.9 (53/3)	301.6 (10/6)	301.6 (21/6)	300.5 (26/6)	301.9 (53/5)	300.0 (30/6)	300.5 (39/6)	300.0 (25/7)	300.5 (26/7)	301.9 (53/6)	300.0 (30/7)	300 (48/7)
1200	1207 (53/1)	1206.3 (10/4)	1205.3 (21/4)	1201.9 (26/4)	1207 (53/3)	1200.0 (30/4)	1201.9 (39/4)	1200.0 (25/5)	1201.9 (26/5)	1207 (53/4)	1200.0 (30/5)	1200 (48/5)
2400	2415 (53/0)	2412.5 (10/3)	2410.7 (21/3)	2403.8 (26/3)	2415 (53/2)	2400.0 (30/3)	2403.8 (39/3)	2400.0 (25/4)	2403.8 (26/4)	2415 (53/3)	2400.0 (30/4)	2400 (48/4)
4800	4740.7 (27/0)	4825 (10/2)	4821 (21/2)	4807.6 (26/2)	4830 (53/1)	4800.0 (30/2)	4807.7 (39/2)	4800/0 (25/3)	4807.7 (26/3)	4830 (53/2)	4800.0 (30/3)	4800 (48/3)
9600	9846.2* (13/0)	9650 (10/1)	9642 (21/1)	9615.4 (26/1)	9660.4 (53/0)	9600.0 (30/1)	9615.4 (39/1)	9600.0 (25/2)	9615.4 (26/2)	9660.4 (53/1)	9600.0 (30/2)	9600 (48/2)
19.2K		19.13 (10/0)	19.29 (21/0)	19.23 (26/0)	18.96 (27/0)	19.2 (30/0)	19.23 (39/0)	19.2 (25/1)	19.23 (26/1)	18.96 (27/1)	19.20 (30/1)	19.20 (48/1)
38.4K		38.6 (5/0)		38.46 (13/0)	39.38** (13/0)	38.4 (15/0)	37.5 (10/1)	38.4 (25/0*)	38.46 (13/1)	39.38 (13/1)	38.4 (15/1)	38.4 (24/1)
48.0K		48.25 (4/0)				48.0 (12/0)	46.5 (8/1)	48.0 (10/1)	50** (10/1)	46.54** (11/1)	48.0 (12/1)	48.5 (19/1)
64.0K	64.0 (2/0)	64.33 (3/0)		62.5 (8/0)	64.0 (8/0)	64.0 (9/0)	62.5 (6/1)	64.0 (15/0*)	62.5 (8/1)	64.0 (8/1)	64.0 (9/1)	65.83** (14/1)
96.0K		96.5 (2/0)				96.0 (6/0)	93.75 (4/1)	96.0 (5/1)			96.0 (6/1)	92.16** (10/1)
115.2K						115.2 (5/0)					115.2 (5/1)	115.2 (8/1)
144K						144.0 (4/0)			142.85 (7/1)	146.29 (7/1)	144.0 (4/1)	
192K		193 (1/0)				192 (3/0)	187.5 (2/1)	192.0 (5/0*)			192.0 (3/1)	
288K						288 (1/1)					288.0 (2/1)	
384K							375 (1/1)					
768K												
CK/ 16Baud (max.)	128K	193K	405K	500K	512K	576K	750K *	960K *	1000K *	1024K *	1152K *	1843.2K *

The value in brackets is (N+1 / M*) and is used to determine the baud rate as follows:
Baud = FXTAL / 16 x (N+1) x 2^M

Maximum tolerance <2.5% except where indicated by ** when it is <5%
M=0* may not be supported for XTAL frequencies above 10 MHz.

Where 0< N < 63 and N is programmed in bits BR5 - BR0 in register BRG
and 0 < M < 15 and M is programmed in bits BR9 - BR6 in register BRG and CCR2 registers

* to be characterized

Table 3: Enhanced Baud Rate Generator Selections (continued)

Baud Rate	29.4912 MHZ
50	50 (36/10)
75	75 (48/9)
110	109.09 (33/9)
134.5	133.3 (54/8)
150	150 (48/8)
200	200 (36/8)
57.6K	57.6K (16/1)
76.8K	76.8 (12/1)
153.6K	153.6K (6/1)
230.4	230.4K (4/1)
307.2K	307.2K (3/1)
460.8K	460.8K (2/1)
614.4K	
921.6	921.6K (1/1)
CK/16 Baud (max.)	1.8432 MHz *

The value in brackets is (N+1 / M) and is used to determine the baud rate as follows:
Baud = FXTAL / 16 x (N+1) x 2^M
Maximum tolerance <2.5% except where indicated by ** when it is <5%
M=0* may not be supported for XTAL frequencies above 10 MHz.

Where 0 < N < 63 and N is programmed in bits BR5 - BR0 in register BRG
and 0 < M < 15 and M is programmed in bits BR9 - BR6 in register BRG and CCR2 registers.

* to be characterized