SIEMENS

ICs for Communications

Enhanced Serial Communications Controller ESCC2

SAB 82532
SAF 82532

Version 3.2A

Errata Sheet 02.97

T8253-2V32-E1-7600

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Errata Sheet for the Version 3.2A

All Sent (ALLS) Interrupt in Master Clock Mode

If in master clock mode an ALLS interrupt is generated, this interrupt might be indicated via the interrupt status register 1 (ISR1) more than once.

Workaround:
Do not use the ALLS interrupt in master clock mode. Instead, use the XPR interrupt, if applicable.