SIEMENS

ICs for Communications

Enhanced Serial Communications Controller
ESCC2

SAB 82532
SAF 82532

Version 3.2A

Addendum 02.97 (to User's Manual 07.96)

T8253-2V32-U2-7600

SAB 82532 **SAF 82532** **Revision History:** **Current Version: 02.97**		
Previous Version: 09.96		
Page (in previous Version)	Page (in new Version)	Subjects (major changes since last revision)
249	249	Timing t_{31} and t_{32}
-	260	Timing t_{75}
-	265	Upgrades of ESCC2 Version V3.2A

SIEMENS

Enhanced Serial Communications Controller ESCC2

SAB 82532
SAF 82532

Version 3.2A

This addendum replaces the addendum version 09.96.

It replaces the pages 241 to 264 of the User's Manual version 07.96 and it provides the upgrades of ESCC2 version V3.2A.

The changes between the User's Manual version 07.96 and the addendum version 02.97 refer to the timing values 32, 50 ... 52A, and 75. The value 50A has been left out, whereas the value 52A is new.
The value 53 on page 246 was replaced by the value 52.

The changes between the addendum version 09.96 and the addendum version 02.97 are described in the revision history.

Note that the numbering of the pages (241-264), chapters and figures (53-70) is identical to the User's Manual version 07.96.

11.4 AC Characteristics

SAB: V_{DD} = 5 V ± 5 %; V_{SS} = 0 V; T_A = 0 to 70 °C
SAF: V_{DD} = 5 V ± 5 %; V_{SS} = 0 V; T_A = – 40 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
Inputs						
All inputs except XTAL1 and WIDTH are driven to	V_{IH}		2.4		V	for logical ‘1’
	V_{IL}		0.4		V	for logical ‘0’
XTAL1 and WIDTH (CMOS inputs) are driven to	V_{IH}		4.0		V	for logical ‘1’
	V_{IL}		0.4		V	for logical ‘0’
Timing Measurements						
Measurements except for XTAL2 are driven to	V_H		2.0		V	for logical ‘1’
	V_L		0.8		V	for logical ‘0’
Measurements for XTAL2 are driven to	V_H		3.5		V	for logical ‘1’
	V_L		1.0		V	for logical ‘0’

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

The AC testing input/output waveforms are shown below:

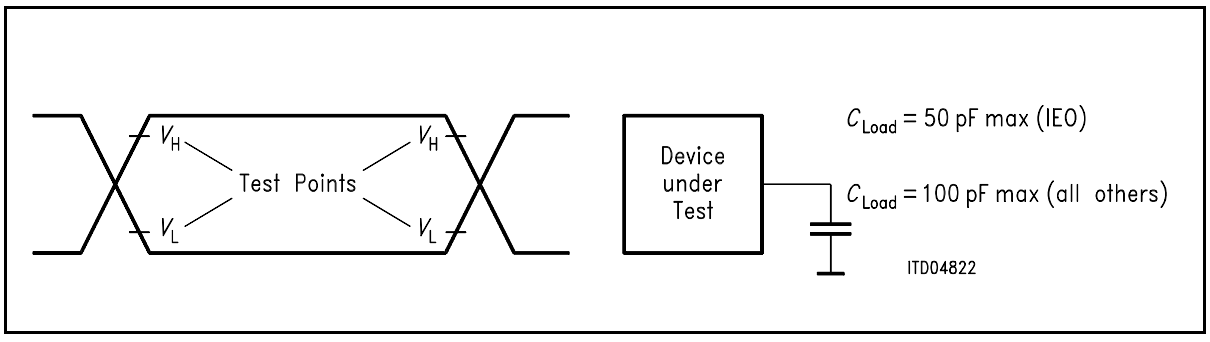

Figure 53
Input/Output Waveform for AC Tests

11.4.1 Microprocessor Interface

11.4.1.1 Siemens/Intel Bus Interface Mode

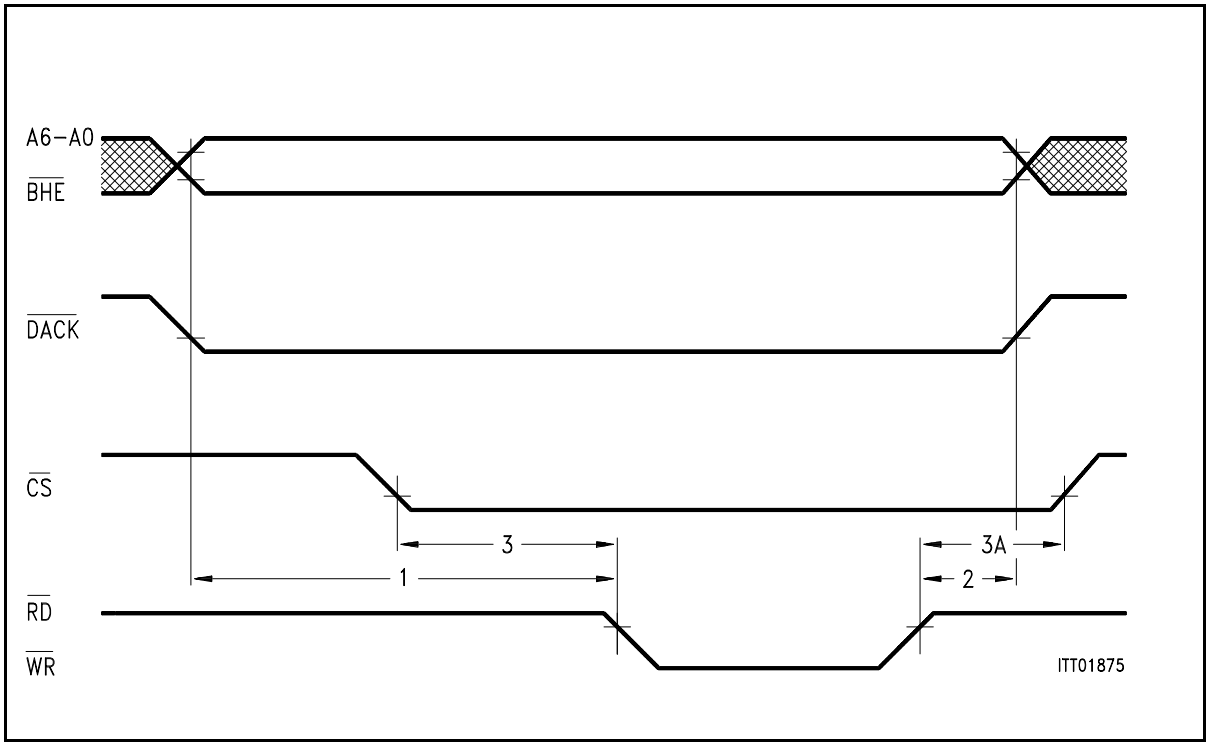

Figure 54
Siemens/Intel Non-Multiplexed Address Timing

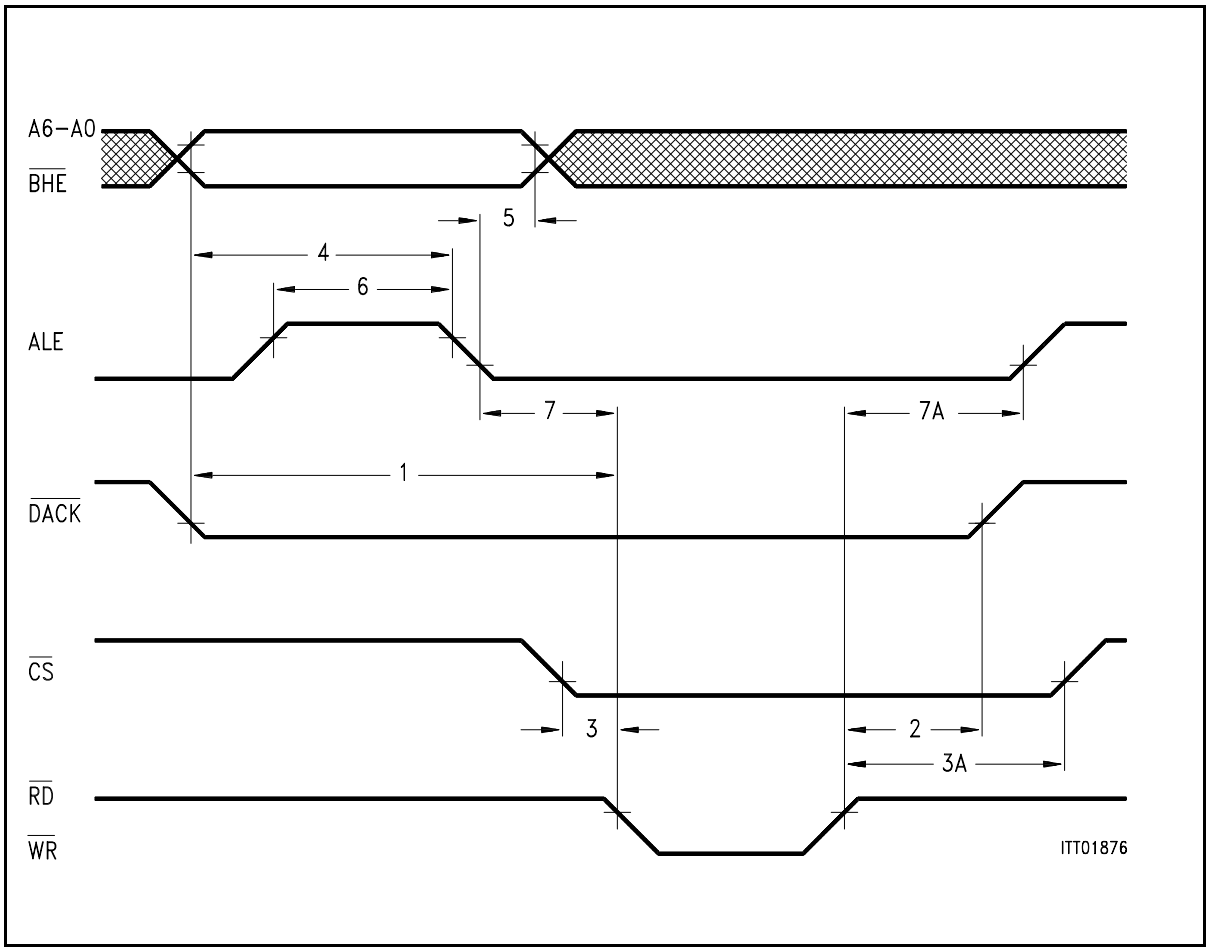

Figure 55
Siemens/Intel Multiplexed Address Timing

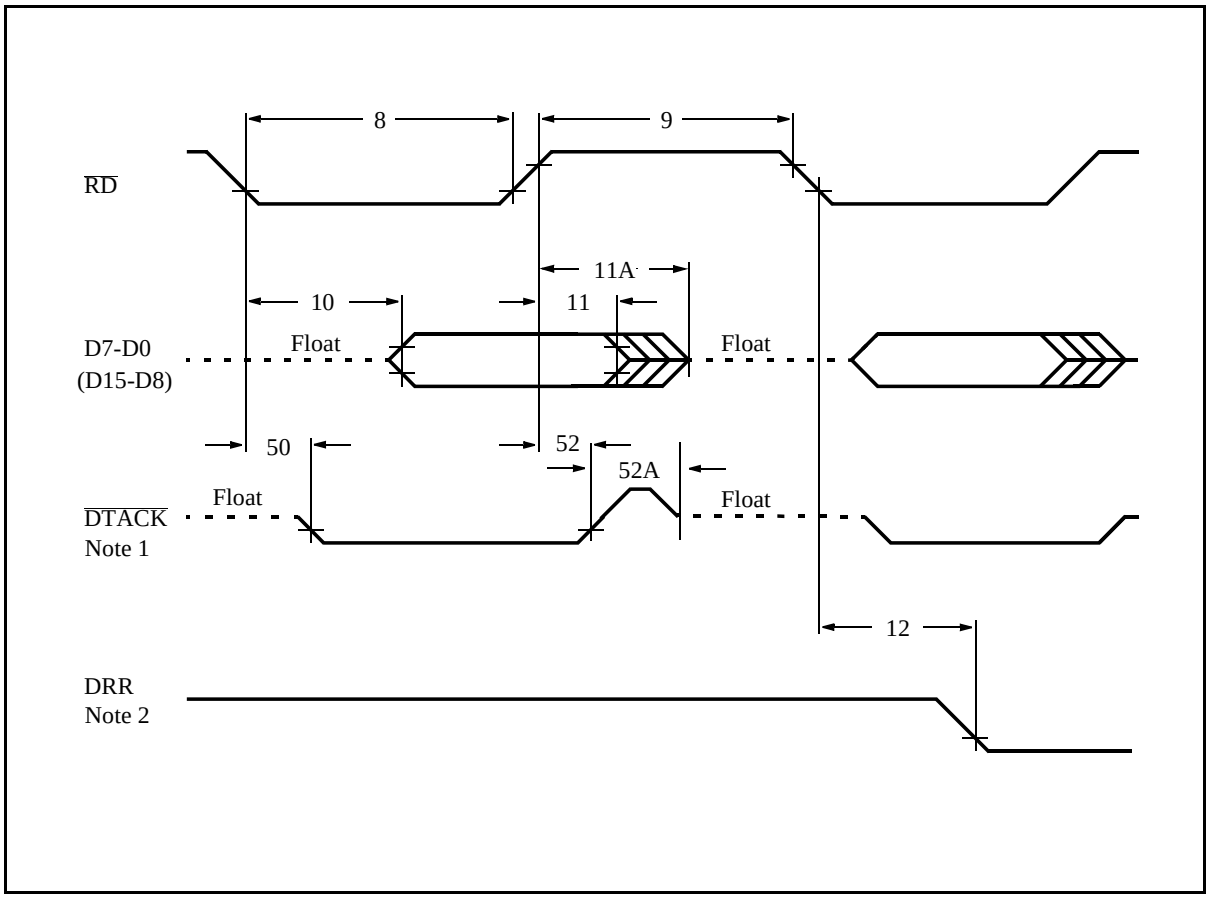

Figure 56
Siemens/Intel Read Cycle Timing

Note 1: Function of DTACK is described logically as:
$\overline{DTACK} = (CS \times DACKA \times DACKB + RD \times WR) \times \overline{INTAi}$.
$\overline{INTAi}$ is an internally generated signal.

Note 2: DRR is reset with the falling edge of $\overline{RD}$ during the last read access to RFIFO.

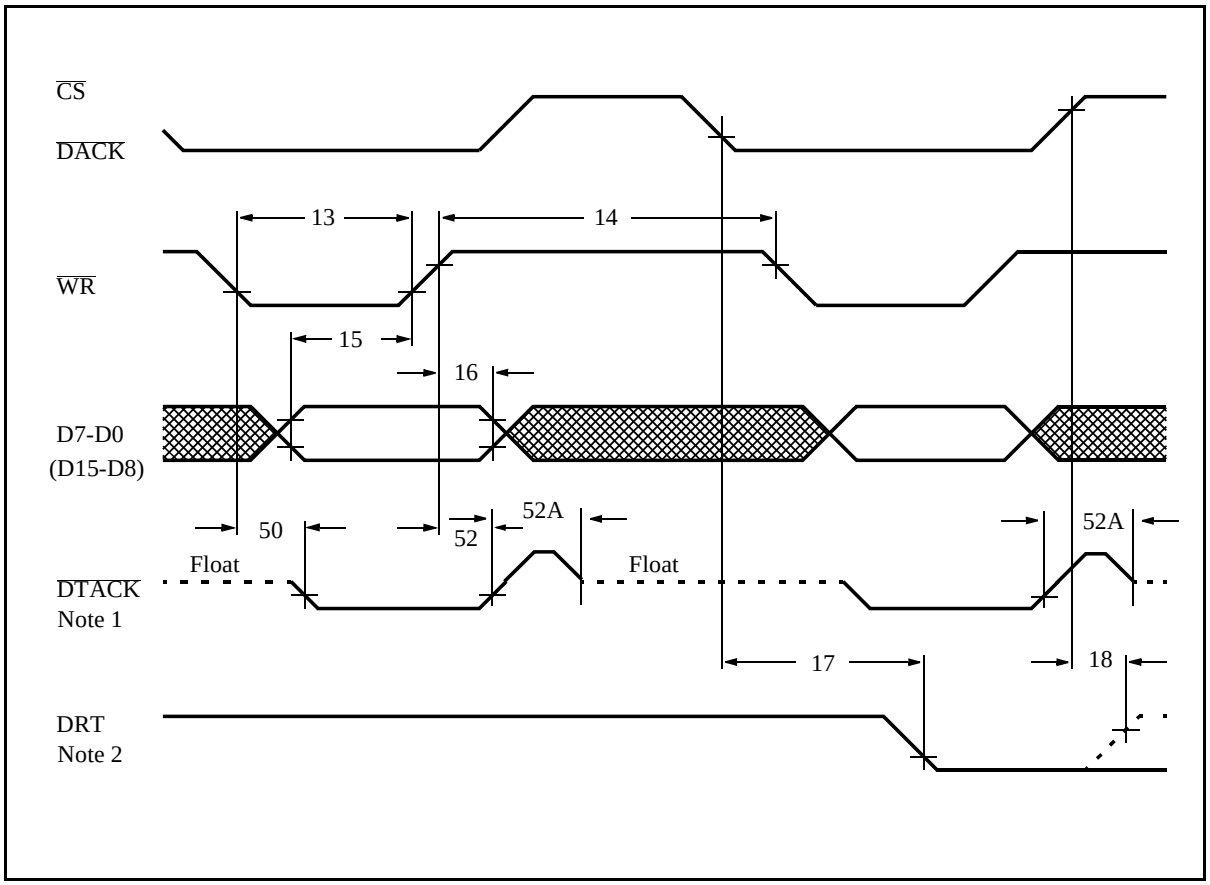

Figure 57
Siemens/Intel Write Cycle Timing

Note 1: Function of $\overline{DTACK}$ is described logically as:
$\overline{DTACK} = (\overline{CS} \times \overline{DACKA} \times \overline{DACKB} + \overline{RD} \times \overline{WR}) \times \overline{INTAi}$.
INTAi is an internally generated signal.

Note 2: DRT is reset with the falling edge of $\overline{CS}$ or $\overline{DACK}$ if the last write access to XFIFO is expected. However, DRT will be activated again in the case of an access to any other register or FIFO.

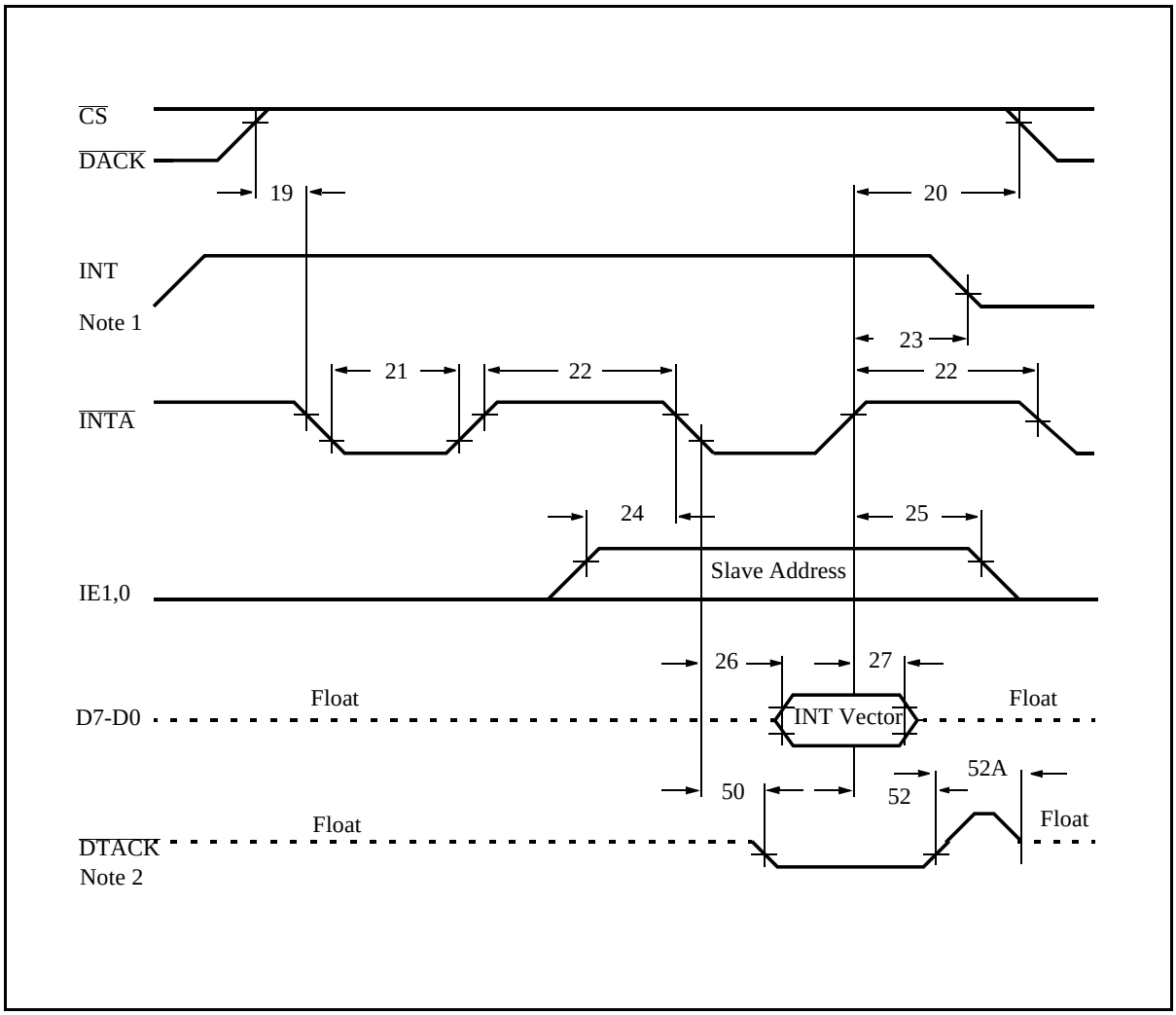

Figure 58
Siemens/Intel Interrupt Timing (slave mode)

Note 1: Timing valid for active-high push-pull signal, timing for active-low push-pull signal is the same.
In case of an open drain output, reset time (T23) depends on external devices.

Note 2: Function of $\overline{DTACK}$ is described logically as:
$\overline{DTACK} = (\overline{CS} \times \overline{DACKA} \times \overline{DACKB} + \overline{RD} \times \overline{WR}) \times \overline{INTAi}$.
$\overline{INTAi}$ is an internally generated signal. It is generated if the interrupt acknowledge cycle is considered valid.

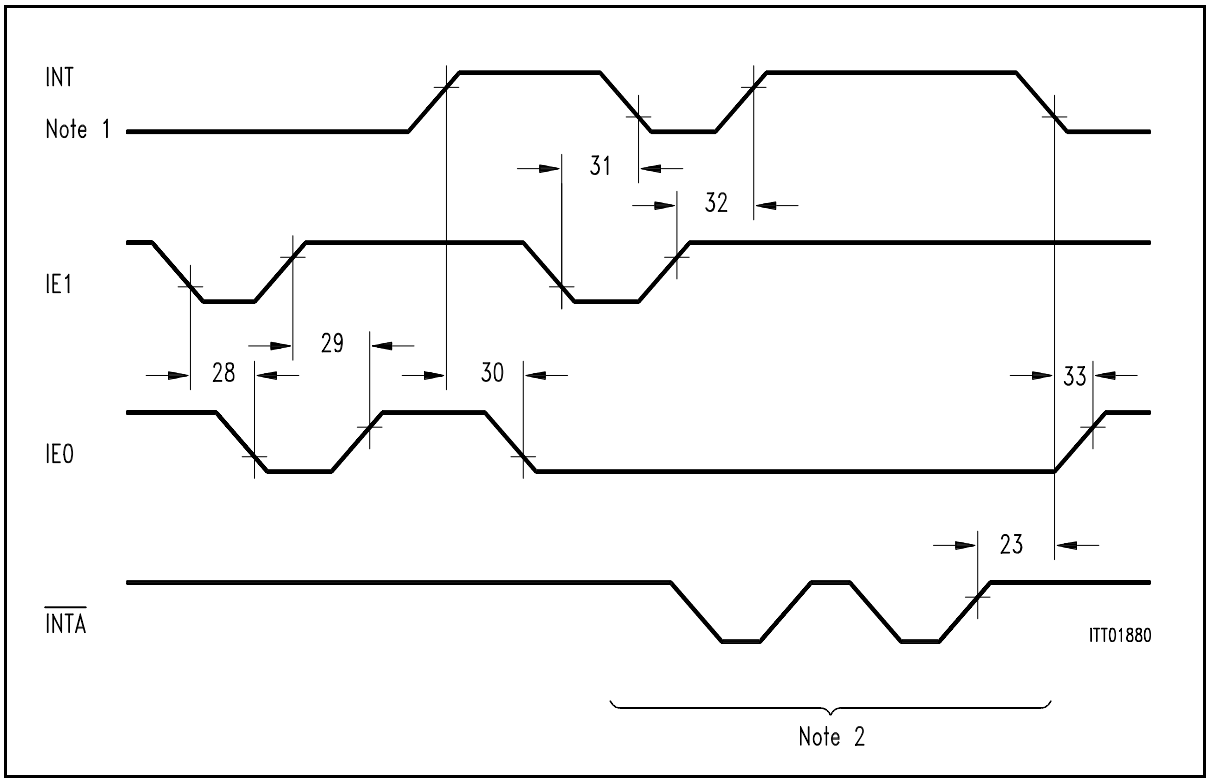

Figure 59
Siemens/Intel Interrupt Timing (Daisy Chaining)

Note 1: Timing valid for active-high push-pull signal. Timing for active-low push-pull signal is the same.
In case of an open-drain output, reset times (T23, T31) depend on external devices.

Note 2: Timing for $\overline{CS}$, $\overline{DACK}$, INT, $\overline{INTA}$ and D7 … D0 is similar to slave mode.

Siemens/Intel Bus Interface Timing and Interrupt Timing

No.	Parameter	Symbol	Limit Values		Unit
			min.	max.	
1	Address, $\overline{BHE}$, $\overline{DACK}$ setup time	$t_{su(A)}$	5		ns
2	Address, $\overline{BHE}$, $\overline{DACK}$ hold time	$t_{h(A)}$	10		ns
3	$\overline{CS}$ setup time	$t_{su(A)}$	0		ns
3A	$\overline{CS}$ hold time	$t_{h(A)}$	0		ns
4	Address, $\overline{BHE}$ stable before ALE inactive	$t_{su(A-ALE)}$	20		ns
5	Address, $\overline{BHE}$ hold after ALE inactive	$t_{su(ALE-A)}$	10		ns
6	ALE pulse width	$t_{w(ALE)}$	30		ns
7	Address latch setup time before command active	$t_{su(ALE)}$	0		ns
7A	ALE to command inactive delay	$t_{rec(ALE)}$	20		ns
8	$\overline{RD}$ pulse width	$t_{w(R)}$	70		ns
9	$\overline{RD}$ control interval	$t_{rec(R)}$	50		ns
10	Data valid after $\overline{RD}$ active	$t_{a(R)}$		65	ns
11	Data hold after $\overline{RD}$ inactive	$t_{v(R)}$	10		ns
11A	$\overline{RD}$ inactive to data bus tristate[1)]	$t_{dis(R)}$		40	ns
12	DRR low after $\overline{RD}$ active	$t_{p(DRR)}$		45	ns
13	$\overline{WR}$ pulse width	$t_{w(W)}$	35		ns
14	$\overline{WR}$ control interval	$t_{rec(W)}$	35		ns
15	Data stable before $\overline{WR}$ inactive	$t_{su(D)}$	30		ns
16	Data hold after $\overline{WR}$ inactive	$t_{h(D)}$	5		ns
17	DRT low after $\overline{CS}$, $\overline{DACK}$ active	$t_{dis(DRT)}$		30	ns
18	DRT return to one after $\overline{CS}$, $\overline{DACK}$ inactive	$t_{p(DRT)}$		30	ns
19	$\overline{CS}$, $\overline{DACK}$ inactive setup ($\overline{INTA}$ cycle) [1)]	$t_{dis(S-INT)}$	0		ns
20	$\overline{CS}$, $\overline{DACK}$ inactive hold ($\overline{INTA}$ cycle) [1)]	t_{INTA-S}	0		ns
21	$\overline{INTA}$ pulse width	$t_{w(INTA)}$	70		ns
22	$\overline{INTA}$ control interval	$t_{rec(INTA)}$	30		ns
23	INT reset after last $\overline{INTA}$ inactive	$t_{INTA-INT}$		30	ns
24	Slave address (IE0, IE1) setup time	$t_{su(IE)}$	10		ns
25	Slave address (IE0, IE1) hold time	$t_{h(IE)}$	5		ns

[1)] Not testet in production

Siemens/Intel Bus Interface Timing and Interrupt Timing (cont'd)

No.	Parameter	Symbol	Limit Values		Unit
			min.	max.	
26	Interrupt vector (D7 … D0) valid after $\overline{\text{INTA}}$ active	$t_{a(VEC)}$		50	ns
27	Interrupt vector (D7 … D0) hold after $\overline{\text{INTA}}$ inactive	$t_{v(VEC)}$	10	40	ns
28	IE0 low after IE1 low	$t_{IE1L\text{-}IE0L}$		20	ns
29	IE0 high after IE1 high	$t_{IE1H\text{-}IE0H}$		20	ns
30	IE0 low after INT active	$t_{INTV\text{-}IE0L}$		10	ns
31	INT inactive after IE1 low	$t_{dis(INT)}$		35	ns
32	INT reactivated after IE1 high	$t_{IE1H\text{-}INTV}$		35	ns
33	IE0 high after INT reset	$t_{INTV\text{-}IE0H}$		30	ns
50	$\overline{\text{DTACK}}$ active after command active	$t_{p(DTK)}$		30	ns
52	$\overline{\text{DTACK}}$ hold after command inactive	$t_{v(DTK)}$	0	40	ns
52A	$\overline{\text{DTACK}}$ high impedance pulse width	t_{vHZ}		40	ns

Note: $t_{27\,max}$ not tested in production

11.4.1.2 Motorola Bus Interface Mode

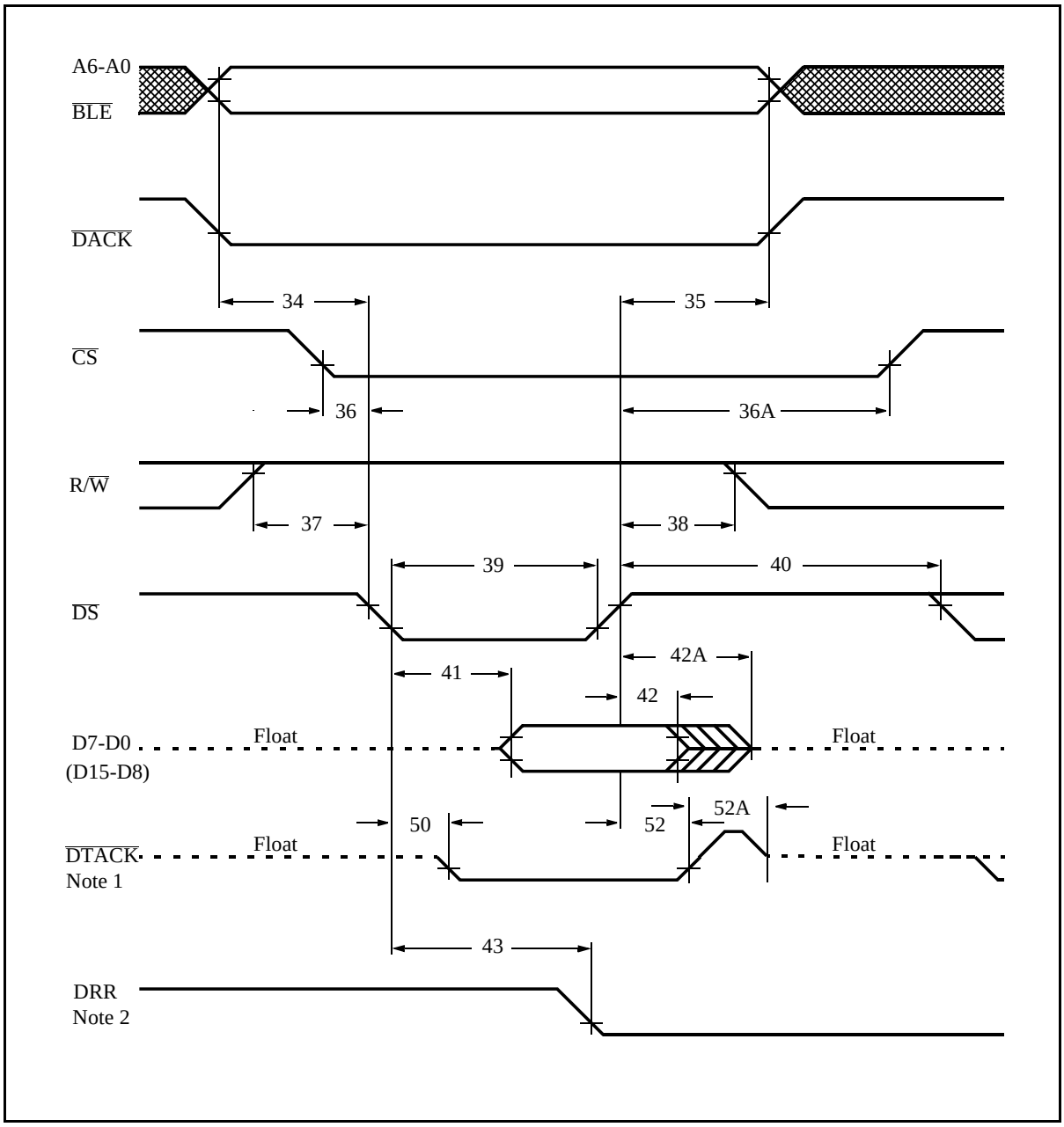

Figure 60
Motorola Read Cycle Timing

Note 1: Function of $\overline{DTACK}$ is described logically as:
$\overline{DTACK} = \overline{CS} \times \overline{DACKA} \times \overline{DACKB} \times \overline{INTAi} + \overline{DS} \times R/\overline{W}$) i.e. in accordance with common specifications of Motorola read accesses the timing of $\overline{DTACK}$ is normally determined by $\overline{DS}$.

Note 2: DRR is reset with the falling edge of $\overline{DS}$ during the last read access to RFIFO.

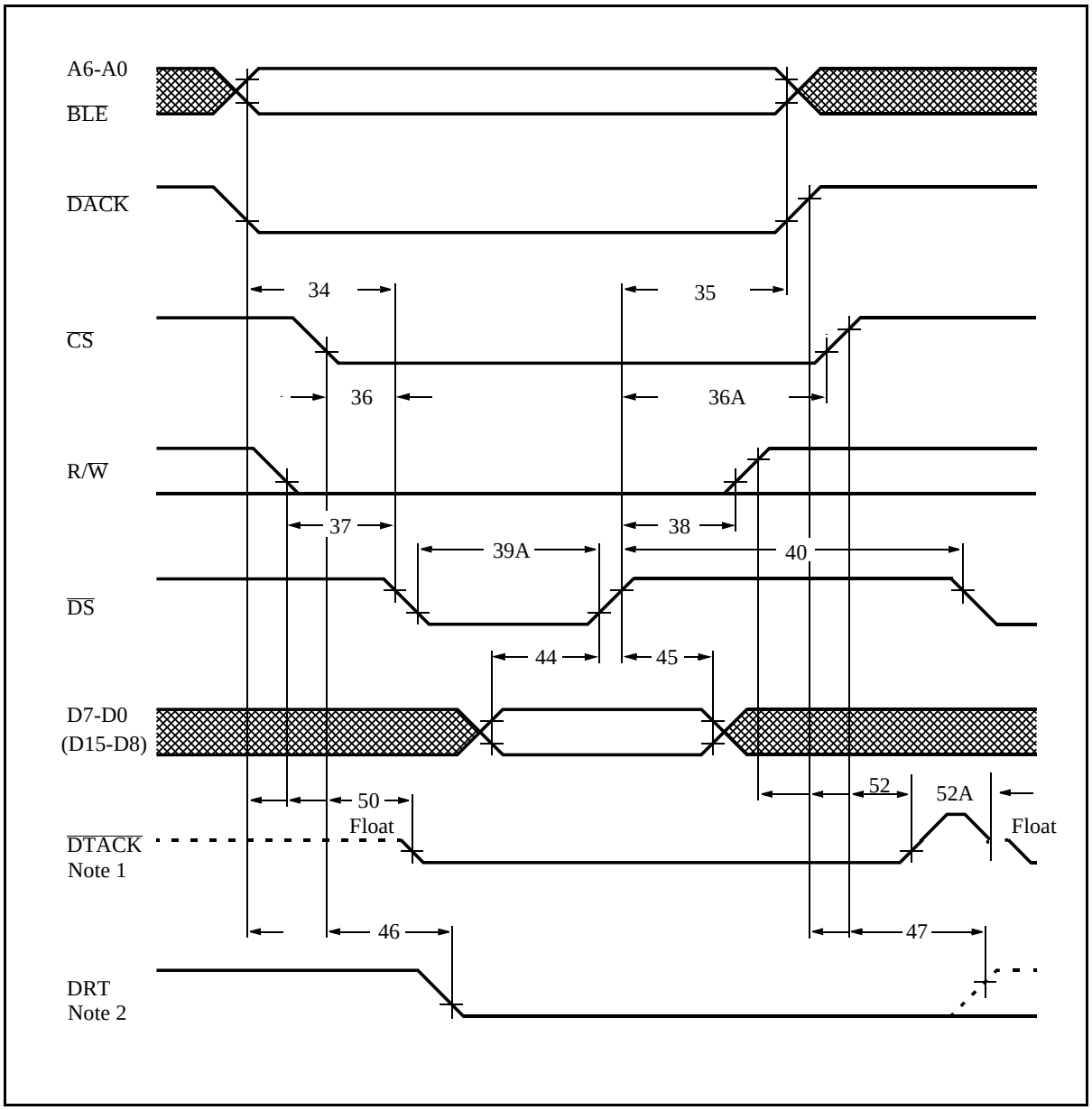

Figure 61
Motorola Write Cycle Timing

Note 1: Function of $\overline{DTACK}$ is described logically as:
$\overline{DTACK} = \overline{CS} \times \overline{DACKA} \times \overline{DACKB} \times \overline{INTAi} + \overline{DS} \times \overline{R/W}$ i.e. in accordance with common specifications of Motorola accesses.
$\overline{DTACK}$ goes active if either $\overline{CS}$ or $\overline{DACKx}$ is active and $\overline{R/W}$ goes low.
$\overline{DTACK}$ goes inactive if $\overline{CS}$ and $\overline{DACKx}$ are inactive or write $\overline{R/W}$ goes high.
To guarantee correct function in the case of write bursts signals $\overline{CS}$ and $\overline{DACKx}$ have to be inactive after each write access (e.g. by deriving them from the Address Strobe $\overline{AS}$).

Note 2: DRT is reset with the falling edge of $\overline{CS}$ or $\overline{DACK}$ if the last write access to XFIFO is expected. However, DRT will be activated again in the case of an access to any other register or FIFO.

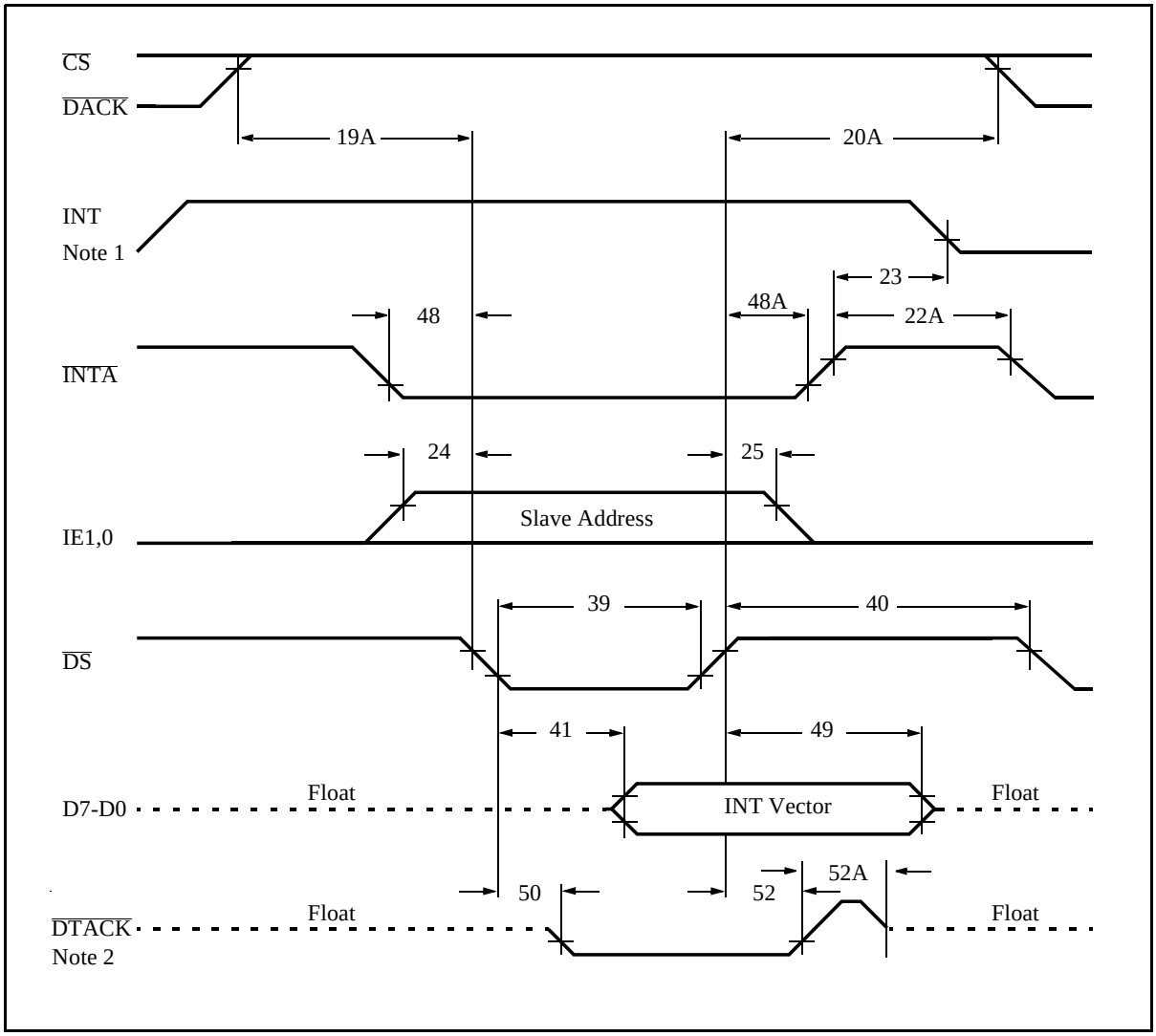

Figure 62
Motorola Interrupt Timing (slave mode)

Note 1: Timing valid for active-high push-pull signal. Timing for active-low push-pull signal is the same.
In the case of an open-drain output, reset times (T23, T31) depend on external devices.

Note 2: Function of $\overline{DTACK}$ is described logically as:
$\overline{DTACK} = \overline{CS} \times \overline{DACKA} \times \overline{DACKB} \times \overline{INTAi} + \overline{DS} \times \overline{R/W}$.
$\overline{INTAi}$ is an internal signal. It is generated if the interrupt acknowledge cycle is considered valid.

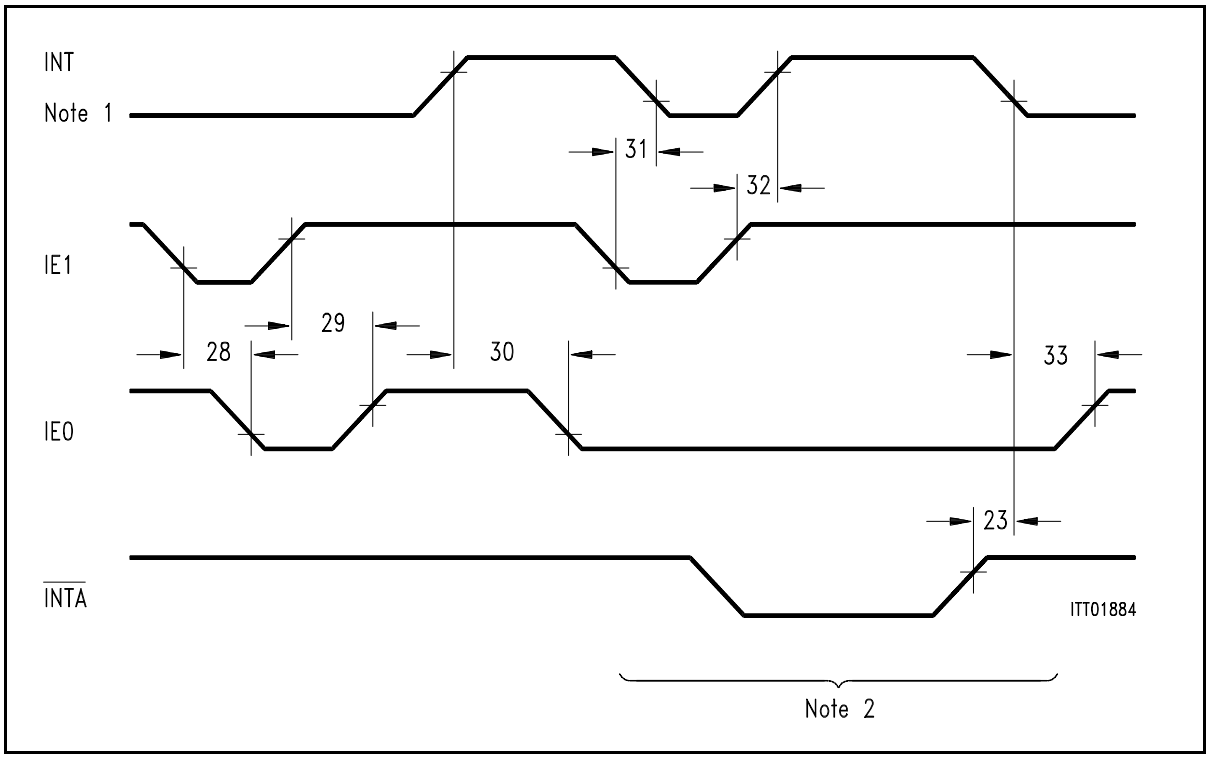

Figure 63
Motorola Interrupt Timing (Daisy Chaining)

Note 1: Timing valid for active-high push-pull signal. Timing for active-low push-pull signal is the same.
In the case of an open-drain output, reset times (T23, T31) depend on external devices.

Note 2: Timing for $\overline{CS}$, $\overline{DACK}$, INT, $\overline{INTA}$, $\overline{DS}$ and D7 … D0 is similar to slave mode.

Motorola Bus Interface Timing and Interrupt Timing

No.	Parameter	Symbol	Limit Values		Unit
			min.	max.	
34	Address, $\overline{BLE}$, $\overline{DACK}$ setup time before $\overline{DS}$ active	$t_{su(A)}$	5		ns
35	Address, $\overline{BLE}$, $\overline{DACK}$ hold after $\overline{DS}$ inactive	$t_{h(A)}$	0		ns
36	$\overline{CS}$ active before $\overline{DS}$ active	$t_{su(A)}$	0		ns
36A	$\overline{CS}$ hold after $\overline{DS}$ inactive	$t_{h(A)}$	0		ns
37	R/$\overline{W}$ stable before $\overline{DS}$ active	$t_{su(RW)}$	5		ns
38	R/$\overline{W}$ hold after $\overline{DS}$ inactive	$t_{h(RW)}$	0		ns
39	$\overline{DS}$ pulse width (read access)	$t_{w(DS)R}$	70		ns

Motorola Bus Interface Timing and Interrupt Timing (cont'd)

No.	Parameter		Symbol	Limit Values		Unit
				min.	max.	
39A	$\overline{DS}$ pulse width	(write access)	$t_{w(DS)W}$	35		ns
40	$\overline{DS}$ control interval		$t_{rec(DS)}$	50		ns
41	Data valid after $\overline{DS}$ active	(read access)	$t_{a(DS)}$		65	ns
42	Data hold after $\overline{DS}$ inactive	(read access)	$t_{v(DS)}$	10		ns
42A	$\overline{DS}$ inactive to databus tristate[1)]	(read access)	$t_{dis(DS)}$		40	ns
43	DRR low after $\overline{DS}$ active[1)]		$t_{p(DRR)}$		45	ns
44	Data stable before $\overline{DS}$ inactive	(write access)	$t_{su(D)}$	30		ns
45	Data hold after $\overline{DS}$ inactive	(write access)	$t_{h(D)}$	5		ns
46	DRT low after $\overline{DS}$ or $\overline{DACK}$ active[1)]		$t_{dis(DRT)}$		30	ns
47	DRT return to one after $\overline{CS}$ or $\overline{DACK}$ inactive[1)]		$t_{p(DRT)}$		30	ns
19A	$\overline{CS}$, $\overline{DACK}$ inactive setup before $\overline{DS}$ ($\overline{INTA}$ cycle)[1)]		$t_{dis(S\text{-}INTA)}$	20		ns
20A	$\overline{CS}$, $\overline{DACK}$ inactive hold after $\overline{DS}$ ($\overline{INTA}$ cycle)[1)]		$t_{h(INTA\text{-}S)}$	20		ns
22A	$\overline{INTA}$ control interval		$t_{rec(INTA)}$	30		ns
23	INT reset after last $\overline{INTA}$ inactive		$t_{INTA\text{-}INT}$		30	ns
24	Slave address (IE0, IE1) setup time		$t_{su(IE)}$	10		ns
25	Slave address (IE0, IE1) hold time		$t_{h(IE)}$	5		ns
28	IE0 low after IE1 low		$t_{IE1L\text{-}IE0L}$		20	ns
29	IE0 high after IE1 high		$t_{IE1H\text{-}IE0H}$		20	ns
30	IE0 low after INT active		$t_{INTV\text{-}IE0L}$		10	ns
31	INT inactive after IE1 low		$t_{dis(INT)}$		25	ns
32	INT reactivated after IE1 high		$t_{IE1H\text{-}INTV}$		25	ns
33	IE0 high after INT reset[1)]		$t_{INT\text{-}IE0H}$		20	ns
48	$\overline{INTA}$ setup time		$t_{su(INTA)}$	0		ns
48A	$\overline{INTA}$ hold time		$t_{h(INTA)}$	0		ns
49	Interrupt vector hold after $\overline{DS}$ or $\overline{INTA}$ inactive[1)]		$t_{v(VEC)}$	10	40	ns
50	$\overline{DTACK}$ active delay		$t_{p(DTK)}$		30	ns
52	$\overline{DTACK}$ hold after command inactive[1)]		$t_{v(DTK)}$	0	40	ns
52A	$\overline{DTACK}$ high impedance pulse width		t_{vHZ}		40	ns

[1)] Not testet in production

11.4.2 Parallel Port Timing

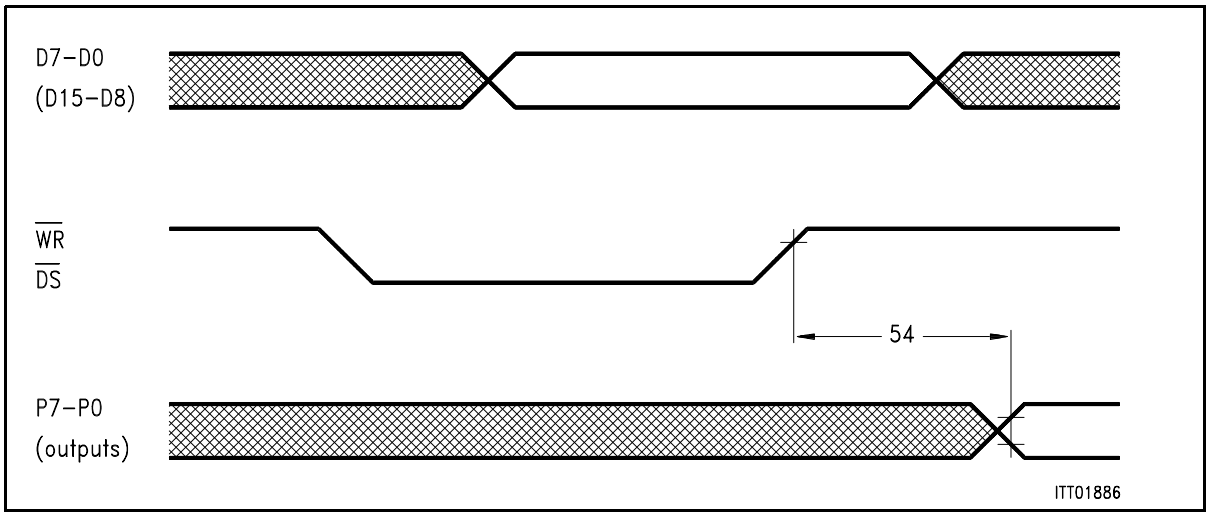

Figure 64
Parallel Port Write Access

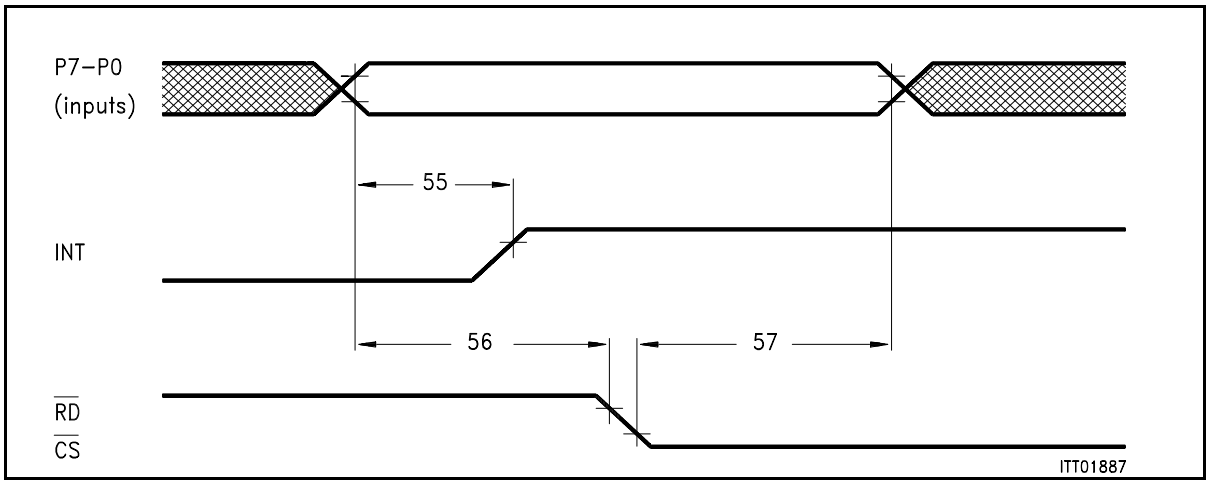

Figure 65
Parallel Port Read Access

Parallel Port Timing

No.	Parameter	Symbol	Limit Values		Unit
			min.	max.	
54	Port output data valid after $\overline{WR}$, $\overline{DS}$ inactive	t_{QV}		60	ns
55	Port input data change to INT active delay	$t_{p(PV\text{-}INT)}$		50	ns
56	Port input data stable before $\overline{RD}$, $\overline{DS}$ active	$t_{su(P)}$	20		ns
57	Port input data hold after $\overline{RD}$, $\overline{DS}$ active	$t_{h(P)}$	30		ns

11.4.3 Serial Interface

11.4.3.1 Clock Input Timing

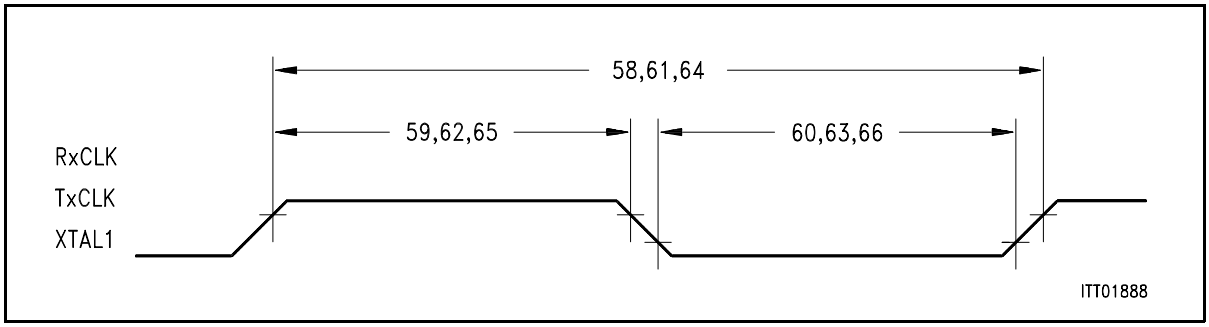

Figure 66

Clock Timing

No.	Parameter	Symbol	Limit Values				Unit
			N		N-10		
			min.	max.	min.	max.	
58	RxCLK clock period	$t_{c(RxC)}$	480[1] 30[3]		100[1] 30[3]		ns ns
59	RxCLK high time	$t_{w(RxCH)}$	150[1] 13[3]		45[1] 13[3]		ns ns
60	RxCLK low time	$t_{w(RxCL)}$	150[1] 13[3]		45[1] 13[3]		ns ns
61	TxCLK clock period	$t_{c(TxC)}$	480		100		ns
62	TxCLK high time	$t_{w(TxCH)}$	150		45		ns
63	TxCLK low time	$t_{w(TxCL)}$	150		45		ns
64	XTAL1 clock period	$t_{c(XTAL1)}$	480[2] 30[3]		50[2] 30[3]		ns ns
65	XTAL1 high time	$t_{w(XTAL1H)}$	150[2] 13[3]		23[2] 13[3]		ns ns
66	XTAL1 low time	$t_{w(XTAL1L)}$	150[2] 13[3]		23[2] 13[3]		ns ns

[1] Externally clocked: clock mode 0, 1 except ASYNC, BCR = 16.
[2] Externally clocked: clock mode 4 except ASYNC, BCR = 16;
Master clock mode generally.
[3] Internally clocked: HDLC, BISYNC: DPLL + baud rate generator used; ASYNC all other clocking modes.

11.4.3.2 Receive Cycle Timing

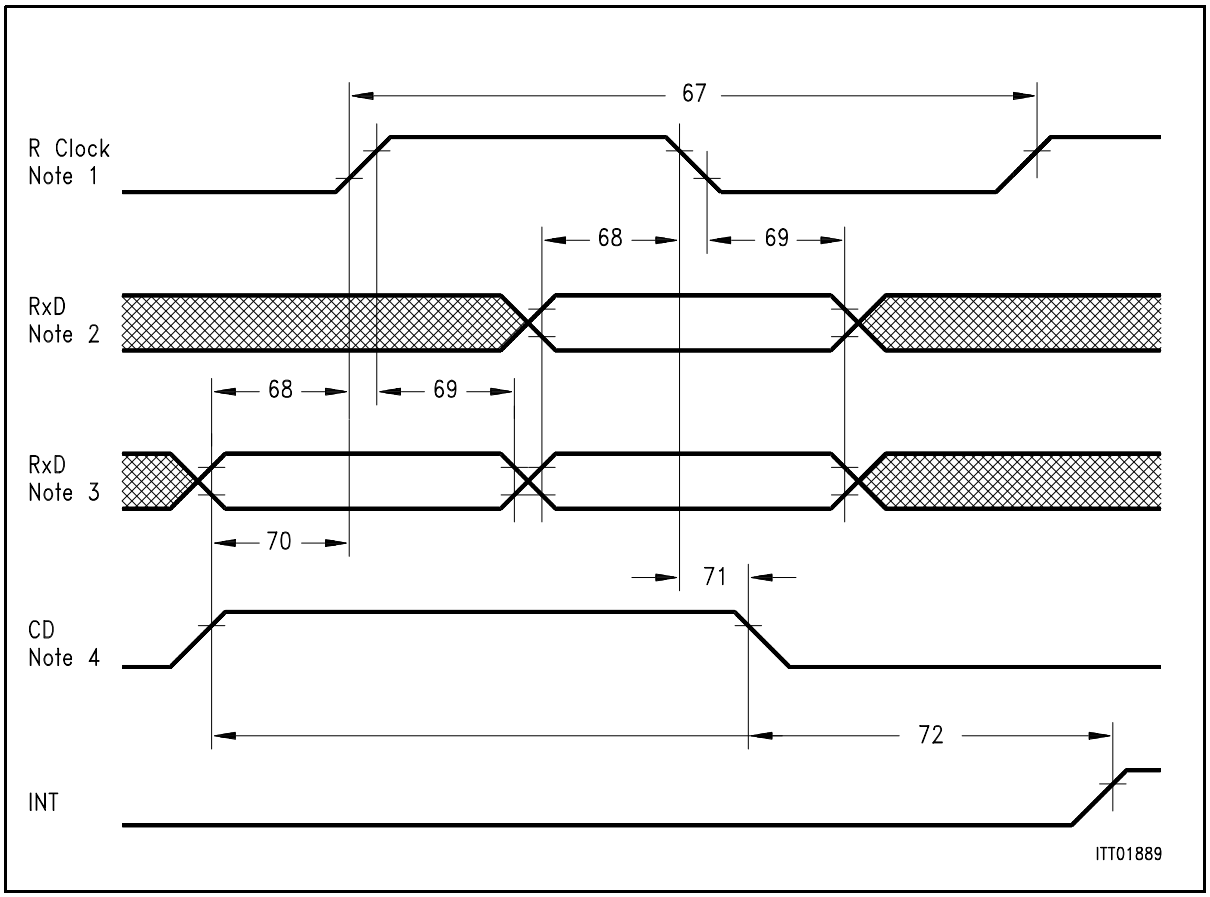

Figure 67
Receive Cycle Timing

*Note 1: Whichever supplies the clock: externally clocked by RxCLK or XTAL1, or, internally derived from DPLL, BRG or BCR divider (refer to **table 5**).*

Note 2: NRZ, NRZI and Manchester coding.

Note 3: FM0 and FM1 coding.

Note 4: Carrier detect auto start enabled (not for clock modes 1, 5).

Receive Cycle Timing

No.	Parameter		Symbol	Limit Values				Unit
				N		N-10		
				min.	max.	min.	max.	
	Receive data rate	ext. clocked (exept ASYNC, BCR = 16)			2		10	Mbit/s
		int. clocked (HDLC, BISYNC: only DPLL)			2		2	Mbit/s
		int. clocked (all other internal modes)			2		2	Mbit/s
67	Clock period	ext. clocked (exept ASYNC, BCR = 16)	$t_{c(RC)}$	480		100		ns
		int. clocked (HDLC, BISYNC: only DPLL)		480		480		ns
		int. clocked (all other internal modes)		480		480		ns
68	Receive data setup		$t_{su(R\times D)}$	10		10		ns
69	Receive data hold		$t_{h(R\times D)}$	30		30		ns
70	Carrier detect setup		$t_{su(CD)}$	50		50		ns
71	Carrier detect hold		$t_{h(CD)}$	30		30		ns
72	CD status change to INT delay		$t_{CD\text{-}INT}$		T73 + 60		T73 + 60	ns

11.4.3.3 Transmit Cycle Timing

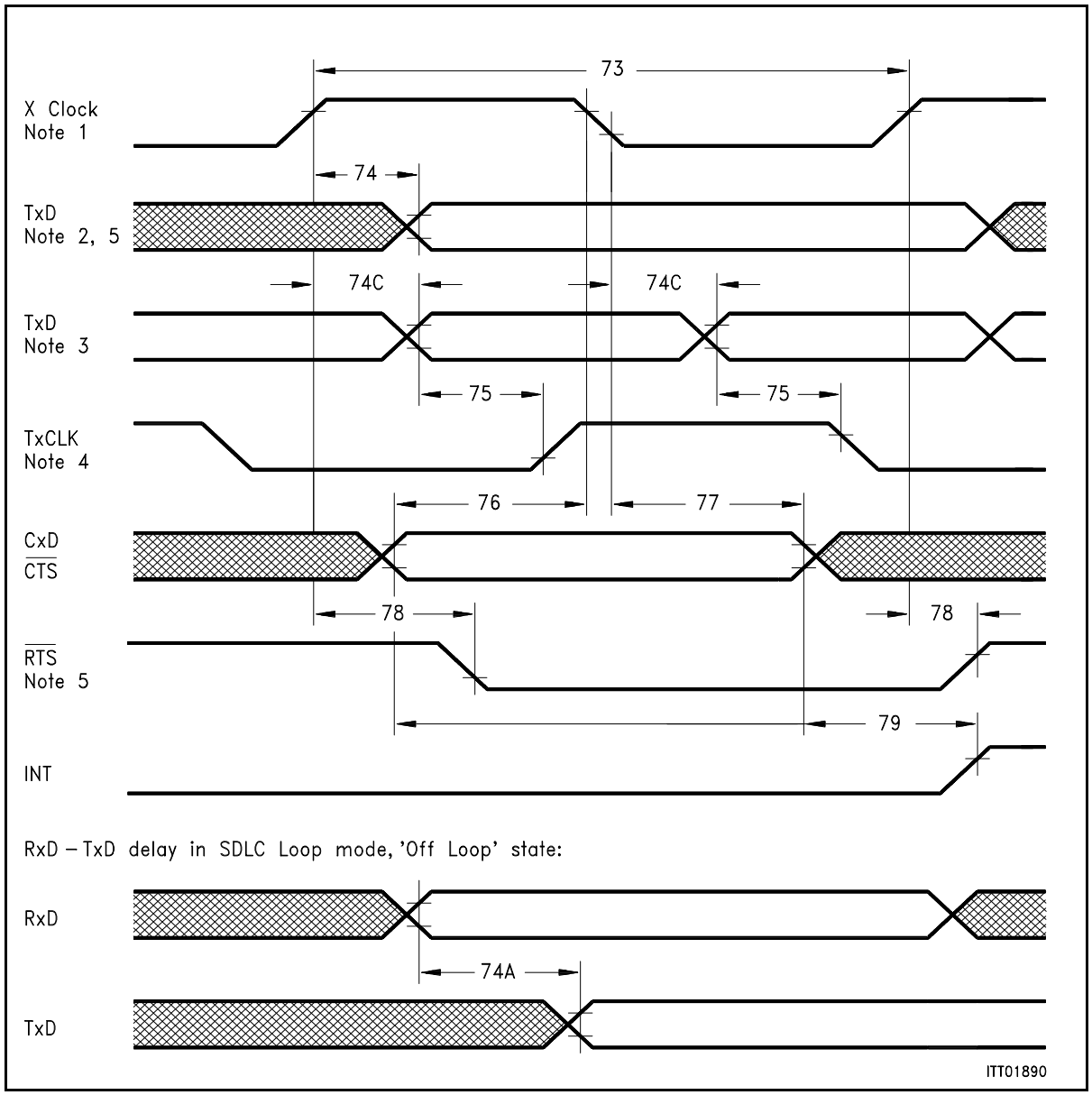

Figure 68
Transmit Cycle Timing

*Note 1: Whichever supplies the clock: externally clocked by TxCLK, XTAL1 or RxCLK or, internally derived from DPLL, BRG or BCR divider (refer to **table 5**).*

Note 2: NRZ and NRZI coding.

Note 3: FM0, FM1 and Manchester coding.

*Note 4: If output function is enabled (refer to **table 5**).*

Note 5: The timing shown is valid for normal operation and bus configuration mode 1. In bus configuration mode 2, $\overline{RTS}$ and TxD are shifted for 1/2 × clock period.

Transmit Cycle Timing

No.	Parameter		Symbol	Limit Values				Unit
				N		N-10		
				min.	max.	min.	max.	
	Transmit data rate	ext. clocked (exept ASYNC, BCR = 16)			2		10	Mbit/s
		int. clocked (HDLC, BISYNC: only DPLL)			2		2	Mbit/s
		int. clocked (all other internal modes)			2		2	Mbit/s
73	Clock period	ext. clocked (exept ASYNC, BCR = 16)	$t_{c(XC)}$	480		100		ns
		int. clocked (HDLC, BISYNC: only DPLL)		480		480		ns
		int. clocked (all other internal modes)		480		480		ns
74	Transmit data delay		$t_{p(TxD)}$		55		55	ns
74c	Transmit data delay		$t_{p(TxD)}$		75		75	ns
74A	RxD to TxD delay (SDLC loop, 'Off Loop' state		$t_{p(RxD-TxD)}$		50		50	ns
75	Clock output to transmit data delay		$t_{p(XC-TxD)}$	– 40	20	– 40	20	ns
76	Collision data and $\overline{CTS}$ setup time		$t_{su(CxD)}$	10		10		ns
77	Collision data and $\overline{CTS}$ hold time		$t_{h(CxD)}$	30		30		ns
78	Request to send delay	normal operation	$t_{p(RTS)}$		60		60	ns
		bus configuration			50		50	
79	$\overline{CTS}$ status change to INT delay		$t_{CTS-INT}$		T73 + 60		T73 + 60	ns

11.4.3.4 Strobe Timing (clock mode 1)

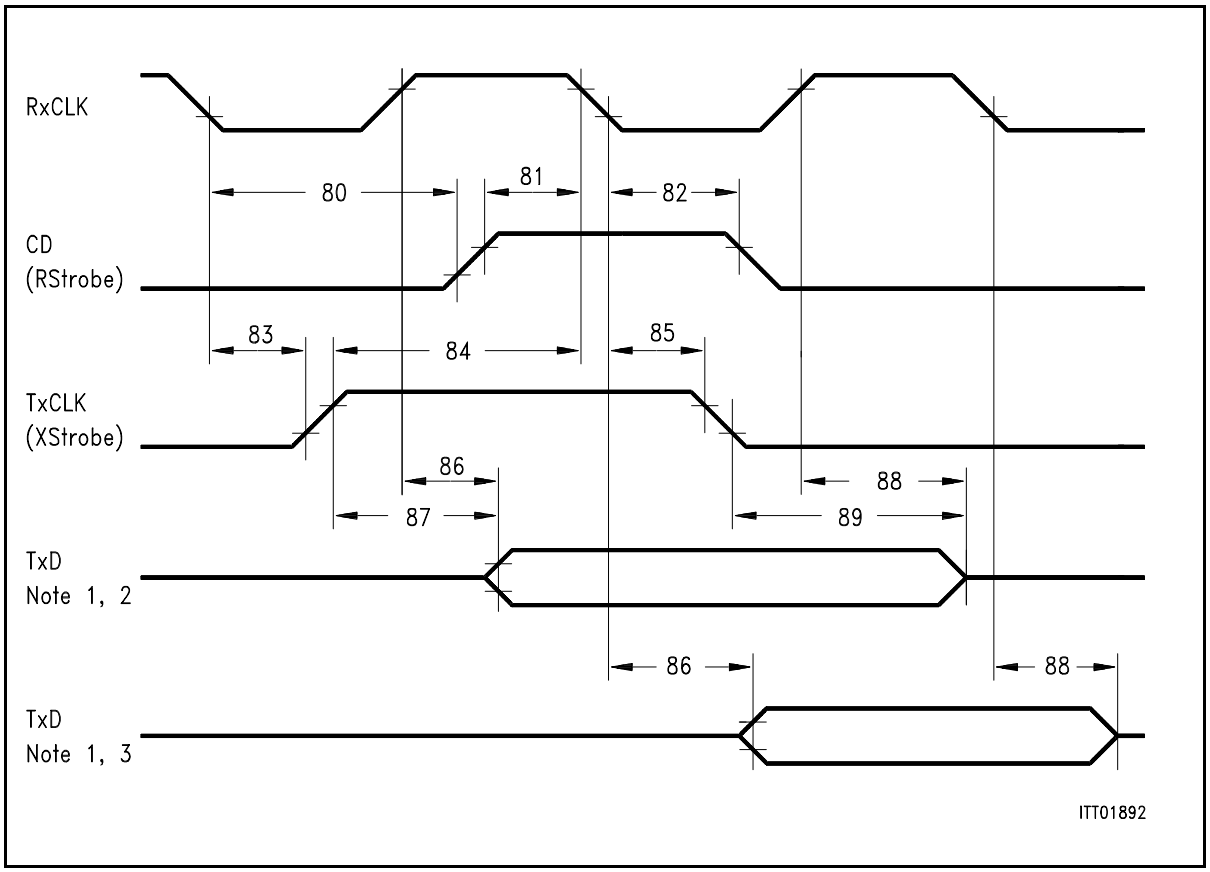

Figure 69
Strobe Timing

Note 1: High impedance if TxD is set to 'open drain' function. Otherwise, active 'high'.

Note 2: Normal operation and bus configuration mode 1.

Note 3: Bus configuration mode 2.

Strobe Timing

No.	Parameter		Symbol	Limit Values				Unit
				N		N-10		
				min.	max.	min.	max.	
80	Receive strobe delay		$t_{RxCL-RS}$	30		30		ns
81	Receive strobe setup		$t_{su(RS)}$	30		30		ns
82	Receive strobe hold		$t_{h(RS)}$	30		30		ns
83	Transmit strobe delay		$t_{RxCL-XS}$	30		30		ns
84	Transmit strobe setup		$t_{su(XS)}$	30		30		ns
85	Transmit strobe hold		$t_{h(XS)}$	30		30		ns
86	Transmit data delay	from clock	$t_{p(RxC-TxD)}$		55		55	ns
87	Transmit data delay	from strobe	$t_{p(XS-TxD)}$		50		50	ns
88	High Impedance	from clock	$t_{dis(RxC)}$		50		50	ns
89	High Impedance	from strobe	$t_{dis(XS)}$		50		50	ns

11.4.3.5 Synchronization Timing (clock mode 5)

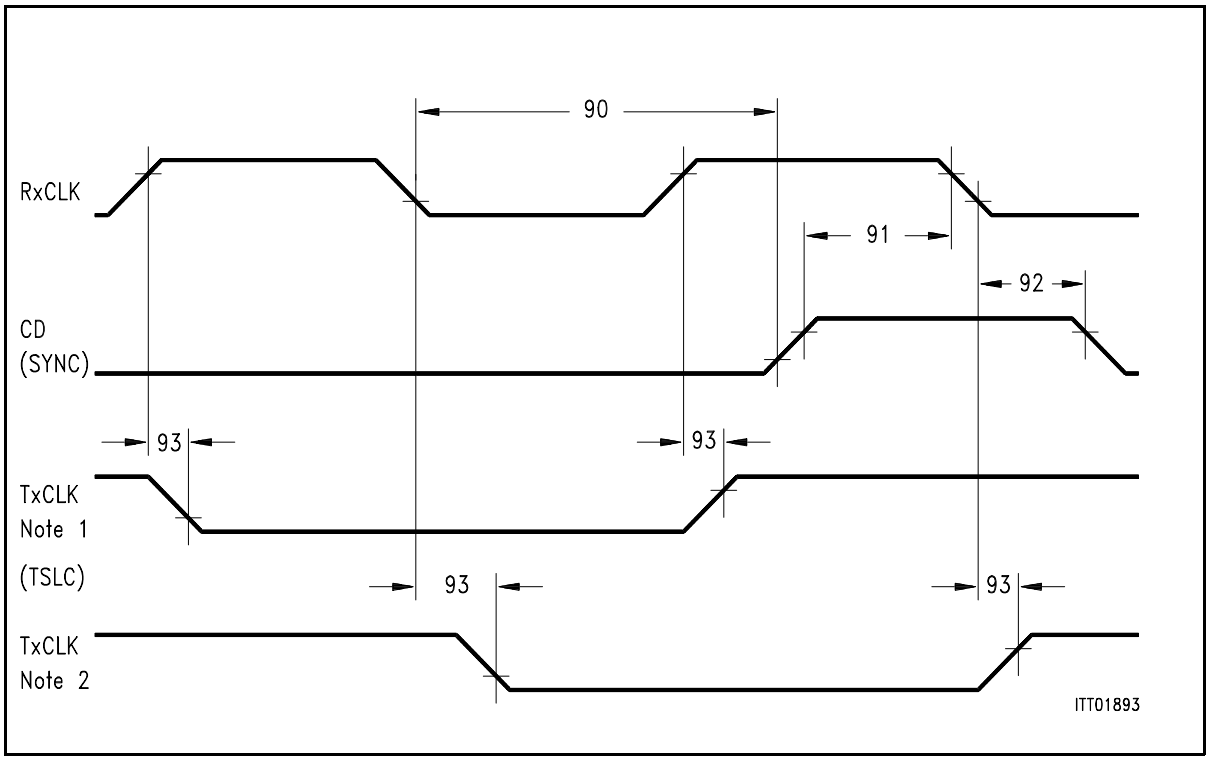

Figure 70
Synchronization Timing

Note 1: Normal operation and bus configuration mode 1.

Note 2: Bus configuration mode 2

Synchronization Timing

No.	Parameter	Symbol	Limit Values				Unit
			N		N-10		
			min.	max.	min.	max.	
90	Sync pulse delay	$t_{RxC\text{-}SYNC}$			30		ns
91	Sync pulse setup	$t_{su(SYNC)}$			30		ns
92	Sync pulse hold	$t_{h(SYNC)}$			25		ns
93	Time-slot control delay	$t_{p(TSLC)}$			20	75	ns

Note 1: Clock mode 5 only specified for versions SAB/SAF 82532 N-10 and SAB/SAF 82532 H-10, but not for versions SAB 82532 N and SAB 82532 H.

11.4.3.6 Reset Timing

Reset Timing

No.	Parameter	Symbol	Limit Values				Unit
			N		N-10		
			min.	max.	min.	max.	
80	RES pulse width	$t_{w(RES)}$	5000		5000		ns

Appendix

Upgrades of ESCC2 Version V3.2A

The ESCC2 Version V3.2A is fully upward compatible to Version V2.2. The following additional features are implemented in ESCC2:

1) Selectable enhanced resolution baud rate generator
(refer to User's Manual 07.96, p.87)

2) Selectable out-of-band flow control for transmitter and receiver in ASYNC mode
(refer to User's Manual 07.96, pp.72ff.)

3) In-band flow control transparency
(refer to User's Manual 07.96, p.75)

4) Higher transfer rate of the HDLC controller
All basic versions of the ESCC2, SAB 82532 and SAF 82532, support in HDLC mode the transfer rate of up to 2.048 Mbit/s.