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High-Performance DMA Controller for 16-bit Microcomputer Systems

SAB 82C257 Version 2.1

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1 Introduction

About this Manual Addendum

The Siemens High Performance DMA Controllers of the ADMA class are part of various high performance systems (e.g. data communication, graphics, networking, etc.) that require fast and efficient transfer of single bytes, words or doublewords or of whole data blocks up to sizes of 16 MBytes.

The initial NMOS devices have been replaced with even more powerful CMOS devices that double the maximum allowable system clock frequency while reducing the power consumption to a fraction compared to the NMOS devices. Together with the capability of 32-bit fly-by transfers and its Remote Mode stand-alone operation this makes the ADMA a powerful element of high performance systems.

Siemens offers the ADMA in

- the standard full featured version, the SAB 82C258A, providing the full power of the ADMA architecture, and
- the function reduced version, the SAB 82C257, for smaller and/or cost sensitive applications.

The SAB 82C257 is a 100% subset of the SAB 82C258A which means full compatibility on three levels:

- **Pin compatibility:** both versions use the same package with the same pin-out
- **Software compatibility:** both versions execute a common set of identical instructions with the same basic operating modes
- **Hardware compatibility:** both versions can be used in the same environment (bus interface, peripheral interface).

So the differences between the two devices do not include changes to parts of the architecture but represent only reductions of functionality. This reduction of features also includes the associated resources, i.e. control bits, registers, etc.

This compatibility opens up a straight forward upgrade path from the function reduced SAB 82C257 to the full featured SAB 82C258A in case the application's performance must be increased.

The ADMA architecture and its performance is described in the standard User's Manual

SAB 82258A/SAB 82C258A
Advanced DMA Controller for 16-bit Microcomputer Systems (ADMA) 9.90.

Ordering No. B158-B6305-x-x-7600

This Addendum is for SAB 82C257 users and describes the differences between the standard ADMA and the “econo”-version SAB 82C257 as well as their common features.

It is structured according to the structure of the SAB 82C258A User’s Manual.
This structure is not always necessary for this Addendum but it allows an easy correlation to the respective sections in the SAB 82C258A User’s Manual that describe the mentioned functions or features in detail.

2 Overview

The SAB 82C257 is a high performance general purpose DMA controller taylored for efficient high speed data transfer between peripheral devices and memories. As the SAB 82C257 is a function reduced DMA controller of the ADMA class it provides many of the performance oriented features of the ADMA architecture. It also can be directly connected to industry standard 16-bit processors, or operate autonomously in remote mode. The SAB 82C257 controls 4 independent high speed DMA channels, has several modes to generate interrupts and handles command chaining, data chaining and conditional execution of command blocks. While the extended features of the ADMA architecture like compare (match/mismatch), verify, 32-bit transfer, etc. are not provided, the functions listed above are 100% compatible with the SAB 82C258A, the full featured version.

The brief survey of the SAB 82C257’s features summarizes its functionality:

- 16-bit DMA controller for 16-bit family processors (286, 186/188, 86/88)
- 4 independent channels
- 16 MByte addressing range
- 16 MByte byte count
- Memory based communication with CPU
- Transfer rates up to 10 MByte/sec
- Single-cycle and two-cycle transfer
- Automatic chaining of command blocks
- Automatic chaining of data blocks
- Local and remote (standalone) mode
- Support of 16-bit and 8-bit buses
- Programmable synchronization modes
- Programmable control of channel priorities
- Direct and fast CPU/channel communication

The Differences between SAB 82C257 and SAB 82C258A include the following items:

- No Multiplexer channel,
  Data transfer on 4 high-speed selector channels.
- No compare function,
  Transferred data cannot be matched/mismatched with a given pattern.
- No verify function,
  Data blocks cannot be compared to each other.
- No data translation,
  Data bytes cannot be transformed during the transfer.
- No order reverse transfer,
  Combination of incrementing and decrementing pointers is not supported.
- No 32-bit fly-by transfers,
  Bytes and/or words can be transferred.
- No extended status block,
  Pointers and byte count after transfer cannot be stored, but are available from registers only.
- Restricted condition code,
  Conditional execution of type 2 commands possible on byte count end and external termination only (match and verify not provided).

Operations

Although the functionality of the SAB 82C257 is reduced by the extended On-the-Fly operations known from the SAB 82C258A, it is fully upward compatible. Channel programs written for the SAB 82C257 need not be modified when upgrading the system to the SAB 82C258A. It is possible to easily activate the additional features in this case using structured extensions to the existing channel programs, however. The SAB 82C257 executes both modes of data chaining (list chaining and linked list chaining) without any restrictions. This is advantageous especially in data communication applications. Fast channel switching is executed between all 4 channels of the SAB 82C257 without any delays. Depending on the channel requests and the priority scheme used, as for example

- fixed priority for all channels, or
- rotating priority for all channels

the data transfer can be switched from one channel to another after each bus cycle. In case of rotating priority there is not discrimination of any channel. Thus a data transfer rate of 2.5 MByte/s can be processed per channel if all channels are active.

External synchronization allows the data source or the destination to trigger a data transfer (single-cycle or two-cycle) as it is required. Data may also be transferred „free-running“, i.e. without external synchronization, which is useful e.g. for memory-memory transfers.

The SAB 82C257 is internally divided into the functional units depicted schematically in the figure below. The SAB 82C257 block diagram also includes the major logic blocks and some of the accessible, user visible registers. The data interconnection paths are also shown. Not shown are the various control signals between the functional units. A detailed description of the logic blocks and their functions can be found in the respective sections of the SAB 82C258A User's Manual.

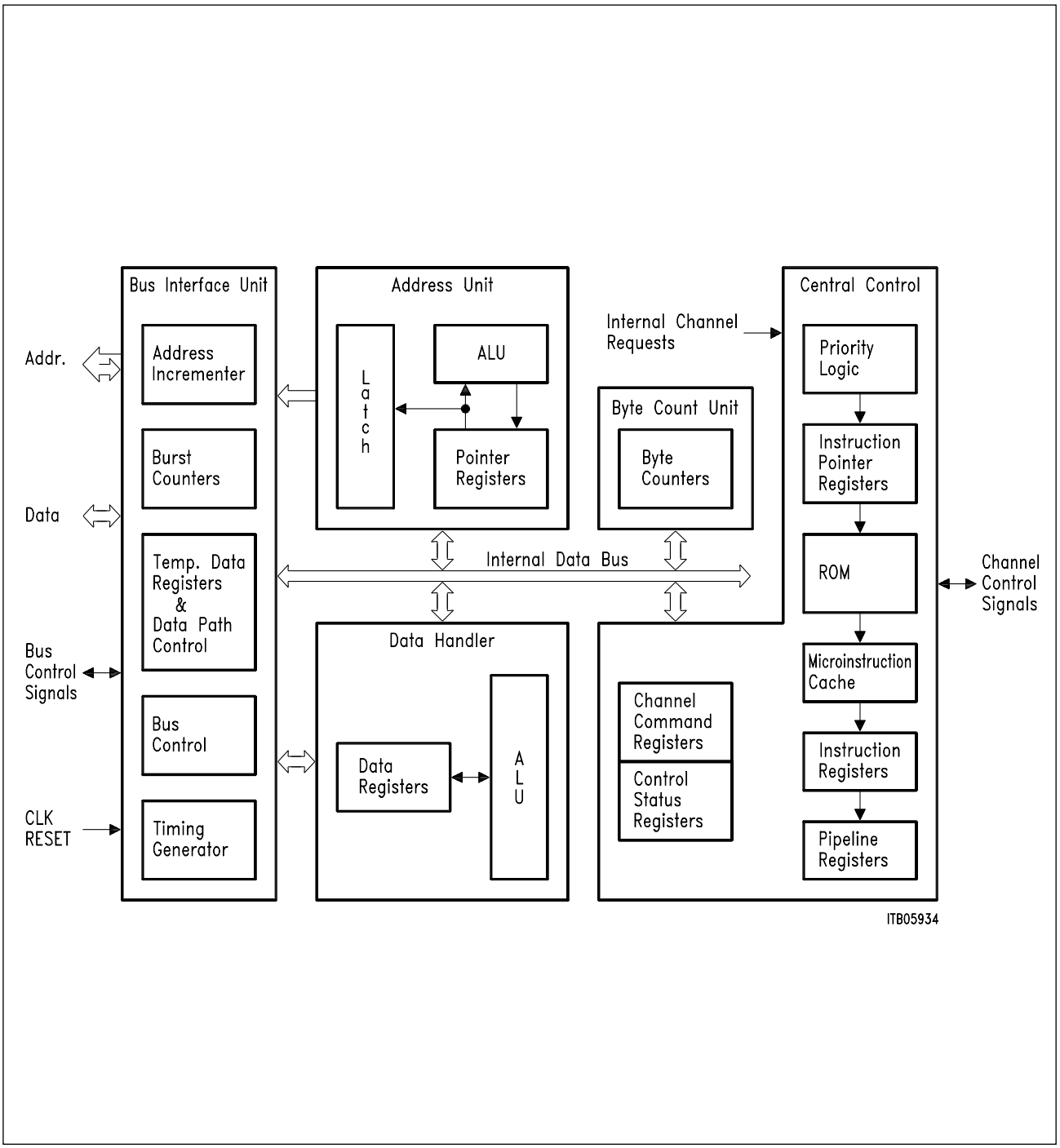

Figure 1
SAB 82C257 Block Diagram

Upgradability

The SAB 82C257 provides complete upward-compatibility with the Advanced DMA controller SAB 82C258A. The SAB 82C258A offers enhanced functions (i.e. data handling, improved flexibility of DMA channels, etc.) beyond the performance of the SAB 82C257 and is also available in higher clock speed versions. Each system or application can easily be upgraded, as the SAB 82C257 provides compatibility on any level.

Interfaces

Both devices have identical bus interfaces for 286 mode, 186 mode and remote mode. Therefore both DMA controllers fit into all the processor systems described. The DMA interfaces are compatible as well. Upgrading a system hardware is no problem at all, because hardware redesigns in existing systems are not required due to compatibility (except for enhanced functions, of course).

Programming Technique

Portating system software to an SAB 82C258A system is also no problem. The arrangement of the SAB 82C257 control registers and even the bit arrangement within these registers can be found within the SAB 82C258A as well.

The locations of the control bits have been chosen such that upgrading is allowed directly. If the control registers and the bits are used as described in the SAB 82C258A User's Manual the programmer can be sure that any software (channel programs including data chain lists, etc.) written for the SAB 82C257 will run on the SAB 82C258A without requiring changes.

Note: Changing the channel programs will be necessary, of course, when utilizing the additional functional features of the SAB 82C258A!

Summary

In addition to offering excellent performance the SAB 82C257 opens the door to more advanced DMA controllers. For the reasons pointed out in this section the SAB 82C257 is the ideal component for getting into touch with the DMA controllers of the ADMA class (please also refer to section "Reflections on Compatibility").

3 Operating Modes

The SAB 82C257 may be used in all bus configurations described for the SAB 82C258A. The peripheral subsystem consists of up to 4 high-speed peripherals. The multiplexer channel accepting requests from up to 32 low-speed peripherals is not available in the SAB 82C257.

32-bit systems can use the SAB 82C257 in a limited way. While the SAB 82C258A can control doubleword fly-by transfers the maximum data size for the SAB 82C257 is 16-bit words. It can be used to perform 32-bit doubleword transfers when its address bus is connected to the system shifted by one. However, this requires to modify the addresses and byte counts for the command blocks.

4 Bus Operation

The SAB 82C257's bus interface is absolutely compatible with the SAB 82C258A's bus interface. The SAB 82C257 also executes identical bus cycles with the exception of

- compare and match operations
- 32-bit fly-by transfers
- multiplexer channel IO acknowledge cycles.

The passive bus cycles are identical i.e. the SAB 82C257 is accessed in the same way as the SAB 82C258A. The SAB 82C257 allows system clock frequencies of up to 10 MHz i.e. input clock frequencies of up to 20 MHZ in 286 mode and remote mode, up to 10 MHz in 186 mode.

5 Communication Mechanism

The memory based communication with the SAB 82C257 uses standard command blocks that contain all necessary information to execute a specific operation. The last word of each type 1 command block (data transfer) receives the contents of the appropriate channel status register once the command block has been completely executed.

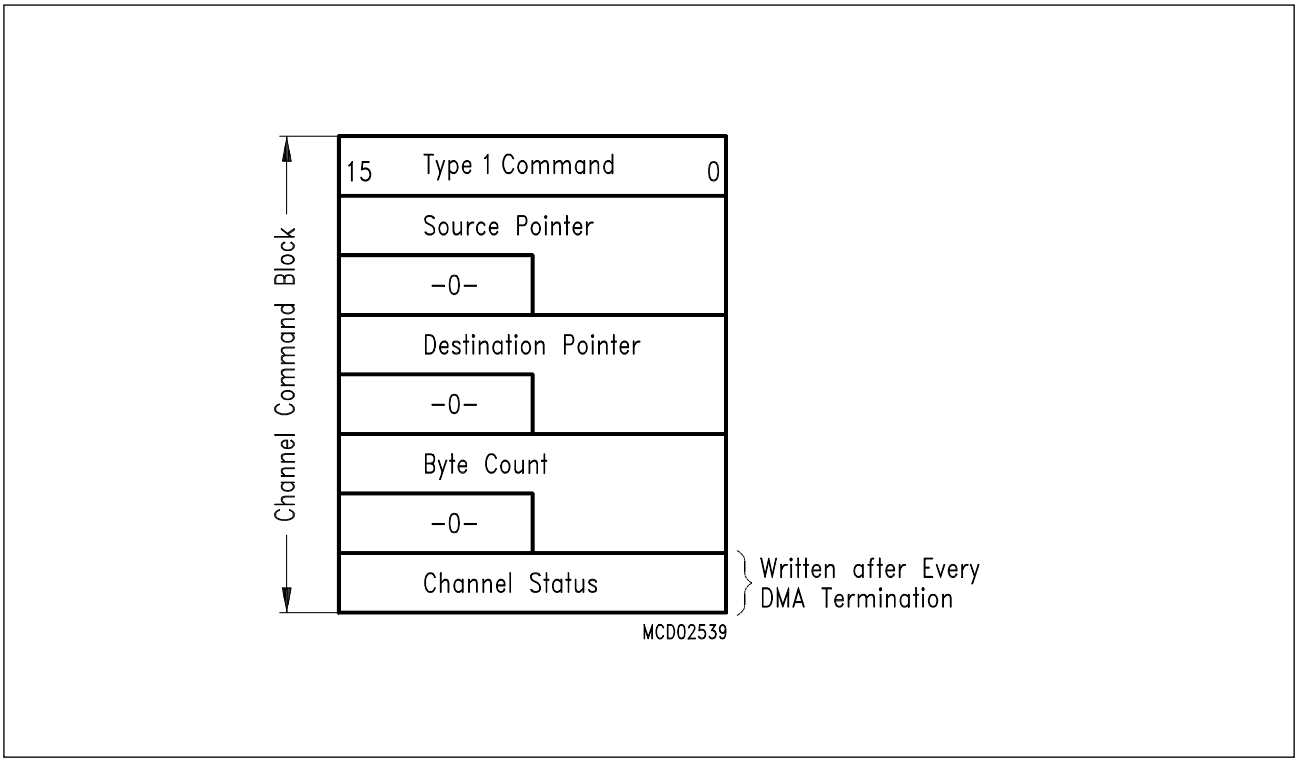

Figure 2
SAB 82C257 Status Fields

This allows the CPU to examine the execution status of a complete command chain e.g. for debugging or error recovery analysis. The extended status block containing the pointers and the byte count upon termination is not available with the SAB 82C257.

6 Programming and Control

The SAB 82C257 employs a large number of programmable, user-accessible and logically ordered registers to control its operation and maintain address pointers, status information, etc.

These registers are classified as:

- **General registers:** A set of five registers used for all 4 channels.
- **Channel registers:**A set of 32 registers.
  For each channel there is a separate, independent set of 8 channel registers.

All these user-visible registers can be read or loaded by the CPU although the SAB 82C257 will load most of them itself during the setup routine after a channel start. All registers can be accessed bytewise or wordwise, mostly for setup and test purposes.

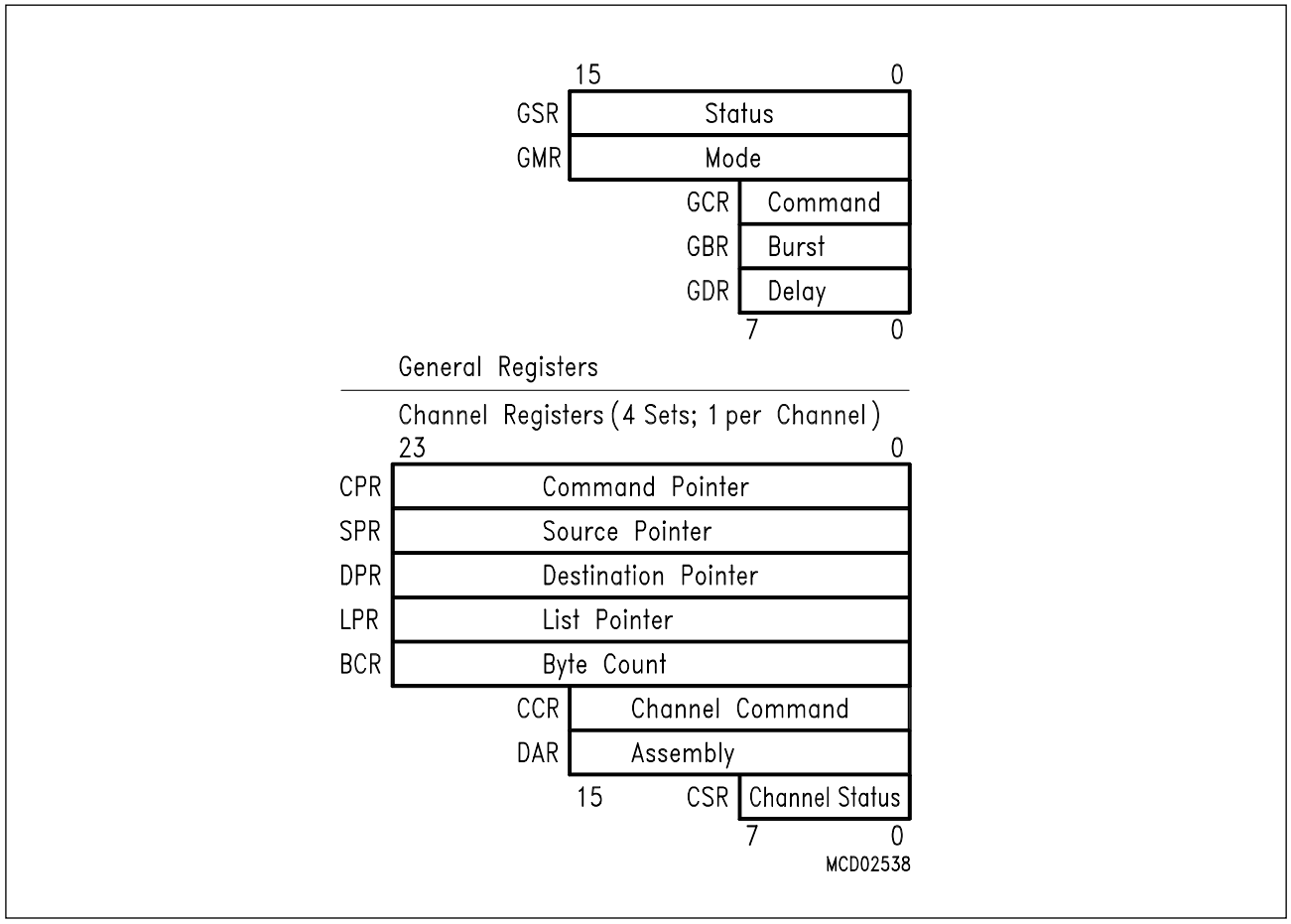

Figure 3
Register Set

Note: Not defined locations are reserved. They should not be addressed to prevent the occurring of undefined effects. This also applies to those registers and bits which are not defined or are reserved in the SAB 82C257 but will be provided in the SAB 82C258A. This is very important for a safe upgrade to the SAB 82C258A.

Register Address Arrangement

Address Bits 5...0		Address Bits 7,6			
		0 0	0 1	1 0	1 1
	00	GCR			
	02				
	04	GSR			
	06				
	08	GMR			
	0A	GBR			
	0C	GDR			
	0E				
	10	CSR 0	CSR 1	CSR 2	CSR 3
	12	DAR 0	DAR 1	DAR 2	DAR 3
	14				
	16				
	18				
	1A				
	1C				
	1E				
	20	CPR L0	CPR L1	CPR L2	CPR L3
	22	CPR H0	CPR H1	CPR H2	CPR H3
	24	SPR L0	SPR L1	SPR L2	SPR L3
	26	SPR H0	SPR H1	SPR H2	SPR H3
	28	DPR L0	DPR L1	DPR L2	DPR L3
	2A	DPR H0	DPR H1	DPR H2	DPR H3
	2C				
	2E				
	30	LPR L0	LPR L1	LPR L2	LPR L3
	32	LPR H0	LPR H1	LPR H2	LPR H3
	34				
	36				
	38	BCR L0	BCR L1	BCR L2	BCR L3
	3A	BCR H0	BCR H1	BCR H2	BCR H3
	3C	CCR L0	CCR L1	CCR L2	CCR L3
	3E	CCR H0	CCR H1	CCR H2	CCR H3

General Registers

GSR = General Status Register
GMR = General Mode Register
GCR = General Command Register
GBR = General Burst Register
GDR = General Delay Register

n = Channel Number
L = Low Word
H = High Byte

Channel Registers

CPR = Command Pointer Register
SPR = Source Pointer Register
DPR = Destination Pointer Register
LPR = List Pointer Register
BCR = Byte Count Register
CCR = Channel Command Register
DAR = Data Assembly Register
CSR = Channel Status Register

Note: Some register locations which are not specified are used for internal working registers. Therefore these locations should never be accessed and - what is even more important - should never be written to. This applies especially for those SAB 82C258A register which are not defined in the SAB 82C257.

Control Register Differences

The following registers of the SAB 82C257 are different from the ones of the SAB 82C258A.

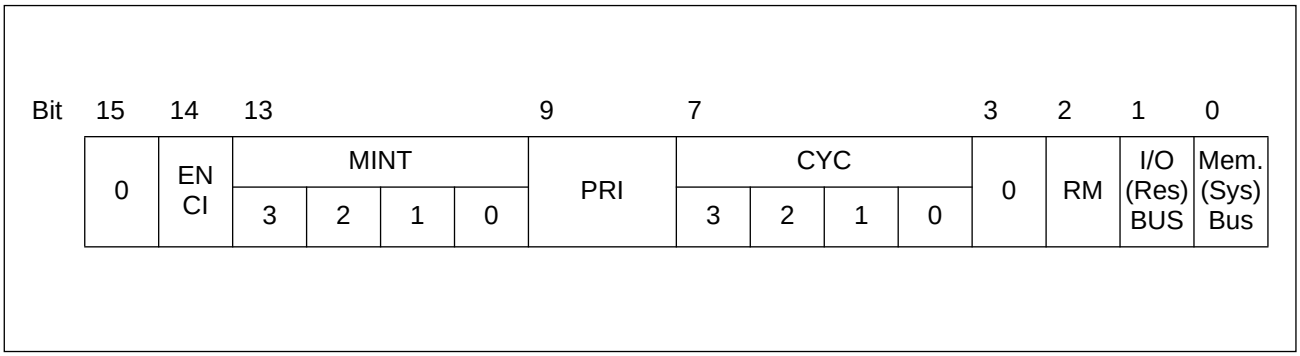

Figure 4
General Mode Register Fields

Bit 3 could activate the multiplexer channel in the SAB 82C258A and therefore must be zero in the SAB 82C257.

The priority bitfield (PRI) selects the channels' priority:

PRI	Priority
0 0	All channels have fixed priority (0 = highest, 3 = lowest).
0 1	**Reserved.** These combinations are only used in the SAB 82C258A and therefore are reserved in the SAB 82C257.
1 0	
1 1	All channels have rotating priority.

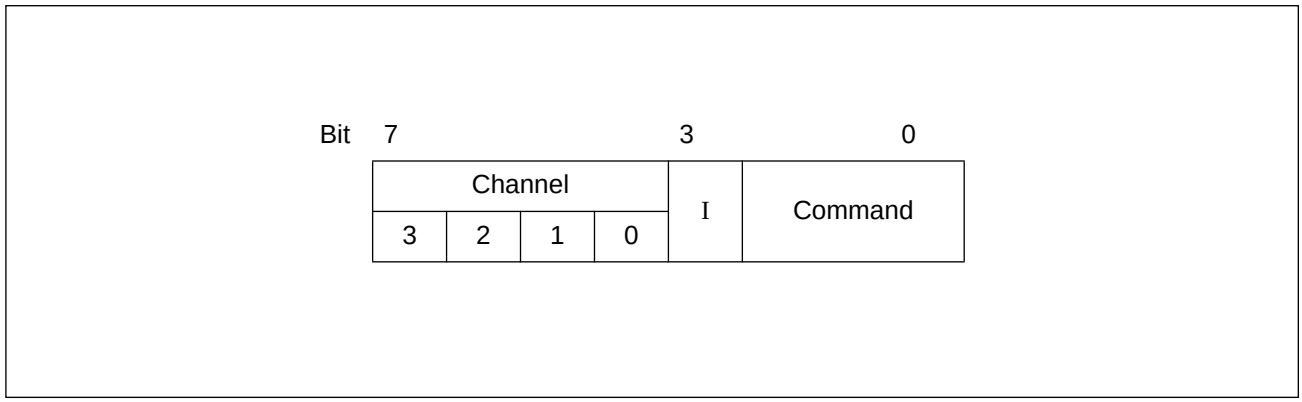

Figure 5
General Command Register Fields

The COMMAND bitfield selects the general command for the channels of the SAB 82C257.

Bitfield	Channel Command
0 0 0	NOP (no operation)
0 0 1	CONTINUE channel(s) operation after it has been stopped by the STOP command
0 1 0	START channel(s), command blocks in system/memory space
0 1 1	START channel(s), command blocks in resident/IO space
1 0 0	STOP channel(s)
1 0 1	Reserved. Not defined in the SAB 82C257.
1 1 0	Reserved. Not defined in the SAB 82C257.
1 1 1	HALT/single step channel(s).

Channel Command Blocks

There are two basic types of channel commands:

- **Type 1** channel commands for data transfers
- **Type 2** channel commands for command chaining control.

The SAB 82C257 is able to execute all kinds of type 2 channel command blocks and standard (short) type 1 command blocks containing

- a 16-bit type 1 channel command
- a 24-bit source pointer
- a 24-bit destination pointer
- a 24-bit byte count (block length)
- a 16-bit status word updated by the SAB 82C257 after DMA operation.

The command block extension and the extended status block are not available.

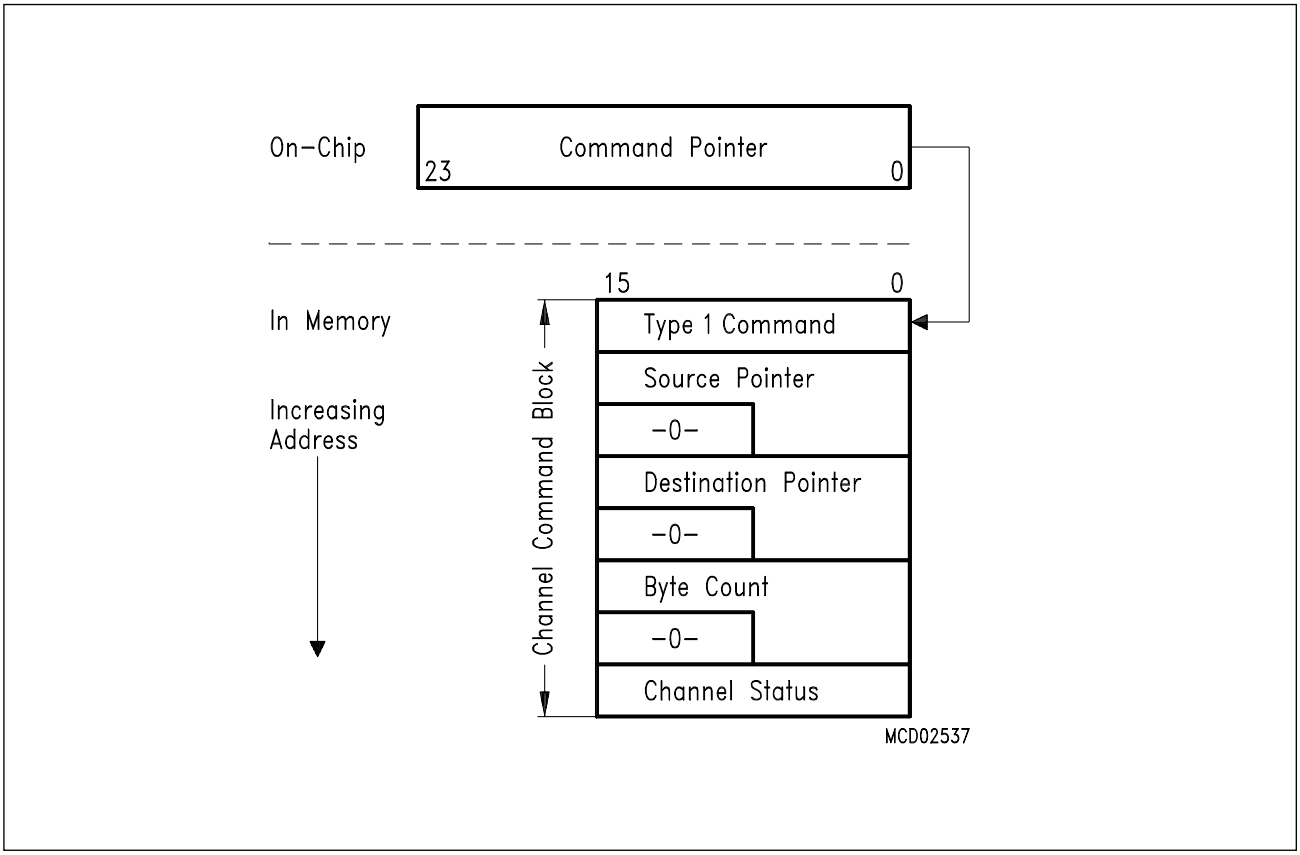

Figure 6
Type 1 Channel Command Block

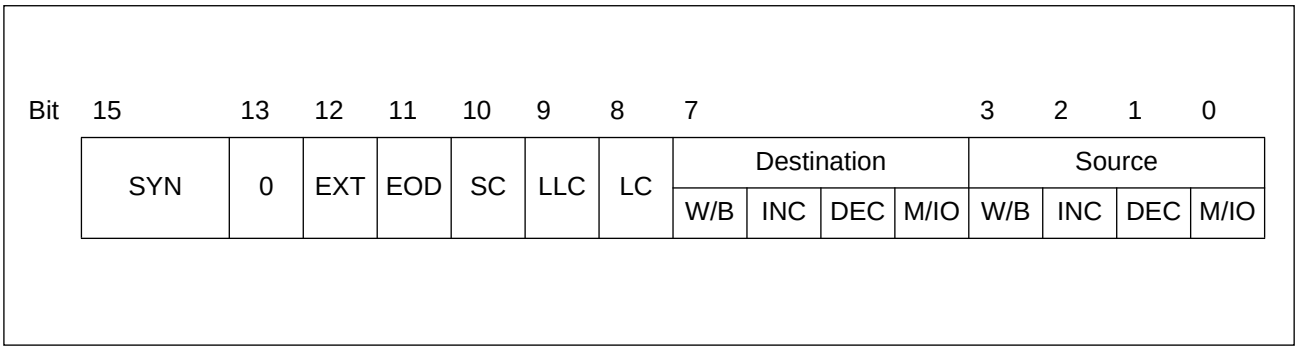

Figure 7
Type 1 Command Fields

All possible type 2 command blocks can be used. The conditional execution of type 2 blocks is limited to

- BC: byte count exceeded, and
- ET: external termination of block transfer.

The other two condition bits are reserved as the associated functions (match and verify) are not available.

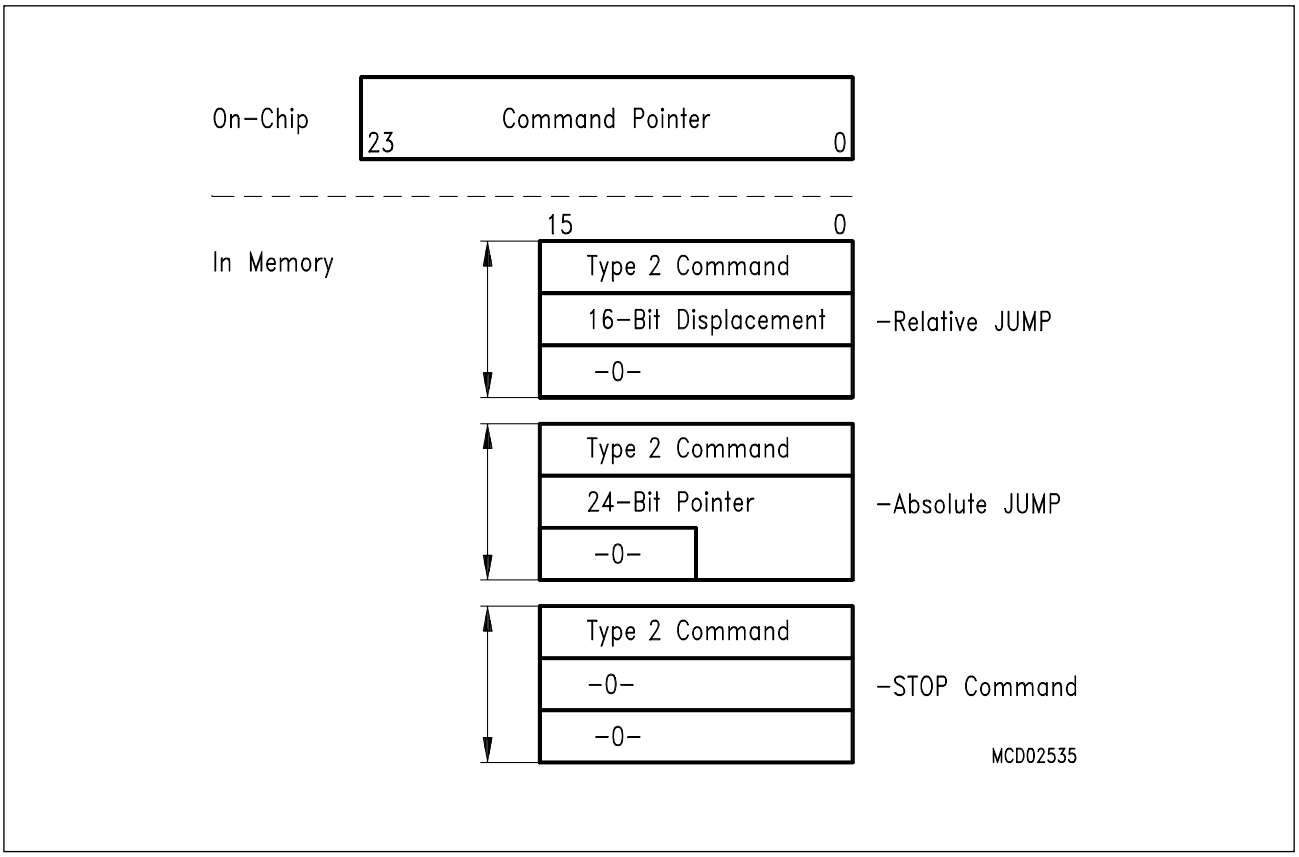

Figure 8
Structure of Type 2 Channel Commands

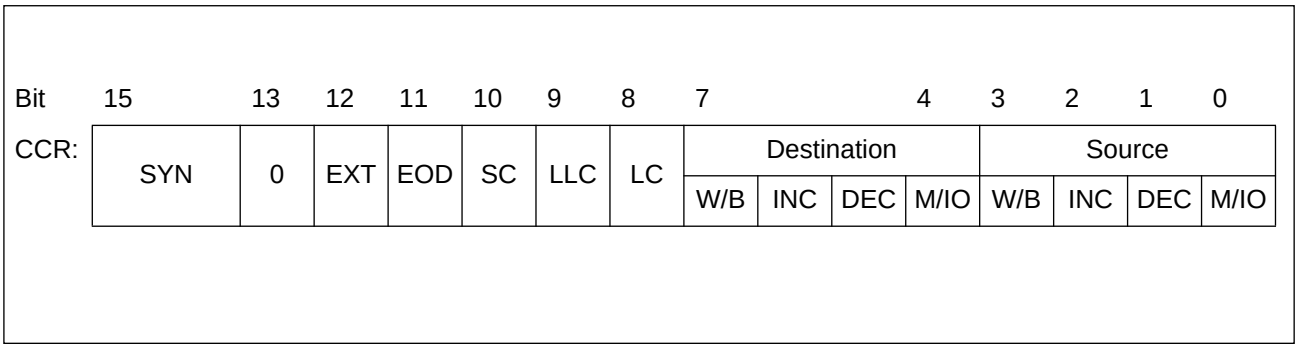

Figure 9
Type 1 Channel Command Register Fields

Bit 13 would activate the channel command extension in the SAB 82C258A and therefore must be zero in the SAB 82C257.

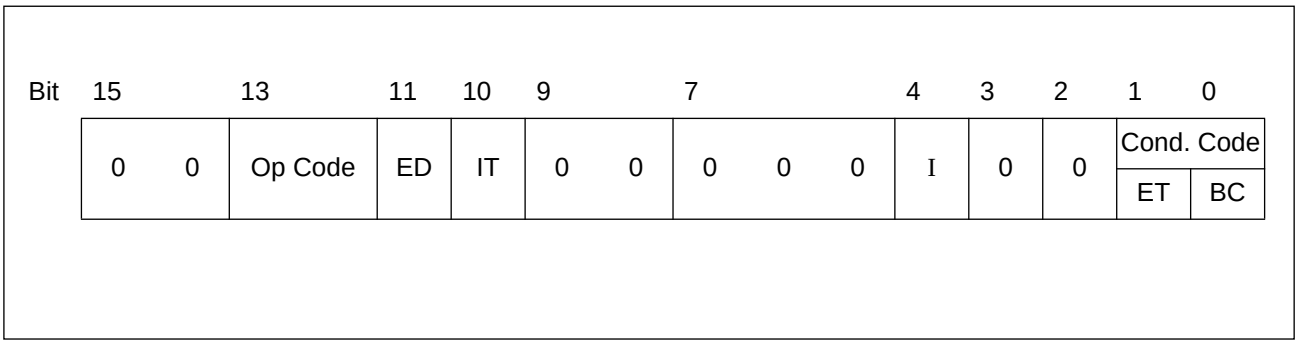

Figure 10
Type 2 Channel Command Register Fields

Condition code bits 2 and 3 refer to extended operations and therefore are reserved in the SAB 82C257.

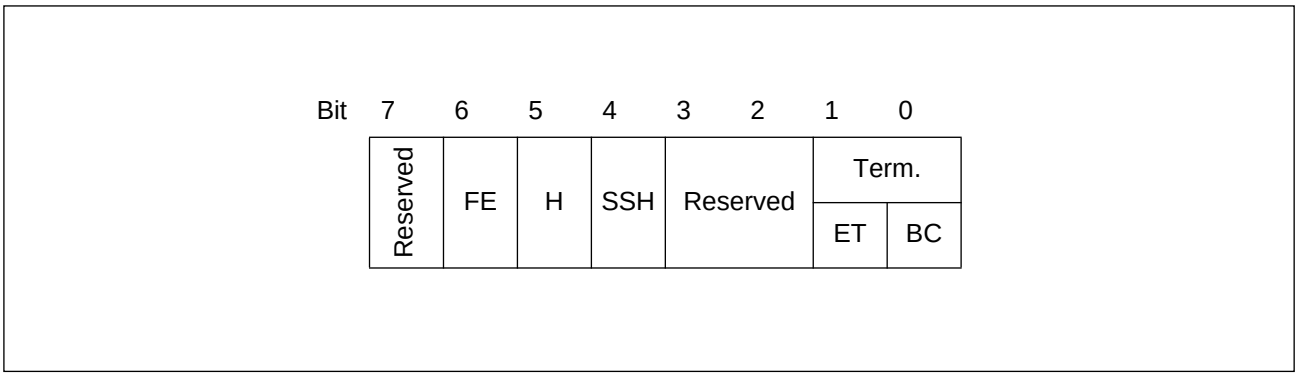

Figure 11
Channel Status Register Fields

Bits 2 and 3 indicate a termination due to extended operations and therefore are reserved in the SAB 82C257.

Command chaining is executed in exactly the same way as in the SAB 82C258A.

Setup Routine

As the SAB 82C257 only executes standard type 1 command blocks the setup routine will never load any parameters for extended operations, i.e. it will always switch from step 8 to step 13 (please refer to the respective table in the SAB 82C258A User's Manual).

Reflections on Compatibility

When designing software to operate the SAB 82C257 in a system environment you might want to provide compatibility with other DMA controllers, especially with the SAB 82C258A. This can be achieved by observing a few principles while writing your own software. Special attention should be paid to the 24-bit quantities (pointer, byte count) used with the SAB 82C257. 24-bit quantities within command blocks are placed into two 16-bit words with the most significant byte (MSbyte) left unused. 24-bit registers will normally be accessed as 16-bit word and consecutive byte.

For reasons of compatibility with other DMA controllers it is recommended to treat the MSbytes as zeros.

This means that within command blocks these MSbytes should be set to zero or discarded, respectively. While writing or reading SAB 82C257 registers only word accesses should be used. Hereby the MSbytes again should be zero (write) or discarded (read), respectively.

Also reserved control bits of the SAB 82C257 should be cleared (zero) when written and discarded/ignored when read. Undefined or explicitly reserved register locations should be ignored when read and never be written to.

By observing these principles you will be able to run user software written for the SAB 82C257 also on the SAB 82C258A or other DMA controllers (e.g. 32-bit controllers) without changes. This applies to control programs executed by the CPU as well as to channel programs executed by the SAB 82C257.

Note: Software designed uniquely for the SAB 82C257, of course, is not subject to the above rules. No compatibility, however, will be provided in this case. The SAB 82C257 itself will not bother if the MSbytes contain something else than zeros. Information contained in the MSbytes, however, will be lost or invalid. Writing to undefined locations in the SAB 82C257 may lead to unexpected system behaviour.

7 DMA Transfer

The SAB 82C257 performs two transfer modes:

- **Forward Transfer Mode**
  Data transfer with incrementation of source pointer and/or destination pointer (both pointers may be steady)
- **Reverse Transfer Mode**
  Data transfer with decrementation of source pointer and/or destination pointer (one pointer may be steady)

Note: The data cycle control of the SAB 82C257 does not support Byte/Word-Order Reverse Transfer Modes.

No data cycles for the SAB 82C257 are defined that involve match, verify and translate functions or control doubleword transfers. All data chaining modes are provided, however.

Termination of Data Transfer

A data transfer can be terminated due to one or two of the following conditions:

1. Byte Count End

Condition ①: Byte count is zero and no data chaining is enabled (standard termination condition)

Condition ②: Data chaining is enabled and the new fetched byte count is zero.

2. External Termination

Condition ⑤: External termination via the channel's $\overline{\text{EOD}}$ line if enabled by bit EXT in the CCR.

Note: The above condition numbering refers to the SAB 82C258A User's Manual. Conditions 3 and 4 are not provided.

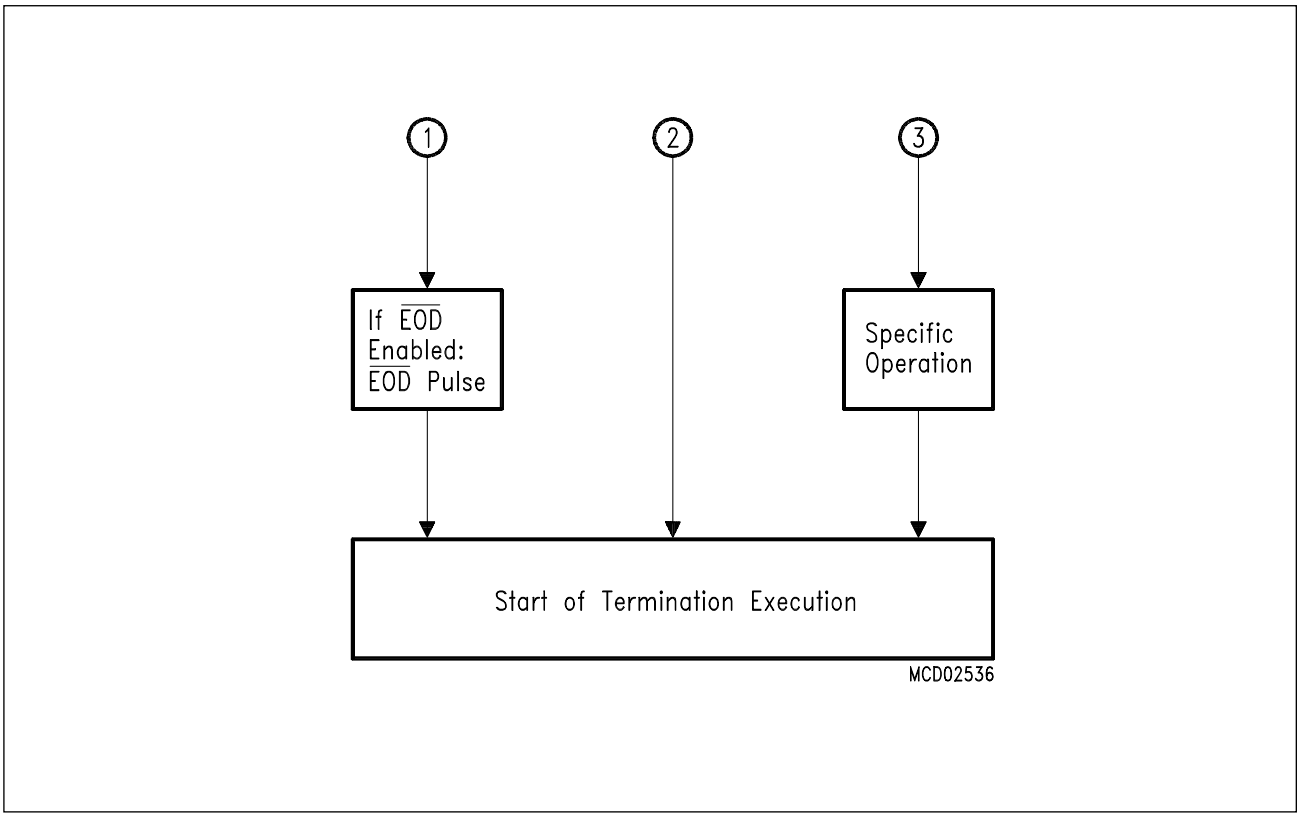

Figure 12
Termination Conditions

Execution of Transfer Termination

1. Change channel status - indicated by DMST bits in the CCR - from “DMA in progress” to “organizational processing” (masking of following data requests).
2. ---
3. Generation of termination status bits (BC, ET) in the channel status register (CSRn). One or two of the termination status bits can be activated.
4. Store CSR into status word location of type 1 channel command block.
5. ---
6. Increment channel command pointer in CPR by 16.
7. Without change of the channel’s status bits in GSR (i.e. channel still remains in status “organizational processing”:
   Fetch next type 1 or type 2 channel command block with the new command pointer (execution of command chaining).

The execution of termination belongs to the last data transfer request or to external $\overline{\text{EOD}}$ request. Therefore no extra priority request control is performed for termination execution. With the execution of transfer termination the type 1 channel command (transfer command) processing is finished.

8 Concurrent Channel Operation

The SAB 82C257's lock mechanism combines the following "unseparable bus cycles":

- Read 24-bit pointer or byte count from control space
- Word transfer on odd addresses where each transfer is a byte.

The priority of concurrent channels can be controlled in two ways:

Bitfield PRI	Priority of Channel 3 2 1 0	Comments
0 0	3 2 1 0	All channels have fixed priority (channel 0: highest priority).
0 1 1 0	- - - - - - - -	Not valid!
1 1	R R R R	All channels have rotating priority (i.e. all channels appear to have the same priority).

Priority Control of Requests

Types of Channel Requests	Priority
Channel STOP (command from CPU via GCR).	0
External asynchronous termination request (via $\overline{\text{EOD}}$).	1
Internal CONTINUE request of previously interrupted sequence.	2
Internal (without synchronization) data service request.	4
External (with synchronization) data service request.	4
Channel WAIT (idle).	5

Note: The priority numbers in the above table refer to the SAB 82C258A User's Manual. Please note that level 3 is missing.

The slave operations where the SAB 82C257 is addressed by the CPU have highest priority of all SAB 82C257 activities. The SAB 82C257 is immediately halted (remote mode) for taking over the slave part of the bus cycle transaction.

9 Interrupt Control

The same interrupt generation modes are provided as in the SAB 82C258A except for the multiplexer channel interrupts (9.7) which do not apply for the SAB 82C257.

10 Error Detection

All error conditions that refer to extended operations (match, verify, translate) or the multiplexer channel (not indicated fatal errors) do not apply for the SAB 82C257.

11 Operating Instructions

Of course the basic programming techniques described in this chapter of the SAB 82C258A User's Manual also apply to the SAB 82C257 and show how to develop channel programs. Please note, however, that many of the shown command blocks in the examples use extended features (like match) and therefore cannot be executed by the SAB 82C257.

Channel programs for the SAB 82C257 are restricted to data transfers (with all its variations including data chaining) and command chaining (conditional or unconditional).

Performance

The **Latencies** for setup and execution of a command block must be considered for short type 1 blocks only and no multiplexer channel.

The **Transfer Rates** given for single-cycle byte/word transfer without mask/compare or verify operations and for two-cycle transfer without data translation are valid. Please note that the clock frequency range for the SAB 82C257 is limited compared to the SAB 82C258A's.