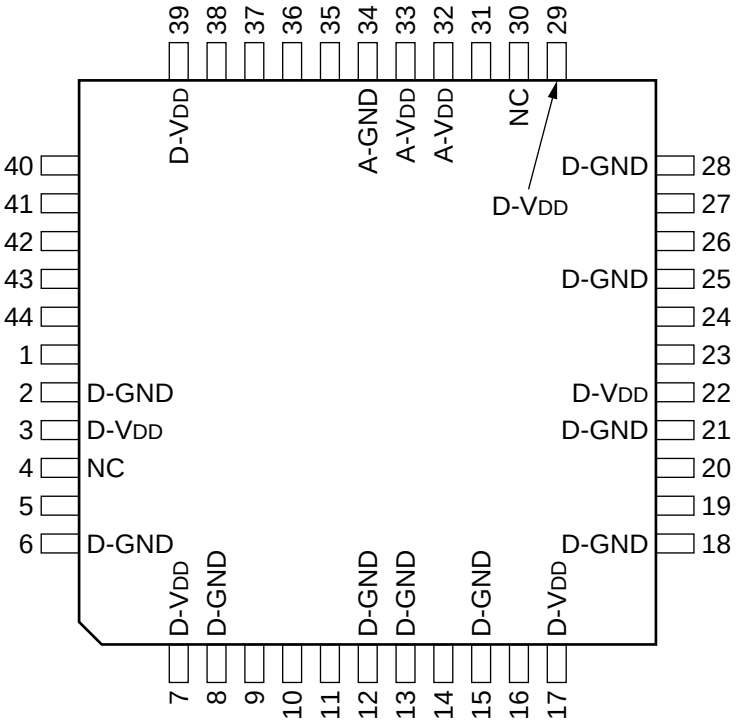
C-MOS CLOCK GENERATOR

—TOP VIEW—



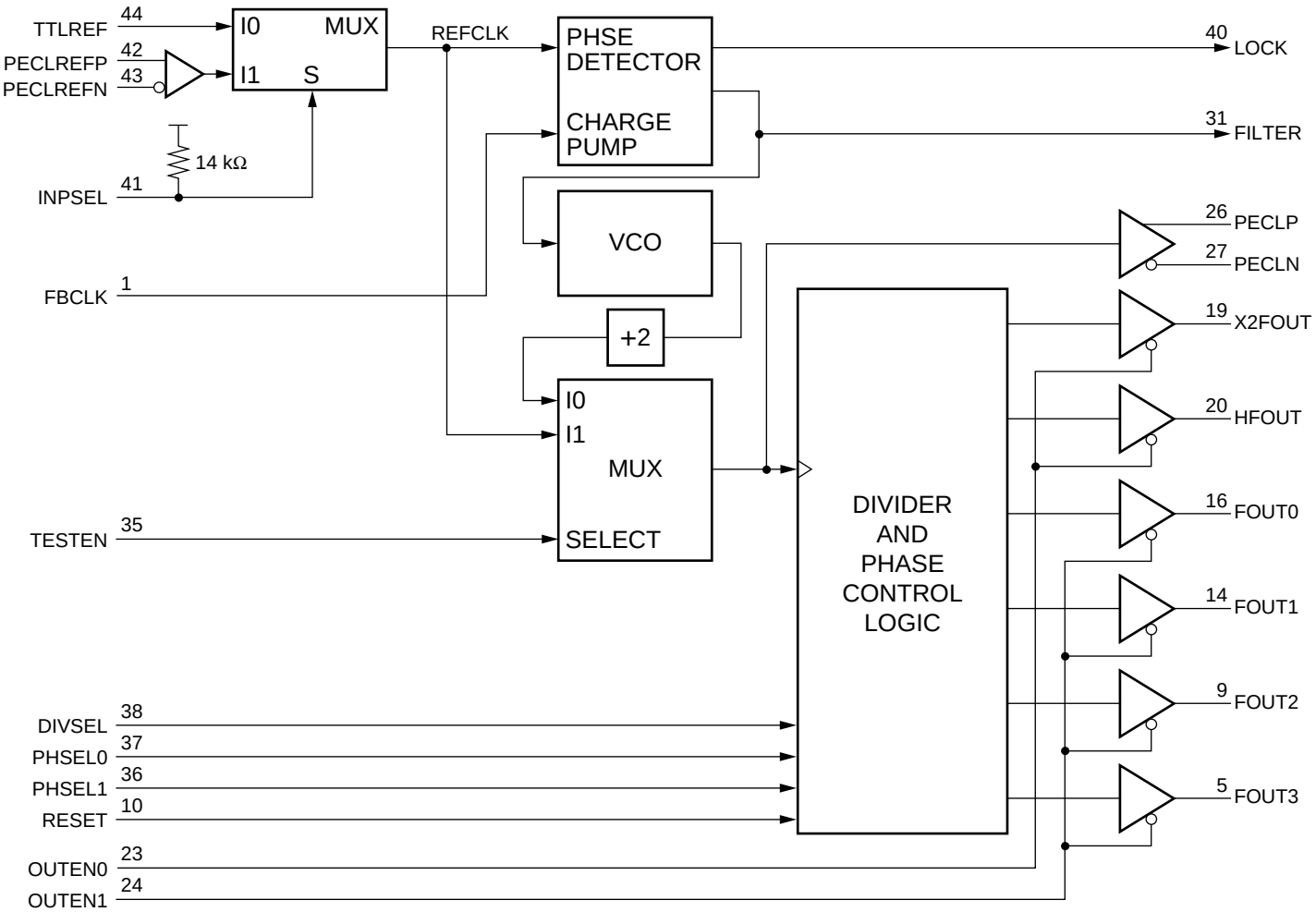
PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	FBCLK	12	—	D-GND	23	I	OUTEN0	34	—	A-GND
2	—	D-GND	13	—	D-GND	24	I	OUTEN1	35	I	TESTEN
3	—	D-VDD	14	O	FOUT1	25	—	D-GND	36	I	PHSEL1
4	—	NC	15	—	D-GND	26	O	PECLP	37	I	PHSEL0
5	O	FOUT3	16	O	FOUT0	27	O	PECLN	38	I	DIVSEL
6	—	D-GND	17	—	D-VDD	28	—	D-GND	39	—	D-VDD
7	—	D-VDD	18	—	D-GND	29	—	D-VDD	40	O	LOCK
8	—	D-GND	19	O	X2FOUT	30	—	NC	41	I	INPSEL
9	O	FOUT2	20	O	HFOUT	31	O	FILTER	42	I	PECLREFP
10	I	RESET	21	—	D-GND	32	—	A-VDD	43	I	PECLREFN
11	—	D-VDD	22	—	D-VDD	33	—	A-VDD	44	I	TTLREF

INPUT

DIVSEL	:	DIVIDER SELECT
FBCLK	:	FEEDBACK CLOCK
INPSEL	:	INPUT SELECT
OUTEN0	:	HFOUT AND X2FOUT CONTROLLING
OUTEN1	:	FOUT0 - 3 CONTROLLING
PECLREFP	:	DIFFERENTIAL PECL P
PECLREFN	:	DIFFERENTIAL PECL N
PHSEL0 - PHSEL1	:	PHASE SELECTORS
RESET	:	RESET
TESTEN	:	TEST ENABLE
TTLREF	:	TTL REFERENCE CLOCK

OUTPUT

FILTER	:	FILTER
FOUT0 - FOUT3	:	TTL CLOCK OUTPUTS
HFOUT	:	TTL OUTPUT
LOCK	:	LOCK
PECLP	:	PSEUDO ECL OUTPUT
PECLN	:	PSEUDO ECL OUTPUT
X2FOUT	:	TTL OUTPUT


TTLREF
44
PECLREFP
42
PECLREFN
43
I0
MUX
I1
S
INPSEL
41
14 kΩ
REFCLK
PHSE
DETECTOR
CHARGE
PUMP
40
LOCK
31
FILTER
VCO
FBCLK
1
+2
I0
I1
MUX
SELECT
TESTEN
35
DIVIDER
AND
PHASE
CONTROL
LOGIC
26
PECLP
27
PECLN
19
X2FOUT
20
HFOUT
16
FOUT0
14
FOUT1
9
FOUT2
5
FOUT3
DIVSEL
38
PHSEL0
37
PHSEL1
36
RESET
10
OUTEN0
23
OUTEN1
24