

S-2919GR/I

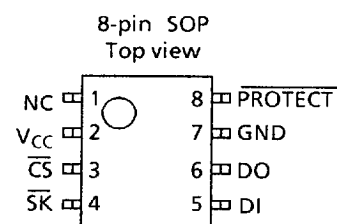
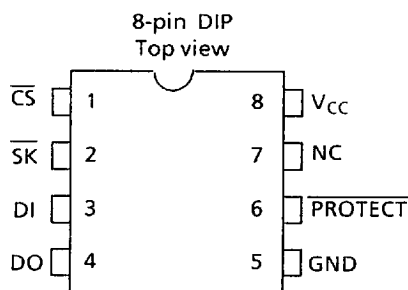
CMOS 1K-bit serial E²PROM Easy interface with serial port With memory protection, CS active "L"

The S-2919GR/I is a high speed, low power 1K-bit E²PROM that uses the CMOS floating-gate process. The organization is 64-word × 16-bit, and it is read or written serially. Memory protection is valid in 512 bits (addresses 0 to 31). Chip select is active low.

■ Features

- Low power consumption
Operating: 2.0 mA max.
Standby: 1.0 μ A max.
- Wide operating voltage range
Write: 2.7 to 6.5 V
Read: 1.8 to 6.5 V
- Write operation with built-in timer
- Chip erase operation
- Memory protection
- Easy interface with serial port
- Rewritings: 10⁴ or 10⁵ times
- Data retention: 10 years

■ Pin Arrangement



$\overline{CS}$	Chip select
$\overline{SK}$	Serial clock
DI	Serial data input
DO	Serial data output
GND	Ground (0 V)

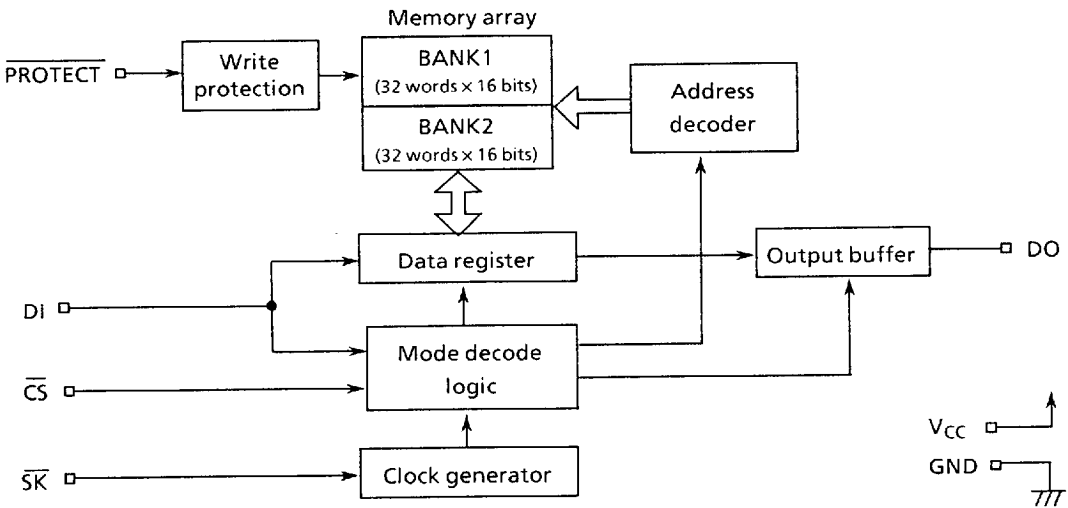
V_{CC}	Power supply voltage (+ 5 v)
$\overline{PROTECT}$	Memory protection control* Protection : Connected to GND or open Without protection : Connected to V_{CC}

* Memory protection

This function protects memory contents from erroneous writing when the CPU malfunctions. When the $\overline{PROTECT}$ pin is connected to GND or open, write to BANK 1 (addresses 0 to 31) of the memory array is inhibited. Since $\overline{PROTECT}$ pin has a built-in pull-down resistor, a memory protection functions automatically when it is open.

Figure 1

■ Block Diagram



■ Instruction Set

Table 1

Instruction		Start bit	Op code	Address	Data
READ	(Read data)	1	1000xxx	xxA ₅ to A ₀	D ₁₅ to D ₀
PROGRAM	(Program)	1	x100xxx	xxA ₅ to A ₀	D ₁₅ to D ₀
WRAL	(Write all)	1	0001xxx	xxxxxxxx	D ₁₅ to D ₀
ERAL	(Erase all)	1	0010xxx	xxxxxxxx	—
PEN	(Program enable)	1	0011xxx	xxxxxxxx	—
PDS	(Program disable)	1	0000xxx	xxxxxxxx	—

x : Don't care

■ Absolute Maximum Ratings

Table 2

Item	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{CC}		-0.3 to +7.0	V
Input voltage	V_{IN}		-0.3 to $V_{CC} + 0.3$	V
Output voltage	V_{OUT}		-0.3 to V_{CC}	V
Storage temperature under bias	T_{bias}	S-2919GR	-10 to +85	°C
		S-2919GI	-50 to +95	°C
Storage temperature	T_{stg}	S-2919GR	-65 to +125	°C
		S-2919GI	-65 to +150	°C

■ Recommended Operating Conditions

Table 3

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	Read	1.8	—	6.5	V
		Write	2.7	—	6.5	V
High level input voltage	V_{IH}	$V_{CC} = 5.0 \pm 10\%$	2.0	—	V_{CC}	V
		$V_{CC} = 2.7$ to $6.5V$	$0.8 \times V_{CC}$	—	V_{CC}	V
		$V_{CC} = 1.8$ to $2.7V$	$0.8 \times V_{CC}$	—	V_{CC}	V
Low level input voltage	V_{IL}	$V_{CC} = 5.0 \pm 10\%$	0.0	—	0.8	V
		$V_{CC} = 2.7$ to $6.5V$	0.0	—	$0.15 \times V_{CC}$	V
		$V_{CC} = 1.8$ to $2.7V$	0.0	—	$0.2 \times V_{CC}$	V
Operating temperature	T_{opr}	S-2919GR	0	—	+70	°C
		S-2919GI	-40	—	+85	°C

S-2919GR/I

DC Electrical Characteristics

Table 4

(S-2919GR : Ta = 0°C to 70°C, S-2919GI : Ta = -40°C to 85°C)

Item	Smb1	Conditions	Read/write operations						Read operation			Unit
			V _{CC} = 5.0 V ± 10 %			V _{CC} = 3.0 V ± 10 %			V _{CC} = 1.8 to 2.7 V			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I _{CC1}	DO unloaded	—	—	2.0	—	—	1.0	—	—	0.5	mA
Current consumption (PROGRAM)	I _{CC2}	DO unloaded	—	—	5.0	—	—	2.0	—	—	—	mA

Table 5

(S-2919GR : Ta = 0°C to 70°C, S-2919GI : Ta = -40°C to 85°C)

Item	Smb1	Conditions	Read/write operations						Read operation			Unit
			V _{CC} = 5.0 V ± 10 %			V _{CC} = 2.7 to 6.5 V			V _{CC} = 1.8 to 2.7 V			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I _{SB}	Input: V _{CC} or GND	—	—	1.0	—	—	1.0	—	—	1.0	μA
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Output leakage current	I _{LO}	V _{OUT} = GND to V _{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Low level output voltage	V _{OL}	CMOS I _{OL} = 100 μA	—	—	0.1	—	—	0.1	—	—	0.1	V
		TTL I _{OL} = 2.1 mA	—	—	0.45	—	—	—	—	—	—	V
High level output voltage	V _{OH}	CMOS V _{CC} = 2.7 to 6.5 V: I _{OH} = -100 μA V _{CC} = 1.8 to 2.7 V: I _{OH} = -10 μA	V _{CC} -0.7	—	—	V _{CC} -0.7	—	—	V _{CC} -0.3	—	—	V
		TTL, I _{OH} = -400 μA	2.4	—	—	—	—	—	—	—	—	V
Write enable latch data hold voltage	V _{DH}		1.5	—	—	1.5	—	—	1.5	—	—	V
Pull down current	I _{PD}	PROTECT = V _{CC}	15	40	120	4	—	200	1	—	40	μA

Rewriting Times

Table 6

(S-2919GR : Ta = 0°C to 70°C, S-2919GI : Ta = -40°C to 85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Rewriting times	N _W	S-2919GR/I01	10 ⁴	—	—	times/word
		S-2919GR/I10	10 ⁵	—	—	times/word

Pin Capacitance

Table 7

(Ta = 25°C, f = 1.0 MHz, V_{CC} = 5 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0 V	—	—	6	pF
Output capacitance	C _{OUT}	V _{OUT} = 0 V	—	—	10	pF

■ AC Electrical Characteristics

Table 8 Measuring conditions

Input voltage level	$0.1 \times V_{CC}$ to $0.9 \times V_{CC}$
Output voltage level	$0.5 \times V_{CC}$
Output load	100pF

Table 9

(S-2919GR : Ta = 0°C to 70°C, S-2919GI : Ta = -40°C to 85°C)

Item	Symbol	Read / Write operations						Read operation			Unit
		$V_{CC} = 5.0 \pm 10\%$			$V_{CC} = 2.7 \text{ to } 6.5 \text{ V}$			$V_{CC} = 1.8 \text{ to } 2.7 \text{ V}$			
		Min.	Typ	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
$\overline{CS}$ setup time	t_{CSS}	0.2	—	—	0.4	—	—	1.0	—	—	μs
$\overline{CS}$ hold time	t_{CSH}	0.2	—	—	0.4	—	—	1.0	—	—	μs
$\overline{CS}$ setup time (CPU)	$t_{CSS(CPU)}$	0.2	—	—	0.4	—	—	1.0	—	—	μs
$\overline{CS}$ hold time (CPU)	$t_{CSH(CPU)}$	0.2	—	—	0.4	—	—	1.0	—	—	μs
$\overline{CS}$ reset time	t_{CDS}	0.2	—	—	0.2	—	—	0.4	—	—	μs
Data setup time	t_{DS}	0.2	—	—	0.4	—	—	0.8	—	—	μs
Data hold time	t_{DH}	0.2	—	—	0.4	—	—	0.8	—	—	μs
1 data output delay	t_{PD1}	—	—	0.4	—	—	1.0	—	—	2.0	μs
0 data output delay	t_{PD0}	—	—	0.4	—	—	1.0	—	—	2.0	μs
Clock frequency	f_{SK}	0.0	—	2.0	0.0	—	0.5	0.0	—	0.2	MHz
Clock pulse width	t_{SKH}, t_{SKL}	0.25	—	—	1.0	—	—	2.5	—	—	μs
Output disable time	t_{HZ}	0	50	150	0	500	1000	—	—	—	ns
Output enable time	t_{SV}	0	50	150	0	500	1000	—	—	—	ns
Program time	t_{PR}	2.0	4.0	10	2.0	4.0	10	—	—	—	ms

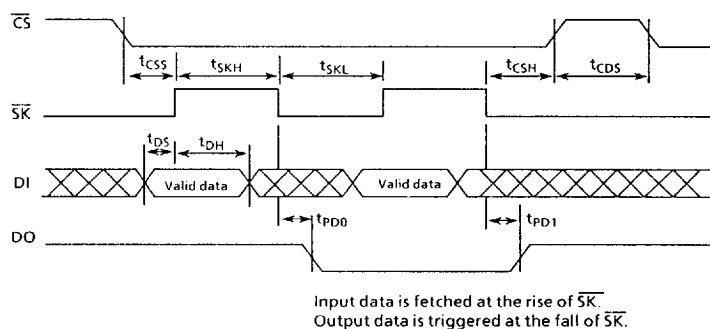


Figure 3 Timing chart

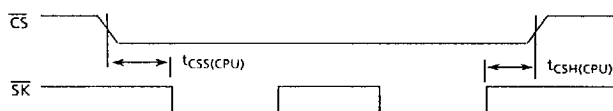


Figure 4 Timing chart of $t_{CSS(CPU)}$ and $t_{CSH(CPU)}$ when connected to CPU

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■ Operation

Each of op code with a start bit, address and data is composed of eight bits, and the S-2919GR/I is easily interfaced with a CPU serial I/O port. A start bit is recognized when high of DI is fetched at the rise of $\overline{SK}$ after falling of $\overline{CS}$, and operation starts.

Note

- $\overline{CS}$ must be "H" between instructions.
- $\overline{SK}$ and DI must be "L" during verify operation
- It is not necessary to erase data before PROGRAM or WRAL operation.

(1) Read mode

This mode reads data from a specified address. By the READ instruction, data is triggered at the fall of $\overline{SK}$, and output serially to DO pin.

The READ instruction is executed for all memory array bits regardless of the state of the $\overline{PROTECT}$ pin, program enable/disable mode.

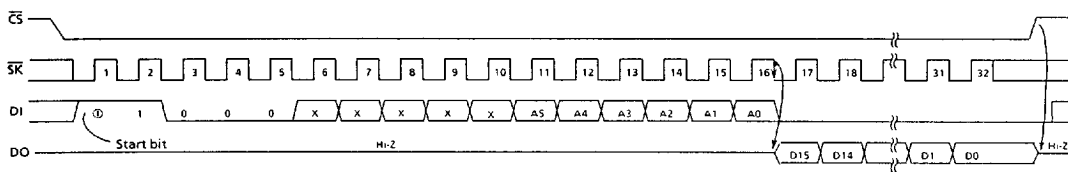


Figure 5 Read mode timing

(2) Program mode

After the PROGRAM instruction, address and data are sent in program enable mode, $\overline{CS}$ must be high once. At the rising edge of its high, data is written into the specified address. This operation is performed by the internal auto-timing generation circuit and $\overline{SK}$ is not necessary. The READY/BUSY status can be found by falling $\overline{CS}$ and by checking the DO pin. During write operation, low level is output to the DO pin, and after operation, high level is output.

Note : When the $\overline{PROTECT}$ pin is connected to GND or open, the PROGRAM instruction to BANK1 is invalid and data cannot be written into BANK1. However, the internal auto-timing generation circuit operates.

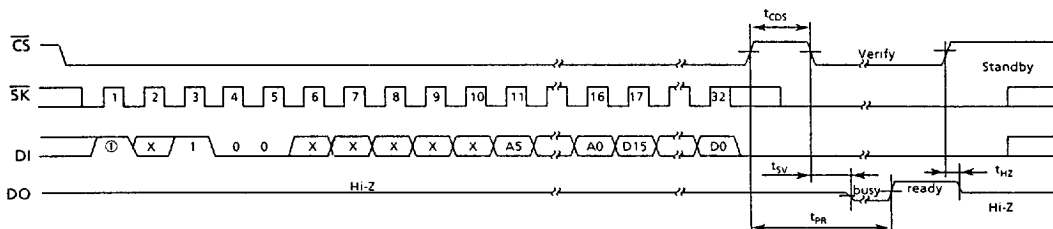


Figure 6 Program mode timing

(3) Write all (WRAL) mode

After the WRAL instruction is sent, in program enable mode, $\overline{CS}$ must be high once. At the rising edge of its high, the same data is written into all memory array bits. This operation is performed by the internal auto-timing generation circuit and $\overline{SK}$ is not necessary. The READY/BUSY status can be found by falling $\overline{CS}$ and checking the DO pin. During write operation, low level is output to the DO pin, and after operation, high level is output.

NOTE : When the $\overline{PROTECT}$ pin is connected to GND or open, the WRAL instruction to BANK1 is invalid, and data cannot be written into BANK1.

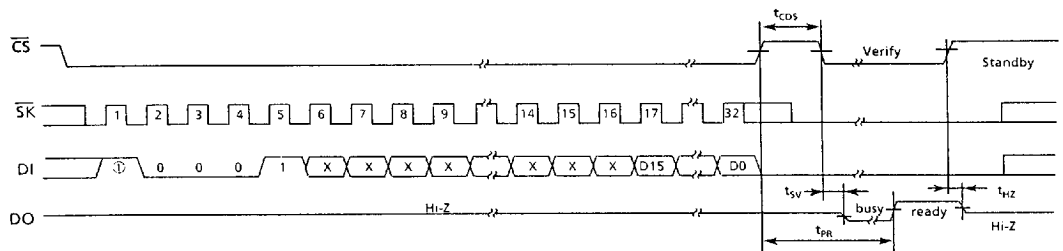


Figure 7 WRAL mode timing

(4) Erase all (ERAL) mode

After the ERAL instruction is sent, in program enable mode, $\overline{CS}$ must be high once. At the rising edge of its high, all memory array bits is set to 1. This operation is performed by the internal auto-timing generation circuit and $\overline{SK}$ is not necessary. The READY/BUSY status can be found by falling $\overline{CS}$ and checking the DO pin. During erase operation, low level is output to the DO pin, and after operation, high level is output.

Note : When the $\overline{PROTECT}$ pin is connected to GND or open, the ERAL instruction to BANK1 is invalid and data in BANK1 cannot be erased.

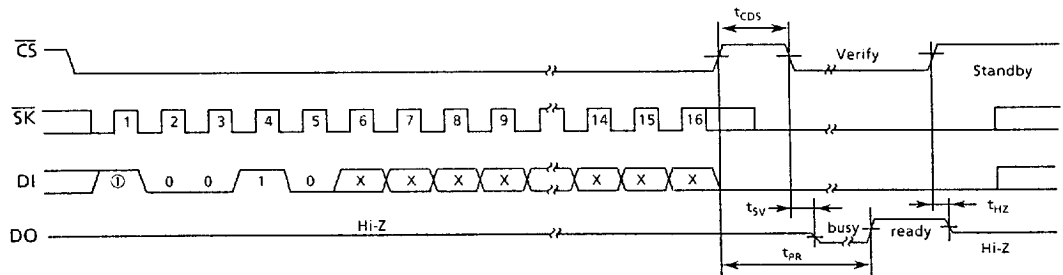


Figure 8 ERAL mode timing

S-2919GR/I

(5) Program enable (PEN) and program disable (PDS) modes

The PEN instruction puts the S-2919GR/I into program enable (PEN) mode. In this mode, PROGRAM, WRAL and ERAL instructions are enabled. The S-2919GR/I remains in PEN mode until a PDS instruction is executed. The PDS instruction puts the S-2919GR/I into program disable (PDS) mode. The PROGRAM, WRAL and ERAL instructions are ignored in the PDS mode; this mode is used to protect data against accidental programming. The S-2919GR/I is in program disable mode when power is turned on.

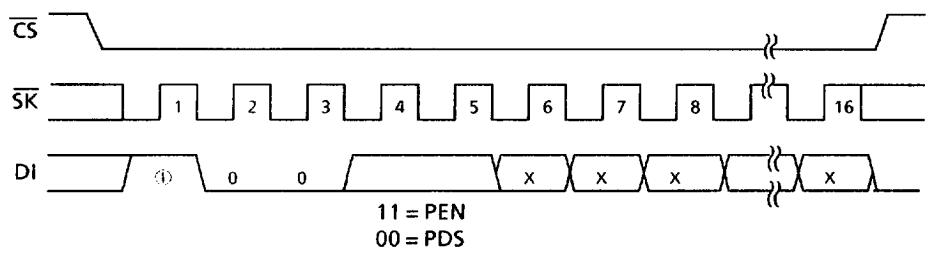


Figure 9 PEN/PDS mode timing

■ Interface with CPU Serial Port

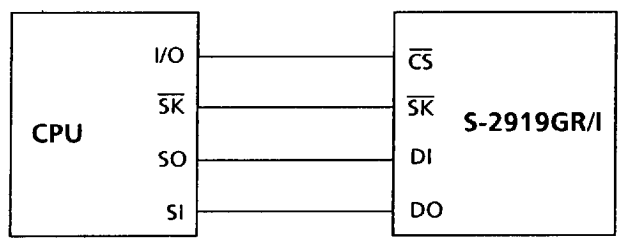


Figure 10 Circuit example

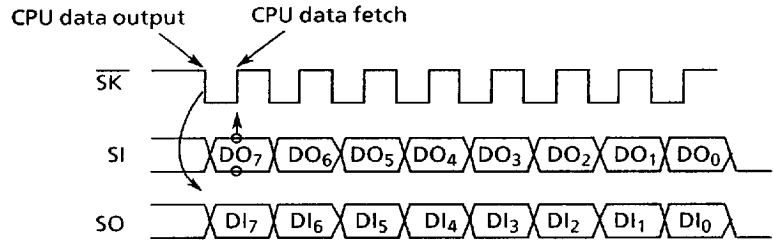


Figure 11 Serial shift timing

■ Dimensions (Unit:mm)

1. S-2919GR/I (8-pin DIP)

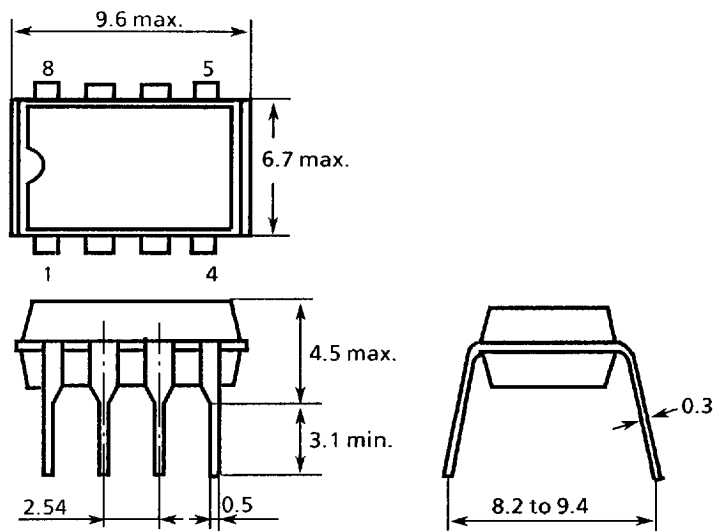


Figure 12

2. S-2919GRF/IF (8-pin SOP)

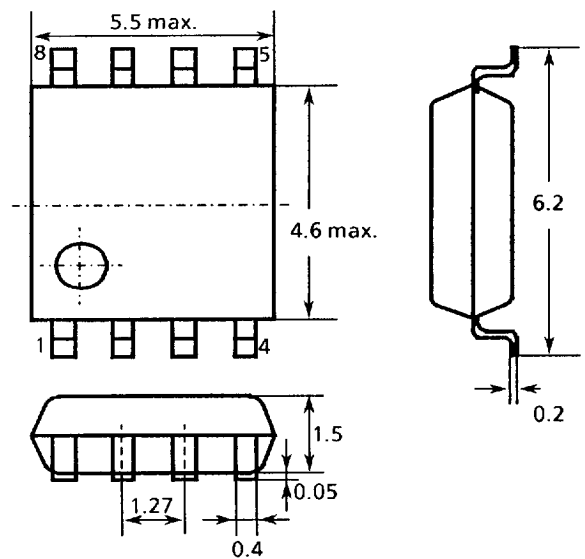
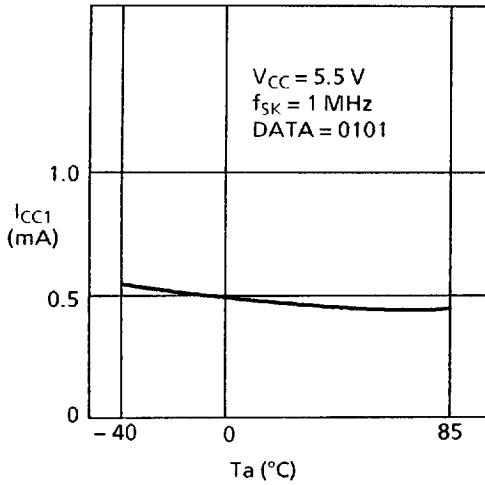


Figure 13

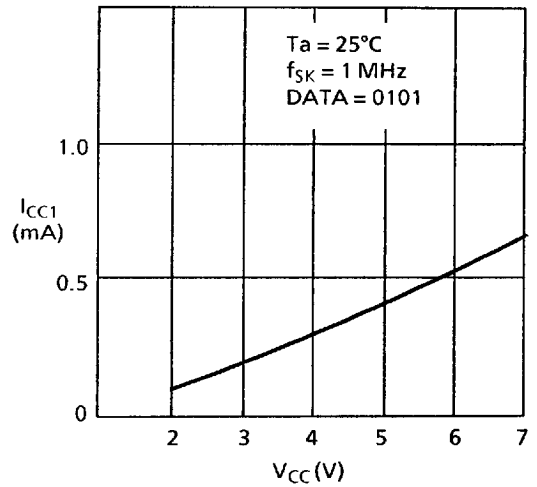
■ Characteristics

1. DC Characteristics

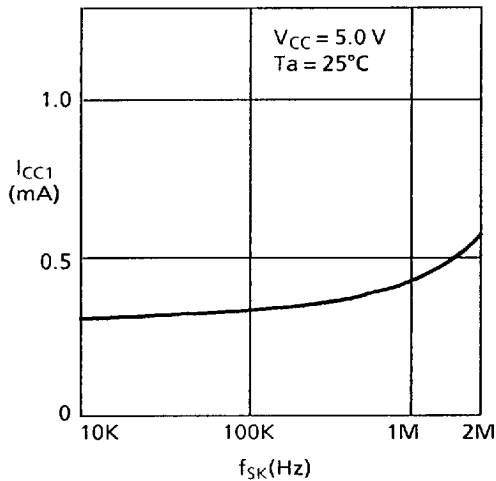
1.1 Current consumption (READ) I_{CC1} — Ambient temperature T_a



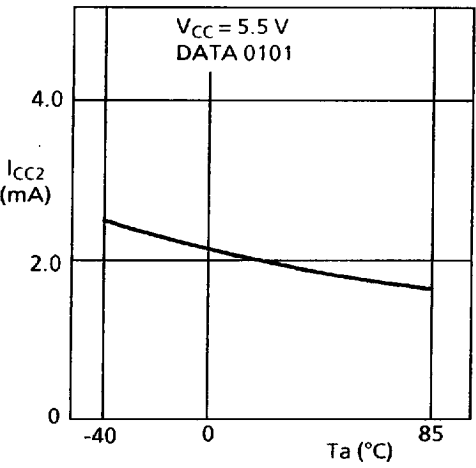
1.2 Current consumption (READ) I_{CC1} — Power supply voltage V_{CC}



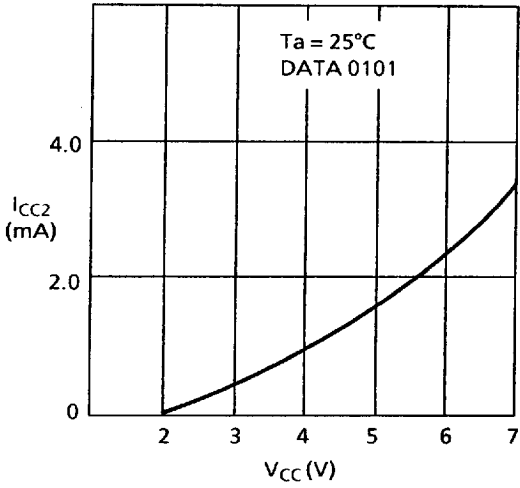
1.3 Current consumption (READ) I_{CC1} — Clock frequency f_{SK}



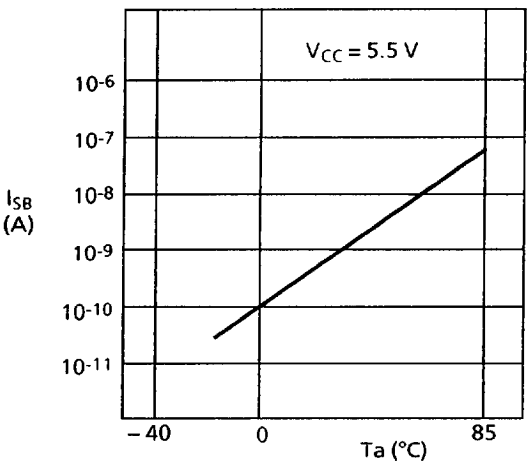
1.4 Current consumption (PROGRAM) I_{CC2} – Ambient temperature T_a



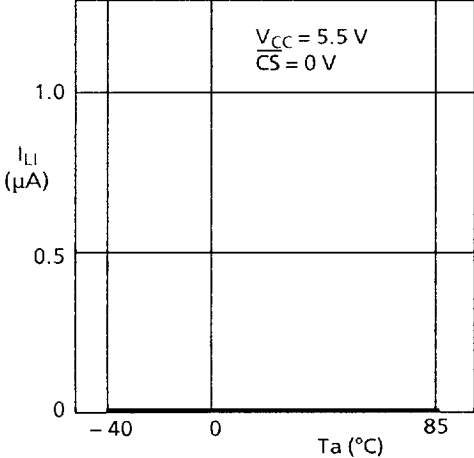
1.5 Current consumption (PROGRAM) I_{CC2} – Power supply voltage V_{CC}



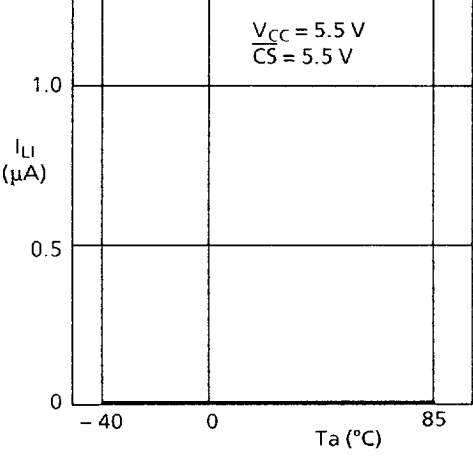
1.6 Standby current consumption I_{SB} — Ambient temperature T_a



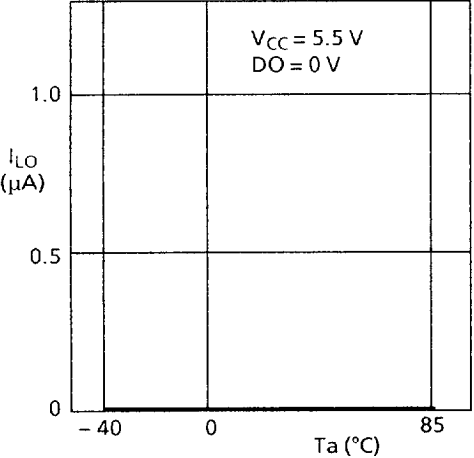
1.7 Input leakage current I_{LI} – Ambient temperature T_a



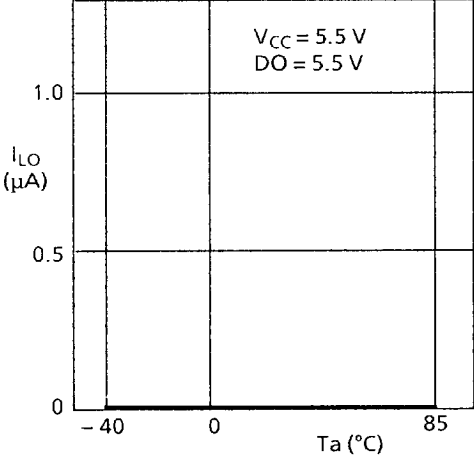
1.8 Input leakage current I_{LI} – Ambient temperature T_a



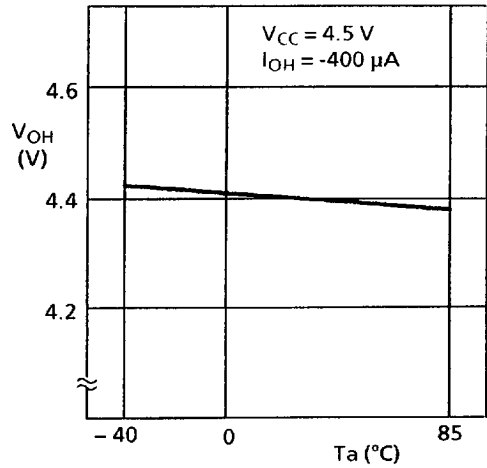
1.9 Output leakage current I_{LO} – Ambient temperature T_a



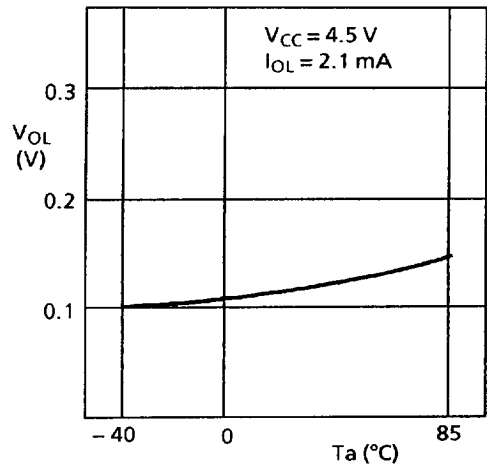
1.10 Output leakage current I_{LO} – Ambient temperature T_a



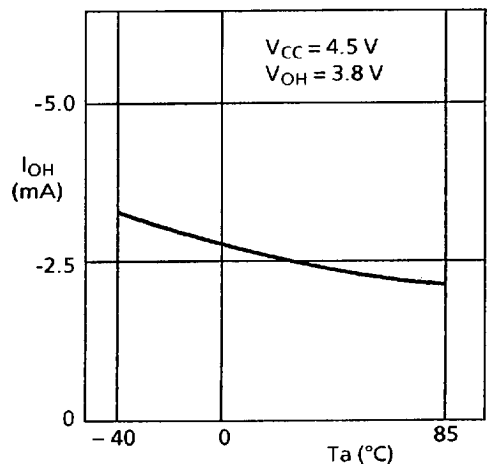
1.11 High level output voltage V_{OH} – Ambient temperature T_a



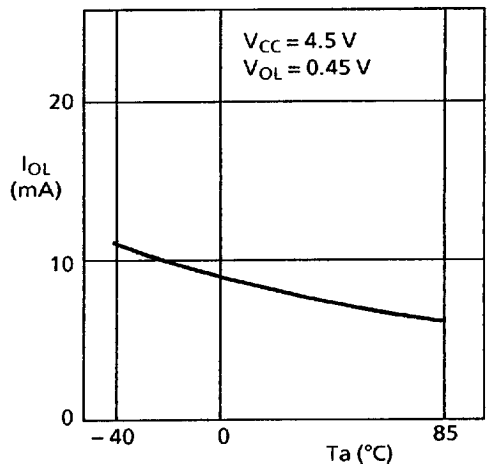
1.12 Low level output voltage V_{OL} – Ambient temperature T_a



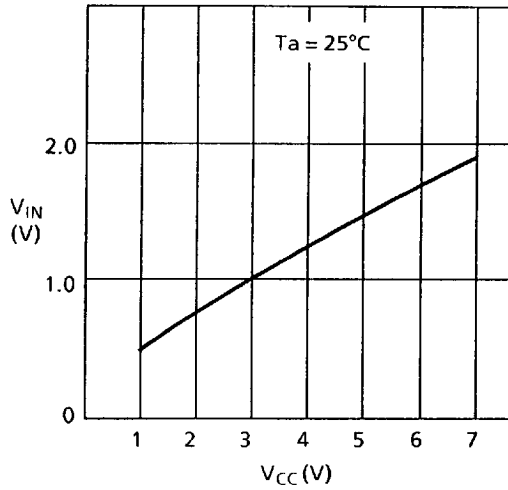
1.13 High level output current I_{OH} – Ambient temperature T_a



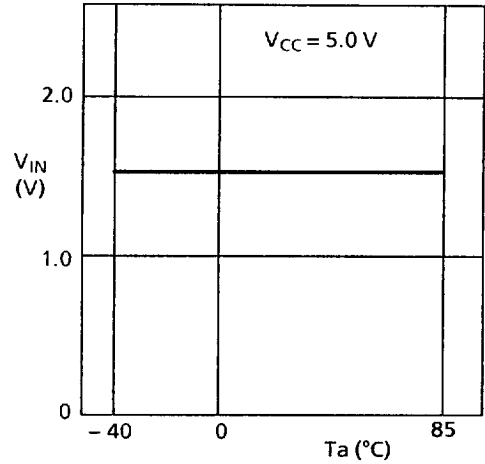
1.14 Low level output current I_{OL} – Ambient temperature T_a



1.15 Input voltage V_{IN} –
Power supply voltage V_{CC}

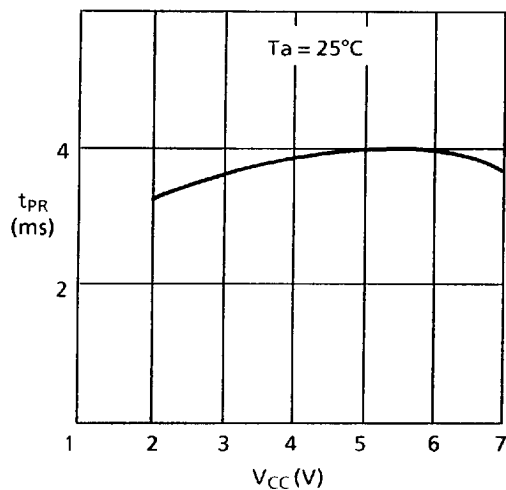


1.16 Input voltage V_{IN} –
Ambient temperature T_a

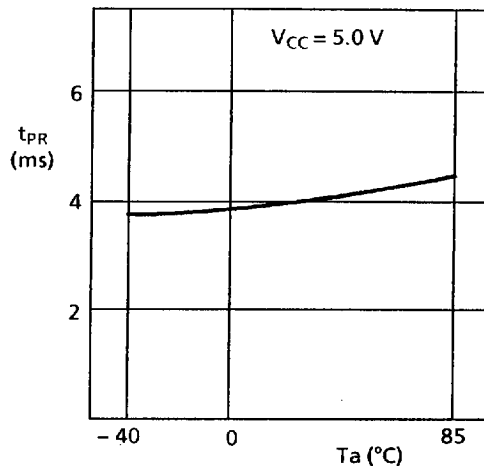


2. AC Characteristics

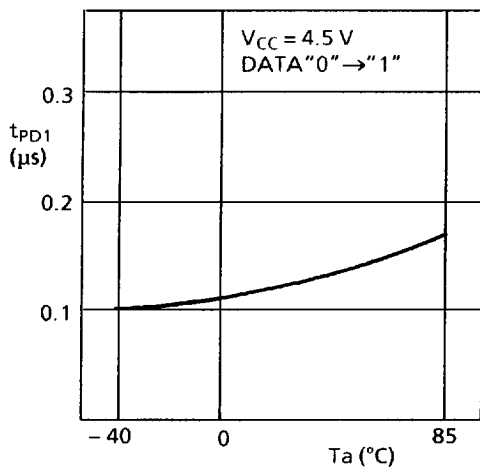
2.1 Program time t_{PR} –
Power supply voltage V_{CC}



2.2 Program time t_{PR} –
Ambient temperature T_a



2.3 1 data output delay time t_{PD1} –
Ambient temperature T_a



2.4 0 data output delay time t_{PD0} –
Ambient temperature T_a

