■ GENERAL DESCRIPTION

The S-2444R is a 256-bit Non Volatile CMOS Memory, one to one combination of static CMOS RAM and Non Volatile Electric Erasable Programmable Read Only Memory (E^2PROM) as a back up. The device is organized as 16 words of 16 bits each. Serial access allows the use of a cost-effective 8-pin package, making the S2444R ideal for cost sensitive and compact design applications.

STORE signal, RECALL signal and instructions sent from the processor transfer data between RAM and E^2PROM. Non Volatile data is retained in the E^2PROM while data in the RAM can be accessed and updated.

There is no need of high voltage pulses and supplies. A signal 5V supply is the only power source needed, and all I/O are TTL compatible.

The S-2444R offers many modes to minimize the current consumption. When it is deselected, the chip is placed in the STANDBY mode. And when the sleep instruction is carried out, the chip is placed in the SLEEP mode. The chip will automatically return active from STANDBY mode when selected by CE, and will exit the SLEEP mode when the next RECALL operation is performed, either by the RCL instruction or by taking the $\overline{\text{RECALL}}$ input low.

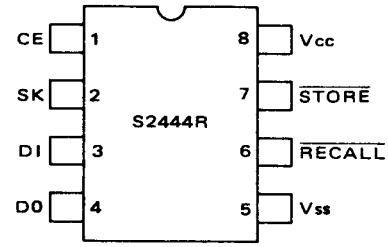
■ FEATURES

- Ideal use for Periphery of Microcomputers.
  - Static Timing
  - Minimum I/O Interface
  - Serial Port Compatible (8051)
  - Minimum Support Circuits
- Software and Hardware Control of Nonvolatile Functions.
  - False Store Protection
- TTL Compatible
  - High Drive Ability Output
- Constitution 16 words x 16 bits
- CMOS Floating Gate Process
- 5V Single Power Supply (5V±10%)
- Low Current Consumption

Power Supply Current	10mA TYP
Store Current	8mA TYP
Standby Current	5μA TYP
Sleep Current	5μA TYP

- 8 Pin-Dip
  - Low Cost, Compact

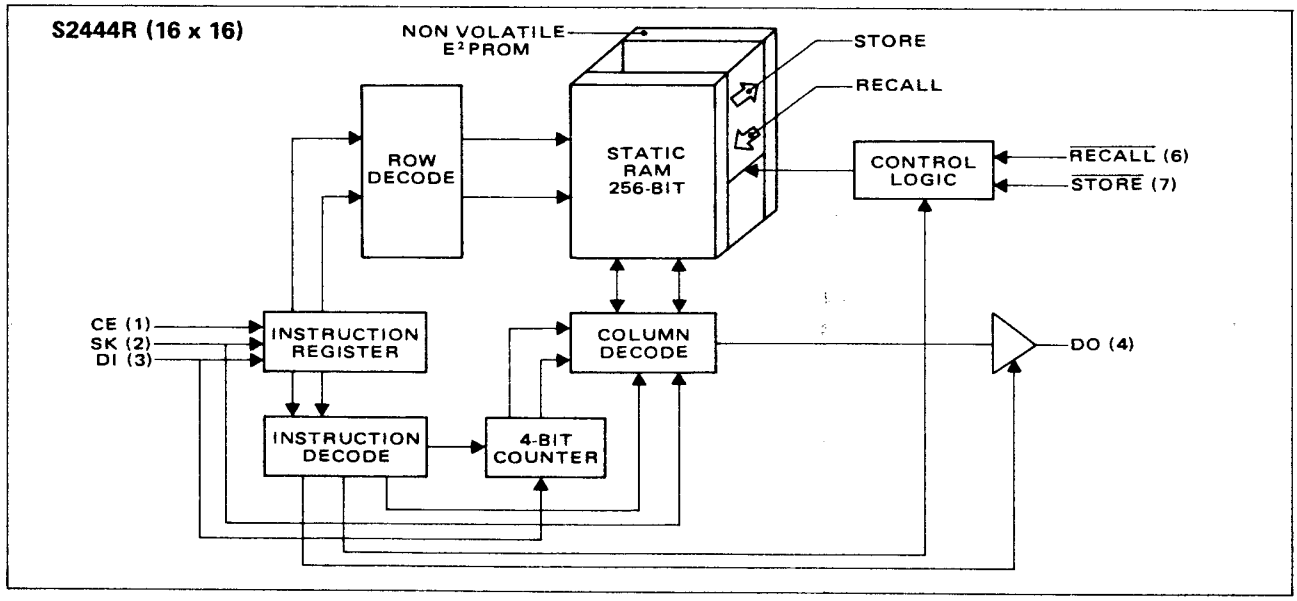
■ PIN CONFIGURATION



■ PIN NAMES

CE	CHIP ENABLE
SK	SERIAL CLOCK
D1	SERIAL DATA IN
D0	SERIAL DATA OUT
RECALL	RECALL
STORE	STORE
Vcc	+5V
Vss	GROUND

■ FUNCTIONAL DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Condition	Unit
T_{STG}	Storage Temperature	−65 to +125	°C
T_{OPR}	Operating Temperature	−10 to +85	°C
V_{CC}	Power Supply Voltage	−0.3 to +6.0	V
V_{IN}	Input Voltage	−0.3 to V_{CC} +0.3	V
V_{OUT}	Output Voltage	−0.0 to V_{CC}	V

■ D.C. ELECTRIC CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = +5V ±10%)

Symbol	Item	Condition	MIN	TYP	MAX	Unit
V_{CC}	Operating Voltage		4.5		5.5	V
I_{CC}	Power Supply Current	$I_{I/O}$ = 0mA	–	10	20	mA
I_{SL}	Sleep Current		–	5	30	μA
I_{SB}	Standby Current	CE = V_{IL}	–	5	30	μA
I_{STO}	Store Current		–	8	15	mA
I_{LI}	Input Load Current	V_{IN} = 5.5V	–	0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V	–	0.1	10	μA
V_{IL}	Input Low Voltage		0.0	–	0.8	V
V_{IH}	Input High Voltage		2.0	–	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.0mA	2.4	–	–	V
V_{DH}	Data Holding Voltage		1.5	–	5.5	V

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz, V_{CC} = 5V)

Symbol	Item	Condition	MIN	TYP	MAX	Unit
C_O	Output Capacitance	V_O = 0V			8	pF
C_{IN}	Input Capacitance	V_{IN} = 0V			6	pF

■ A.C. CONDITIONS OF TEST

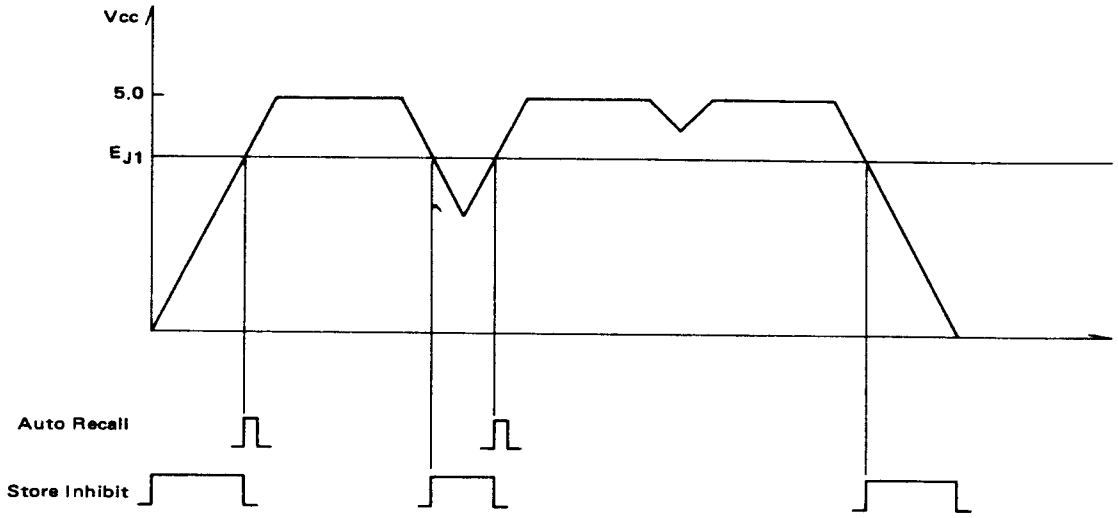
Input Pulse Levels	V_{IL} = 0.65V, V_{IH} = 2.2V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{OL} = 0.65V, V_{OH} = 2.2V
Output Load	1 TTL + 100PF

■ OPERATING MODE

MODE	$\overline{STORE}$	$\overline{RECALL}$	INST.	WRITE ENABLE LATCH	PREVIOUS RECALL LATCH
Hardware Recall	1	0	NOP	X	X
Software Recall	1	1	RCL	X	X
Hardware Store	0	1	NOP	SET	TRUE
Software Store	1	1	STO	SET	TRUE

■ AUTO RECALL AND FALSE STORE PROTECTION ARE TRIGGERED ON POWER UP AND POWER DOWN RESPECTIVELY.

Conditions . . . . . Vcc Rise and Fall times should be between 10ms and 1000ms.



■ A.C. ELECTRIC CHARACTERISTICS (Ta = 0 ~ 70°C, Vcc = 5V ±10%)

Symbol	Item	MIN	TYP	MAX	Unit
FSK	SK Frequency			1.0	MHz
t_{SKH}	SK Positive Pulse Width	0.4			μs
t_{SKL}	SK Negative Pulse Width	0.4			μs
t_{DS}	Data Setup Time	0.4			μs
t_{DH}	Data Hold Time	0.08			μs
t_{PD}	SK to Data Valid Time			0.75	μs
t_Z	Chip Disable Time			1.0	μs
t_{CES}	Chip Enable Setup Time	0.8			μs
t_{CEH}	Chip Enable Hold Time	0.4			μs
t_{CDS}	Chip De-select Time	0.8			μs

■ CONTROL/DATA TIMING

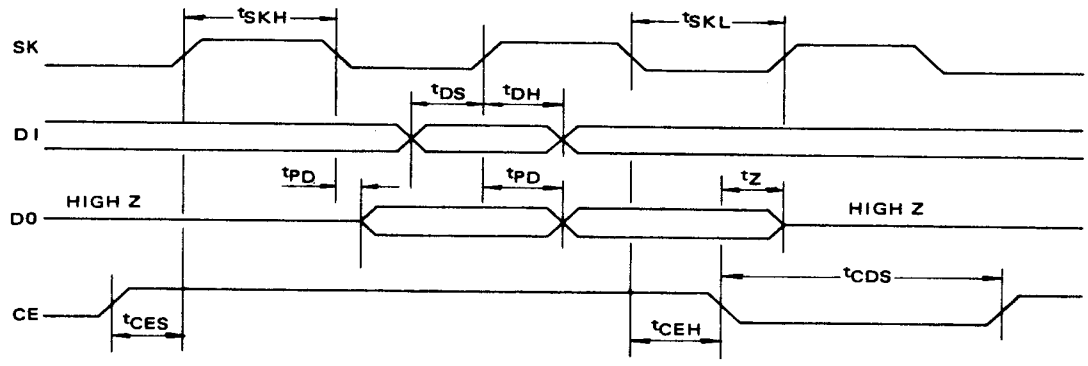


Diagram 1

- CE must be taken high between instructions.
- Once the chip has been selected with CE, the first logic "1" clocked by the rising edge of SK into the DI input marks the beginning of an instruction. All previous logic "0" is ignored.

INSTRUCTION SET		
Instruction	Format, I_2 I_1 I_0	Operation
WRDS (Diagram 5)	1XXXX000	Reset Write Enable Latch (Disables writes and stores)
STO (Diagram 5)	1XXXX001	Store RAM data in E^2PROM
SLEEP (Diagram 5)	1XXXX010	Enter SLEEP Mode
WRITE (Diagram 3)	1AAAA011	Write Data into RAM Address AAAA
WREN (Diagram 5)	1XXXX100	Set Write Enable Latch (Enables writes and stores)
RCL (Diagram 5)	1XXXX101	Recall E^2PROM Data into RAM
READ (Diagram 2)	1AAAA11X	Read Data from RAM Address AAAA

X = Don't Care
A = Address Bit

■ DATA OPERATIONS

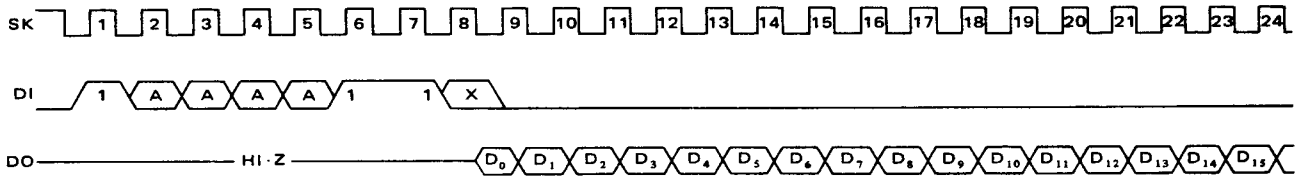


Diagram 2. RAM Read

** Bit 8 of Read Instruction is Don't Care.*

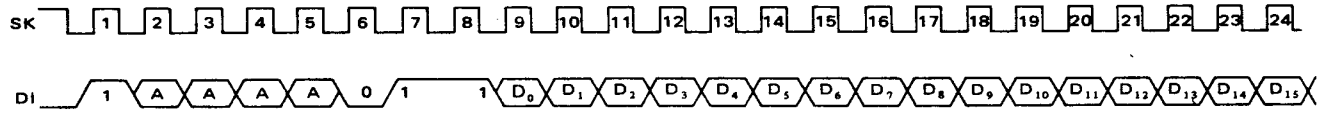


Diagram 3. RAM Write

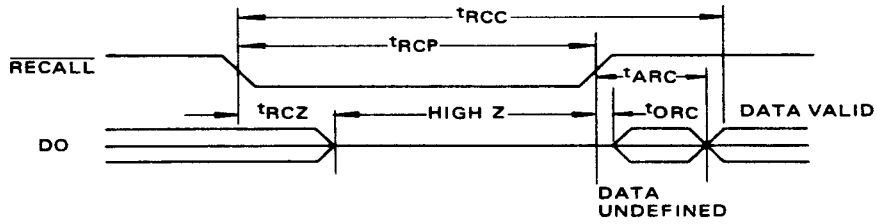


Diagram 4. Hardware Recall

■ ARRAY RECALL CYCLE

Symbol	Item	MIN	TYP	MAX	Unit
t_{RCC}	Recall Cycle Time	2.5			μs
t_{RCP}	Recall Pulse Width	0.5			μs
t_{RCZ}	Recall to Output High Z			0.5	μs
t_{ORC}	Recall Enable Time	0.01			μs
t_{ARC}	Recall Data Access Time			1.5	μs

Recall Time is not limited.

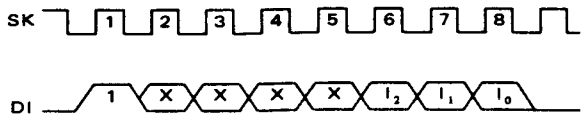


Diagram 5. Non-Data Operations

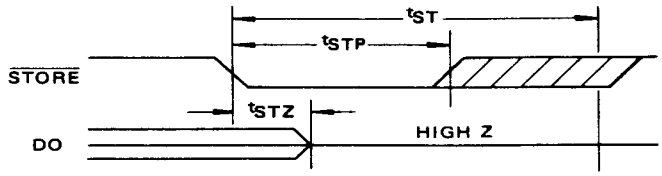


Diagram 6. Hardware Store

■ STORE CYCLE

Symbol	Item	MIN	TYP	MAX	Unit
t_{ST}	Store Time			10	ms
t_{STP}	Store Pulse Width	0.2			μs
t_{STZ}	Store to Output High Z			1.0	μs

Minimum store cycle is 10,000. 10,000 data change per bit. 10 years' Data Retention.

■ RECALL OPERATIONS

RECALL operation transfers the data currently in the nonvolatile E^2PROM into the RAM section of the S2444R. RECALL operation can be initiated either from the RECALL input driven low, or the execution of the RCL instruction. Once operated, all other operations are inhibited, and the previous data in the RAM is overwritten. If the chip had been already placed in SLEEP mode, the RECALL operation will put the chip in Active mode. The first Recall after power-on will set the previous latch, which must be set in order to do set STORE operations.

■ STORE OPERATION

STORE operation transfers the data currently in the RAM to E^2PROM. The data currently in the E^2PROM is overwritten. The STORE operation can be initiated from either the STORE input being driven low, or the execution of a STO instruction in order to protect against inadvertent stores which destroy important information in the E^2PROM, several conditions must be true in order to perform the STORE OPERATION.

1. STO Command issued or STORE driven low
2. Write Enable Latch must be set.
3. Privious Recall Latch must be set.

STORE operation inhibits all other operations, and any data spread the part during a STORE operation will result in the output remaining in the high impedance state. The STORE operation clears the Write Enable latch. If the S2444R is performing a WRITE operation, the STORE input is ignored until CE is taken low.

■ WRITE/STORE PROTECTION

WRITE/STORE protection is provided by the S2444R internal Write Enable Latch. This latch must be set in order to do the WRITE or STORE operation. The latch can be set with the WREN instruction and reset with the WRDS instruction. The Write Enable latch is automatically reset after a STORE operation is performed.

■ READ/WRITE MEMORY

The RAM in the chip is accessed by the READ and WRITE instructions. These instructions include a 4-bit address, which selects which word is to be written or read. After the instruction and address have been sent, serial data (16-bits) will be either output on the DO pin in the case of a read, or input through the DI pin in the case of a write. S2444R design allows the connection of the DI and DO lines together form a bi-directional serial interface.
The least significant bit of the READ instruction is a don't care to enhance the use of the shared I/O capability of the DI and DO lines.

■ SLEEP MODE

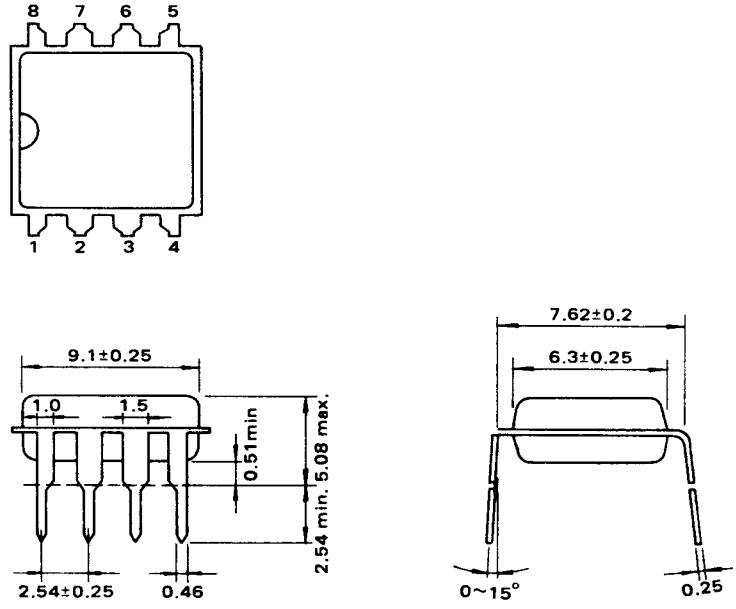
The SLEEP mode places the S2444 into a low power quiescent mode. Internal RAM is turned off, and any data currently in RAM becomes invalid. Data is maintained in E^2PROM, as it was saved in the last STORE operation. The SLEEP mode can only be exited by a hardware or software initiated Recall operation.

■ ORDERING INFORMATION

Model	Overwrite Times	Overwrite Times/Bit	Temperature Range	Package
S2444R01	10^4	10^4	0°C ~ +70°C	Plastic
S2444R10	10^5	10^5	0°C ~ +70°C	Plastic

Note: All values are typical.

■ DIMENSIONS (Unit: mm)



(Specifications subject to change without notice.)

Seiko Instruments Inc.

Head Office:
31-1, 6-chome, Kameido, Koto-ku, Tokyo 136, Japan Telex: 2622162 DSEIKO J
IC Sales Section Phone: (03) 636-3821
Seiko Instruments U.S.A. Inc.:
2990 W. Lomita Blvd., Torrance Calif. 90505
Phone: 213-530-8777 Telex: 910-347-7307 Fax: (213) 539-8621
Seiko Instruments GmbH:
Arabella Center 13 OG Lyoner Strasse 44-48, 6000 Frankfurt/Main 71 W. Germany
Phone: 069-6666971 Telex: 413045 SIG D
Precision Engineering Ltd. Sales Division:
7th, 9th Fl., Koon Wah Industrial Building, 40-46 Lam Tin Street, Kwai Chung, N.T., Kowloon, Hong Kong
Phone: 0-218611 Telex: 40211 PELSD HX

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