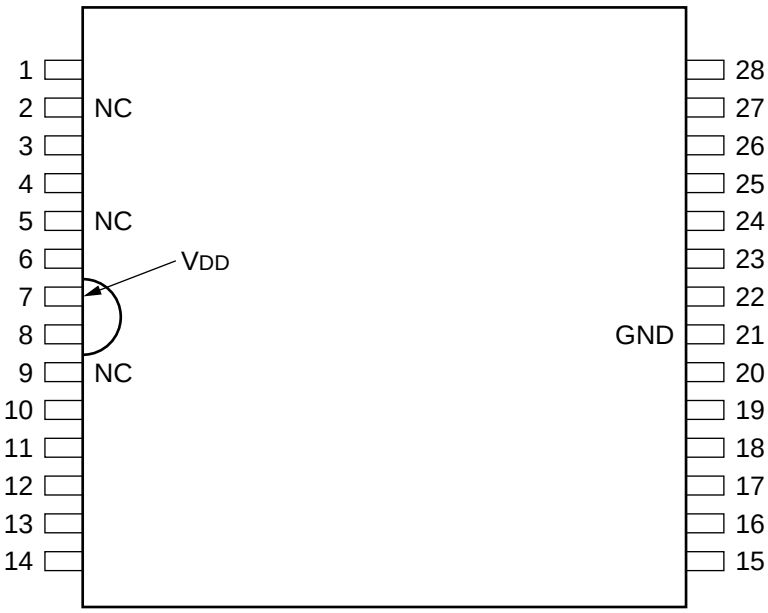
C-MOS 16 K (2 K × 8)-BIT PARALLEL EEPROM

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	$\overline{OE}$	15	I	A2
2	—	NC	16	I	A1
3	I	A9	17	I	A0
4	I	A8	18	I/O	I/O0
5	—	NC	19	I/O	I/O1
6	I	$\overline{WE}$	20	I/O	I/O2
7	—	V_{DD}	21	—	GND
8	O	R/$\overline{B}$	22	I/O	I/O3
9	—	NC	23	I/O	I/O4
10	I	A7	24	I/O	I/O5
11	I	A6	25	I/O	I/O6
12	I	A5	26	I/O	I/O7
13	I	A4	27	I	$\overline{CE}$
14	I	A3	28	I	A10

INPUT

A0 - A10 : ADDRESS
$\overline{CE}$: CHIP ENABLE
$\overline{OE}$: OUTPUT ENABLE
$\overline{WE}$: WRITE ENABLE

OUTPUT

R/$\overline{B}$: READY/$\overline{BUSY}$

INPUT/OUTPUT

I/O0 - I/O7 : DATA