HARRIS SEMICONDUCTOR

RHR1Y75120CC

October 1995

75A, 1200V Hyperfast Dual Diode

Features

- Hyperfast with Soft Recovery . . . . <85ns
- Operating Temperature . . . . $+175^oC$
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RHR1Y75120CC is a hyperfast dual diode with soft recovery characteristics (t_{RR} < 85ns). It has half the recovery time of ultrafast diodes and is silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as freewheeling/clamping diode and rectifier in a variety of switching power supplies and other power switching applications. Its low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

PACKAGING AVAILABILITY

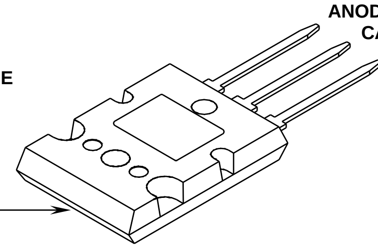
PART NUMBER	PACKAGE	BRAND
RHR1Y75120CC	TO-264AA	RHR75120C

NOTE: When ordering, use the entire part number.

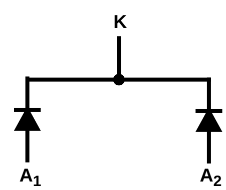
Formerly developmental type TA49042.

Package

JEDEC TO-264AA



Symbol



Absolute Maximum Ratings (Per Leg) $T_C = +25^oC$, Unless Otherwise Specified

		RHR1Y75120CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current $T_C = 42^oC$	$I_{F(AV)}$	75	A
Repetitive Peak Surge Current Square Wave, 20kHz	I_{FSM}	150	A
Nonrepetitive Peak Surge Current Halfwave, 1 Phase, 60Hz	I_{FSM}	500	A
Maximum Power Dissipation	P_D	190	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	50	mJ
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	^oC

Electrical Specifications (per leg) $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
V_F	I_F = 75A, T_C = +25^{o}C	-	-	3.2	V
	I_F = 75A, T_C = +150^{o}C	-	-	2.6	V
I_R	V_R = 1200V, T_C = +25^{o}C	-	-	250	µA
	V_R = 1200V, T_C = +150^{o}C	-	-	2.0	mA
t_{RR}	I_F = 1A, dI_F/dt = 200A/µs	-	-	85	ns
	I_F = 75A, dI_F/dt = 200A/µs	-	-	100	ns
t_A	I_F = 75A, dI_F/dt = 200A/µs	-	45	-	ns
t_B	I_F = 75A, dI_F/dt = 200A/µs	-	40	-	ns
Q_{RR}	I_F = 75A, dI_F/dt = 200A/µs	-	380	-	nC
C_J	V_R = 10V, I_F = 0A	-	225	-	pF
$R_{\theta JC}$		-	-	0.8	^{o}C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
Q_{RR} = Reverse recovery charge.
C_J = Junction Capacitance.
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled Avalanche Energy (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

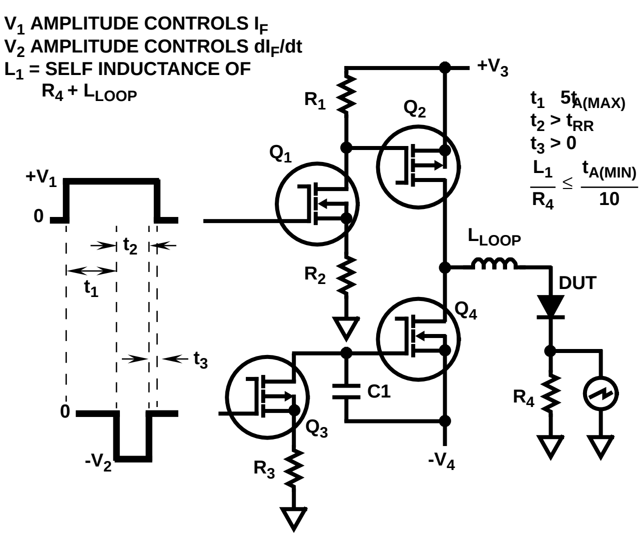


FIGURE 1. t_{RR} TEST CIRCUIT

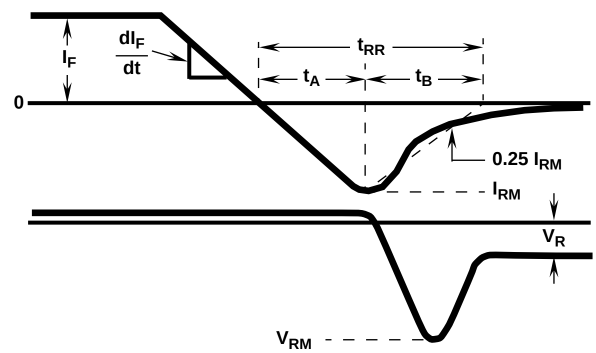


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

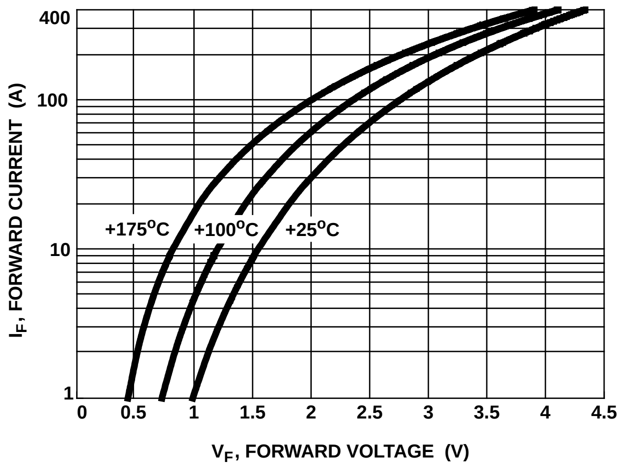


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

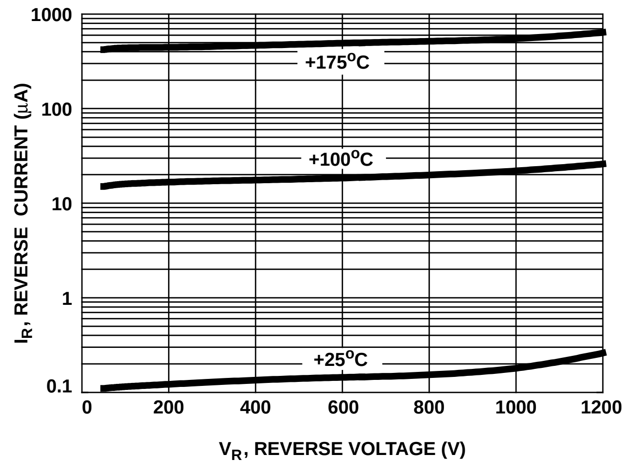


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

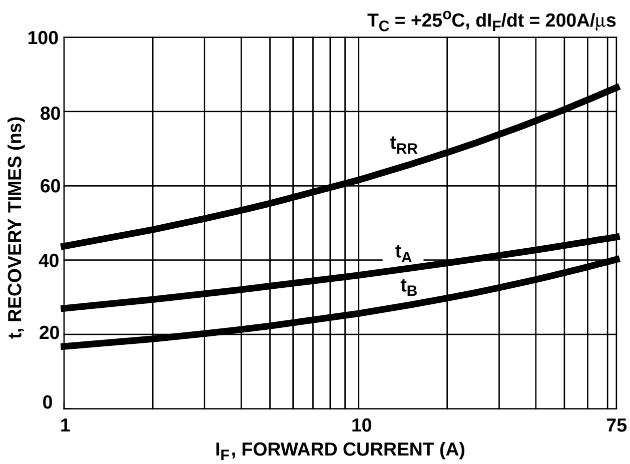


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25^{o}C

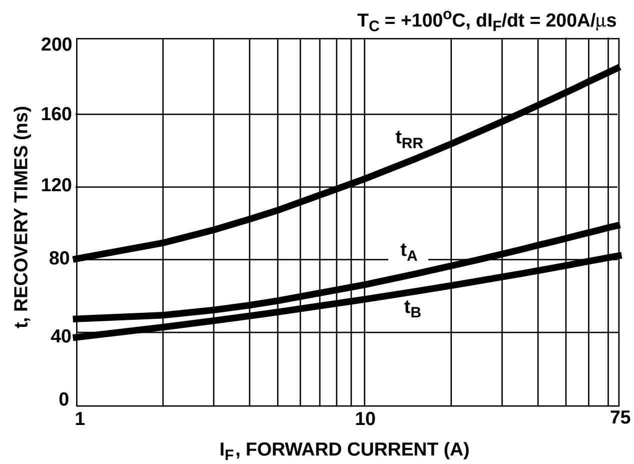


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100^{o}C

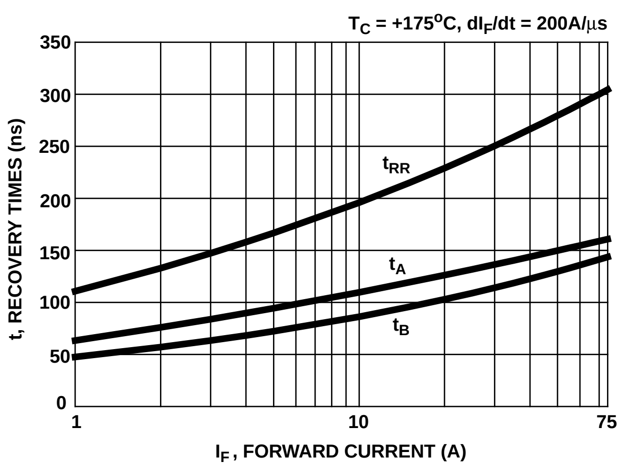


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175^{o}C

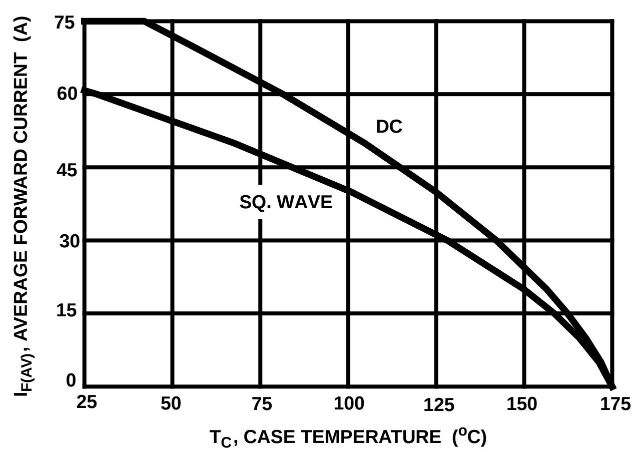


FIGURE 8. CURRENT DERATING CURVE

Typical Performance Curves

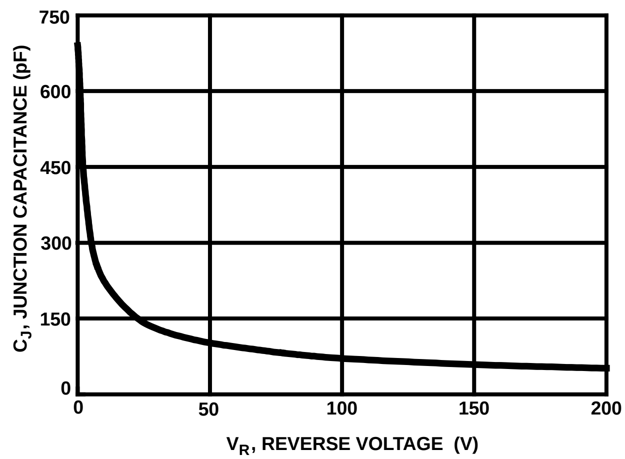


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

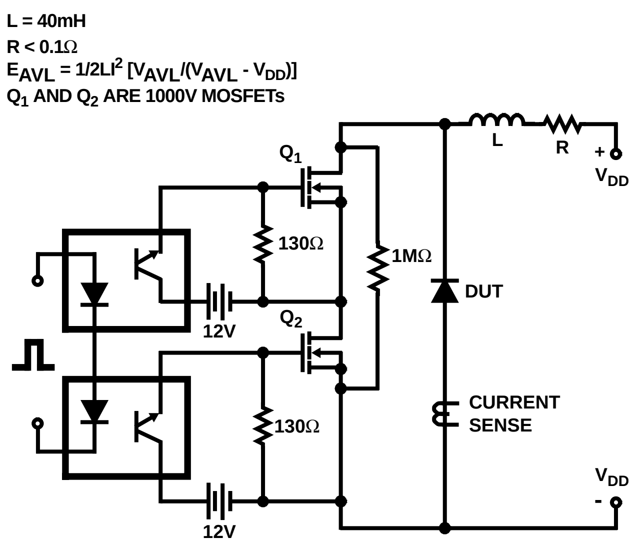


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

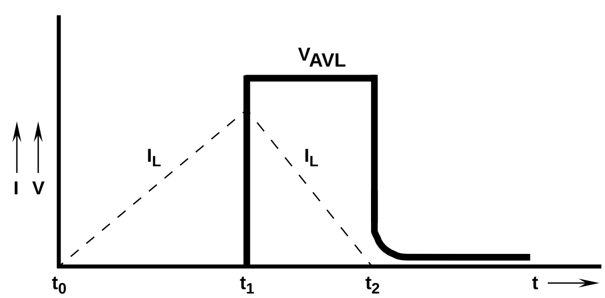
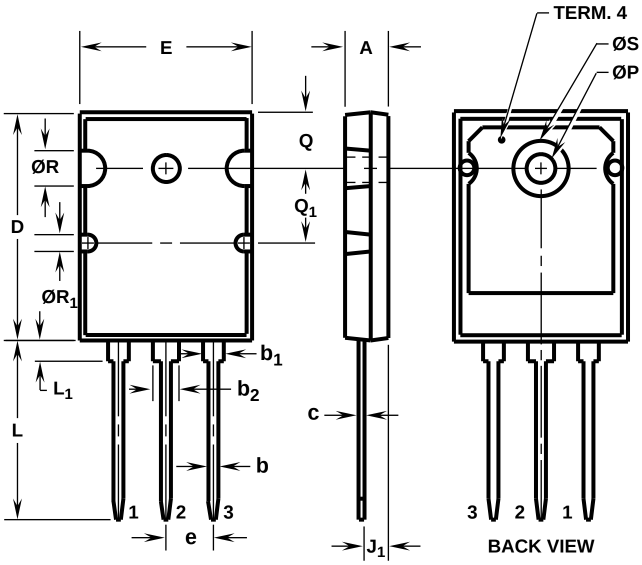


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

Packaging



TO-264AA

3 LEAD JEDEC TO-264AA PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.185	0.209	4.70	5.31	-
b	0.037	0.055	0.94	1.40	3, 4
b_1	0.087	0.102	2.21	2.59	2, 3
b_2	0.110	0.126	2.79	3.20	2, 3
c	0.017	0.029	0.43	0.74	2, 3, 4
D	1.007	1.047	25.58	26.59	-
E	0.760	0.799	19.30	20.29	-
e	0.215 BSC		5.46 BSC		5
J_1	0.102	0.118	2.59	3.00	6
L	0.779	0.842	19.79	21.39	-
L_1	0.087	0.102	2.21	2.59	2
ØP	0.122	0.138	3.10	3.51	-
Q	0.240	0.256	6.10	6.50	-
Q_1	0.330	0.346	8.38	8.79	-
ØR	0.155	0.187	3.94	4.75	-
ØR_1	0.085	0.093	2.16	2.36	-
ØS	0.270	0.280	6.87	7.12	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. B of JEDEC TO-264AA outline dated 11-93.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 5-95.

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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