SIEMENS

3.3V 168 pin Registered SDRAM Modules

32MB, 64MB, 128MB & 256MB Density

HYS72V4000GR-8
HYS72V8000GR-8
HYS72V1600GR-8
HYS72V3200GR-8

Target Information

- 168 Pin JEDEC Standard, Registered 8 Byte Dual-In-Line SDRAM Module
- 1 bank 4Mx72, 8M x 72, 16M x 72 & 32M x 72 organisation
- Optimized for ECC applications
- JEDEC standard Synchronous DRAMs (SDRAM)
- Performance:

		-8	Units
f_{CK}	Clock frequency (max.)	100	MHz
t_{CK}	Clock cycle time (min.)	10	ns
t_{AC}	Clock access time (min.) $\overline{\text{CAS}}$ latency = 3	6	ns

- Single +3.3V(± 0.3V) power supply
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs are LVTTL compatible
- Serial Presence Detect with E^2PROM
- Utilizes 16M SDRAMs in TSOPII-44 and 64M & 256M SDRAMs in TSOPII-54 packages with registers and registers
- 4096 refresh cycles every 64 ms
- Gold contact pad
- Card Size: 133,35 mm x 38,10mm x 4,00 mm
- This specification largely follows the JEDEC defined 168-pin-8-Byte Registered SDRAM DIMM Product Overview as of the JEDEC committe meeting of December 1996 (document number JC-42.5-96-146A) and - as far as applicable - INTEL‘s preliminary ‘PC SDRAM Registered DIMM Specification”Rev.0.8 (Dec.1997).

Target Information

The HYS72Vxx00GR family are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) which are organised as 4M x 72, 8M x 72, 16M x 72 & 32M x 72 high speed memory arrays designed with Synchronous DRAMs (SDRAMs) for ECC applications. All control and address signals are registered on-DIMM and the design incorporates a PLL circuit for the Clock inputs. Use of an on-board register reduces capacitive loading on the input signals but are delayed by one cycle in arriving at the SDRAM devices. Decoupling capacitors are mounted on the PC board.

The DIMMs use a serial presence detects scheme implemented via a serial E^2PROM using the two pin I^2C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All SIEMENS 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133,35 mm long footprint.

Target Information

Ordering Information

Type	Ordering Code	Package	Descriptions
HYS 72V4000GR-8	PC100-322-620R	L-DIM-168	32 MB Reg. DIMM with PLL
HYS 72V8000GR-8	PC100-322-620R	L-DIM-168-	64 MB Reg. DIMM w/o PLL
HYS 72V3200GR-8	PC100-322-620R	L-DIM-168-	256 MB Reg. DIMM w/o PLL
HYS 72V8000GR-8	PC100-322-620R	L-DIM-168-	64 MB Reg. DIMM with PLL
HYS 72V1600GR-8	PC100-322-620R	L-DIM-168-	128 MB Reg. DIMM with PLL
HYS 72V3200GR-8	PC100-322-620R	L-DIM-168-	256 MB Reg. DIMM with PLL

Pin Names

A0-A11,A12	Address Inputs	DQMB0 - DQMB7	Data Mask
BA0, BA1	Bank Selects	$\overline{CS0}$, $\overline{CS2}$	Chip Select
DQ0 - DQ63	Data Input/Output	REGE	Register Enable
CB0-CB7	Check Bits (x72 organisation only)	VDD	Power (+3.3 Volt)
$\overline{RAS}$	Row Address Strobe	VSS	Ground
$\overline{CAS}$	Column Address Strobe	SCL	Clock for Presence Detect
$\overline{WE}$	Read / Write Input	SDA	Serial Data Out for Presence Detect
$\overline{CKE0}$, $\overline{CKE1}$	Clock Enable	N.C.	No Connection
CLK0 - CLK3	Clock Input		

Address Format:

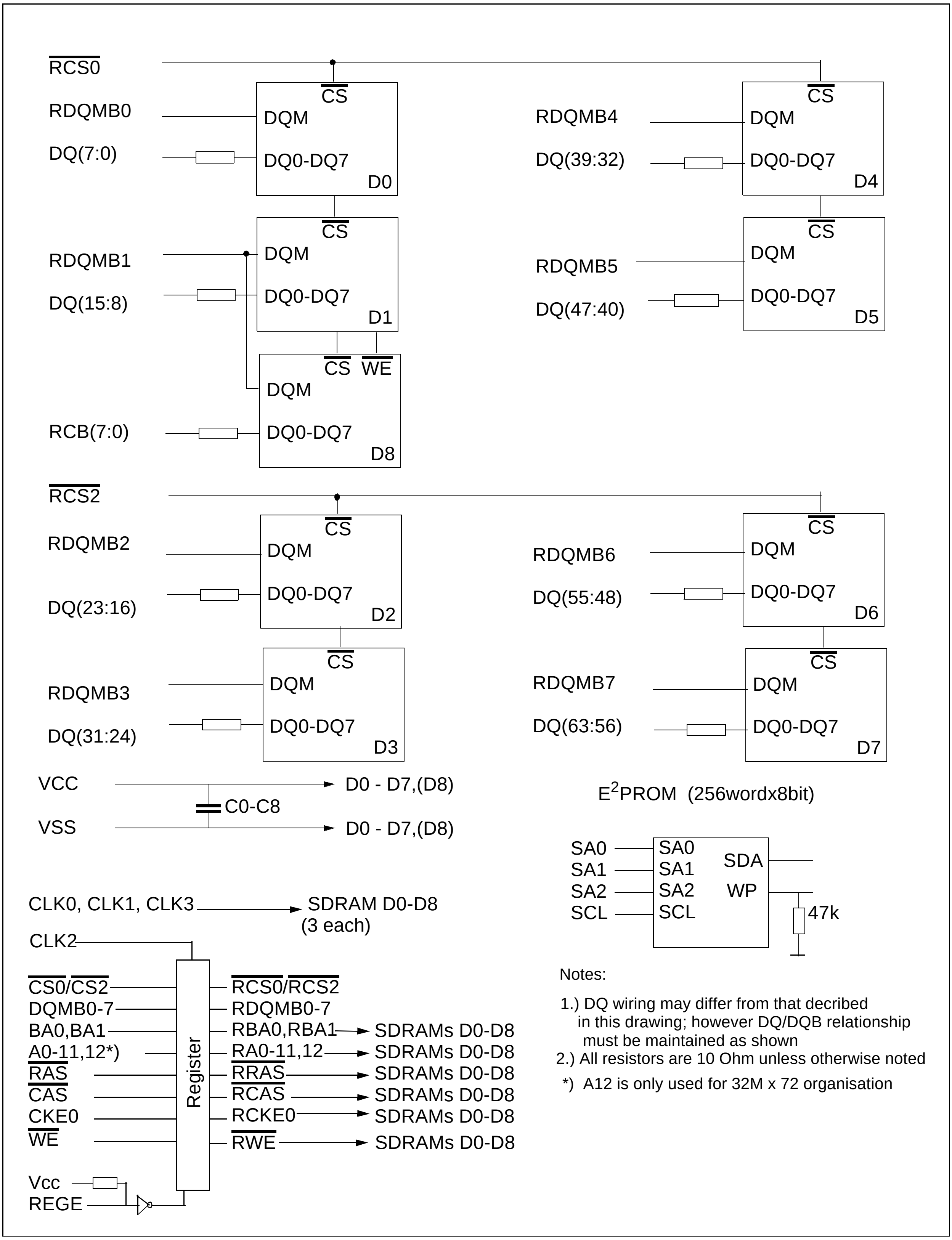
Density	Org.	Memory Banks	SDRAMs	# of SDRAMs	# of row/bank/ column bits	Refresh	Period	Interval
32 MB	4M x 72	1	4M x 4	18	11 / 1 / 10	4k	64 ms	15,6 µs
64 MB	8M x 72	1	8M x 8	9	12 / 2 / 9	4k	64 ms	15,6 µs
128 MB	16M x 72	1	16M x 4	18	12 / 2 / 10	4k	64 ms	15,6 µs
256 MB	32M x 72	1	32M x 8	9	13 / 2 / 10	4k	64 ms	15,6 µs

Target Information

Pin Configuration

PIN #	Symbol	PIN #	Symbol	PIN #	Symbol	PIN #	Symbol
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	CS2	87	DQ33	129	CS3
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VCC	48	DU	90	VCC	132	NC
7	DQ4	49	VCC	91	DQ36	133	VCC
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VCC	101	DQ45	143	VCC
18	VCC	60	DQ20	102	VCC	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	DU	104	DQ47	146	DU
21	CB0	63	CKE1	105	CB4	147	REGE
22	CB1	64	VSS	106	CB5	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VCC	68	VSS	110	VCC	152	VSS
27	WE	69	DQ24	111	CAS	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	CS0	72	DQ27	114	NC	156	DQ59
31	DU	73	VCC	115	RAS	157	VCC
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	CLK2	121	A9	163	CLK3
38	A10 (AP)	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	VCC	82	SDA	124	VCC	166	SA1
41	VCC	83	SCL	125	CLK1	167	SA2
42	CLK0	84	VCC	126	A12	168	VCC

Note : Pinnames in brackets are for the x72 ECC versions



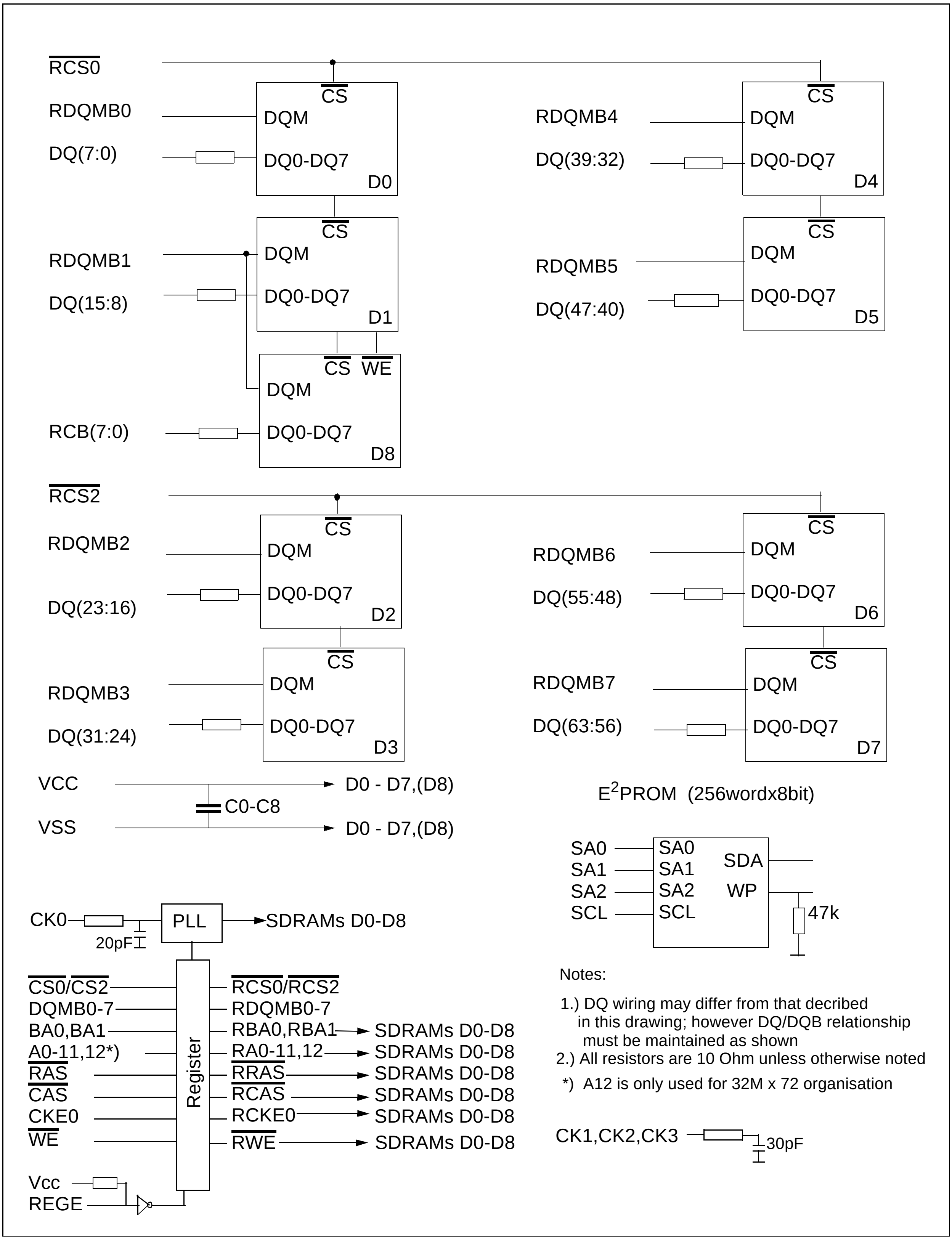
Notes:

1.) DQ wiring may differ from that decribed in this drawing; however DQ/DQB relationship must be maintained as shown

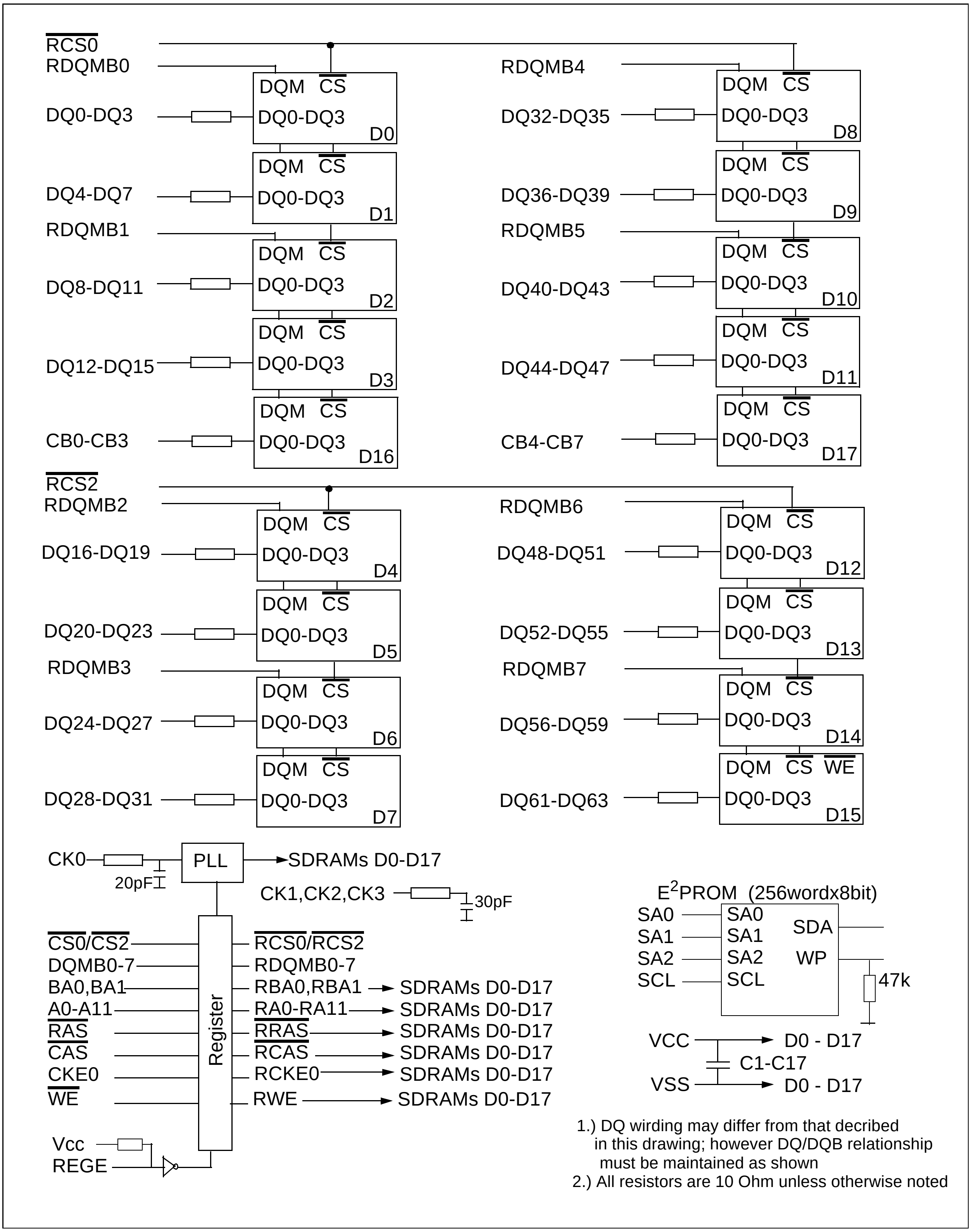
2.) All resistors are 10 Ohm unless otherwise noted

*) A12 is only used for 32M x 72 organisation

Block Diagram for 8M x 72 & 32M x 72 SDRAM DIMM modules (without PLL circuit)



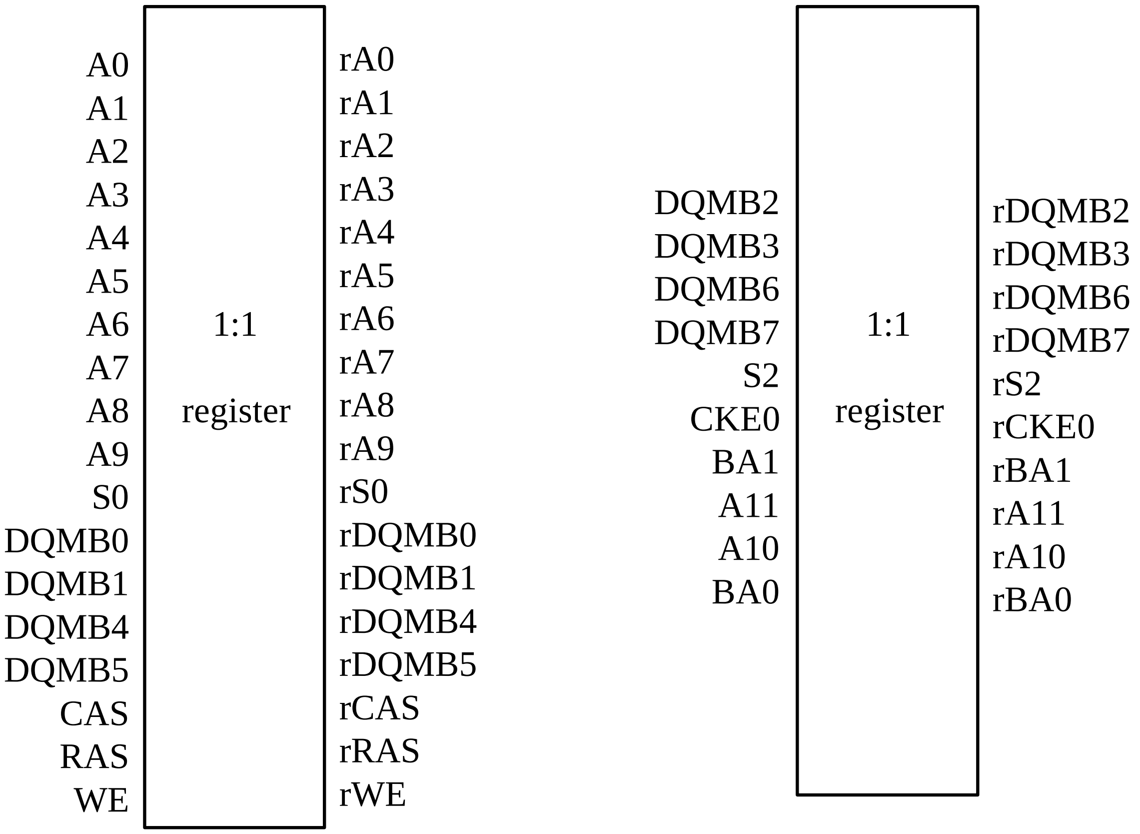
Block Diagram for 8M x 72 & 32M x 72 SDRAM DIMM modules (with PLL circuit)



Block Diagram for 4M x 72 & 16M x 72 SDRAM DIMM modules (with PLL circuit)

Target Information

Register Wiring and Partnumbers:



Target Information

Manufacturer	Partnumber	Description
TI / Hitachi	74ALVC162835	18Bit, 1:1 Register with internal damping resistors
TI / Hitachi	72ALVC16835	18Bit, 1:1 Register
TI	CDC2509	1:9 PLL Based Clock Driver
TI	CDC2510	1:10 PLL Based Clock Driver

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD}, V_{DDQ} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	V_{IH}	2.0	Vcc+0.3	V
Input low voltage	V_{IL}	– 0.5	0.8	V
Output high voltage (I_{OUT} = – 2.0 mA)	V_{OH}	2.4	–	V
Output low voltage (I_{OUT} = 2.0 mA)	V_{OL}	–	0.4	V
Input leakage current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 80	80	µA
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	– 80	80	µA

Capacitance

T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values	Unit
		min.	
Input capacitance (A0 to A10, BA0)	C_{I1}	10	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{I2}	10	pF
Input capacitance (CKE0, CKE1)	C_{I3}	10	pF
Input capacitance (CLK0 - CLK3, CS0, CS2)	C_{I4}	10	pF
Input capacitance (DQMB0 - DQMB7)	C_{I5}	10	pF
Input / Output capacitance (DQ0-DQ63,CB0-CB7)	C_{IO}	10	pF
Input Capacitance (SCL,SA0-2)	C_{sc}	8	pF
Input/Output Capacitance	C_{sd}	10	pF

Target Information

Standby and Refresh Currents (T_a = 0 to 70°C, VCC = 3.3V ± 0.3V**)**

Parameter	**Symbol**	**Test Condition**	**64MB**	**128MB**	**256MB**		**Note**
Operating Current	Icc1	Burst length = 1, CL=3 trc>=trc(min.), tck>=tck(min.), Io=0 mA 2 bank interleave operation				mA	1,2
Operating Current	Icc1	Burst length = 4, CL=3 trc>=trc(min.), tck>=tck(min.), Io=0 mA 2 bank interleave operation				mA	1,2
Precharged Standby Current in Power Down Mode	Icc2P	CKE<=VIL(max), tck>=tck(min.)				mA	
	Icc2PS	CKE<=VIL(max), tck=infinite				mA	
Precharged Standby Current in Non-power Down Mode	Icc2N	CKE>=VIH(min), tck>=tck (min.), input changed once in 3 cycles				mA	$\overline{CS}$= High
	Icc2NS	CKE>=VIH(min), tck=infinite, no input change				mA	
Active Standby Current in Power Down Mode	Icc3P	CKE<=VIL(max), tck>=tck(min.)				mA	
	Icc3PS	CKE<=VIL(max), tck=infinite				mA	
Active Standby Current in Non-power Down Mode	Icc3N	CKE>=VIH(min), tck>=tck (min.) input changed one time				mA	$\overline{CS}$= High
	Icc3NS	CKE=>VIH(min),tck=infinite, no input change				mA	
Burst Operating Current	Icc4	Burst length = full page, trc = infinite, CL = 3, tck>=tck (min.), Io = 0 mA 2 banks activated				mA	1,2
Auto (CBR) Refresh Current	Icc5	trc>=trc(min)				mA	1,2
Self Refresh Current	Icc6	CKE=<0,2V				mA	1,2

AC Characteristics (SDRAM Device Specification) 3)4)
T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values		Unit	
		-8			
		min	max		
Clock and Clock Enable					
Clock Cycle Time $\overline{CAS}$ Latency = 2	t_{CK}	10	–	ns	
Clock Frequency $\overline{CAS}$ Latency = 2	t_{CK}	–	100	MHz	
Access Time from Clock $\overline{CAS}$ Latency = 2	t_{AC}	–	6	ns	4
Clock High Pulse Width	t_{CH}	3	–	ns	
Clock Low Pulse Width	t_{CL}	3	–	ns	
Transition time	t_T	0.5	10	ns	
Setup and Hold Times					
Input Setup Time	t_{IS}	2	–	ns	5
Input Hold Time	t_{IH}	1	–	ns	5
CKE Setup Time	t_{CKS}	2	–	ns	5
CKE Hold Time	t_{CKH}	1	–	ns	5
Mode Register Set-up time	t_{RSC}	16	–	ns	
Power Down Mode Entry Time	t_{SB}	0	8	ns	
Common Parameters					
Row to Column Delay Time	t_{RCD}	20	–	ns	6
Row Precharge Time	t_{RP}	20	–	ns	6
Row Active Time	t_{RAS}	45	100k	ns	6
Row Cycle Time	t_{RC}	60	–	ns	6
Activate(a) to Activate(b) Command period	t_{RRD}	16	–	ns	6
$\overline{CAS}$(a) to $\overline{CAS}$(b) Command period	t_{CCD}	1	–	CLK	

Target Information

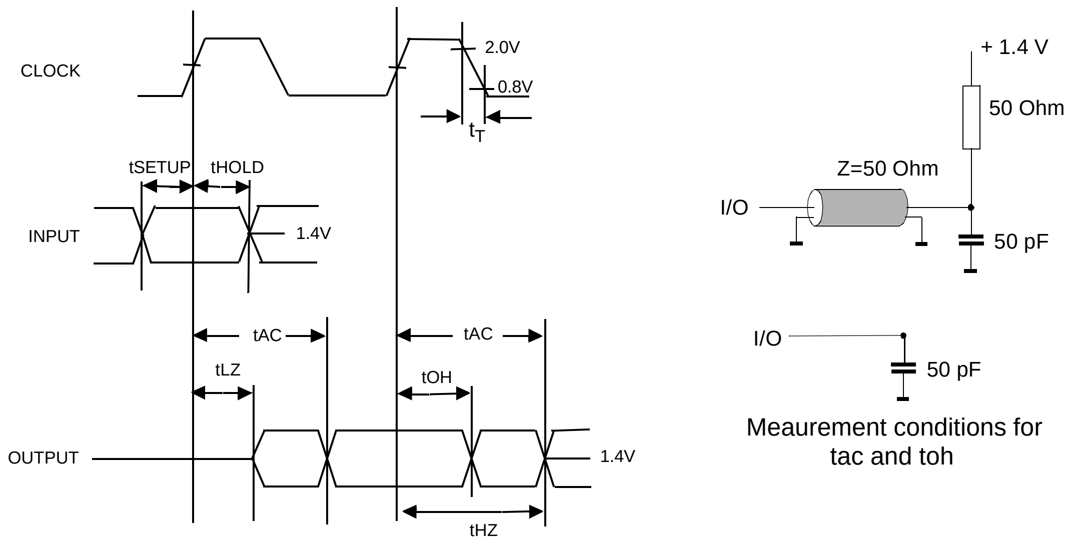
Parameter	Symbol	Limit Values -8 min	Limit Values -8 max	Unit	
Refresh Cycle					
Refresh Period (4096 cycles)	t_{REF}	–	64	ms	
Self Refresh Exit Time	t_{SREX}	10		ns	
Read Cycle					
Data Out Hold Time	t_{OH}	3	–	ns	
Data Out to Low Impedance Time	t_{LZ}	0	–	ns	
Data Out to High Impedance Time	t_{HZ}	3	8	ns	8
DQM Data Out Disable Latency	t_{DQZ}	2	–	CLK	
Write Cycle					
Write Recovery Time	t_{WR}	8	–	ns	
DQM Write Mask Latency	t_{DQW}	0	–	CLK	

Clock Frequency and Latency (Registed DIMM Module Specification): 9)

Parameter		Symbol		Unit	Notes
Clock Frequency	max.	t_{CK}	**100**	MHz	
Clock Cycle Time	min.	t_{CK}	10	ns	
$\overline{CAS}$ Latency	min.	t_{AA}	3	CLK	10)
RAS to CAS Delay	min.	t_{RCD}	2	CLK	
RAS Latency	min.	t_{RL}	6	CLK	10)
Precharge Time	min.	t_{RP}	2	CLK	
Data In to Precharge	min.	t_{DPL}	2	CLK	
Data In to Active / Refresh	min.	t_{DAL}	5	CLK	
Bank to Bank Delay Time	min.	t_{RRD}	2	CLK	
$\overline{CAS}$ to $\overline{CAS}$ delay time	min.	t_{CCD}	1	CLK	
Write Latency	fixed	t_{WL}	1	CLK	10)
DQM Write Mask Latency	fixed	t_{DQW}	1	CLK	
DQM Data Disable Latency	fixed	t_{DQZ}	1	CLK	
Clock Suspend Latency	fixed	t_{CSL}	1	CLK	10)

Notes:

1. The specified values are valid when addresses are changed no more than once during tck(min.) and when No Operation commands are registered on every rising clock edge during tRC(min).
2. The specified values are valid when data inputs (DQ's) are stable during tRC(min.).
3. An initial pause of 100µs is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin. Also the on-DIMM PLL must be given enough clock cycles to stabilize (t_{STAB}) before any operation can be guaranteed.
4. AC timing tests have V_{il} = 0.8V and V_{ih} = 2.0V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{ih} and V_{il}. All AC measurements assume t_T=1ns with the AC output load circuit shown. Specified tac and toh parameters are measured with a 50



pF only, without any resisitve termination and with a input signal of 1V / ns edge rate between 0.8V and 2.0 V.
5. Any time that the refresh Period has been exceeded, a minimum of two Auto (CRB) Refresh commands must be given to "wake-up" the device.
6. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to tRC is satisfied once the Self Refresh Exit command is registered.
7. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.
8. t_{DAL} is equivalent to t_{DPL} + t_{RP}.
9. Due to the usage of a register device on all input and address signals, all external command cycle are delayed by one clock (Reg-DIMM Latency = 1) on the module board.
10. Delayed by one clock cycle due to the use of the register device.

Target Information

A serial presence detect storage device - E ^{2}PROM 34C02 - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E ^{2}PROM device during module production using a serial presence detect protocol (I^{2}C synchronous 2-wire bus)

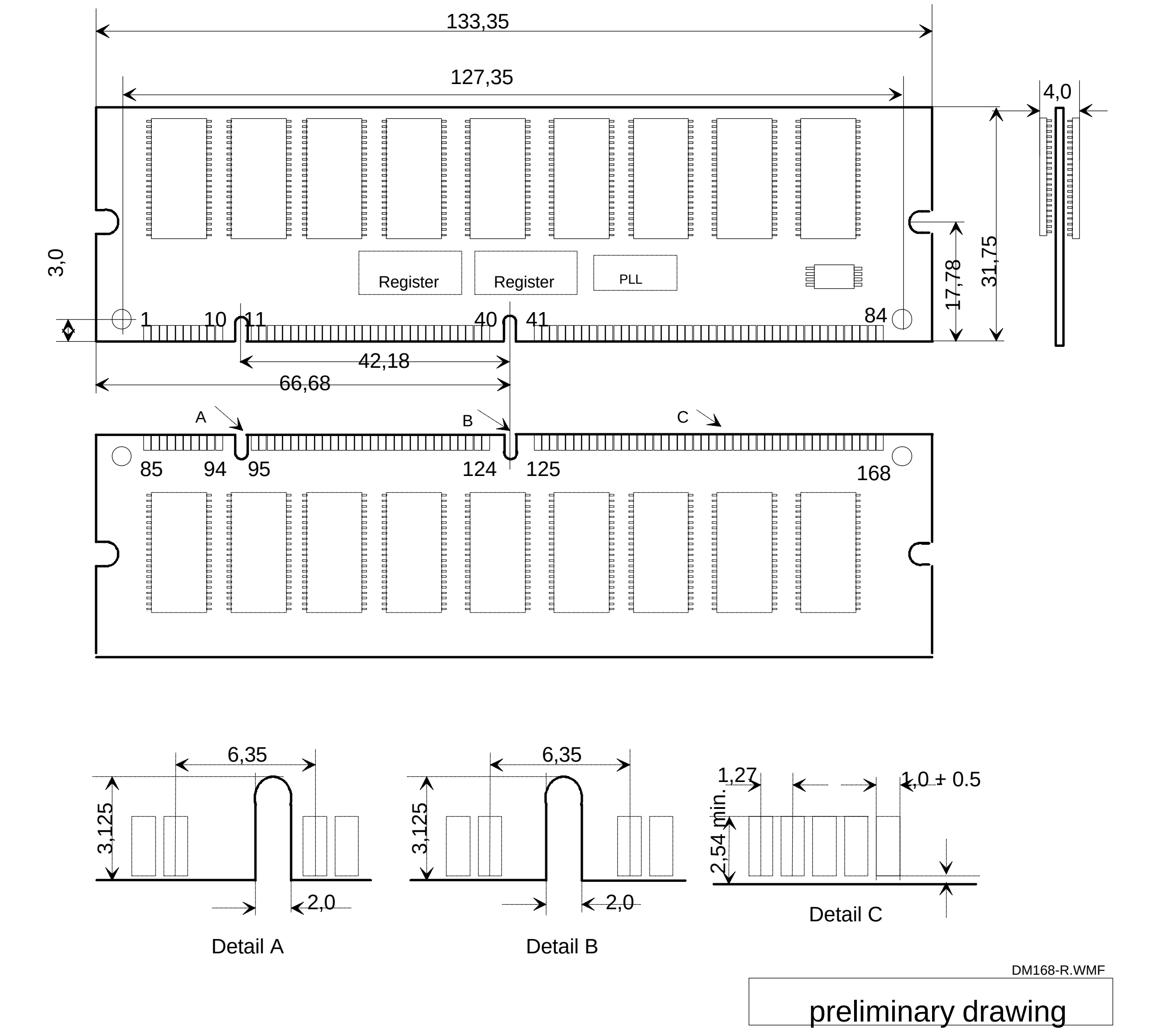
SPD-Table:

Byte#	Description	SPD Entry Value	Hex			
			32 MB	64MB	128MB	256MB
0	Number of SPD bytes	128	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04
3	Number of Row Addresses (without BS bits)	11/ 12 / 13	0B	0C	0C	0D
4	Number of Column Addresses	9 / 10	0A	09	0A	0A
5	Number of DIMM Banks	1	01	01	01	01
6	Module Data Width	72	48	48	48	48
7	Module Data Width (cont'd)	0	00	00	00	00
8	Module Interface Levels	LVTTL	01	01	01	01
9	Cycle Time at CL=3	10.0 ns	A0	A0	A0	A0
10	Access time from Clock at CL=3	6.0 ns	60	60	60	60
11	Dimm Config (Error Det/Corr.)	ECC	02	02	02	02
12	Refresh Rate/Type	Self-Refresh, 15.6µs	80	80	80	80
13	SDRAM width, Primary	x4, x8	04	08	04	08
14	Error Checking SDRAM data width	n/a / x4	04	08	04	08
15	Minimum tCCD	t_{ccd} = 1 CLK	01	01	01	01
16	Burst Length supported	1, 2, 4, 8 & full page	8F	8F	8F	8F
17	Number of SDRAM banks	4	02	04	04	04
18	SDRAM Supported CAS Latencies	$\overline{\text{CAS}}$ latency = 2 & 3	06	06	06	06
19	SDRAM CS Latencies	CS latency = 0	01	01	01	01
20	SDRAM WE Latencies	Write latency = 0	01	01	01	01
21	SDRAM DIMM module attributes	registered with PLL	16	16	16	16
		registered w/o PLL	--	12	--	12
22	SDRAM Device Attributes :General	Vcc tol +/- 10%	06	06	06	06
23	Min. Clock Cycle Time at CAS Latency = 2	10 ns	A0	A0	A0	A0
24	Max. data access time from Clock for CL=2	6 ns	60	60	60	60
25	Min. Clock Cycle Time at CL = 1	not supported	FF	FF	FF	FF
26	Max. Data Access Time from Clock at CL=1	not supported	FF	FF	FF	FF
27	SDRAM Minimum tRP	20 ns	14	14	14	14
28	SDRAM Minimum tRRD	16 ns	10	10	10	10
29	SDRAM Minimum tRCD	20 ns	14	14	14	14
30	SDRAM Minimum tRAS	45 ns	2D	2D	2D	2D
31	Module Bank Density (per bank)	32/64/128/256 MByte	08	10	20	40
32	SDRAM input setup time	2 ns	20	20	20	20
33	SDRAM input hold time	1 ns	10	10	10	10
34	SDRAM data input setup time	2 ns	20	20	20	20
35	SDRAM data input hold time	1 ns	10	10	10	10
36-61	Superset information (may be used in future)		FF	FF	FF	FF
62	SPD Revision	Revision 1.2	12	12	12	12

Target Information

63	Checksum for bytes 0 - 62		EE	00	ndy	ndy
64-125	Manufacturer's information (optional) (FFh if not used)		FF	FF	FF	FF
126	Frequency Specification	100 MHz	64	64	64	64
127	Details of 100 MHz support	registered with PLL	8F	8F	8F	8F
128+	Unused storage locations		FF	FF	FF	FF

Module Package
L-DIM-168-xx



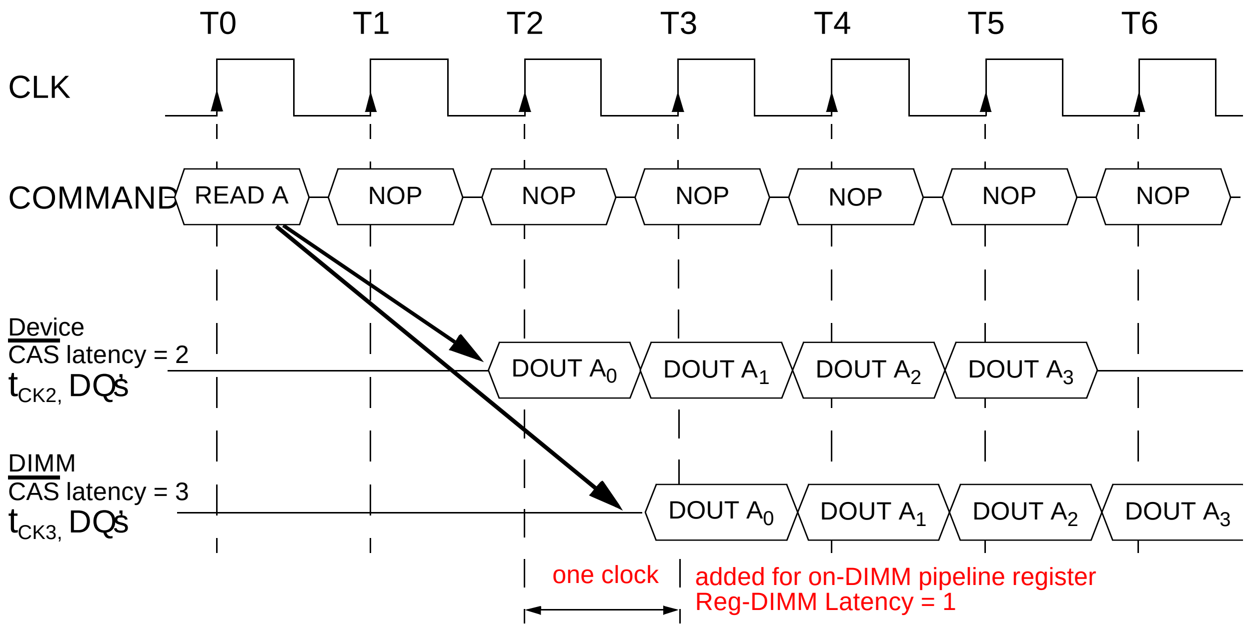
Functional Description

All 168 Pin Registered DIMMs conform to a compatible set of timing and operation characteristics intended to comply with the 100 MHz standards. The Registered DIMMs achieve high speed data transfer rate up to 100 MHz.

All control and address signals are synchronized with the positive edge of externally supplied clocks and are registerd on-DIMM and hence delayed by one clock cycle in arriving at the SDRAM devices. The use of the on-board register reduces the capacitive loading of the DIMM on input controll and address signals. The SDRAM device data lines (DQ) are connected directly to the DIMM tabs through 10 Ohm series resistors. All the following timing diagrams and explanations show DIMM operation at the tabs, not SDRAM operation.

The picture below depicts an overview of the effect of the Registered Mode on the data outputs (DQs) for a Read operation. Without the registers, the data is delayed according to the device $\overline{CAS}$ latency, in the case two clocks. With the register, the data is delayed according to the device $\overline{CAS}$ latency plus an additional clock cycle. This is know as the DIMM $\overline{CAS}$ latency, and in this example is four three. The data path can be thought of as a pipeline in which the register effectively lengthens the pipe by one clock cycle.

Registered DIMM Burst Read Operation (BL=4)



Target Information

In case of a Burst Write Command the data-in is delayed one clock due th the op-DIMM pipeline register also. Therefore, data for the first Burst Write cycle must be applied on the DQ pins on the next clock cycle after the Write command is issued. the remainig data inputs must be supplied on each subsequent rising clock edge until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored.