RCD16-47B

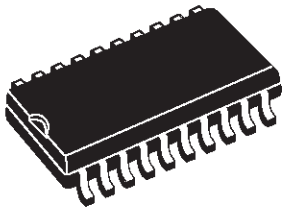
Application Specific Discretes
A.S.D.™

RCD NETWORK FOR BUS TERMINATION

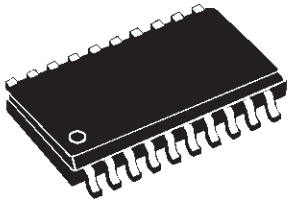
MAIN APPLICATIONS

In any electronic equipment where a suitable bus termination is required to avoid signal reflections and distortions :

- PC and workstation computer
- Data-line analyzers



SO20



SSOP20

DESCRIPTION

With the increasing speed of data transmission, line reflections provide signal distorsions and the overshoots or undershoots produced on the signal edges can cause the malfunction of the whole system.

To avoid these negative effects from leading to problems, a suitable termination is required. Dedicated to bus termination, the RCD16-47B provides by far the best method to minimise stray emissions from PCB tracks.

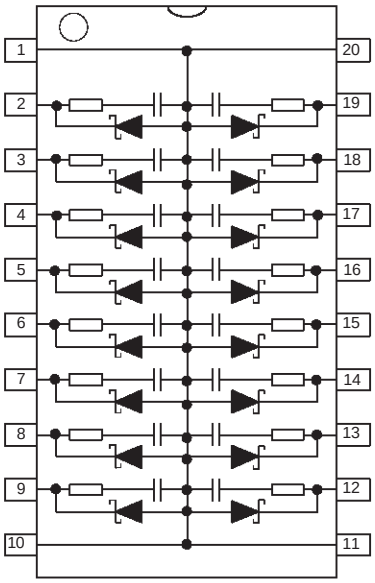
FEATURES

- NETWORK OF 16 R-C-D LINE TERMINATIONS
- RESISTANCE : R = 47 Ω, TOLERANCE +/- 10%
- CAPACITANCE : C = 33 pF, TOLERANCE +/- 10%
- SCHOTTKY DIODE : (D)

BENEFITS

- Provides impedance matching, thus increasing noise immunity and minimizing distortion.
- Lowers EMI / RFI radiation.
- No DC power dissipation.
- Eliminates negative voltages : no current will change the bias of the protected device.
- Uses the best of all termination schemes.

FUNCTIONAL DIAGRAM



R = 47 Ω, tolerance +/– 10 %
C = 33 pF, tolerance +/- 10 %
D = Schottky diode

COMPLIES WITH THE FOLLOWING STANDARDS:

MIL STD 883C - Method 3015-6

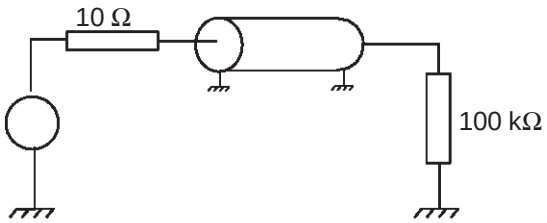
- V_{PP} = 2 kV C= 100 pF R = 1500 Ω
- 3 positive strikes and 3 negative strikes (F = 1 Hz)

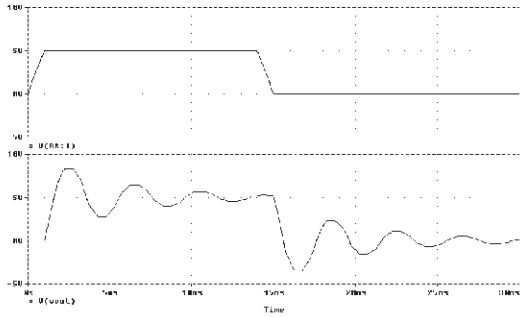
APPLICATION NOTE : BUS TERMINATION

With the increasing speed of data transmission (PC, TV, ...), engineers are naturally confronted with effects that were of less significance with slower circuits. Among these are the effects described in transmission line theory : line reflections provide signal distortions and the overshoots or undershoots produced on the signal edges can finally cause the malfunction of the whole system.

1. Reflection at a non terminated line

The figure below shows the circuit of a transmission system in which a memory device (input impedance of 100 kΩ) is connected at the end of a line with line impedance Zo.





If this line is not properly terminated, a certain amount of the energy is reflected back, inducing a reflection phenomena that can distort the signal. This can result in improper operation of the system.

The simulation shown on the above figure illustrates the signal distortion produced by line reflection at the end of the line which is not well terminated.

Even if the signal at the start of the line has the correct form (upper curve), considerable distortion arises at the end of the line (lower curve). On the positive edge, the overshoot can exceed the maximum operating voltage of the used circuit technology which will then be destroyed. Also, the following negative undershoot may reach a level low enough to change the value of the logic state. If it affects of an address line, a wrong memory cell will be addressed, and in the case of a data line, the data can be corrupted.

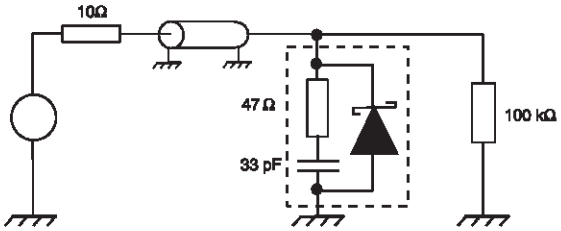
This phenomena also occurs on the falling edge.

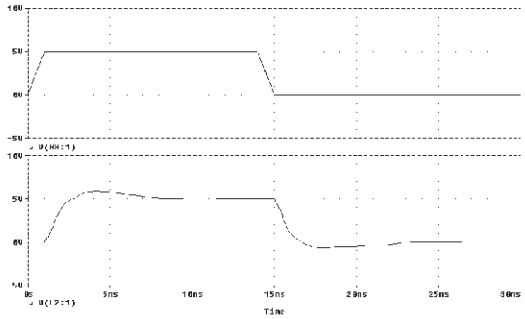
To avoid these negative effects from leading to problems in a system, a suitable termination is required.

2. The RCD termination

The traditional solution to properly match each line of the bus consists of the use of several discrete resistances, capacitors and small schottky diodes. For a 16-bit bus, this requires 48 discrete components.

SGS-THOMSON offers an innovating solution with a monolithic structure using **ASD™** technology (*).
The **ASD™** technology enables to integrate monolithically 16 of these RCD "basic cells" onto a single chip device. The **RCD16-47B** reduces component cost and assembly cost, saves board space and improves reliability.





The simulation illustrates the signal distortion produced by line reflection at the end of the line when such a termination is used.

- The resistor provides the path termination for PCB track, thus resulting in low reflection phenomena.
- The capacitor of 33 pF blocks DC currents while acting as a short circuit during signal transitions, and holds the bus at the last logic level. It reduces power consumption and avoids excessive current.
- The small Schottky diode clamps the negative remaining undershoots which can result from impedance mismatch. This damps negative voltages and prevents the logic signal from rising above the logic level '0' threshold after a falling edge.

The RCD termination provides optimal solution compared to all other termination techniques.

(*) ASD™ = Apllicaion Specific Discretes.

ABSOLUTE MAXIMUM RATINGS ($0°C \leq T_{amb} \leq 70°C$)

Symbol	Parameter	Value	Unit
P	Total power dissipation per package	500	mW
I_F	Continuous forward current per Schottky diode	50	mA
V_{RRM}	Repetitive peak reverse voltage	7.5	V
V_{PP}	Maximum electrostatic discharge MIL STD 883C - METHOD 3015-6	2	kV
T_{stg} T_j	Storage temperature range Maximum junction temperature	- 55 to + 150 150	°C °C

THERMAL RESISTANCE

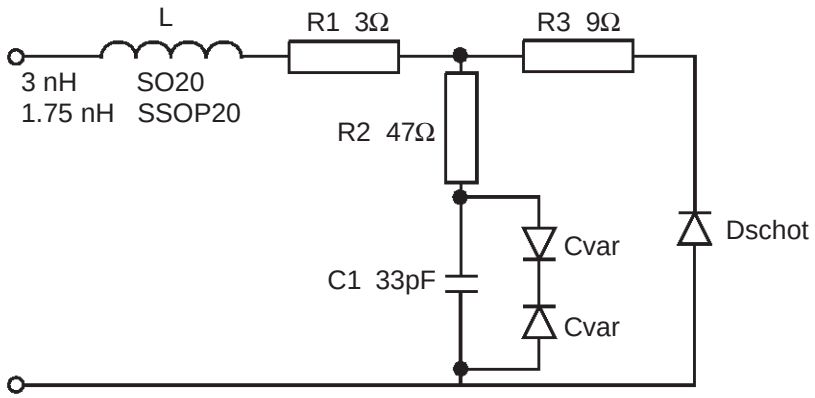
Symbol	Parameter	Package	Value	Unit
$R_{th(j-a)}$	Junction to ambient	SO20 SSOP20	100 140	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter and test conditions			Typ.	Max.	Unit
R_C	Connection resistance (note1)		T_{amb} = 25°C		0.25	Ω
C_t	Total capacitance	F = 1 MHz, V_R = 0V, V_{RMS} = 30 mV		45		pF
I_R	Leakage current	$V_R = V_{RRM}$	T_j = 25 °C T_j = 70 °C		1 10	µA
V_F	Forward voltage	I_F = 1 mA I_F = 16 mA	T_j = 25 °C T_j = 25 °C		0.5 1	V

Note 1 : Rc is the resistance between pin 1 and pin 11 or between pin 10 and pin 20

PSPICE MODEL per RCD CELL



Dschot parameters

Spec. parameters
- Vf / If
  - 0.3V / 1 nA
  - 0.35V / 100nA
  - 0.5V / 1mA
  - 1.0V / 16mA
- Capacitance (JC)
  - 0.1V / 6pF
  - 5V / 3pF
- Leakage (RL)
  - 7.5V / 1µA
- Breakdown (RB)
  - Vz=18V Iz=1mA Zz=100
- Recovery (RR)
  - trr=0

PSpice parameters
- DBREAK model
  - IS=1.570E-12
  - N=1.258
  - RS=1.000E-3
  - IKF=504.2E-6
  - CJO=6.279E-12
  - M=.3626
  - VJ=.75
  - ISR=419.2E-9
  - BV=18.14
  - IBV=.2586
  - TT=5.000E-9

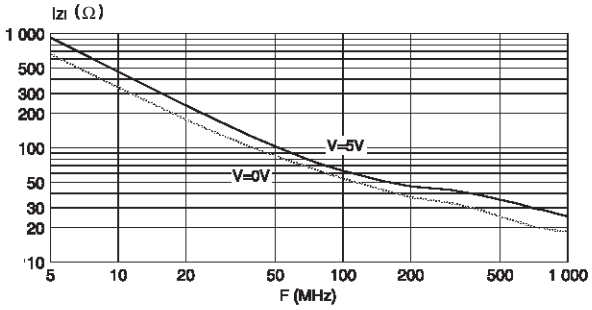
Cvar parameters

Spec. parameters
- Vf / If
  - 0.3V / 1 nA
  - 0.35V / 100nA
  - 0.5V / 1mA
  - 1.0V / 16mA
- Capacitance (JC)
  - 0.1V / 24pF
  - 5V / 2pF
- Leakage (RL)
  - 7.5V / 1µA
- Breakdown (RB)
  - Vz=18V Iz=1mA Zz=100
- Recovery (RR)
  - Trr=0

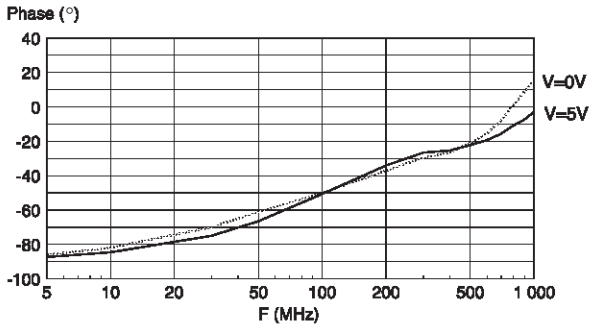
PSpice parameters
- DBREAK model
  - IS=1.570E-12
  - N=1.258
  - RS=1.000E-3
  - IKF=504.2E-6
  - CJO=28.24E-12
  - M=1.300
  - VJ=.75
  - ISR=44.30E-9
  - BV=18.14
  - IBV=.2586
  - TT=5.000E-9

SO20 Package

Z magnitude versus frequency

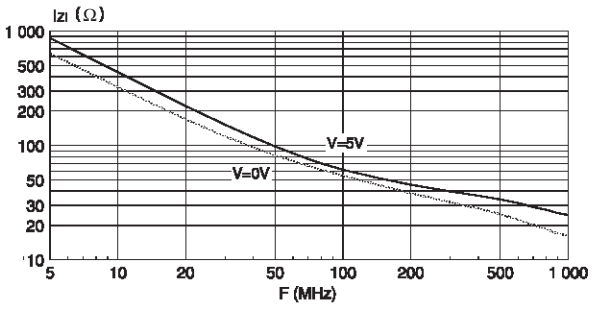


Phase versus frequency

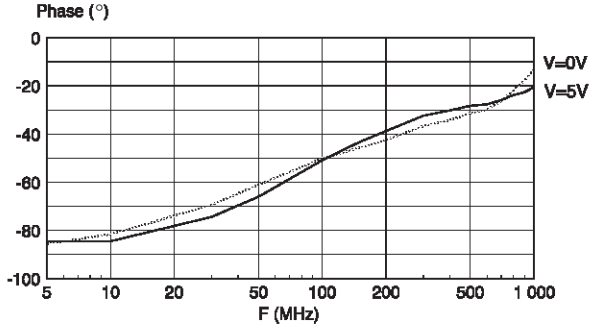


SSOP 20 Package

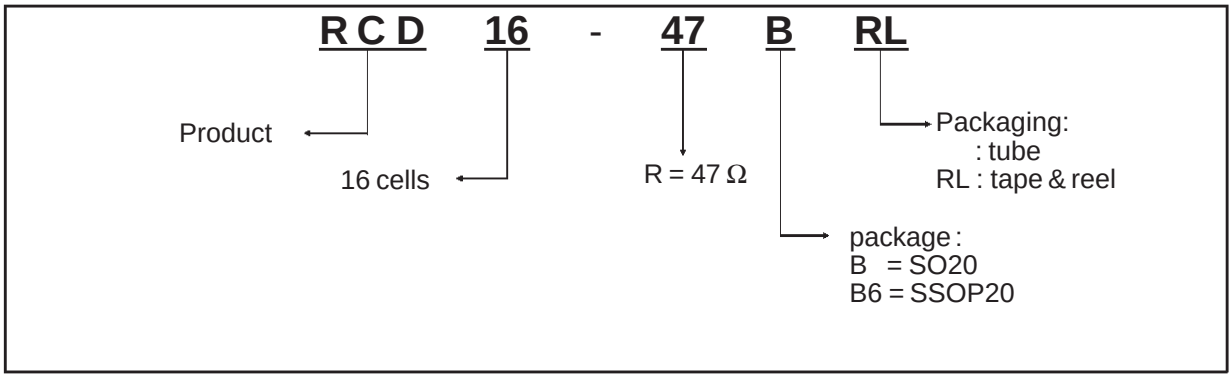
Z magnitude versus frequency



Phase versus frequency



ORDER CODE



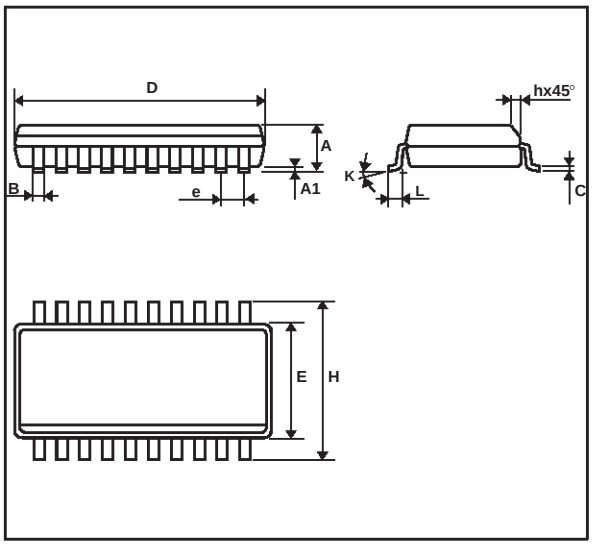
Product	Package	Base Qty	
		Tube	Tape & reel
RCD16-47B	SO20	40	1000
RCD16-47B6	SSOP20	66	2000

MARKING

Type	Package	Marking
RCD16-47B	SO20	RCD1647B
RCD1647B6	SSOP20	RCD1647B6

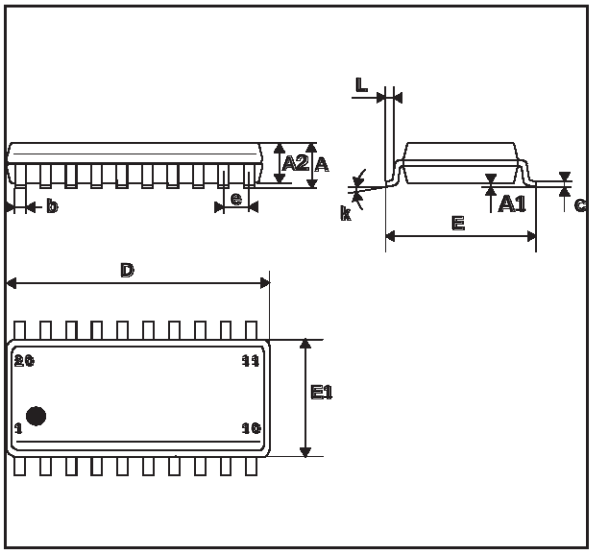
Packging : Preferred packaging is tape and reel.

PACKAGE MECHANICAL DATA
SO20 (Plastic)



REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.35		2.65	0.092		0.104
A1	0.10		0.20	0.004		0.008
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.6		13.0	0.484		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.029
L	0.50		1.27	0.020		0.050
K	8° (max)					

SSOP20 (Plastic)



REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.00			0.079
A1			0.25			0.010
A2	1.51		2.00	0.059		0.079
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10		0.35	0.004		0.014
D	7.05		8.05	0.278		0.317
E	7.60		8.70	0.299		0.343
E1	5.02	6.10	6.22	0.198	0.240	0.245
e		0.65			0.026	
k	0°		10°	0°		10°
L	0.25	0.50	0.80	0.010	0.020	0.031