SIEMENS

ICs for Communications

Interworking Element
IWE8

PXB 4220 Version 1.1

Preliminary Data Sheet 11.96

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1 Overview

The Interworking Element (IWE8) PXB 4220 is a member of the Siemens ATM chip set. Together with framing and line interface components (e.g. Siemens PEB 2254) the IWE8 provides connection of 8 E1 or T1 input and output ports to an Asynchronous Transfer Mode (ATM) network.

Each port can be configured independently to operate in one of two basic modes:

ATM mode

ATM mode ports operate as an ATM User Network Interface (UNI) at 2.048 Mbit/s (E1) or 1.544 Mbit/s (T1).

The IWE8 supports the mapping of ATM cells in T1/E1 frames according to ITU-T G.804 [].

The functions of the transmission medium independent Transmission Convergence (TC) sublayer of the Physical Layer (PHY) defined in ITU-T I.432 [21] are implemented by the IWE8.

AAL mode

AAL mode ports operate as an ATM Circuit Emulation Service Interworking Function (CES-IWF) between Constant Bit Rate (CBR) equipment and an ATM network as described by the ATM Forum in [24].

The CBR circuits are converted into ATM constant bit-rate virtual channels using the ATM Adaptation Layer type 1 (AAL1) or without any ATM Adaptation Layer overhead (referred to as AAL type 0 throughout the rest of this document).

The IWE8 provides the segmentation and reassembly function.

Both the “Unstructured DS1/E1 Service” and the “Structured DS1/E1 N x 64 kbit/s Basic Service” as described by the ATM Forum in [24] are supported. For simplicity reasons the shorthand notation “unstructured CES” will be used to identify the “Unstructured DS1/E1 Service” while the “Structured DS1/E1 N x 64 kbit/s Basic Service” will be referred to as “N x 64 kbit/s” throughout the rest of this document.

Typical applications

Figure 1 illustrates three typical application areas which utilize the IWE8 chip in Line Interface Cards (LICs) or Network Interface Controllers (NICs).

Application 1 utilizes the IWE8 as an internetworking device for communication between a narrowband Time-Slot based network and an ATM network.

Application 2 utilizes the IWE8 chip to enable the use of an existing T1/E1 access line for connection to an ATM network.

Overview

In application 3, the IWE8 chip enables terminals using a Leased Line or Time-Slot based service to convert from T1/E1 network connection to ATM network connection without noticeable changes to the subscriber. Note that connection from Frame Relay to an ATM network is best handled by Siemens' SARE chip, the PXB 4110, instead of the IWE8. The SARE is capable of translating frames into cells, whereas the IWE8 is designed for translating Constant Bit Rate (CBR) data formats.

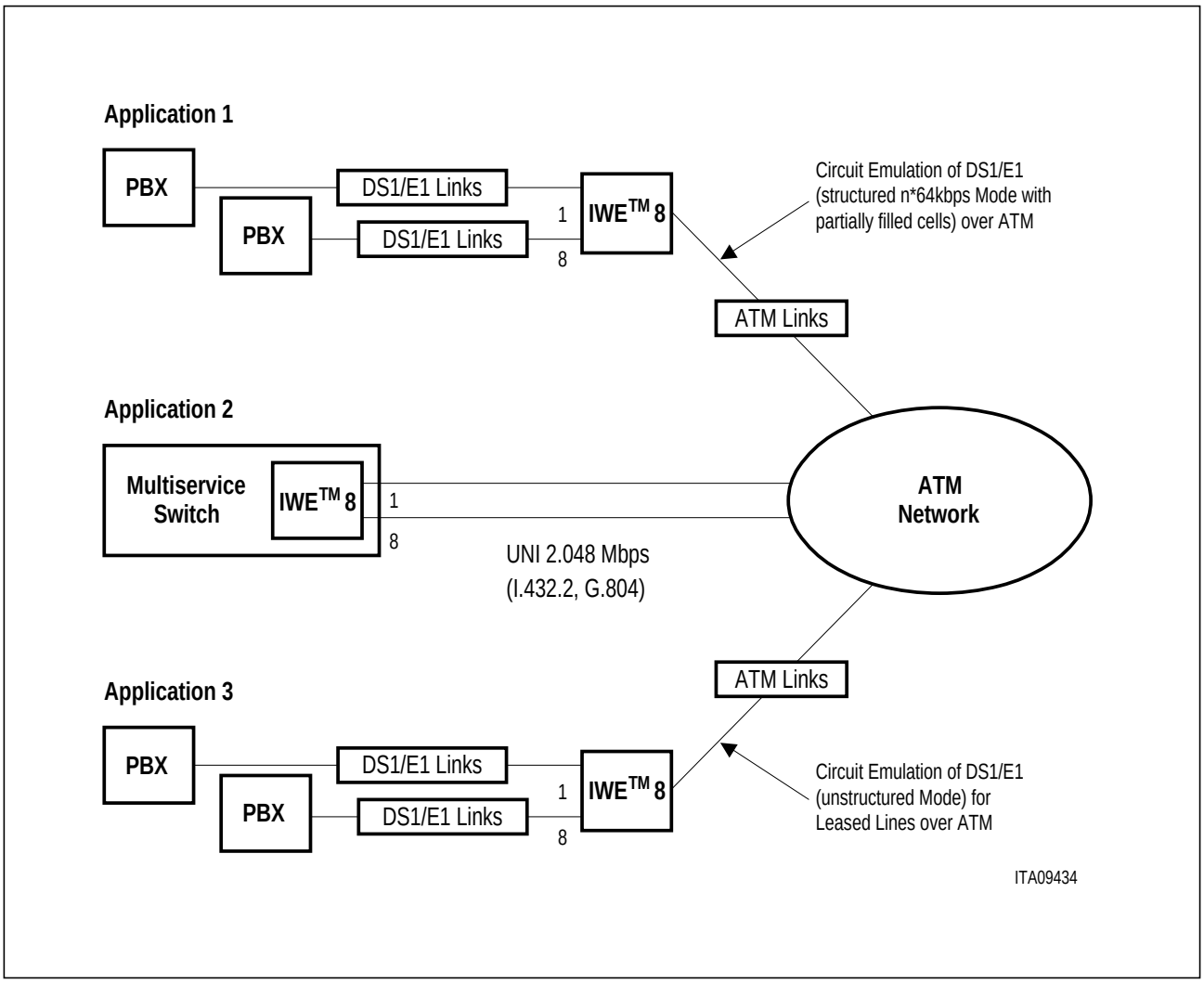

Figure 1
Typical IWE8 Applications

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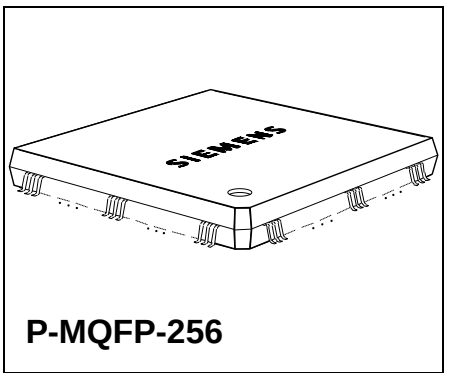
Interworking Element **PXB 4220**
IWE8

Version 1.1 **CMOS**

1.1 Features



P-MQFP-256

- Configurable to T1 or E1 mode via external pin
- 8 T1/E1 ports configurable independently to:
  - ATM mode
    - * G.804 mapping of ATM cells in T1/E1
    - * PHY layer functions of the UNI
  - AAL mode : unstructured CES
    unstructured T1/E1 Circuit Emulation Service
  - AAL mode : N x 64 kbit/s
    structured T1/E1 N x 64 kbit/s basic service:
    - * M channels of N x 64 kbit/s (M=1..24 N=1..24 for T1) (M=1..32 N=1..32 for E1)
- Partially filled cells with programmable filling thresholds
- AAL1 with or without Structured Data Transfer (SDT)
- Sequence Count Algorithm selectable between:
  - Standard: according to ETSI (prl-ETS 300353 annex D)
  - Fast: saves 6 ms during reassembly for 1x64-kbit/s connection
- AAL0 option: 48 bytes user payload per ATM cell, no AAL overhead
- Reassembly buffer can compensate up to 8-ms Cell Delay Variation (CDV)
- OAM counters per channel for lost/misinserted/errored cells etc.
- 8 direct interfaces to PEB 2254 Framer and Line Interface Component (FALC)
- Single port UTOPIA Level 1 industry standard interface
- External synchronous SRAM 2 x 64K x 18 bit required
- Interface provided for external clock recovery using Synchronous Residual Time Stamp (SRTS) or Adaptive Clock Method (ACM)
- 16-bit universal microprocessor interface for control and operation of the chip
- 256-pin Fine Pitch Quad Flat Pack package (0.4-mm pitch)

Type	Ordering Code	Package
PXB 4220	Q67101-H6590	P-MQFP-256

1.2 Logic Symbol

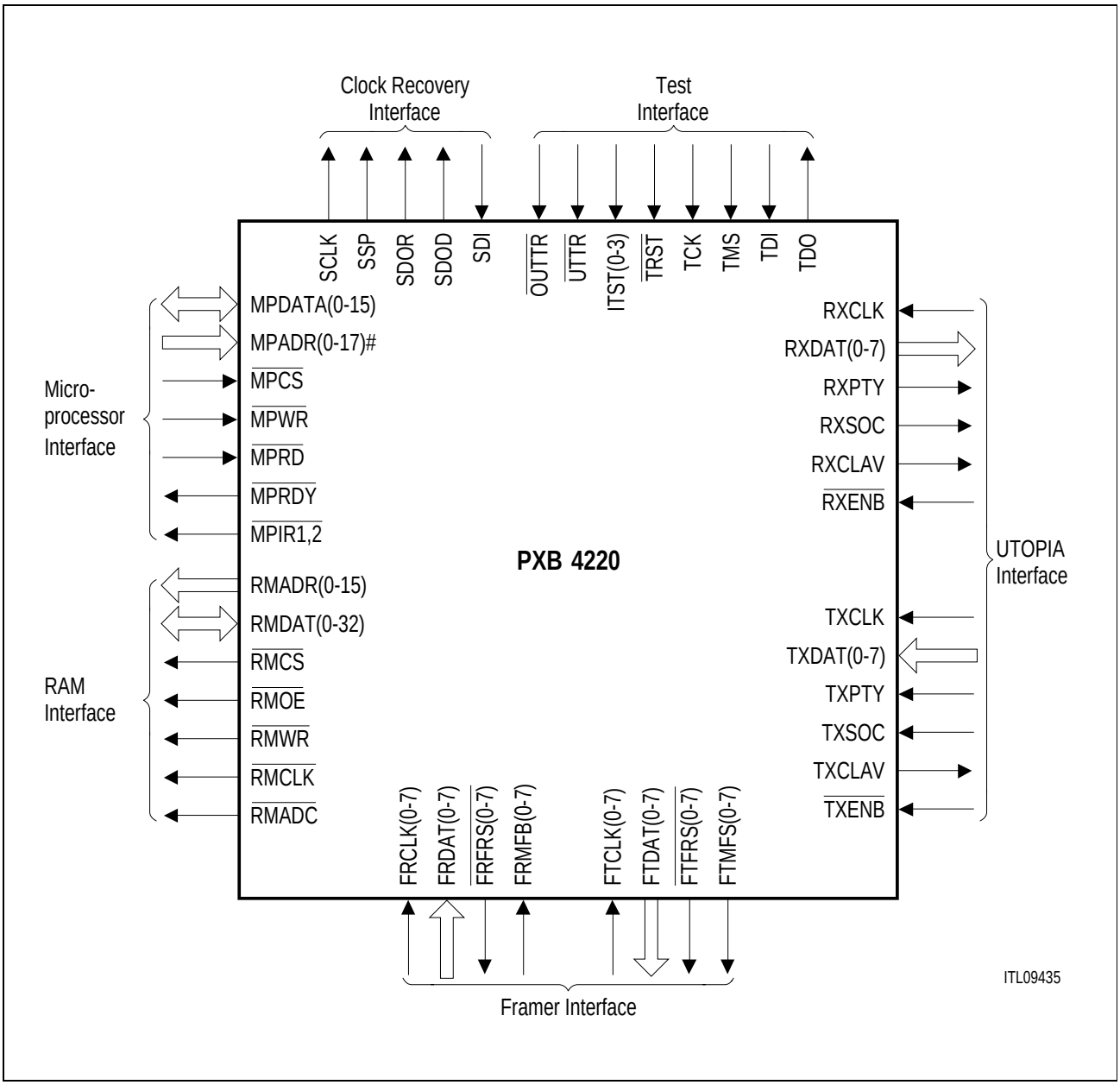


Figure 2
IWE8 Logic Symbol

1.3 Pin Configuration

(top view)

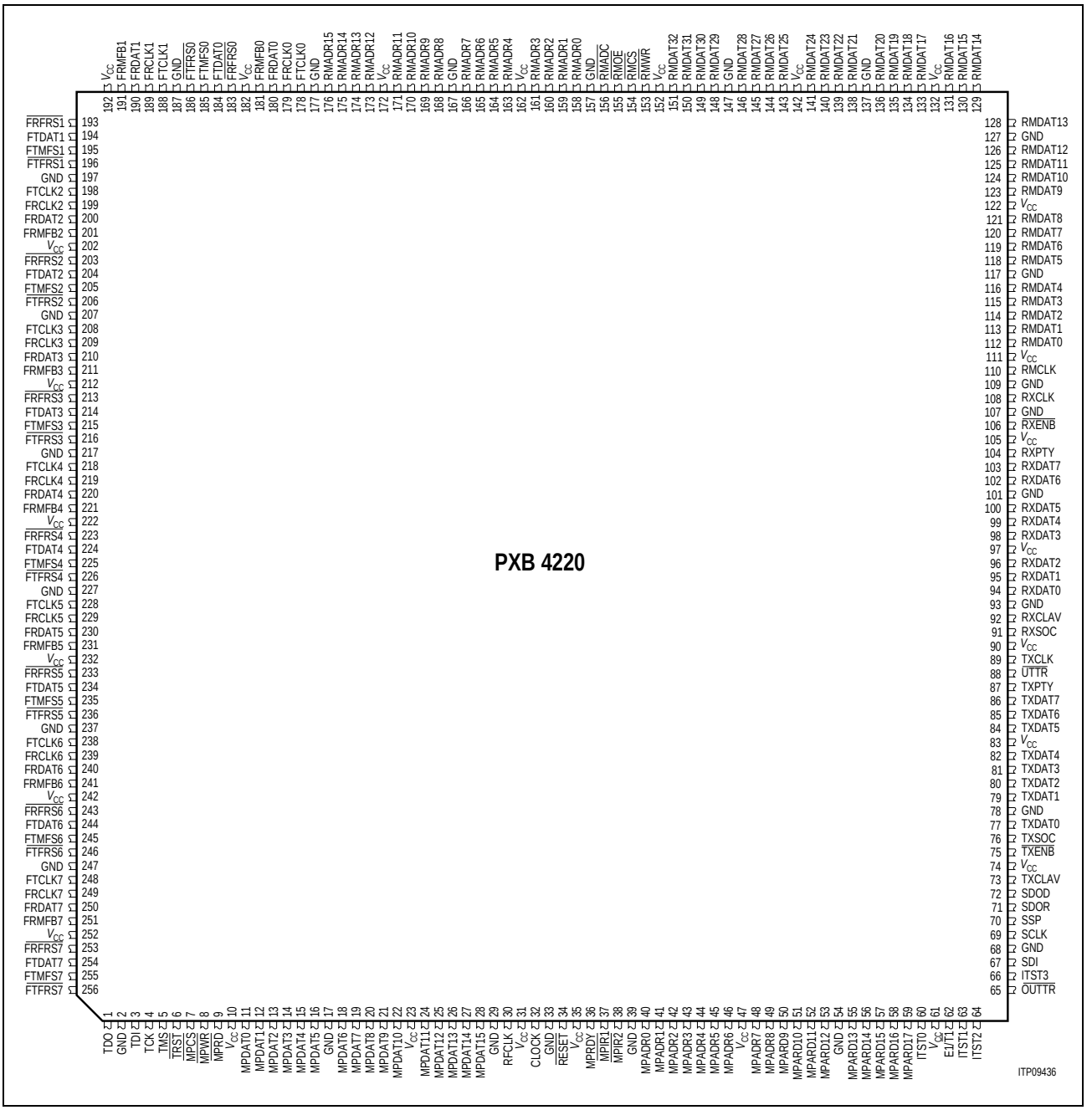


Figure 3
IWE8 Pin Configuration

1.4 Pin Definitions and Functions

Table 1 Framer Interface

Pin No.	Symbol	Input (I) Output (O)	Function
180, 190, 200, 210, 220, 230, 240, 250	FRDAT0–7	I	**Framer Receive Data Input**
184, 194, 204, 214, 224, 234, 244, 254	FTDAT0–7	O	**Framer Transmit Data Output**
183, 193, 203, 213, 223, 233, 243, 253	$\overline{\text{FRFRS0–7}}$	O	**Framer Receive Frame Synchronization Pulse**
186, 196, 206, 216, 226, 236, 246, 256	$\overline{\text{FTFRS0–7}}$	O	**Framer Transmit Frame Synchronization Pulse**
181, 191, 201, 211, 221, 231, 241, 251	FRMFB0-7	I	**Framer Receive Multiframe Begin**
185, 195, 205, 215, 225, 235, 245, 255	FTMFS0–7	O	**Framer Transmit Multiframe Synchronization**
179, 189, 199, 209, 219, 229, 239, 249	FRCLK0–7	I	**Framer Receive Clock**
178, 188, 198, 208, 218, 228, 238, 248	FTCLK0–7	I	**Framer Transmit Clock**

Table 2 Microprocessor Interface

Pin No.	Symbol	Input (I) Output (O)	Function
11–16	MPDAT0–5	I/O	**Microprocessor Data Bus**
18–22	MPDAT6–10		
24–28	MPDAT11–15		
40–46	MPADR0–6	I	**Microprocessor Address Bus**
48–53	MPADR7–12		
55–59	MPADR13–17		
7	$\overline{\text{MPCS}}$	I	**Microprocessor Chip Select**
8	$\overline{\text{MPWR}}$	I	**Microprocessor Write Enable**
9	$\overline{\text{MPRD}}$	I	**Microprocessor Read Enable**
36	MPRDY	O	**Microprocessor Ready**
37	$\overline{\text{MPIR1}}$	O	**Microprocessor Interrupt Request 1**
38	$\overline{\text{MPIR2}}$	O	**Microprocessor Interrupt Request 2**

Table 3 UTOPIA Receive Interface

Pin No.	Symbol	Input (I) Output (O)	Function
94–96	RXDAT0–2	O	**UTOPIA Receive Data Bus**
98–100	RXDAT3–5		
102–103	RXDAT6–7		
104	RXPTY	O	**UTOPIA Receive Odd Parity Bit**
91	RXSOC	O	**UTOPIA Receive Start-of-Cell**
92	RXCLAV	O	**UTOPIA Receive Cell Available**
108	RXCLK	I	**UTOPIA Receive Clock**
106	$\overline{\text{RXENB}}$	I	**UTOPIA Receive Enable**

Table 4 UTOPIA Transmit Interface

Pin No.	Symbol	Input (I) Output (O)	Function
77	TXDAT0	I	**UTOPIA Transmit Data Bus**
79–82	TXDAT1–4		
84–86	TXDAT5–7		
87	TXPTY	I	**UTOPIA Transmit Odd Parity Bit**
76	TXSOC	I	**UTOPIA Transmit Start-of-Cell**
73	TXCLAV	O	**UTOPIA Transmit Cell Available**
89	TXCLK	I	**UTOPIA Transmit Clock**
75	$\overline{\text{TXENB}}$	I	**UTOPIA Transmit Enable**

Table 5 Clock Recovery Interface

Pin No.	Symbol	Input (I) Output (O)	Function
67	SDI	I	**Serial Data Input**
72	SDOD	O	**Serial Data Output Data frames**
71	SDOR	O	**Serial Data Output Reset frames**
70	SSP	O	**Serial Synchronization Pulse**
69	SCLK	O	**Serial Clock**

Table 6 External RAM Interface

Pin No.	Symbol	Input (I) Output (O)	Function
112–116	RMDAT0–4	I/O	**RAM Data Bus** (RMDAT32 is parity bit)
118–121	RMDAT5–8		
123–126	RMDAT9–12		
128–131	RMDAT13–16		
133–136	RMDAT17–20		
138–141	RMDAT21–24		
143–146	RMDAT25–28		
148–151	RMDAT29–32		

Table 6 External RAM Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
158–161	RMADR0–3	O	**RAM Address Bus**
163–166	RMADR4–7		
168–171	RMADR8–11		
173–176	RMADR12–15		
154	$\overline{\text{RMCS}}$	O	**RAM Chip Select**
155	$\overline{\text{RMOE}}$	O	**RAM Output Enable**
153	$\overline{\text{RMWR}}$	O	**RAM Write Enable**
156	$\overline{\text{RMADC}}$	O	**RAM Address Control**
110	RMCLK	O	**RAM Clock**

Table 7 Test Interface

Pin No.	Symbol	Input (I) Output (O)	Function
1	TDO	O	**Boundary Scan Test Data Output**
3	TDI	I	**Boundary Scan Test Data Input**
4	TCK	I	**Boundary Scan Test Clock**
5	TMS	I	**Boundary Scan Test Mode Select**
6	$\overline{\text{TRST}}$	I	**Boundary Scan Test Reset**
60	$\overline{\text{ITST0}}$	I	**Internal Test Pins** $\overline{\text{ITST0}}$ must be high ITST1, ITST2 and ITST3 must be low for proper operation
63	ITST1		
64	ITST2		
66	ITST3		
88	$\overline{\text{UTTR}}$	I	**All Utopia Outputs in TRI-STATE**
65	$\overline{\text{OUTTR}}$	I	**All Outputs except TDO in TRI-STATE**

Table 8 Miscellaneous

Pin No.	Symbol	Input (I) Output (O)	Function
62	E1/$\overline{\text{T1}}$	I	**E1 or T1 Mode Select**
30	RFCLK	I	**Emergency Reference Clock**

Table 8 Miscellaneous (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
32	CLOCK	I	**Master Clock**
34	$\overline{\text{RESET}}$	I	**Master Hardware Reset**

Table 9 Supply Interface

Pin No.	Symbol	Input (I) Output (O)	Function
10, 23, 31, 35, 47, 61, 74, 83, 90, 97, 105, 111, 122, 132, 142, 152, 162, 172, 182, 192, 202, 212, 222, 232, 242, 252	V_{CC}		**3.3 V Power Supply Voltage**
2, 17, 29, 33, 39, 54, 68, 78, 93, 101, 107, 109, 117, 127, 137, 147, 157, 167, 177, 187, 197, 207, 217, 227, 237, 247	GND		**Ground**

1.5 Functional Block Diagram

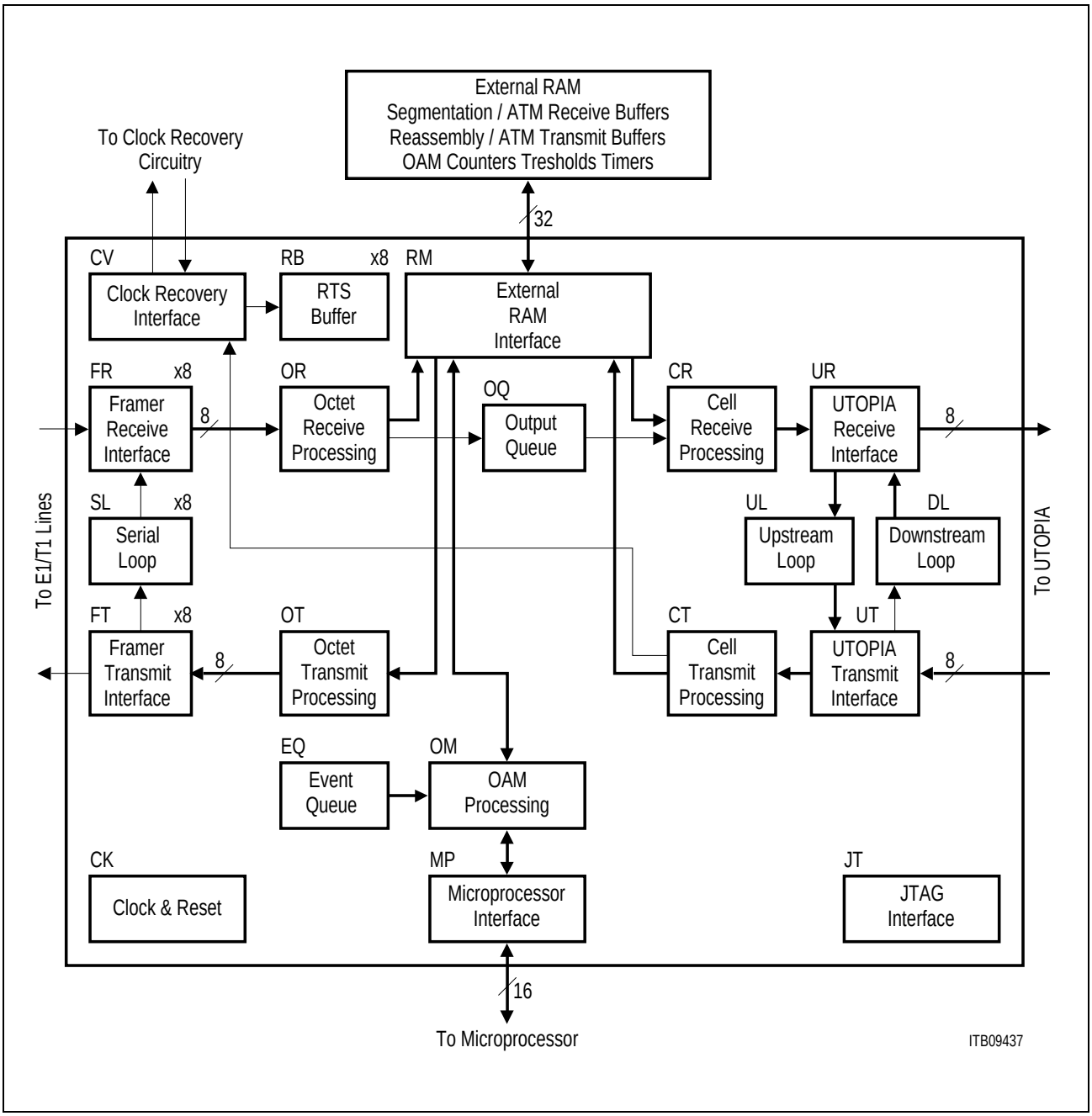


Figure 4
IWE8 Block Diagram

The functional block diagram of the IWE8 is shown in **Figure 4**. **Table 10** contains a function list for all blocks.

Table 10 Functions of IWE8 blocks

Block	Functions
FR	**Framer Receive interfaces** - FRCLK synchronization - 8 bit serial to parallel conversion - Frame and multiframe synchronization - Timeslot counter - Timeslot assignment and channel configuration (RAM1) AAL ports: - Decorrelation counter
OR	**Octet Receive processing** ATM ports: - Cell delineation - HEC check: header error detection and correction - Cell payload descrambling - OAM counter event generation - Write control of ATM receive buffer AAL ports: - Segmentation - SN/SNP generation - SDT pointer generation - SRTS value insertion - OAM counter event generation - Write control of segmentation buffer
OQ	**Output Queue** FIFO containing 256 addresses of cells to be sent to UTOPIA Receive
CR	**Cell Receive processing** - Reading cells from segmentation/ATM receive buffer in external RAM
UR	**UTOPIA Receive interface** - Cell level handshaking - Output buffer for 2 cells - Padding of partially filled cells
UL	**Upstream Loop** - Cell loopback from Cell Receive to Cell Transmit processing - Loopback buffer for 2 cells
DL	**Downstream Loop** - Cell loopback from UTOPIA Transmit to UTOPIA Receive - Loopback buffer for 2 cells

Table 10 Functions of IWE8 blocks (cont'd)

Block	Functions
UT	**UTOPIA Transmit interface** - Cell level handshaking - Input buffer for 2 cells
CT	**Cell Transmit processing** - Port and channel identification ATM ports: - Write control of ATM transmit buffer AAL ports: - SNP error detection and correction - SN algorithm: standard or fast - Bit count integrity (dummy cell insertion) - SDT pointer handling - SRTS value extraction - Extracting reassembly buffer filling for ACM - OAM counter event generation - Write control of reassembly buffer
OT	**Octet Transmit processing** ATM ports: - Reading cells from ATM transmit buffer - Cell rate decoupling: idle cell insertion - HEC generation - Cell payload scrambling AAL ports: - Reading octets from reassembly buffer - Reassembly buffer underflow and overflow handling - Reassembly buffer initialization to compensate CDV - Synchronization of SDT structure with single frame or multiframe - OAM counter event generation
FT	**Framer Transmit interfaces** - FTCLK synchronization - 8 bit parallel to serial conversion - Generation of frame and multiframe synchronization - Timeslot counter - Timeslot assignment and channel configuration (RAM2, RAM3)
SL	**Serial Loop** - Serial loopback from Framer Transmit to Framer Receive

Table 10 Functions of IWE8 blocks (cont'd)

Block	Functions
OM	**OAM processing** - Processing of OAM counter events - Interrupt queue control - Microprocessor access control to external RAM
EQ	**Event Queue** - FIFO of 256 OAM counter events
MP	**Microprocessor interface** - Synchronization of asynchronous microprocessor interface signals - Internal registers - Interrupt generation
RM	**External RAM interface** - Generation of external RAM interface signals - Generation of basic RAM cycle - Access control to external RAM for different blocks - Parity generation and checking
CV	**Clock Recovery interface** - Generation of serial communication frames to external clock recovery circuit, containing SRTS values and or ACM buffer filling - Generation of synchronization for SRTS generation by external clock recovery circuit. - Reception of frames with SRTS values from external clock recovery circuit
RB	**RTS Buffer** - Buffer for 2 incoming RTS values per port
CK	**Clock & Reset** - Clock distribution and reset control
JT	**JTAG interface** - Boundary Scan register and TAP controller

1.6 System Integration

The PXB 4220 IWE8 chip is designed to handle up to eight T1/E1 ports. It transfers data between the Pulse Code Modulation (PCM)-highway and an UTOPIA ATM Interface.

Figure 5 shows an example Line Interface Card (LIC) utilizing the IWE8 in a switch environment. Eight Siemens PEB 2254 Framer and Line Interface Component (FALC) chips are connected at the PCM ports. An ATM Layer circuit is connected at the UTOPIA Interface port and could be implemented using Siemens' PXB 43201/2 ATM Switching Preprocessor (ASP) upstream/downstream chip set.

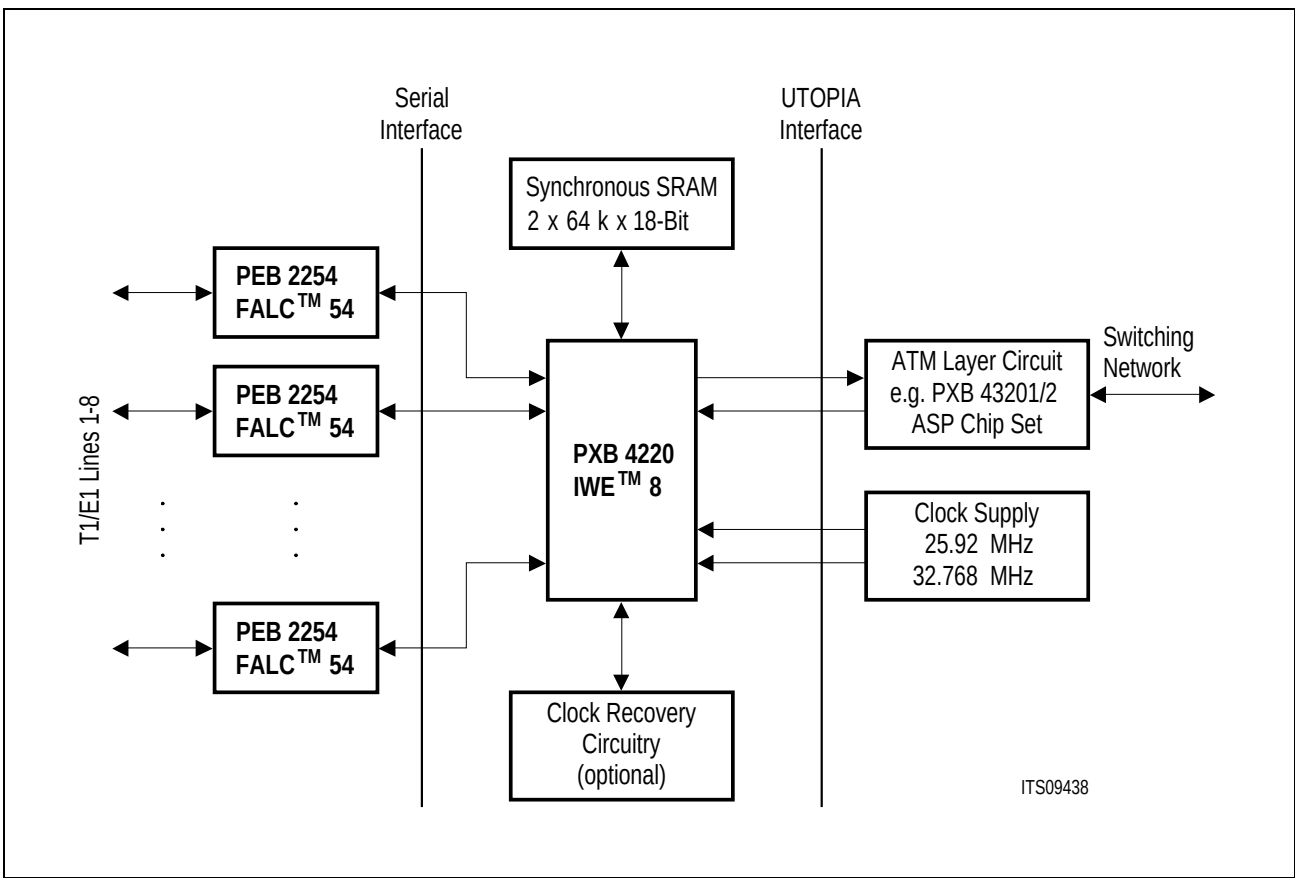


Figure 5
Line Card for 8 T1/E1 Channels

Figure 6 shows the IWE8 chip on a PC Adapter Card or Network Interface Card (NIC). In this single-port example, only one FALC chip is required and is connected to the IWE8 at one of its PCM ports. As the segmentation and reassembly function is done in the PXB 4110 SARE device, the IWE8 port is used in ATM mode for the PHY layer functions.

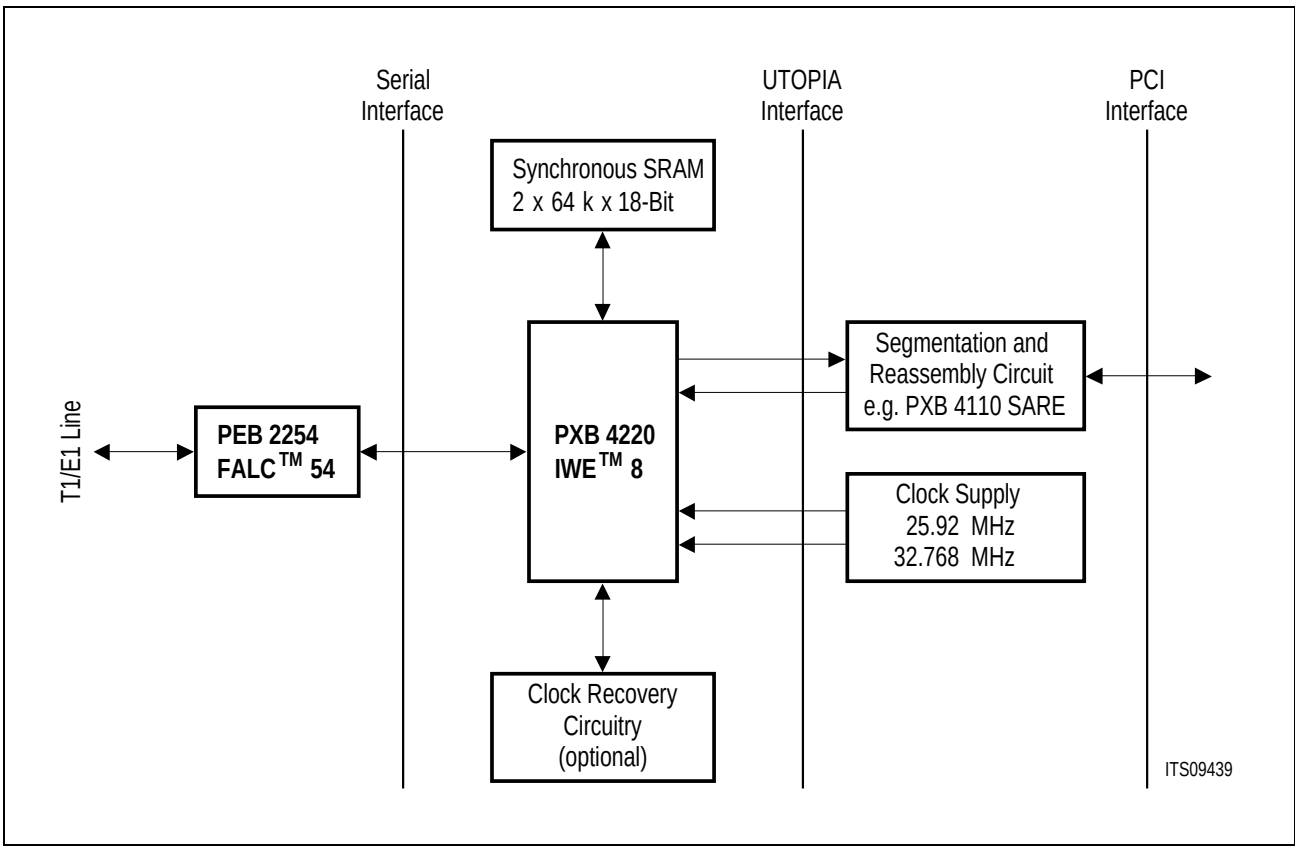


Figure 6
T1/E1 Network Interface Card (PC Adapter Card)

External synchronous SRAM is always required for proper IWE8 operation. The external Clock Recovery circuitry is optional for implementation of SRTS, ACM, or a combination of the two methods. The IWE8 requires only one main operating clock of +/- 25 MHz. An emergency clock of 32.768 Mhz is optional. The Framer and Utopia interface clocks can be completely asynchronous with respect to the main clock. A microprocessor controls and operates the IWE8 via a generic 16-bit interface.

2 Interfaces

The exact timing diagrams of the different interfaces can be found in the AC timing characteristics of **chapter 5**.

2.1 Framer Interface

The IWE8 can be directly connected to eight Siemens PEB 2254 “Framer and Line interface” components FALC 54 as shown in **figure 7**.

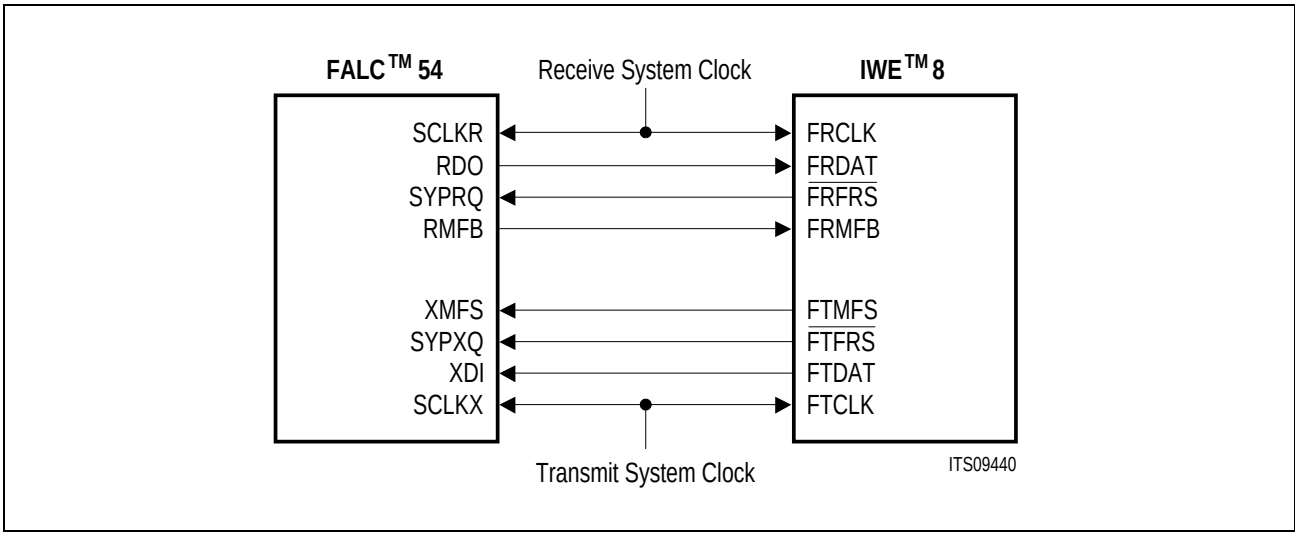


Figure 7
Connection of IWE8 to FALC54

The data is transferred between the FALC 54 and the IWE8 via a system internal highway.

The receive system clock and transmit system clock are both 8.192 MHz, and may be independent from each other. The data is transferred in 2048 kbit/s mode. This means that each bit lasts 4 clock periods.

The data on the system internal highway is structured in frames of 256 bits every 125 µs. The data is transmitted in 32 slots numbered from 0 to 31 with slot 0 transmitted first. The data bits in a slot are numbered from 1 to 8. The first transmitted bit ‘bit 1’ is the most significant bit. Figure 8 shows the bit ordering.

The beginning of slot 0 in a frame is defined by a synchronization pulse. The IWE8 generates the $\overline{\text{FRFRS}}$ and $\overline{\text{FTFRS}}$ synchronization pulses every 125 µs. The pulses are 2 clock periods wide.

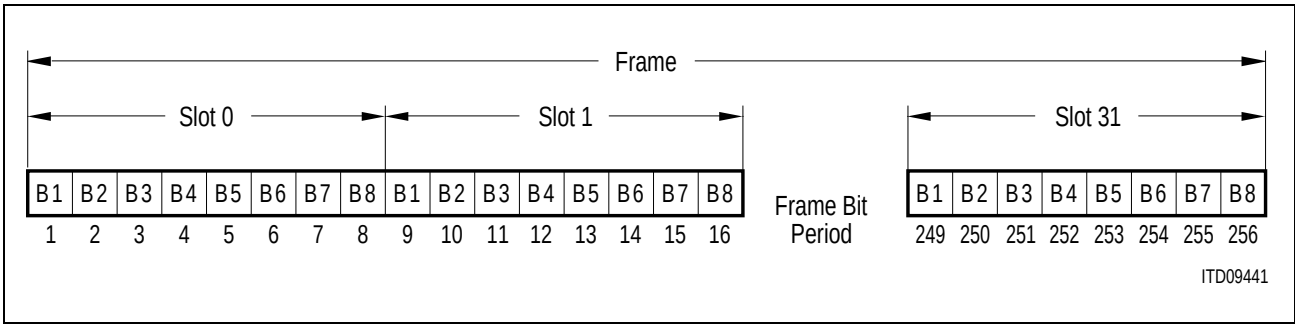


Figure 8
Bit ordering on the system highway between FALC 54 and IWE8

T1 Translation mode

In T1 mode there is one FS/DL slot and 24 timeslots numbered from 1 to 24. The mapping into the 32 slots of a frame using translation mode 0 (See FALC54 datasheet) is shown in **table 11**.

Table 11 Translation mode 0 for T1 timeslot mapping.

Frame slot	T1 timeslot	Frame slot	T1 timeslot
0	FS/DL slot	16	
1	timeslot 1	17	timeslot 13
2	timeslot 2	18	timeslot 14
3	timeslot 3	19	timeslot 15
4		20	
5	timeslot 4	21	timeslot 16
6	timeslot 5	22	timeslot 17
7	timeslot 6	23	timeslot 18
8		24	
9	timeslot 7	25	timeslot 19
10	timeslot 8	26	timeslot 20
11	timeslot 9	27	timeslot 21
12		28	
13	timeslot 10	29	timeslot 22
14	timeslot 11	30	timeslot 23
15	timeslot 12	31	timeslot 24

The FS/DL slot only contains the FS/DL signaling bit. The format of the FS/DL slot is shown in **figure 9**.

MSB			**FS/DL slot**				**LSB**
bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	bit 8
							FS/DL

Figure 9 FS/DL slot format in T1 mode

E1 Translation mode

In E1 mode there are 32 timeslots numbered from 0 to 31. The timeslots directly correspond to the 32 frame slots.

2.2 Microprocessor Interface

The connection of the 16 bit Intel compatible asynchronous microprocessor interface to an Intel 386EX processor is shown in **figure 10**. Address bit 1 of the microprocessor (ADR1) must be connected with address bit 0 of the IWE8 (MPADR0).

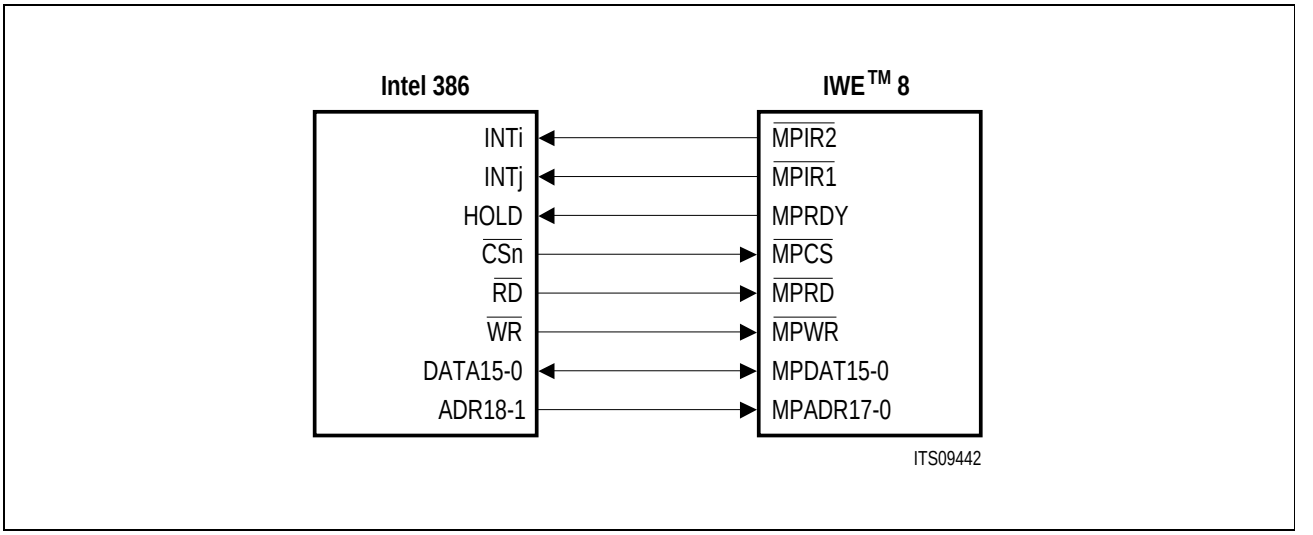


Figure 10
Connection of IWE8 to microprocessor

The IWE8 contains 32 internal registers. Accesses to the 32 internal registers are 16 bit oriented.

The IWE8 contains 3 internal RAMs of 256 x 32 bits and an external RAM of 64k x 32 bits that can be read and written by the microprocessor. Accesses to the 3 internal RAMs or to the external RAM are 32 bit oriented.

Table 12 shows the address locations of the internal registers, the 3 internal RAMs and the external RAM in the IWE8.

Table 12 IWE8 addresses

MPADR17 - 0	Access	Type
11 1111 11 76 5432 1098 7654 3210		
00 0000 0000 000x xxxx	Internal Registers	16 bit
00 0000 001x xxxx xxxx	Internal RAM1	32 bit
00 0000 010x xxxx xxxx	Internal RAM2	32 bit
00 0000 011x xxxx xxxx	Internal RAM3	32 bit
1x xxxx xxxx xxxx xxxx	External RAM	32 bit

The 32 bit oriented accesses must be done by two consecutive 16 bit accesses, the first with MPADR0 = 0 and the second with MPADR0 = 1. The IWE8 will not verify whether the address bits MPADR1-17 during the second access are the same as during the first access.

The data of the first of two consecutive write cycles (MPADR0 = 0) is written temporarily into an internal write-cache register. Actual writing the 32 bits into internal or external RAM is done during the second of the two consecutive writes (MPADR0 = 1).

During the first of two consecutive read cycles (MPADR0 = 0), the 32 bit data are actually read from internal or external RAM. Bits 15-0 are transferred to the databus MPDAT. Bits 31-16 are written into an internal read-cache register. During the second read (MPADR0 = 1), the read-cache register is transferred to the databus. When only bits 15-0 are needed, the second read cycle can be omitted.

Cycle length control

The length of the read or write cycles is always controlled by the MPRDY signal. The MPRDY goes low at the start of each cycle and becomes high when the cycle is complete.

Interrupt handling

The IWE8 provides two independent interrupt pins $\overline{\text{MPIR1}}$ and $\overline{\text{MPIR2}}$.

$\overline{\text{MPIR1}}$ is the main interrupt pin which goes active low when a special event occurs in the IWE8.

The interrupt handling software should read the interrupt status register 1 (isr1) to identify the causes of the interrupt (see Register Description).

When some of the bits eis1 to eis4 in isr1 are set, the corresponding extended interrupt status register (eis1-4) should also be read to identify the interrupt causes.

When bit 15 (iq_ne: interrupt queue not empty) in isr1 is set, there are also events in the interrupt queue in external RAM. The interrupt queue is organized as a FIFO queue. The microprocessor can always read at the same address and the IWE8 will automatically provide the next event. Bit 15 of each entry is the same as bit 15 of the isr1 register and directly indicates whether the queue is empty and no further reading is necessary.

Each of the 16 interrupt sources of isr1 can be individually masked in the interrupt mask register imr1. If the interrupt source is masked, the interrupt pin $\overline{\text{MPIR1}}$ will not go active low when the corresponding event occurs.

$\overline{\text{MPIR2}}$ is an auxiliary interrupt pin. The IWE8 provides two sets of 8 independent timers in external RAM (timer set 1 and 2). Timer set 2 can be used independently from the rest of the IWE8 driver software. When one of the timers of timer set 2 expires, a bit will be set in the isr2 register and $\overline{\text{MPIR2}}$ goes active low.

2.3 External RAM Interface

The IWE8 needs to be connected to an external synchronous SRAM of 64k x 33 bits. A possible connection with 2 external SRAM 64k x 18 components is shown in **figure 11**.

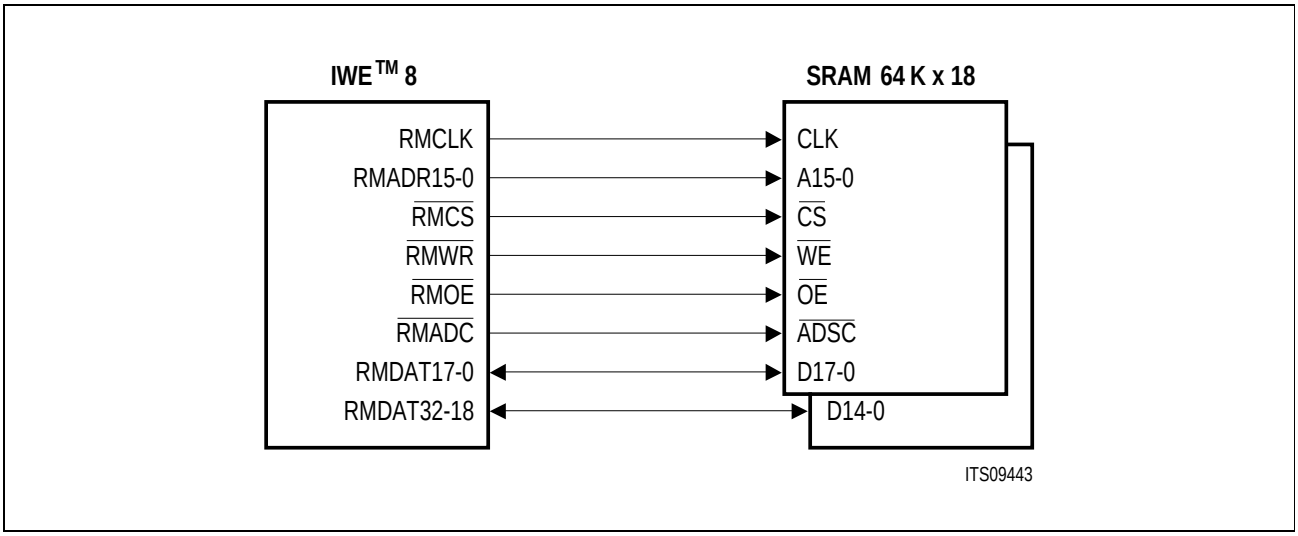


Figure 11.
External RAM connection

The RMCLK output is the buffered CLOCK input.

The RMADC and RMOE output signals define a basic RAM cycle of 12 clock periods that is continuously repeated. The basic RAM cycle consists of 6 consecutive read cycles, a dummy address cycle and 5 consecutive write cycles. Whether the IWE8 actually reads data from the external RAM or writes data into the external RAM is controlled by the RMCS and RMWR signals.

2.4 UTOPIA Interface

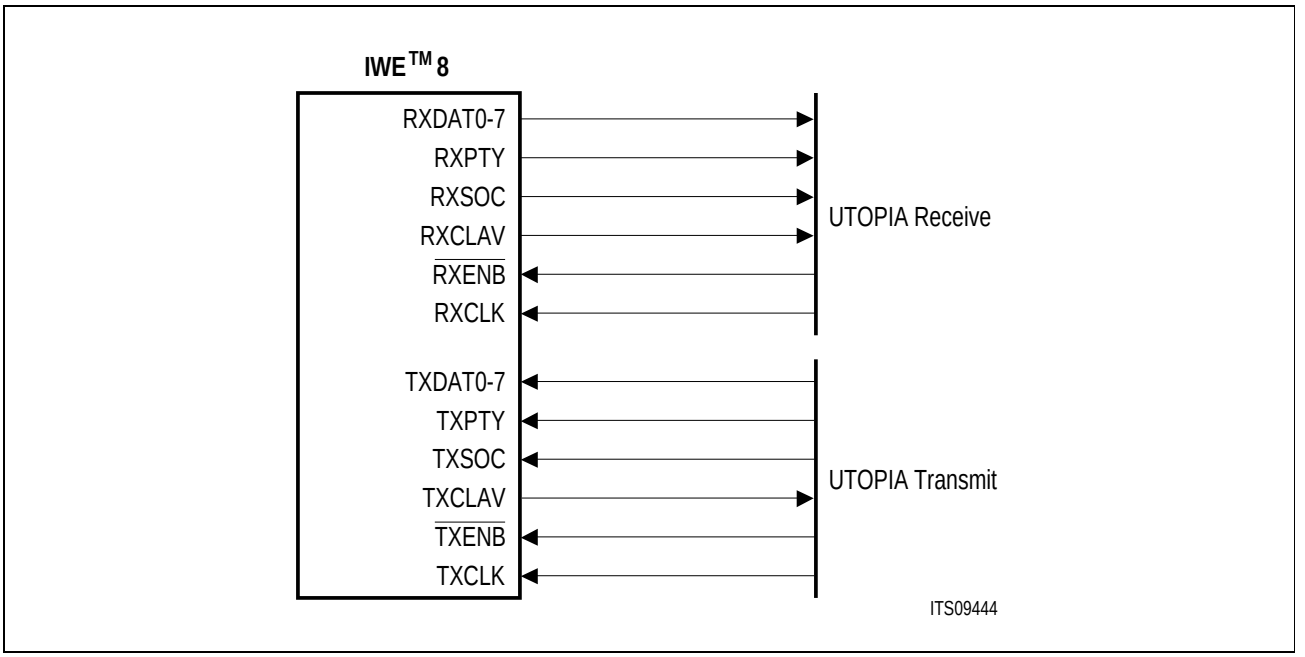


Figure 12
UTOPIA receive and transmit interfaces.

The UTOPIA receive and transmit interfaces are implemented according to the ATM forum specification level 1 described in [24].

Table 13 Header Octets of an ATM Cell

Header Octet	MSBs (7:4)	LSBs (3:0)
1	GFC	VPI
2	VPI	VCI
3	VCI	
4	VCI	PTI(3:1), CLP
5	UDF = 0000 0PPP	

PPP = Port Number

The User Defined Field (UDF) is used to transmit the source or destination port number of the ATM cell as shown in **table 13**.

In AAL mode, the channel number should be transmitted on the UTOPIA transmit interface in the 5 LSB bits of the VCI field VCI(4:0).

2.5 Clock Recovery Interface

The Clock Recovery Interface is a 4 line serial interface: 1 data input SDI, 2 data outputs SDOD and SDOR and 1 synchronization output SSP. The interface allows connection to external clock recovery circuits. Two methods for clock recovery are supported: Synchronous Residual Time Stamp (SRTS) and Adaptive Clock Method (ACM).

The data sent over the serial lines is always formatted in frames of 32 bits. The SSP pulse indicates the frame start for both directions. Table 14 shows the interface frame format. Bit 31 is sent first. When no data is to be sent, idle frames are transmitted consisting of bits 31-1 all 1 and parity bit 0 = 0. Table 14 also indicates which data fields are used on the different interface signals.

Table 14 Clock Recovery Interface frame format

Bits	Data field	SDI	SDOD	SDOR
31- 29	111			
28 - 25	RTS(3:0)	Yes	Yes	No
24 - 11	buffer_fill(13:0)	No	Yes	No
10	SRTS_valid	No	Yes	No
9 - 8	00			
7 - 5	port_nr(2:0)	Yes	Yes	Yes
4 - 2	type(2:0) 001 : RTS only 010 : buffer_fill only 011 : RTS + buffer_fill 111 : reset SRTS logic others : not used	 No No No No	 Yes Yes Yes No	 No No No Yes
1	frame_invalid	Yes	Yes	Yes
0	odd_parity	Yes	Yes	Yes

SCLK :

The SCLK output is the buffered CLOCK input.

SDI :

The SDI signal is used to input RTS values to the IWE8. The frames with RTS values should come in time intervals equivalent to the payload of 8 ATM cells (e.g. for completely filled cells without SDT every 3008 clock periods). Each valid frame is supposed to contain a valid RTS value on the SDI input.

SDOR :

To allow the external SRTS generation logic to synchronize with the cell segmentation process, the IWE8 will output on the SDOR signal a frame with type = 111 when the segmentation of the first ATM cell for a selected channel starts. The first two sequences of 8 ATM cells will contain a dummy RTS value (programmable in ASIC configuration register ‘acfg’). From the third sequence on the values received on the SDI input will be used.

The IWE8 has internal ‘RTS Buffers’ for 2 RTS values per port.
When one of the ‘RTS Buffers’ overflows, the value in excess will be omitted and a bit in the extended interrupt status register 2 ‘eis2’ will be set.
When ‘RTS Buffer’ underflow occurs, the last received RTS value will be repeated in the next sequence of 8 ATM cells.

SDOD :

The SDOD signal is used by the IWE8 to output RTS values or buffer filling levels or both.

The RTS value extracted from a cycle of 8 ATM cells with sequence count 0 to 7, is transmitted when the cell with sequence count 0 from the next cycle is received. The ‘RTS_valid’ field is used to indicate whether the extracted RTS value is correct or not. The condition to accept the extracted RTS as valid is that in the previous cycle of 8 cells the cells with SN = 1, 3, 5 and 7 were present and were accepted as valid cells.

The buffer filling level is transmitted for use with the Adaptive Clock Method (ACM) and is expressed as a number of octets contained in the ‘Reassembly Buffer’. The buffer filling level is transmitted every time when a new ATM cell for the selected channel is received.

The IWE8 supports a combination of SRTS and ACM. The ‘type’ field indicates whether a frame on the SDOD signal contains RTS values only, buffer filling levels only or both.

2.6 Miscellaneous interface signals

E1/$\overline{\text{T1}}$:

The E1/$\overline{\text{T1}}$ mode pin selects between E1 mode (E1/$\overline{\text{T1}}$ = 1) and T1 mode (E1/$\overline{\text{T1}}$ = 0) for the framer interfaces.

RFCLK :

The emergency reference clock input RFCLK is used when the framer receive clock FRCLK fails. The segmentation continues using the RFCLK divided by four, and using a programmable byte-pattern for the cell payload. In the ASIC configuration register 'acfg' it is possible to select the pattern to be used out of four programmable byte-patterns BP3, BP2, BP1 or BP0.

The RFCLK frequency must be 4 x 8,192 Mhz = 32,768 Mhz.

CLOCK :

The Master clock is the main clock for all flip-flops in the IWE8, except for some flip-flops in the framer interfaces and in the UTOPIA interface blocks. The basic processing time of an octet in the IWE8 is 12 clock cycles. As the time needed to process one octet for each of the 8 ports must be less than the time required to transfer one octet over a framer interface (8 x 4 bit periods), this leads to the condition : $12 \times 8 \times T_{CLOCK} < 8 \times 4 \times T_{FRCLK}$. Hence, the CLOCK frequency must be at least 3 x 8.192 Mhz = 24,576 Mhz.

$\overline{\text{RESET}}$:

The $\overline{\text{RESET}}$ pin asynchronously resets all flip-flops in the IWE8.

$\overline{\text{UTTR}}$:

The $\overline{\text{UTTR}}$ pin can be used to put all UTOPIA outputs in TRI-STATE. This allows easy connection of UTOPIA test equipment on the UTOPIA interface.

$\overline{\text{OUTTR}}$:

The $\overline{\text{OUTTR}}$ pin can be used to put all outputs except TDO in TRI-STATE. This feature can be used during physical board test.

2.7 Boundary Scan Interface

The boundary scan interface implements the Test Access Port (TAP) as defined in IEEE Standard 1149.1-1990 [25] including the optional $\overline{\text{TRST}}$ reset signal.

The device identification register, the instruction register and boundary-scan register are described in the electrical characteristics.

3 Functional description

3.1 ATM mode

A port N is operating in ATM mode if bit ‘p_atm’ of the port configuration register ‘pcfN’ is set to 1.

3.1.1 ATM cell mapping.

The IWE8 supports any mapping scheme of ATM cells into N of the 32 slots of the framer interfaces.

The mapping scheme is defined by programming 32 slot positions in the internal RAM’s. RAM1 is used for receive port configuration and RAM2 for transmit port configuration (See Register Description).

The first slot used should be programmed as the ‘ATM Reference Slot’.
The following slots used should be programmed as ‘ATM Continuation Slots’.
The unused slots should be programmed as ‘Idle Slots’.

In particular the mapping of ATM cells in T1/E1 frames according to ITU-T G.804 [14] can be used by programming RAM1 and RAM2 as shown in **table 15**.

Table 15 ATM cell mapping according to ITU-T G.804

E1 slot number	Slot type
0, 16	Idle
1	ATM Reference
2-15, 17-31	ATM Continuation

T1 slot number	Slot type
0, 4, 8, 12, 16, 20, 24, 28	Idle
1	ATM Reference
2-3, 5-7, 9-11, 13-15, 17-19, 21-23, 25-27, 29-31	ATM Continuation

3.1.2 ATM receive functions

The ATM receive functions are controlled by the internal registers ‘catm’, ‘atmc’ and ‘rxid’. The features controlled by these registers are common to all ATM ports.

Some features of the ATM receive functions can be controlled per port, by programming the port specific ‘ATM Receive Reference Slot’ in the internal configuration RAM1.

3.1.2.1 Cell delineation

The cell delineation algorithm is implemented according to the ITU-T I.432 B-ISDN UNI PHY layer specifications [21].

To support ‘Out of Cell Delineation’ (OCD) anomalies and ‘Loss of Cell Delineation’ (LCD) defect, the IWE8 generates an interrupt (see extended interrupt status register ‘eis4’) whenever the SYNC state is left (OCD_start) or entered (OCD_end).
The generation of interrupts is per port controllable through the ‘ocd_start_intrpt’ and ‘ocd_end_intrpt’ fields in the ‘ATM Receive Reference Slot’ of RAM1.

The software can then start a timer (e.g. timer_set_1 provided by the IWE8) to establish the LCD defect state.

When the cell delineation is not in the SYNC state, received cells are discarded.

As octet boundaries are available within the receive physical layer prior to cell delineation, the cell delineation process is performed octet by octet in the HUNT state.

The ALPHA and DELTA parameters, which influence the robustness of the algorithm against false misalignment and false delineation, are programmable between 0 and 15, in the ATM control register ‘atmc’ (common for all ATM ports).

To force resynchronization of the cell delineation process, the microprocessor can force individual ports to enter the HUNT state, by setting the ‘go_hunt’ bit in the corresponding ‘ATM Receive Reference Slot’ of RAM1.

With the ‘channel_mode’ set to ‘Standby’ it is possible to test the cell delineation, without passing any cells to the ATM layer.

3.1.2.2 Payload descrambling

The descrambler function is implemented according to the B-ISDN UNI PHY layer specifications [21].

This function can be enabled or disabled per port by programming the ‘x43_descrambling’ field in the ‘ATM Receive Reference Slot’ of RAM1.

3.1.2.3 HEC detection and correction

The Header Error Control (HEC) is implemented according to the B-ISDN UNI PHY layer specifications [21].

According to the HEC algorithm, cells are discarded when a multi-bit header error is detected in the Correction mode or a header error is detected in the Detection mode.

According to the HEC algorithm, cells are corrected when a single-bit error is detected in the Correction mode.

3.1.2.4 Idle, physical layer or unassigned cell deletion

In E1 mode, it is possible to delete idle cells only or to delete all physical layer cells as defined in the B-ISDN protocol reference model [17].

In T1 mode, unassigned cells can be deleted. Invalid cells are passed to the ATM Layer as defined in the B-ISDN UNI and NNI PHY layer generic criteria [7].

Figure 13 and **8** show the headers of special cells in E1 and T1 mode.

Cell Type	Header octet 1	Header octet 2	Header octet 3	Header octet 4
idle	0000/0000	0000/0000	0000/0000	0000/0001
physical layer	XXXX/0000	0000/0000	0000/0000	0000/XXX1

X: Don’t care

Figure 13 Header format of special cell types in E1 mode

Cell Type	Header octet 1	Header octet 2	Header octet 3	Header octet 4
invalid	XXXX/0000	0000/0000	0000/0000	0000/XXX1
unassigned	XXXX/0000	0000/0000	0000/0000	0000/XXX0

X: Don’t care

Figure 14 Header format of special cell types in T1 mode

The 4 MSBs of header octet 1 and the 4 LSBs of header octet 4 of the received cells that must be deleted are programmable in the ‘prg_rx_hd’ field of the RX idle/unassigned cell control register ‘rxid’. All other header bits must be 0 for the cell to be deleted.

The ‘msk_rx_hd’ field of the same ‘rxid’ register allows to mask all or some of the bits specified in ‘prg_rx_hd’. The masked bits are considered as ‘don’t care’ for the cell to be deleted.

In E1 mode, the ‘prg_rx_hd’ field should be set to 0000 0001.
If only idle cells should be deleted, the ‘msk_rx_hd’ should be set to 0000 0000.
If all physical layer cells should be deleted, the ‘msk_rx_hd’ should be set to 1111 1110.

In T1 mode, the ‘prg_rx_hd’ field should be set to 0000 0000.
The ‘msk_rx_hd’ should be set to 1111 1110. This configuration will delete all unassigned cells.

The deletion of idle, physical layer or unassigned cells can be enabled or disabled per port by the ‘delete_idle_cells’ field in the ‘ATM Receive Reference Slot’ of RAM1.

3.1.2.5 ATM receive buffer.

Each port has an ATM receive buffer with a maximum size of 16 cells per port.
The ATM receive buffers are implemented in external RAM. Each ATM cell occupies one memory block of 64 octets, or 16 double-words of 32 bits.

3.1.2.6 Common Output Queue.

When a cell is completely stored in one of the ATM receive buffers, it is ready to be transmitted to the ATM layer over the UTOPIA receive interface. The external RAM address of the cell is stored in a common Output Queue (OQ).

The output queue is a First In First Out (FIFO) queue with a maximum of 256 cell address entries. The output queue is common to all ports, both ATM or AAL mode ports.

As long as the output queue is not empty, the Cell Receive processing (CR) will read the next cell in the output queue from external RAM, and the UTOPIA Receive interface (UR) will transmit the cell on the UTOPIA bus.

3.1.2.7 Activation of ATM receive ports

When activating ATM receive ports, it is important to follow the initialization sequence as shown in table 19. Step 2 with the ‘p_rx_act’ bit of the ‘pcfN’ register set to 1 and the ‘channel_mode’ in the ‘ATM Receive Reference Slot’ in RAM1 set to ‘Inactive’ must be held at least 250 µs. This condition is necessary to internally reset the ATM receive port.

Table 16 Activation sequence for ATM receive ports

Step	p_rx_act	channel_mode	Minimum Time
1	0 = inactive	00 = Inactive	
2	1 = active	00 = Inactive	250 µs
3	1 = active	01 or 11 = Active	

Each ATM receive port can be configured in the ‘channel_mode’ field of the ‘ATM Receive Reference Slot’ in RAM1 to operate in ‘Inactive’, ‘Active’ or ‘Standby’ mode.

In ‘Inactive’ mode, no data is accepted from the framer receive interface.

In ‘Active’ mode, data is accepted from the framer receive interface, cells are written into the ATM receive buffer and cell addresses are written into the output queue.

In ‘Standby’ mode, data is accepted from the framer receive interface but no cells are written into the ATM receive buffer or the output queue. This mode can be used to test the cell delineation.

3.1.3 ATM transmit functions

The ATM transmit functions are controlled by the internal registers ‘catm’, ‘atmc’ and ‘txid’. The features controlled by these registers are common to all ATM ports.

Some features of the ATM transmit functions can be controlled per port, by programming the port specific ‘ATM Transmit Reference Slot’ in the internal configuration RAM2.

3.1.3.1 ATM transmit buffer

Each port has an ATM transmit buffer with a maximum size of 256 cells per port.

The ATM transmit buffers are implemented in external RAM. Each ATM cell occupies one memory block of 64 octets, or 16 double-words of 32 bits.

3.1.3.2 Idle/unassigned cell generation

When the ATM transmit buffer of a port is empty, idle or unassigned cells are transmitted to provide cell rate decoupling.

On E1 ports, idle cells are transmitted as defined in the ITU-T B-ISDN Protocol reference model [17].

On T1 ports, unassigned cells can be inserted, as defined in the B-ISDN UNI and NNI physical layer generic criteria [7].

Cell Type	Header octet 1	Header octet 2	Header octet 3	Header octet 4
E1 idle	0000/0000	0000/0000	0000/0000	0000/0001
T1 unassigned	PPPP/0000	0000/0000	0000/0000	0000/PPP0

P: Programmable

Figure 15 Header formats of idle and unassigned cells

The 4 MSBs of header octet 1 and the 4 LSBs of header octet 4 are programmable in the ‘prg_tx_hd’ field of the TX idle/unassigned cell control register ‘txid’. All other header bits must be 0 for the cell to be deleted.

In E1 mode, the ‘prg_tx_hd’ field the should be set to 0000 0001.

In T1 mode, the ‘prg_tx_hd’ field can be programmed to any value PPPP PPP0.

The payload of idle or unassigned cells consists of the same octet which is repeated 48 times. The payload octet is programmable in the ‘prg_tx_pl’ field of the ‘txid’ register.

3.1.3.3 HEC generation

The HEC generation is implemented according to B-ISDN UNI PHY layer specifications [21].

The coset value is programmable in the ‘coset’ field of the ‘atmc’ register.

3.1.3.4 Payload scrambling

The scrambler function is implemented also according to B-ISDN UNI PHY layer specifications [21].

The scrambler function can be disabled per port in the ‘x43_scrambling’ field of the ‘ATM Transmit Reference Slot’ in RAM2.

3.1.3.5 Activation of ATM transmit ports

When activating ATM transmit ports, it is important to follow the initialization sequence as shown in **table 19**. Step 2 with the ‘p_tx_act’ bit of the ‘pcfN’ register set to 1 and the ‘channel_mode’ in the ‘ATM Transmit Reference Slot’ in RAM2 set to inactive must be held at least 250 µs. This condition is necessary to internally reset the ATM transmit port.

Table 17 Activation sequence for ATM transmit ports

Step	p_tx_act	channel_mode	Minimum Time
1	0 = inactive	00 = Inactive	
2	1 = active	00 = Inactive	250 µs
3	1 = active	01 or 11 = Active	

Each ATM transmit port can be configured in the ‘channel_mode’ field of the ‘ATM Transmit Reference Slot’ in RAM2 to operate in ‘Inactive’, ‘Active’ or ‘Standby’ mode.

In ‘Inactive’ mode, byte-pattern 0 ‘bp0’ is continuously sent to the framer transmit interface.

In ‘Active’ mode, user cells or idle/unassigned cells are sent to the framer transmit interface.

In ‘Standby’ mode, only idle/unassigned cells are sent to the framer transmit interface.

3.1.4 Protocol monitoring of the ATM mode

The following 32 bit counter is provided common to all ATM ports and all AAL ports:

- Number of discarded cells due to output queue, ATM receive buffer or segmentation buffer overflow.

The following 32 bit counters are provided per port:

- Number of received cells with correctable HEC errors
- Number of received cells with non-correctable HEC errors
- Number of times cell delineation SYNC state is left, except when forced by the microprocessor
- Number of discarded cells due to ATM transmit buffer overflow

3.2 AAL mode

A port N is operating in AAL mode if bit ‘p_atm’ of the port configuration register ‘pcfN’ is set to 0.

Some features of the AAL mode are controlled by the internal registers ‘acfg’, ‘caal’, ‘bp32’, ‘bp10’ and ‘cfil’. The features controlled by these registers are common to all AAL ports.

Some features of the AAL mode can be controlled per port, by programming the port configuration registers ‘pcfN’.

Some features of the AAL mode can be controlled per channel, by programming the channel specific ‘AAL Reference Slot’ in the internal configuration RAM’s (RAM1 for receive ports, RAM2 and RAM3 for transmit ports).

3.2.1 Unstructured CES mode

If the ‘p_ces’ bit in the port configuration register ‘pcfN’ is set to 1, the port is programmed for the ‘Unstructured T1/E1 Circuit Emulation Service (CES)’.

A 2.048 Mbit/s (E1) or 1.544 Mbit/s (T1) bitstream is packed into ATM cells without regard to any framing. No alignment between octets in E1 or T1 frames and octets in the ATM cells can be assumed.

ATM adaptation layer type 1(AAL1) with Unstructured Data Transfer (UDT) as defined in ITU-T I.363 should be used.

The complete 47-octet payload of the ATM cells should be used. No partially filled cells should be used.

A segmentation buffer per port with a maximum size of 16 cells is implemented in external RAM.

A reassembly buffer per port with a maximum size of 256 cells is implemented in external RAM.

The IWE8 provides support for clock recovery when asynchronous E1 or T1 circuits are carried. Both the Synchronous Residual Time Stamp (SRTS) method and Adaptive Clock Method (ACM) are supported.

As there is only one channel per port in the unstructured CES mode, and no notion of timeslots exist, the internal configuration RAM1, RAM2 and RAM3 must only be programmed with an ‘AAL Reference Slot’ at the position of slot 0.

3.2.2 N x 64 kbit/s mode

If the ‘p_ces’ bit in the port configuration register ‘pcfN’ is set to 0, the port is programmed for the ‘Structured T1/E1 N x 64 kbit/s Basic Service’.

The N x 64 kbit/s Service is intended to carry N of the 24 (T1) or 32 (E1) across the ATM network, where N can be range from 1 to 24 (T1) or 31 (E1).
An emulated N x 64 kbit/s circuit will be referred to as a channel throughout this document. It is possible that several channels share the same physical interface port.

Mapping of channels to timeslots

The mapping of the N x 64 kbit/s channels into an T1/E1 frame is done by programming the 32 positions of the internal configuration RAM’s (RAM1 for receive ports, RAM2 and RAM3 for transmit ports).

The timeslot in the group of N timeslots with the lowest frame slot number is called the reference slot. The corresponding frame slot position in RAM1, RAM2 and RAM3 should be programmed as an ‘AAL Reference Slot’. The reference slot number is used to identify the channel.

The other (N-1) frame slot positions of the channel should be programmed as ‘AAL Continuation Slots’ in RAM1 and RAM2. The ‘ref_slot_nr’ field entry identifies the channel the continuation slot belongs to.

It is possible to define more than one channel of N timeslots within one frame. In this case there is more than one reference slot.

It is important to notice that the N timeslots of a channel do not need to have consecutive frame slot numbers, but can be deliberately chosen out of the 32 frame slots.

Unused frame slots that do not belong to any channel should be programmed as an ‘Idle Slot’. Notice that for T1 ports, frame slot numbers 0,4,8,12,16,20,24,28 are by definition unused (translation mode 0) and must be programmed as ‘Idle Slots’.

The channel mapping can be dynamically reconfigured without disturbing other active channels of the same port.

3.2.3 AAL segmentation functions

3.2.3.1 ATM cell header generation

Before a channel is put into ‘Active’ mode, the microprocessor must write the ATM cell header consisting of 4 octets at the position of the first cell in the segmentation buffer of the channel (see external RAM description)’

Table 18 shows how the ATM cell header should be programmed in the segmentation buffer in external RAM. Header octet 1 is transmitted first over the UTOPIA interface.

Table 18: ATM cell header in segmentation buffer in external RAM

Bits 31 - 24	Bits 23 - 16	Bits 15 - 8	Bits 7 - 0
Header octet 4	Header octet 3	Header octet 2	Header octet 1

3.2.3.2 SAR-PDU generation AAL type 1

The purpose of this function is to generate the Segmentation And Reassembly - Protocol Data Unit (SAR-PDU) header and the SAR-PDU payload as described in the ITU-T recommendation of the I.360 Series [18] for AAL type 1.

The SAR-PDU header consists of the 4 bit Sequence Number (SN) field and the 4 bit Sequence Number Protection (SNP) field.
The SN field is further divided into the 3 bit Sequence Count (SC) field and the Convergence Sublayer Indication (CSI) bit.
The SNP field is divided into the 3-bit CRC code and an even parity bit.

The ITU-T recommendation of the I.360 Series [18] for AAL type 1 also defines the contents and the location of the pointer field in the SAR-PDU payload for Structured Data Transfer (SDT).

For partially filled cells, the SAR-PDU payload is defined as described in the ITU-T draft recommendations I.363.x [20]. The value, used for dummy fill, is programmable in the ‘cfil’ internal register. The fill octets carry no information and are ignored at the receiver.

Figure 16 shows the SAR-PDU payload without a pointer field (Non-P format).
Figure 17 shows the SAR-PDU payload with a pointer field (P format).

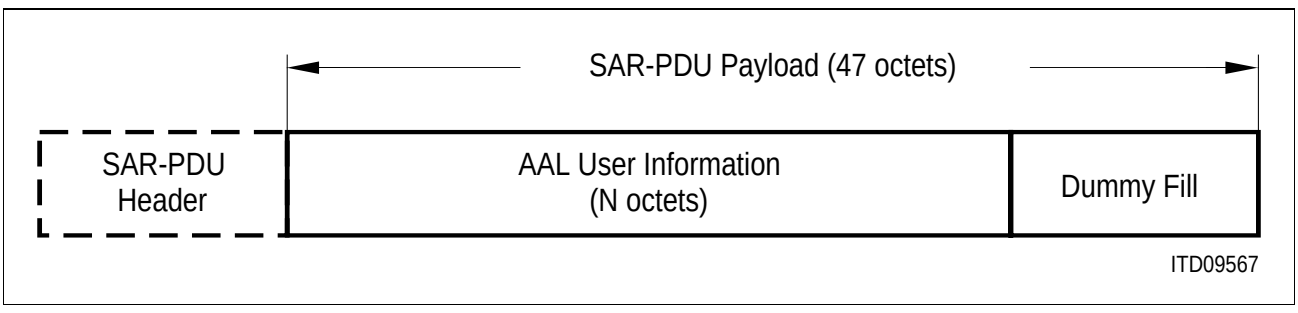


Figure 16
AAL type 1 SAR-PDU payload without pointer field: Non-P format

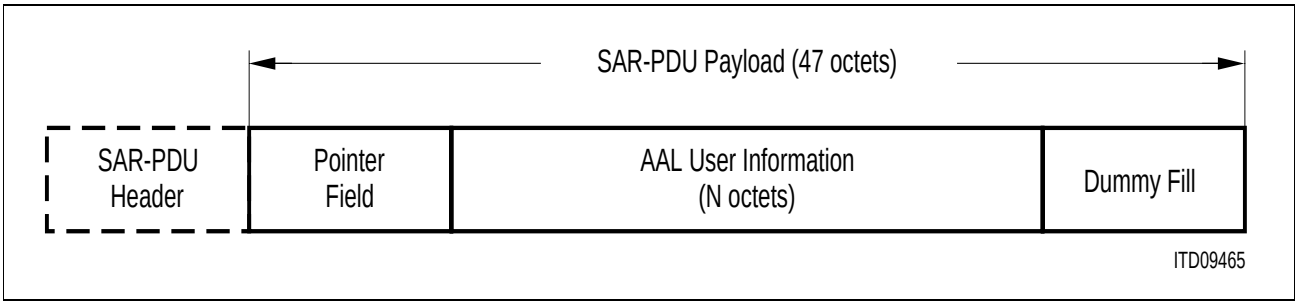


Figure 17
AAL type 1 SAR-PDU payload with pointer field: P format

Sequence Count field value

The first cell generated by the segmentation function has a SC value 0. The SC value is increased by one modulo 8 for each new block of AAL user information.

SDT structure length

The structure length for Structured Data Transfer of N*64-kbit/s channels is:

- N when frame-based SDT is selected
- N x 16 when multiframe-based SDT is selected for E1 ports
- N x 24 when multiframe-based SDT is selected for T1 ports.

The selection between frame-based or multiframe-based SDT is done by the ‘sdt_mfs’ field in the ‘AAL Receive Reference Slot’.

Frequency and value of the pointer field

The pointer field contains the binary value of the offset, measured in octets, between the end of the pointer field and the start of the structured block, in the 93 octet payload. The payload consists of the remaining 46 octets of this SAR-PDU payload and the 47 octets of the next SAR-PDU payload.

The frequency of occurrence of the pointer field is according to the ITU-T draft recommendations I.363.x [20]. The pointer field is used exactly once in every cycle, where a cycle is the sequence of eight consecutive SAR-PDU’s with Sequence Count values 0 through 7. The pointer field is used at the first available opportunity in a cycle to point to a start of a structured block. If a start of a structured block is not present in a cycle, then a pointer field containing a dummy offset value ‘127’ is used at the last opportunity in the cycle.

Synchronization of RTS generation with the segmentation function

Within a single port, only one channel at a time may be programmed to support SRTS. The ‘srts’ field of no more than one ‘AAL Receive Reference Slot’ per port in RAM1 may be set to 1.

If the ‘srts’ field of a channel is set, the RTS value stored in the ‘RTS Buffer’ (RB) of that port will be inserted into the CSI bits of the cells with SC value 1, 3, 5, or 7. The MSB of the RTS is placed in the CSI bit of the SAR-PDU header with the SC value of 1.

The RTS value stored in the RTS buffer of the port is loaded via the SDI pin of the ‘Clock Recovery interface’. A new value should be provided by the external clock recovery circuit once every cycle of 8 cells. To guarantee that the value stored in the RTS buffer of the port is the correct value, the sequence of operations indicated in **figure 18** is followed.

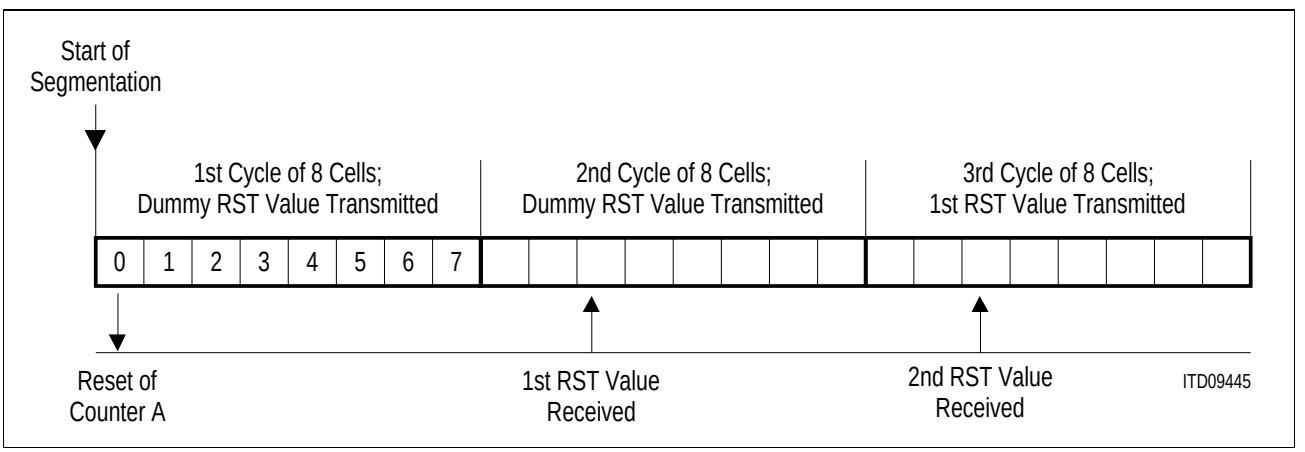


Figure 18
Synchronization of RTS Generation with start of segmentation

At the start of segmentation, the IWE8 informs the external clock recovery circuit to reset Counter A of the corresponding port. This is done by writing a reset frame (Data field = 111) for the corresponding port on the SDOR pin of the ‘Clock Recovery interface’.

As a consequence, the IWE8 expects to receive the first valid RTS value during the second cycle of 8 cells. The first valid RTS value will then be transmitted during the third cycle of 8 cells.

During the first and second cycle of 8 cells, a dummy RTS value is transmitted. The dummy RTS value is programmable in the ‘a_dummy_srts’ field of the ‘acfg’ register and is common for all ports.

If the external clock recovery circuit does not provide new RTS values to the RTS buffer (buffer underflow), the last received value is repeated. If too many RTS values are provided (buffer overflow), the values in excess will be omitted and a bit in the extended interrupt status register 2 ‘eis2’ is set.

A block diagram of the external clock recovery circuitry to generate the RTS values is represented in **figure 19**.

The value of N is equal to the number of bits in the AAL user information in a cycle of 8 cells.

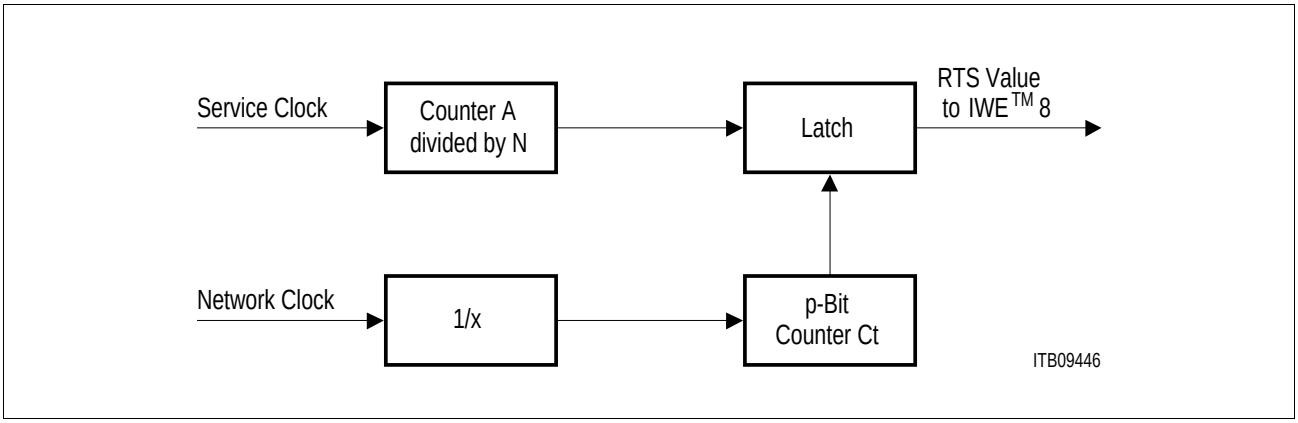


Figure 19
Block Diagram of RTS value generation by external clock recovery

3.2.3.3 SAR-PDU generation AAL type 0

The segmentation and reassembly function can be programmed to use, alternatively to the standard AAL type 1 SAR-PDU, a SAR-PDU that is referred to as AAL type 0 and consists of 48 octets payload without any overhead. The selection is done by programming the ‘AAL0’ field in the ‘AAL Receive Reference Slot’.

Figure 20 shows the AAL type 0 SAR-PDU. By programming the ‘part_fill’ field it is possible to fill only part of the SAR-PDU payload with User Information octets. Completely filled AAL0 cells are used when ‘part_fill’ is programmed to 48 octets.

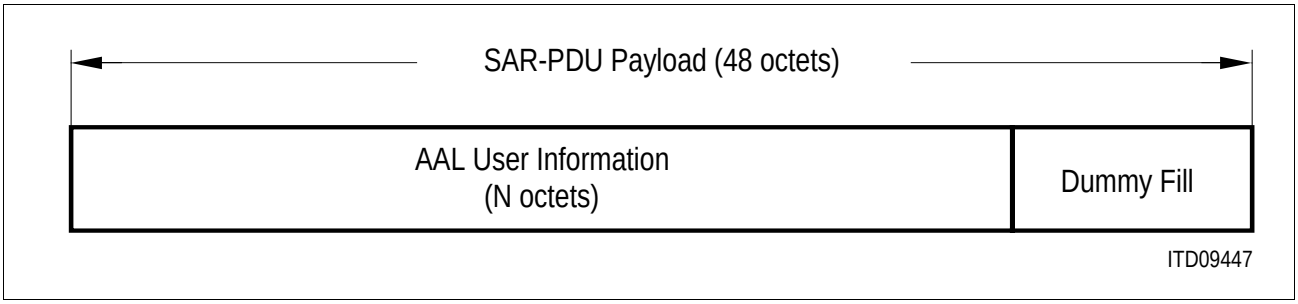


Figure 20
SAR-PDU of AAL type 0

3.2.3.4 Segmentation Buffer

In ‘unstructured CES’ mode, a segmentation buffer per port can store maximum 16 cells.

In ‘N x 64’ mode, a segmentation buffer per channel with a variable capacity depending on N and on the filling level of the partially filled cells is automatically configured by the IWE8.

Maximum number of cells per segmentation buffer:

‘part_fill’	> 24 octets per cell	≤24 octets per cell
N=1	4 cells	8 cells
N=2 or 3	8 cells	16 cells
N>3	16 cells	32 cells

3.2.3.5 Common Output Queue

When a cell is completely stored in one of the segmentation buffers, its external RAM address is written in a FIFO Output Queue (OQ) with 256 entries that is common to all ATM ports and all AAL channels.

3.2.3.6 Decorrelation of segmentation start

Cell segmentation can start with or without the decorrelation circuit activated, determined by the ‘dcor’ field in the ‘AAL Receive Reference Slot’ in RAM1.

Without decorrelation (dcor=0), segmentation is started as soon as the ‘channel_mode’ is set to ‘Active’ by the microprocessor. It should be noted that in synchronous systems, the microprocessor may activate a number of channels consecutively, in phase with the segmentation period of a particular channel, causing a large number of cells to be generated within the same 125 µsec period. This would result in a large number of cells residing in the output queue and increase the Cell Delay Variation (CDV).

In SDT mode, cell segmentation is started when the first ‘start of structure’ signal from the framer receive interface is received after activation of the channel. The resulting SC value and pointer field of the first cell transmitted will both be 0.

When decorrelation is set (dcor=1), the probability of cell concentration in the output queue is reduced by the decorrelation circuit shown in **figure 21**. After activation of a channel, a random waiting period is generated by a 5-bit counter that is free-running at a frequency of about 7.5 kHz (=F_{CLOCK}/12*280).

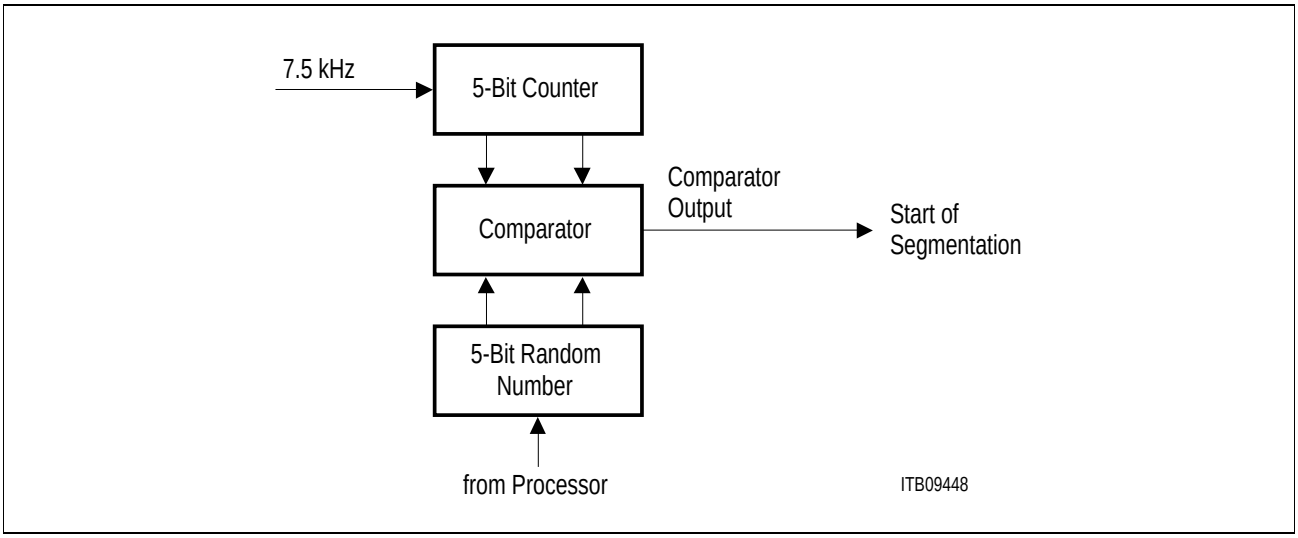


Figure 21
Block Diagram of Decorrelation Circuit

The start of segmentation of a channel consists of the following steps:

- The microprocessor loads a random number in the ‘dcor_random_nr’ field of the ‘AAL Receive Reference Slot’ of the channel in RAM1.
- The ‘channel_mode’ is set to ‘Active’.
- Each time an octet for this channel is received, the ‘Octet Receive processing’ (OR) compares the value of the 5-bit counter with the random number. Only when both values are equal, segmentation is started.

In SDT mode, cell segmentation is started when the first ‘start of structure’ signal from the framer receive interface is received after the comparator output has been generated.

3.2.3.7 AAL segmentation channel activation

When activating the segmentation of AAL receive channels, it is important to follow the initialization sequence as shown in **table 19**. Step 2 with the ‘p_rx_act’ bit of the ‘pcfN’ register set to 1 and the ‘channel_mode’ in the ‘AAL Receive Reference Slot’ in RAM1 set to ‘Inactive’ must be held at least 250 µs. This condition is necessary to internally reset the AAL channel.

Table 19 Activation sequence for AAL segmentation channels

Step	p_rx_act	channel_mode	Minimum Time
1	0 = inactive	00 = Inactive	
2	1 = active	00 = Inactive	250 µs
3	1 = active	01 or 11 = Active	

Each AAL receive channel can be configured in the ‘channel_mode’ field of the ‘AAL Receive Reference Slot’ in RAM1 to operate in ‘Inactive’, ‘Active’, ‘Standby’ or ‘Substitute’ mode.

- In ‘Inactive’ mode, no data is accepted from the framer receive interface.
- In ‘Active’ mode, data is accepted from the framer receive interface, segmented and cells are written into the segmentation buffers and the output queue.
- In ‘Standby’ mode, data is accepted from the framer receive interface but no cells are written in the segmentation buffers.
- In ‘Substitute’ mode, data is accepted from the framer receive interface, but substituted by a programmable byte-pattern. Cells are written into the segmentation buffers and the output queue.

3.2.4 AAL reassembly functions

3.2.4.1 Port and channel identification

Before an incoming cell is processed, it is determined to which port the cell is destined. This is indicated by the 3 LSB bits of the 5th header octet of the ATM cell (UDF field).

For ATM ports (p_atm=1) or AAL ports with unstructured CES service (p_ces=1), all cells are processed without taking into account the first 4 ATM header octets.

For AAL ports with N x 64 kbit/s service (p_atm=0 and p_ces=0), the channel to which the cell is destined is taken from the 5 LSB bits of the VCI field of the ATM header.

Cells that are destined to inactive ports or channels are discarded.

3.2.4.2 AAL type 1: SAR-PDU header and pointer field processing

When the ‘AAL0’ field of the ‘AAL Transmit Reference Slot’ is set to 0, the SAR-PDU header is processed according to AAL type 1. The following functions are discussed in more detail:

- SNP error detection and correction
- Sequence Count processing
- Standard Sequence Count algorithm
- Fast Sequence Count algorithm
- Pointer field detection and verification
- RTS extraction and verification

When the ‘AAL0’ field of the ‘AAL Transmit Reference Slot’ is set to 1, the SAR-PDU header and pointer field processing is disabled. None of the above mentioned functions is executed.

SNP Error Detection and Correction

The SNP error detection and correction is performed according to the ITU-T I.360 series recommendations [18].

When an error is detected and not corrected the Sequence Number (SN) field of the SAR-PDU header is declared invalid, otherwise the SN field is valid. The SN field contains the Sequence Count value (SC) and the CSI bit which are processed in the Sequence Count processing, pointer field detection and RTS assembly. The valid/invalid information of the SN field is used further by these functions.

The SNP error detection and correction function can be enabled or disabled by the ‘snp_check’ bit in the ‘AAL Transmit Reference Slot’. If disabled the SN of all incoming cells are declared valid.

Sequence Count processing

When the ‘sn_check’ bit in the ‘AAL Transmit Reference Slot’ is set to 0, all cells are accepted, no cells are discarded, lost and misinserted cells are not detected.

When the ‘sn_check’ bit in the ‘AAL Transmit Reference Slot’ is set to 1, selection can be made between two algorithms (standard or fast SC algorithm), by setting the ‘sn_fast’ bit in the ‘AAL Transmit Reference Slot’.

A 32-bit protocol monitoring counter is provided for the out-of-sequence events. An out-of-sequence event is detected when the received cell is out-of-sequence with the previous cell (i.e.arrived cell SC value is different from the last SC value plus one).

Standard Sequence Count algorithm

This algorithm is completely described in annex D of the ETSI B-ISDN AAL type 1 Specification [9] and is shown in **figure 22**.

The algorithm is described by a state machine of 5 states. A change in states within the state machine is indicated by an arrow, on which there are two distinct values represented. The first value refers to the event that originates the state change, and the second value refers to the action to be taken as a result of that event.

A decision in this algorithm is taken after evaluation of 2 consecutive SN. This means that when a cell is received it must be temporarily stored, waiting for the next cell before it is finally passed to the reassembly buffer. In the state machine, an action to be taken (accept or discard) always refers to the stored cell.

The sequence counting of modulo 8 permits that the algorithm detects a maximum of to 6 consecutive lost cells and 1 misinserted cell, assuming that misinsertion of one cell is at least as probable as the loss of 7 consecutive cells.

When lost cells are detected, an equal number of dummy cells are inserted into the transmitted data of the channel. This is required to maintain bit count integrity. The number of octets inserted per dummy cell is equal to the number of user information octets in the SAR-PDU payload of each cell. However when completely filled cells with SDT are used, some of the lost cells could have had a pointer field, while all inserted dummy cells contain 47 octets. Because in this particular case, bit count integrity can be lost, a procedure to recover from this error situation is implemented in the IWE8.

When one misinserted cell is detected, the algorithm is able to delete the misinserted cell, because of the delay of one cell in taking a decision.

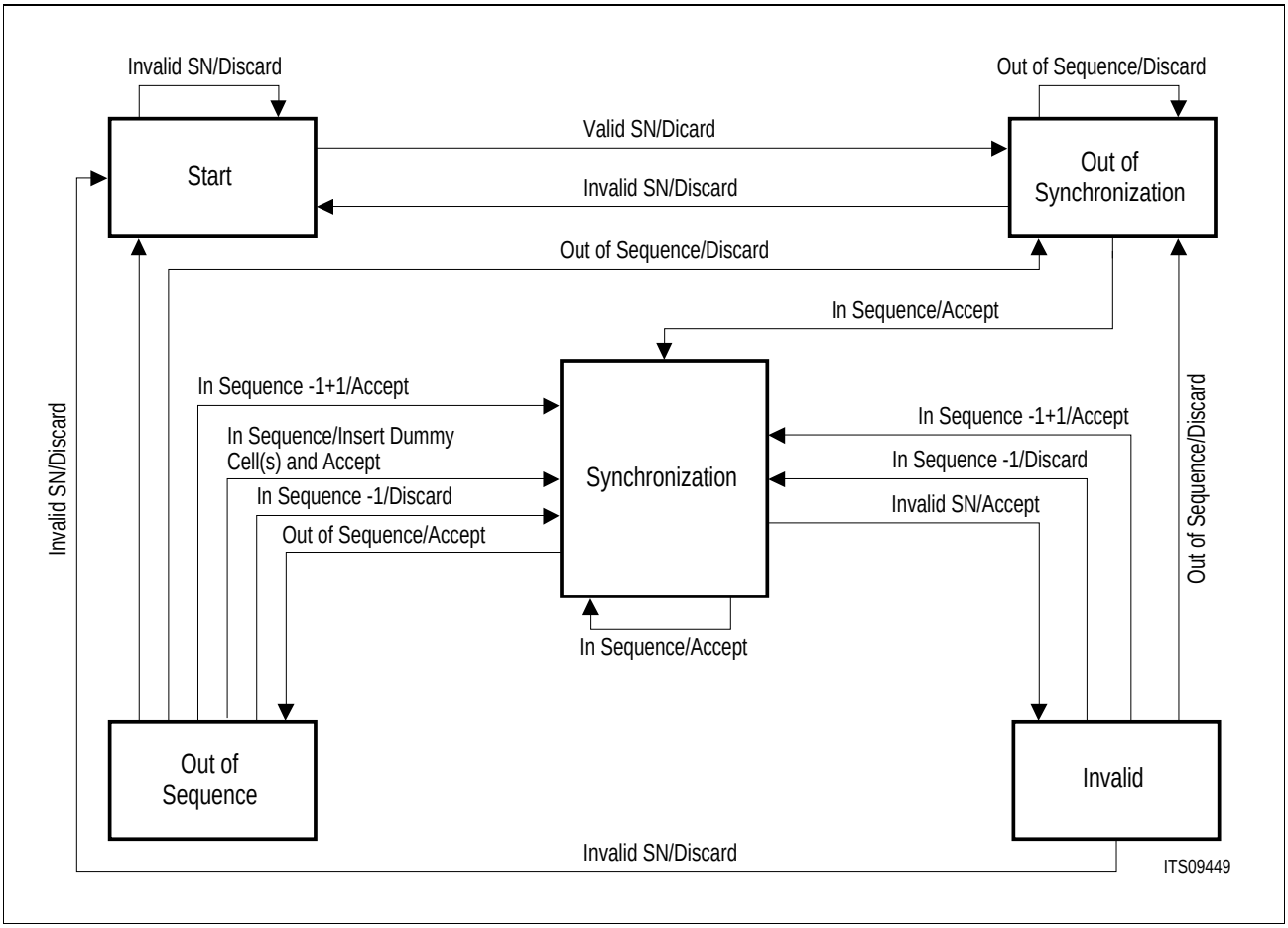


Figure 22
Sequence Count algorithm state machine

Fast Sequence Count algorithm

There is no difference between the state machines of the standard SC algorithm and the fast SC algorithm. The only difference is that in the fast algorithm, the action to be taken always refers to the currently received cell, while in the standard algorithm it refers to the temporarily stored cell. The advantage of the fast SC algorithm is that no additional one-cell delay is introduced.

In the fast SC algorithm, a misinserted cell is immediately accepted in the reassembly buffer. Only at the arrival of the next cell, it is detected that the previous cell was misinserted. Because the misinserted previous cell was already accepted, the current (in sequence) cell will be discarded instead. Provisions are taken in the IWE8 to compensate for the possible presence of pointer fields, maintaining perfectly the bit count integrity.

Lost cells are compensated with the insertion of dummy cells as in the standard algorithm.

Pointer field detection and verification

When the ‘sdt’ bit in the ‘AAL Transmit Reference Slot’ is set to 1, it is assumed that the channel is using Structured Data Transfer. The SAR-PDU payload is supposed to be of the P format under the following conditions:

- The SN field is valid
- The Sequence Count value is 0, 2, 4 or 6
- The CSI field = 1

When the ‘sdt_once’ bit in the ‘AAL Transmit Reference Slot’ is set to 1, only the first cell with CSI bit = 1 in a cycle of 8 cells is supposed to contain a P format SAR-PDU payload. the other cells with CSI bit = 1 within the same cycle are treated as cells with a non-P format SAR-PDU payload.

When the ‘sdt_once’ bit in the ‘AAL Transmit Reference Slot’ is set to 0, it is assumed that all cells with CSI bit = 1 contain a P format SAR-PDU payload.

In the cells with CSI bit = 1 that are supposed to contain a P format SAR-PDU payload, the pointer field is verified and accepted under the following conditions:

- The parity bit is correct as defined in the ITU-T I.363.x draft recommendations [20]
- The value of the offset field is between 0 and 93 or is the dummy value (127).

When an error is detected the pointer field is rejected. This means that the value of the pointer field is not used to indicate the start of the structured block. However, the P format of the SAR-PDU payload is assumed and the first octet of the SAR-PDU payload is not processed as user data.

The ‘sdt_par’ bit in the ‘AAL Transmit Reference Slot’ allows to disable the verification of the parity bit in the pointer field.

RTS extraction and verification

When the ‘crv_en’ bit in the ‘AAL Transmit Reference Slot’ is set to 1, and the port configuration bit ‘p_rts’ is set to 1, the channel is programmed for SRTS. This means that RTS values are extracted from the reassembled cells and verified.

The RTS value consists of the four CSI bits of the cells with odd Sequence Count value within a cycle of 8 cells. When the start of a new cycle is detected, the RTS value of the previous cycle is written to the ‘Clock Recovery Interface’, together with a correctness indication.

A RTS value is accepted as correct if the following condition is true:

- Accepted cells with valid SN fields and SC values equal to 1, 3, 5, and 7 were present in the previous cycle of 8 cells.

3.2.4.3 Reassembly buffer

The purpose of the reassembly buffer is to compensate the Cell Delay Variation (CDV) of the ATM network.

Physical reassembly buffer size

The reassembly buffers are implemented in external RAM. For all reassembly buffers of one port, a RAM block is provided of 256 memory blocks of 64 octets each.

The individual reassembly buffers per channel consist of a number of 64-octet memory blocks. The number of memory blocks used depends on the bandwidth of the channel (N*64-kbit/s). The granularity is 8 memory blocks. Thus for N*64-kbit/s there are N x 8 memory blocks.

Based on the cell filling level, AAL type and use of SDT, a memory block can be divided into subblocks, where the user data octets of a single cell are stored. The size of the memory subblock per reassembly buffer is automatically adapted. Table 20 shows this relationship.

The physical reassembly buffer size, expressed in number of octets, is given by:

Physical size = N x 8 x Cell Filling x Cells per block.

Table 20 Relationship between Cell Filling and Memory Subblock Size

Cell Filling (octets) AAL0	Cell Filling (octets) AAL1, no SDT	Cell Filling (octets) AAL1, with SDT	Subblock Size (octets) to store one cell	Cells per block
29–48	28–47	27–46	64	1
13–28	12–27	11–26	32	2
5–12	4–11	3–10	16	4
0–4	0–3	0–2	8	8

The start location of the first group of 8 memory blocks of the reassembly buffer corresponds to the channel reference time-slot number. The second group’s location corresponds to the next timeslot of the channel. This link is made by the ‘next_slot_nr’ field in the ‘AAL Transmit Reference Slot’. The next group’s locations correspond to the next time-slots of the channel. These links are made by the ‘next_slot_nr’ fields in the ‘AAL Transmit Continuation Slots’. In the last continuation slot (or reference slot itself, when no continuation slots exist (1 x 64 kbit/s)), the entry ‘next_slot_nr’ should refer to the reference slot.

The one-to-one relationship between time-slots and groups of memory blocks allows dynamic (re)configuration of a specific channel without disturbing other channels of the same port.

Logical reassembly buffer size

To avoid excessive delay introduced by the reassembly buffer, it is possible to limit the logical reassembly buffer size to a programmable number of octets in the 14 bit field 'buff_lsize' in the 'AAL Transmit Reference Slot' in RAM3. The relation is given by:

$$\text{bufflsize(octets)} < \frac{\text{MaxDelay} \times \text{N}}{125\mu\text{s}}$$

In the case where the standard SC algorithm is used, there must always be space for intermediate storage of one cell, so the logical size should not be set larger than the physical size - 1 cell.

To allow CDV compensation and SDT structure synchronization, the logical size expressed in number of cells should be programmed to a minimum value given by :

$$\text{bufflsize(cells)} > \left(\frac{(\text{K} \times \text{CDV}) + \text{SDTdelay}}{\text{AverageCellDistance}}\right) + 1$$

where

K = 1 : assuming that the first accepted cell has CDV = 0

K = 2 : assuming that the first accepted cell has maximum negative CDV

with:

$$\text{AverageCellDistance} = (125\mu\text{s} \times \text{CellFill})/\text{N}$$

and SDTdelay is:

$$\text{SDTdelay} = 125\mu\text{s} \times \left(\text{FR} + \left(\frac{\text{Pmax}}{\text{N}}\right)\right)$$

with FR being the number of frames in a structure:

FR = 0 : when SDT is not used

FR = 1 : for frame based SDT

FR = 16 : for multi-frame based SDT in E1 mode

FR = 24 : for multi-frame based SDT in T1 mode

and Pmax being the maximum number of payload octets from the pointer field to the start of structure :

if N x FR < 2 x Cell Fill : Pmax = N x FR

if N x FR > 2 x Cell Fill : Pmax = 2 x Cell Fill

The fact that the logical size must be larger in the case of SDT is due to the fact that the multiframe synchronization on the framer transmit interface is independent from the arrival of ATM cells with a start of a structured block.

Intermediate storage and storage of cells in the reassembly buffer

When the standard SC algorithm is used, the decision on cell acceptance is delayed until the next cell is received. Meanwhile the cell is temporarily stored in the first free memory block above the reassembly buffer. When the cell is accepted by the algorithm, it is stored in the reassembly buffer.

To implement this procedure the physical size of the reassembly buffer must be at least the logical size plus one cell.

In the fast SC algorithm the intermediate storage of a cell is not required. The cell is stored immediately in the reassembly buffer, when accepted.

Measurement of the reassembly buffer filling level for ACM

For ACM, the reassembly buffer filling level is measured in number of octets and passed to the ‘Clock Recovery Interface’ for transmission to the external clock recovery circuit, each time a new accepted cell is stored in the reassembly buffer.

Reading the reassembly buffer

One octet is read from the reassembly buffer each time the framer transmit interface request a new data octet to be transmitted in a time-slot belonging to the corresponding channel.

Insertion of dummy cells at cell loss

When cell loss is detected, it must be possible to insert a burst of up to 6 dummy cells in the reassembly buffer to maintain bit count integrity.

These dummy cells are not physically inserted in the reassembly buffer, but an indication containing the number of dummy cells to be inserted is put in a control field before the payload of the first accepted cell after the burst of lost cells.

When the buffer reading comes to the dummy cell control field, the correct number of octets is expanded, taking into account the number of inserted dummy cells and the cell filling.

Dummy cells inserted in the reassembly buffer are not taken into account in the reassembly buffer filling level calculation for ACM; this means that the buffer filling level is incorrect from the moment dummy cells are inserted, until the last octet of the last dummy cell has been transmitted to the framer transmit interface.

The user data octet used for the dummy cells is the byte-pattern selected by the ‘starv_bpslct’ field of the ‘AAL transmit reference slot’ in RAM3.

Initialization of the reassembly buffer

When the channel is activated by setting the ‘channel_mode’ in the ‘AAL Transmit Reference Slot’ in RAM2 to ‘Active’, the reassembly buffer must be initialized, i.e. the buffer should be filled to a certain amount before reading from the buffer is allowed.

Without SDT, the initialization steps of the reassembly buffer are:

1. Wait for the first accepted cell, while starvation octets are passed to the framer transmit interface
2. After the first accepted cell is stored, ST starvation octets are given to the framer transmit interface. The value of ST is programmable as a number of octets (up to 2047) in the ‘starv_ini’ field of the ‘AAL Transmit Reference Slot’ in RAM3.

$$\text{starvini} \geq K \times N \times \frac{CDV}{125\mu s}$$

   where
   K = 1 : assuming that the first accepted cell has CDV = 0
   K = 2 : assuming that the first accepted cell has maximum negative CDV
3. After ST starvation octets have been transmitted, the contents of the reassembly buffer are passed to the framer transmit interface.

With SDT, the initialization steps are:

1. Wait for the first accepted cell with even Sequence Count value and CSI bit = 1, while starvation octets are passed to the framer transmit interface.
2. After the first accepted cell is stored, ST starvation octets are given to the framer transmit interface.
3. After ST starvation octets have been transmitted, the reassembly buffer is read until the ‘ATM start of structure’ is met (a pointer field indicating the offset to the start of a structured block). Meanwhile starvation octets are transmitted to the framer transmit interface.
4. When the ‘ATM start of structure’ is met, the reading of the reassembly buffer is stopped and starvation octets are further transmitted, until the ‘Port start of structure’ is detected. From that moment on, the ‘ATM and Port start of structure’ are synchronous and the contents of the reassembly buffer can be passed to the framer transmit interface. A ‘Port start of structure’ occurs when the framer transmit interface requests the first time-slot octet belonging to the channel in the frame (frame based SDT) or the multiframe (multiframe based SDT).

The data transmitted in the starvation octets is the byte-pattern selected by the ‘starv_bpslct’ field of the ‘AAL transmit reference slot’ in RAM3.

The reassembly buffer can be re-initialized under microprocessor control by setting the ‘mcp_reinit’ bit in the ‘AAL Transmit Reference Slot’ in RAM2.

Handling of overflow

Overflow is detected when, at the moment of storing an accepted cell, the extra payload of the new cell in the buffer would exceed the logical size of the reassembly buffer.

For AAL type 1 two possible actions exist:

- The cell is discarded
- The cell is accepted but the reassembly buffer is automatically re-initialized.

In the first case, re-initialization of the reassembly buffer is only possible under microprocessor control and is in line with the ITU-T I.360 series recommendations [18], while in the second case re-initialization is done automatically without disturbing the microprocessor. The action chosen is determined by the ‘auto_reinit_of’ field in the ‘AAL Transmit Reference Slot’ in RAM3.

For AAL type 0 the action is:

- The accepted cell is considered to be a misinserted cell and rejected.

Handling of Underflow

An underflow period is detected when no octets are available in the reassembly buffer to be passed to the framer transmit interface. Starvation octets are passed to the framer transmit interface during the underflow period.

For AAL type 1, two possibilities exist:

1. The underflow is considered to be caused by an extremely late cell. The number of starvation octets transmitted during the underflow period is counted (max. 4096 octets). When cells are stored in the reassembly buffer again, the number of transmitted starvation octets is subtracted from the stored octets in the reassembly buffer. The underflow period is ended when the result of the subtraction is positive. To maintain bit count integrity, the same number of transmitted starvation octets is removed from the reassembly buffer before reading proceeds as normal.
2. When one cell is stored in the reassembly buffer again, the underflow period is ended and the reassembly buffer is automatically re-initialized.

In the first case, re-initialization of the reassembly buffer is only possible under microprocessor control and is in line with the ITU-T I.360 series recommendations [18], while in the second case re-initialization is done automatically without disturbing the microprocessor.

For AAL type 0 the action taken is:

- Detection of an underflow period is considered to be the detection of cell loss. For this reason a dummy cell is inserted. The inserted dummy cell insertion must be reflected in the buffer filling level of the reassembly buffer.

During an underflow period, the length of the underflow period is measured by counting the number of transmitted starvation octets, expressed as a number of cells (starvation cells)

Loss of synchronization of start of structure

The structure length used for Structured Data Transfer of N*64-kbit/s channels is:

- N when frame-based SDT is selected
- N x 16 when multiframe-based SDT is selected for E1 ports
- N x 24 when multiframe-based SDT is selected for T1 ports.

During initialization the ‘ATM start of structure’ is synchronized with the ‘Port start of structure’. Since this synchronization may get lost, it is determined whether a reception of an ‘ATM start of structure’ coincides with a ‘Port start of structure’. If they do not coincide, a two bit error counter is incremented. When the error counter equals a programmable threshold value, the reassembly buffer is re-initialized. The threshold value is programmed in the ‘sdt_oos_nr’ field of the ‘AAL Transmit Reference Slot’ in RAM2.

When inserting dummy cells to compensate for cell loss, it is possible that an excess of starvation octets are transmitted. As a result, the ‘ATM start of structure’ out of phase with the ‘Port start of structure’ only for a limited number of octets. Therefore, the following procedure is added:

- At the end of expanding a burst of dummy cell(s), a flag is set, indicating that a phase shift can occur. The maximum phase shift is 2 octets (e.g. 2 cells with pointers are lost within a sequence of eight cells)
- When an ‘ATM start of structure’ is received and a positive phase shift is detected lower than or equal to 2 octets, an equal number of octets is deleted in the reassembly buffer, and the flag is reset.
  When the detected phase shift is larger than the allowed value or negative the flag is reset and the reassembly buffer is re-initialized.
  When no phase shift is detected the flag is reset.

Using this procedure compensates the bit count integrity violation created by inserting dummy cells, when operating in SDT mode with a cell filling of 47 octets.

3.2.4.4 AAL reassembly channel activation

When activating the reassembly of AAL transmit channels, it is important to follow the initialization sequence as shown in table 19. Step 2 with the ‘p_tx_act’ bit of the ‘pcfN’ register set to 1 and the ‘channel_mode’ in the ‘AAL Transmit Reference Slot’ set to ‘Inactive’ must be held at least 250 µs. This condition is necessary to internally reset the AAL channel.

Table 21 Activation sequence for AAL reassembly channels

Step	p_tx_act	channel_mode	Minimum Time
1	0 = inactive	00 = Inactive	
2	1 = active	00 = Inactive	250 µs
3	1 = active	01 or 11 = Active	

Each AAL transmit channel can be configured in the ‘channel_mode’ field of the ‘AAL Transmit Reference Slot’ to operate in ‘Inactive’, ‘Active’ or ‘Standby’ mode.

- In ‘Inactive’ mode, no cells are accepted from the ‘UTOPIA Transmit interface’, and byte-pattern 0 is sent to the framer transmit interface.
- In ‘Active’ mode, cells are accepted from the ‘UTOPIA Transmit interface’, and user data octets are sent to the framer transmit interface.
- In ‘Standby’ mode, cells are accepted from the ‘UTOPIA Transmit interface’, but byte-pattern 0 is sent to the framer transmit interface.

3.2.5 Protocol monitoring of the AAL functions

The following 32 bit counter is provided common to all ATM ports and all AAL ports:

- Number of discarded cells due to output queue, ATM receive buffer or segmentation buffer overflow.

The following 32 bit counters are provided per channel:

- Number of times SDT start of structure changes phase upstream (AAL1)
- Number of discarded downstream cells due to reassembly buffer overflow (AAL0 & AAL1)
- Number of end of reassembly buffer overflow (AAL0 & AAL1)
- Number of downstream cells with invalid SN/SNP (AAL1)
- Number of SC out of sequence (AAL1)
- Number of downstream ‘misinserted cells’ detected by SC algorithm (AAL1)
- Number of downstream cells discarded by SC algorithm
- Number of rejected SDT pointers due to parity error (AAL1)
- Number of SC cycles with no SDT pointer field or more than one pointer field (AAL1)
- Number of end of reassembly buffer underflow (AAL0 & AAL1)
- Number of inserted starvation cells (AAL0 & AAL1) due to reassembly buffer underflow
- Number of times ATM start of structure out of sync with port start of structure (AAL1)
- Number of downstream ‘lost cells’ detected by SC algorithm (AAL1)

3.3 OAM processing

3.3.1 Event queue

All the functional blocks that process octets or cells can generate counter events, i.e. commands to increment a particular counter in the external RAM. All counter events are written in a FIFO queue that can store 256 counter events.

A counter event contains the OAM counter address in external RAM and an increment value.

3.3.2 OAM control register

The OAM control register ‘oamc’ contains a bit ‘oam_act’ that can be used to control the functioning of the OAM processing block (OM).

In RAM test mode, the ‘oam_act’ should be set to 0. In this mode, the microprocessor can write and read the complete external RAM.

In normal mode, the ‘oam_act’ should be set to 1. In this mode, the counter event processing is active. The microprocessor can only read indirectly in the interrupt queue.

The ‘dest_read’ bit determines whether a read operation from the microprocessor in the OAM counter address space in external RAM causes a reset of the counter value.

3.3.3 Counter event processing

The OAM processing block (OM) will read counter events from the event queue as long as the event queue is not empty. The OM will read the counter value ‘count_value’ and the counter threshold from external RAM. If the counter is not yet at its maximum value 4000 0000_H, the value is increased with the increment value given by the counter event. If the counter threshold is active (‘thres_act’ = 1) and the counter equals or exceeds the threshold value ‘thres_value’, the OM block will write an interrupt entry in the interrupt queue in external RAM. The new counter value with indication whether an interrupt was generated in the ‘int_gen’ field will finally be written into external RAM.

The use of the counter thresholds allows the software to reduce the number of generated interrupts and to decide at what error level an interrupt should be generated.

When the software wants to use polling mode, the thresholds can be made inactive, and no interrupts will be generated. The software will read all the counters on regular time intervals in this mode.

A combination of both methods is also possible, all the counters are read and reset on regular time intervals. However thresholds can be used as an extra guard: a counter that reaches an exceptionally high value will cause an interrupt.

3.3.4 Interrupt queue handling

The interrupt queue in external RAM is handled as a FIFO which is written by the OM block whenever a counter reaches its threshold value.

When there are interrupts in the interrupt queue, the ‘iq_ne’ bit in the interrupt status register 1 ‘isr1’ will be set to 1. When the corresponding bit is not masked in the ‘imr1’ register an interrupt will be generated on the $\overline{\text{MPIR1}}$ pin.

The microprocessor should react on the interrupt by reading the interrupt queue. When ‘oam_act’ is set to 1, the MPADR12-1 address bits are don’t care while reading in the interrupt queue. The OM block will automatically provide the next interrupt queue entry.

Each interrupt queue entry identifies a particular OAM counter that has reached its threshold value. The counter is identified by its port_nr, channel_nr and counter_nr. When the microprocessor reads the counter value and the ‘dest_read’ bit is set to 1, the counter is automatically reset.

Each interrupt queue entry also indicates whether there are still more interrupts in the queue in the ‘iq_ne’ field. This allows the software to read the interrupt queue until it is empty without having to read the interrupt status register ‘isr1’ again.

3.4 Loopbacks

For the purpose of testing, it is possible to program 3 different loopbacks in the IWE8.

3.4.1 Serial loopback

The framer transmit clock, data, framesync and multi-framesync signals can be looped to the framer receive interface per port, by setting the ‘p_slp’ bit in the port configuration register ‘pcfN’.

The loopback can be made transparent or non-transparent by setting the ‘tslp’ bit in the loopback control register ‘lpbc’. If the loopback is made non-transparent, all 1’s are transmitted on FTDAT.

3.4.2 Upstream UTOPIA loopback

It is possible to loop ATM cells that are going to be transmitted on the UTOPIA receive interface to the UTOPIA transmit interface through the ‘Upstream Loop’ (UL) block. The UL block contains a buffer of two ATM cells.

When a cell is available in the UL buffer, the UTOPIA transmit interface will put a 0 on the TXCLAV signal, to prevent the ATM layer component from sending cells during the processing of the loopback cell.

To activate the upstream UTOPIA loop, the ‘p_ulp’ bit in the port configuration register ‘pcfN’ must be set to 1.

For ATM mode ports, all ATM cells are looped regardless the ATM header.

For AAL mode ports, it is possible to make a single channel loop using a VCI filter. When the ‘vci_flt_ulp’ bit in the loopback control register ‘lpbc’ is set to 0 all cells are looped. When the bit is set to 1, only those cells with the 5 LSB bits of the VCI matching the ‘vci_val_ulp’ field of the ‘lpbc’ register will be looped.

The loopback can be made transparent or non-transparent by setting the ‘tulp’ bit in the loopback control register ‘lpbc’. If the loopback is made non-transparent, the looped cells are not transmitted on UTOPIA receive interface.

3.4.3 Downstream UTOPIA loopback

It is possible to loop ATM cells that are coming in on the UTOPIA transmit interface to the UTOPIA receive interface through the ‘Downstream Loop’ (DL) block. The DL block contains a buffer of two ATM cells.

When a cell is available in the DL buffer and in the output queue, the UTOPIA receive interface will transmit cells from both buffers with alternating priority.

To activate the downstream UTOPIA loop, the ‘p_dlp’ bit in the port configuration register ‘pcfN’ must be set to 1.

When the downstream UTOPIA loopback is active for at least one port, the UTOPIA transmit interface will only assert the UTCLAV signal to 1 when a free space of one ATM cell is available in both the DL buffer and the UT input buffer.

The loopback can be made transparent or non-transparent by setting the ‘tdlp’ bit in the loopback control register ‘lpbc’. If the loopback is made non-transparent, the looped cells are not transferred to the ‘Cell Transmit processing’ block CT.

4 Register Description

4.1 IWE8 Address Map

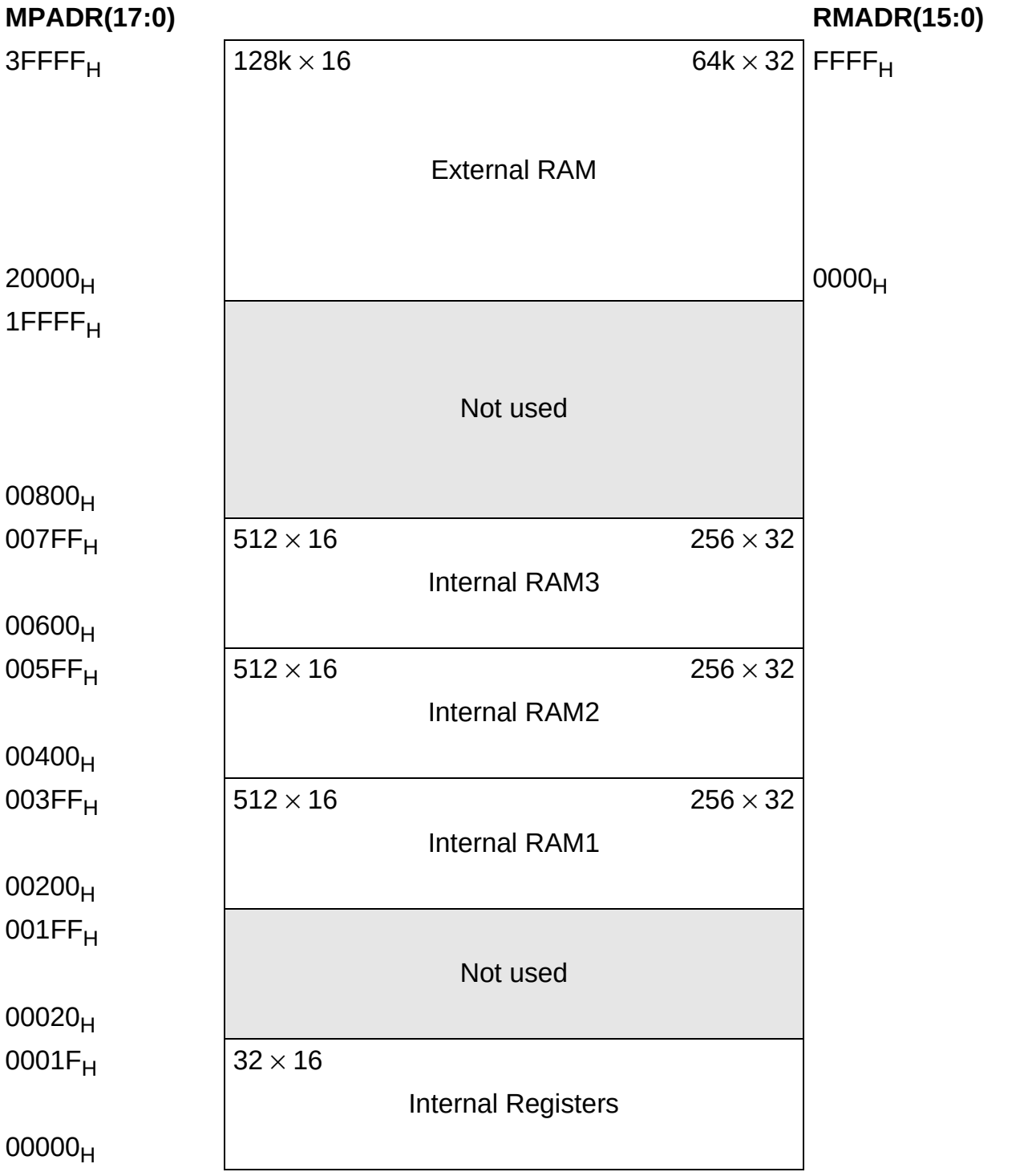


Figure 23 IWE8 Address Map

The IWE8 occupies an address space of 256k x 16 bits. The lower 128k x 16 bits are used for internal registers and internal configuration RAM's. The upper 128k x 16 bits are used to address external RAM.

The 32 internal registers occupy the 32 lowest addresses. Accesses to the internal registers are 16 bit oriented.

The 3 internal configuration RAM's are organised as 256 x 32 bit memories.

The external RAM is organised as a 64k x 32 bit memory.

Accesses to internal configuration RAM's or external RAM are always 32 bit oriented.

4.2 Internal Registers

Entry size = 16 bit

Table 22 IWE8 internal registers

MPADR(17:0)	Width	Name	Register
00000_H	11	pcf0	Port 0 configuration register
00001_H	11	pcf1	Port 1 configuration register
00002_H	11	pcf2	Port 2 configuration register
00003_H	11	pcf3	Port 3 configuration register
00004_H	11	pcf4	Port 4 configuration register
00005_H	11	pcf5	Port 5 configuration register
00006_H	11	pcf6	Port 6 configuration register
00007_H	11	pcf7	Port 7 configuration register
00008_H	13	acfg	ASIC configuration register
00009_H	3	oamc	OAM control register
$0000A_H$	5	catm	OAM-counter enable register for ATM ports
$0000B_H$	16	caal	OAM-counter enable register for AAL ports
$0000C_H$	16	bp32	Byte-pattern register bp3 and bp2
$0000D_H$	16	bp10	Byte-pattern register bp1 and bp0
$0000E_H$	16	atmc	ATM control register
$0000F_H$	16	rxid	rx idle/unassigned cell control register
00010_H	16	txid	tx idle/unassigned cell control register
00011_H	9	lpbc	Loopback control register
00012_H	8	cfil	Cell fill register for partially filled cells
00013_H	16	imr1	Interrupt mask register 1
00014_H	1	time	Timer enable register

Table 22 IWE8 internal registers (cont'd)

MPADR(17:0)	Width	Name	Register
00015_H	—	—	Unused: 0000_H output
00016_H	9	vers	Version register
00017_H	8	ckmo	Clock monitor register
00018_H	16	isr1	Interrupt status 1 register
00019_H	8	eis1	Extended interrupt status 1 register
$0001A_H$	8	eis2	Extended interrupt status 2 register
$0001B_H$	8	eis3	Extended interrupt status 3 register
$0001C_H$	16	eis4	Extended interrupt status 4 register
$0001D_H$	8	isr2	Interrupt status 2 register
$0001E_H$	—	—	Unused: 0000_H output
$0001F_H$	—	—	Unused: 0000_H output

The IWE8 decodes only MPADR bits 17, 10 .. 9, 4 .. 0 for addressing the internal registers. The other address bits are don't care.

4.2.1 Port Configuration Registers (pcfN)

Read/write Address 00_H:07_H
Value after reset 0000_H

15							8
Not used					p_atm	p_ces	p_acm
7							**0**
p_srts	p_slp	p_ulp	p_dlp	p_rx_act	p_rx_em	p_tx_act	p_tx_mfs

p_atm ATM mode port
- 0 AAL (CES) mode port
- 1 ATM (PHY) mode port

p_ces Circuit emulation service
- X When p_atm = 1
- 0 N × 64 kbit/s service
- 1 Circuit emulation service (unstructured)

p_acm Adaptive clock method)

X When p_atm = 1
0 Adaptive clock method not used
1 Adaptive clock method used

p_srts Synchronous Residual Time Stamp method

X When p_atm = 1
0 SRTS method not used
1 SRTS method used

p_slp Serial loopback

0 Serial loopback inactive
1 Serial loopback active

p_ulp Upstream UTOPIA loopback

0 Upstream UTOPIA loopback inactive
1 Upstream UTOPIA loopback active

p_dlp Downstream UTOPIA loopback

0 Downstream UTOPIA loopback inactive
1 Downstream UTOPIA loopback active

p_rx_act Port receive activate

0 Port receive inactive
1 Port receive active

p_rx_em Port receive emergency mode

0 Automatic switch over to emergency mode disabled
1 Automatic switch over to emergency mode enabled

p_tx_act Port transmit activate

0 Port transmit inactive
1 Port transmit active

p_tx_mfs Port transmit multiframe select

When E1/$\overline{T1}$ = 1 (E1 mode)

0 Double frame mode
1 crc multiframe mode

When E1/$\overline{T1}$ = 0 (T1 mode)

0 Superframe mode
1 Extended superframe mode

4.2.1.1 ASIC Configuration Register (acfg)

Read/write Address 08_H
Value after reset: 0000_H

15					8
Not used	a_sw_ reset	a_ut_en	a_ur_en	a_crv_en	a_dummy _rts(3)

7				0
a_dummy _rts(2:0)	a_emg_ bpslct(1:0)	a_ovf_ cnt_en	a_ptr_ prty	a_even_ pck

a_sw_reset Software reset

0 Software reset inactive
1 Software reset active
The IWE8 generates internally a resetpulse when a_sw_reset becomes active. This internal resetpulse will also reset the a_sw_reset to inactive.

a_ut_en UTOPIA transmit enable

0 UTOPIA transmit inactive
1 UTOPIA transmit active

a_ur_en UTOPIA receive enable

0 UTOPIA receive inactive
1 UTOPIA receive active

a_crv_en Clock recovery interface enable

0 Clock recovery interface inactive
1 Clock recovery interface active

a_dummy_rts(3:0) Dummy RTS value

Two dummy RTS values will be transmitted in the first 16 ATM cells after start of segmentation.

Note : The a_dummy_rts value must be programmed before *the a_crv_en bit is made active. Otherwise the first 2 rts values transmitted will be fixed at '0000'.*

a_emg_bpslct Emergency byte-pattern select

00 Select byte-pattern 0, defined in bp10[bp0]
01 Select byte-pattern 1, defined in bp10[bp1]
10 Select byte-pattern 2, defined in bp32[bp2]
11 Select byte-pattern 3, defined in bp32[bp3]

a_ovf_cnt_en Output queue overflow counter enable

0 Overflow counter disabled
1 Overflow counter enabled

a_ptr_prty SDT pointer even parity generation

0 SDT pointer even parity generation disabled
Fixed value in bit 7 of pointer field: ‘0’.
1 SDT pointer even parity generation enabled

a_even_pck Use even parity check for parity checkers internal/external RAM and UTOPIA

0 Odd parity check enabled (default operation)
The parity checkers expect the normal parity.
1 Even parity check enabled
The parity checkers expect the inverse parity. This mode tests the proper operation of the parity generators/ checkers.

4.2.2 OAM Control Register (oamc)

Read/write Address 09_H
Value after reset: 0000_H

15							8
Not used							
7							**0**
Not used					tim_ set1_en	dest_ read	oam_ act

tim_set1_en Timer set 1 enable

0 Timer set 1 disabled
1 Timer set 1 enabled

dest_read Destructive read mode

0 Destructive read mode disable
1 Destructive read mode enabled
only accepted if oam_act bit is set
oam counter values in the external RAM are reset to ‘0’ after read by the micro-processor.

oam_act OAM active

0 OAM inactive
In this mode, the protocol monitoring is disabled and the RAM arbiter (which provides the microprocessor or the protocol monitoring access to the external RAM) only allows access to the external RAM by the microprocessor. In this mode, the microprocessor can read and write the complete external RAM address space (needed for RAM test).

1 OAM active
In this mode, the protocol monitoring is enabled and the RAM arbiter grants both the protocol monitoring and the microprocessor access to the external RAM.
In this mode, reading by the microprocessor in the interrupt queue address space always yields the first interrupt in the queue.

4.2.3 OAM-Counter Enable Register for ATM Ports (catm)

Read/write Address $0A_H$
Value after reset: 0000_H

15							8
Not used							
7							**0**
Not used							cnt_atm_en(4:0)

cnt_atm_en(4:0) OAM-counter enable for ATM ports

0 Counter disabled

1 Counter enabled

For individual counters, see OAM counter addressmap. Applicable to all ports with pcfN[p_atm] = 1

4.2.4 OAM-Counter Enable register for AAL Ports (caal)

Read/write Address $0B_H$
Value after reset: 0000_H

15	14	13	12	11	10	9	8
cnt_aal_en(15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
cnt_aal_en(7:0)							

cnt_aal_en(15:0) OAM-counter enable for AAL ports

0 Counter disabled
1 Counter enabled

For individual counters, see OAM counter addressmap. Applicable to all ports with pcfN[p_atm] = 0

4.2.5 Byte-pattern Register bp3 and bp2 (bp32)

Read/write Address $0C_H$
Value after reset: $FFFF_H$

15	14	13	12	11	10	9	8
bp3(7:0)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
bp2(7:0)							

bp3(7:0) Byte-pattern 3

bp2(7:0) Byte-pattern 2

4.2.6 Byte-pattern Register bp1 and bp0 (bp10)

Read/write Address $0D_H$
Value after reset: $FFFF_H$

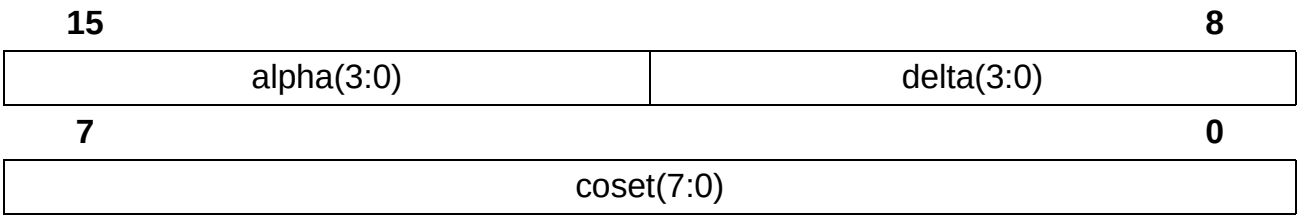
15	14	13	12	11	10	9	8
bp1(7:0)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
bp0(7:0)							

bp1(7:0) Byte-pattern 1

bp0(7:0) Byte-pattern 0

4.2.7 ATM Control Register (atmc)

Read/write Address $0E_H$
Value after reset: 7655_H



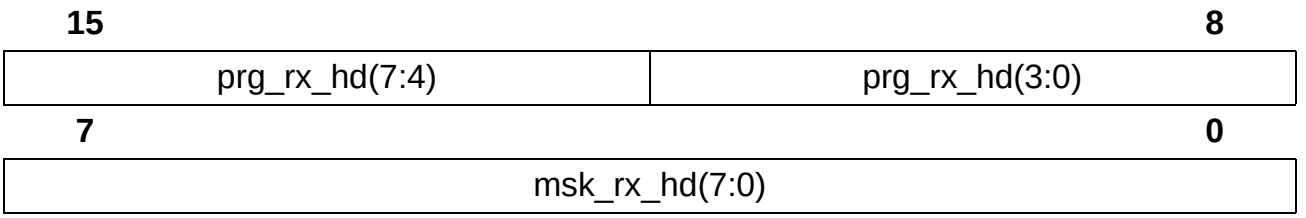
alpha(3:0) Number of consecutive incorrect HEC (SYNC → HUNT)

delta(3:0) Number of consecutive correct HEC (PRESYNC → SYNC)

coset(7:0) Coset value x-ored with HEC

4.2.8 RX Idle/Unassigned Cell Control Register (rxid)

Read/write Address $0F_H$
Value after reset: 0101_H



prg_rx_hd(7:4) Programmable rx idle/unassigned cell header octet 1 bits (7:4)

prg_rx_hd(3:0) Programmable rx idle/unassigned cell header octet 4 bits (3:0)
(All other header bits must be '0')

msk_rx_hd(7:0) Mask rx idle/unassigned cell header

- 0 Corresponding header bit should have value given in prg_rx_hd
- 1 Programmable bit is masked (corresponding header bit is don't care)

4.2.9 TX Idle/Unassigned Cell Control Register (txid)

Read/write Address 10_H
Value after reset: $016A_H$

15							8
prg_tx_hd(7:4)				prg_tx_hd(3:0)			
7							**0**
prg_tx_pl(7:0)							

prg_tx_hd(7:4)	Programmable tx idle/unassigned cell header octet 1 bits 7:4
prg_tx_hd(3:0)	Programmable tx idle/unassigned cell header octet 4 bits 3:0 (Other header bits are fixed at '0')
prg_tx_pl(7:0)	Programmable tx idle/unassigned cell payload octet $6A_H$ according to I.432

4.2.10 Loopback Control Register (lpbc)

Read/write Address 11_H
Value after reset: 0000_H

15							8
Not used							tslp
7							**0**
tulp	tdlp	vci_flt_ ulp	vci_val_ ulp(4:0)				

Note: Transparent loop : data is looped and forwarded.
Non-transparent loop : data is only looped.

tslp	Transparent serial loop
	0 Non-transparent serial loop
	1 Transparent serial loop
tulp	Transparent upstream UTOPIA loop
	0 Non-transparent upstream UTOPIA loop
	1 Transparent upstream UTOPIA loop
tdlp	Transparent downstream UTOPIA loop
	0 Non-transparent downstream UTOPIA loop
	1 Transparent downstream UTOPIA loop

vci_flt_ulp VCI filter enable for upstream UTOPIA loop

0 VCI filter disabled (all VCI's are looped)

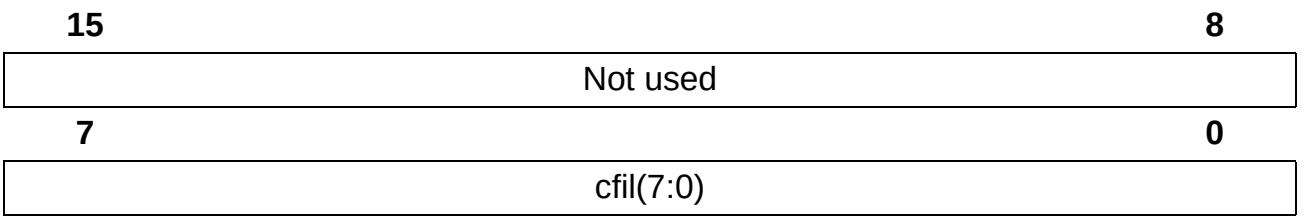
1 VCI filter enabled (only single VCI is looped)

vci_val_ulp(4:0) 5 LSB of the VCI value (i.e. channel number) to be looped on upstream UTOPIA loop

Note: for ATM ports with upstream UTOPIA loopback (pcfN[p_atm] = 1 and pcfN[p_ulp] = 1), all cells are looped regardless the VCI value. The vci_flt_ulp and vci_val_ulp(4:0) bits are don't care.

4.2.11 Cell Fill Register for Partially Filled Cells (cfil)

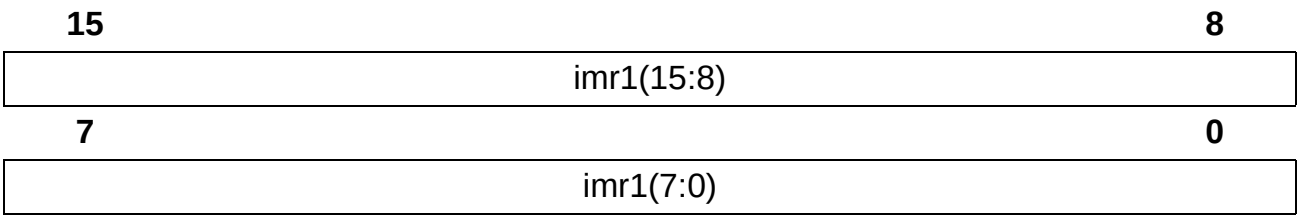
Read/write Address 12_H
Value after reset: 0000_H



cfil(7:0) Dummy fill octet in partially filled cells

4.2.12 Interrupt Mask Register 1 (imr1)

Read/write Address 13_H
Value after reset: $FFFF_H$



A bit set in this register, masks the corresponding interrupt in isr1.

imr1(15:0) Interrupt mask register 1

0 Interrupt not masked

1 Interrupt masked

4.2.13 Timer Enable Register (time)

Read/write Address 14_H
Value after reset: 0000_H

15							8
Not used							
7							**0**
Not used							tim_set2_en

tim_set2_en Timer set 2 enable
- 0 Timer set 2 disabled
- 1 Timer set 2 enabled

4.2.14 Version Register (vers)

Read Address 16_H
Value after reset: $00C9_H$ for E1 mode, 0089_H for T1 mode

15							8
Not used							itst3
7							**0**
itst0	e1/t1	version(5:0)					

itst3 Status ITST3 pin
- 0 external pin low (normal operation mode)
- 1 external pin high

itst0 Status $\overline{\text{ITST0}}$ pin
- 0 external pin low
- 1 external pin high (normal operation mode)

e1/t1 Status E1/$\overline{\text{T1}}$ pin
- 0 external pin low : T1 (1.544 kbit/s) mode
- 1 external pin high : E1 (2.048 kbit/s) mode

version(5:0) Version of IWE8
Value of 001 001 for Version 1.1

4.2.14.1 Clock Monitor Register (ckmo)

Read Address 17_H
Value after reset: 0000_H

15							8
Not used							
7							**0**
frclk_failure(7:0)							

frclk_failure(7:0) FRCLK clock failure on port(7:0)

0 No clock failure
1 Clock failure

Note: The clock failure indication is instantaneous. If the failure disappears the status is not remembered.

4.2.15 Interrupt Status Register 1 (isr1)

Read Address 18_H
Value after reset: 0000_H

15							8
iq_ ne	eis4	eis3	eis2	eis1	oq_par	eq_par	rm1_par
7							**0**
rm3_par	rm2_par	utx_par	ex_par	crv_par	oq_ovf	eq_ovf	ck_eme

iq_ne	Interrupt queue not empty
eis4	A bit is set in eis4 (16 bits)
eis3	A bit is set in eis3 (8 bits)
eis2	A bit is set in eis2 (8 bits)
eis1	A bit is set in eis1 (8 bits)
oq_par	Parity error on internal RAM output queue
eq_par	Parity error on internal RAM event queue
rm1_par	Parity error on internal configuration RAM1
rm3_par	Parity error on internal configuration RAM3
rm2_par	Parity error on internal configuration RAM2
utx_par	Parity error on UTOPIA transmit bus
ex_par	Parity error on external RAM

crv_par	Parity error on clock recovery interface
oq_ovf	Output queue overflow
eq_ovf	Error queue overflow
ck_eme	Emergency mode state change on one of the emergency mode enabled ports (see ckmo)

Note: In order to prevent external RAM parity errors the external RAM should be written completely during board initialization by the microprocessor.

Note: Bits 10:0 are used for tracing error events. They are set by the ASIC on the occurence of an error event pulse. They are reset by a microprocessor read operation (Destructive read).
Bits 15:11 are static status bits, they remain active only as long as their cause is active.

4.2.16 Extended Interrupt Status 1 Register (eis1)

Destructive read Address 19_H
Value after reset: 0000_H

15	8
Not used	
7	**0**
int_ram_par(7:0)	

Internal RAM parity errors

int_ram_par(7:0)	Internal RAM parity error 0 No parity error 1 Parity error
int_ram_par(7)	internal RAM : OR (Octet Receive processing)
int_ram_par(6)	internal RAM : OT (Octet Transmit processing) ram b
int_ram_par(5)	internal RAM : OT (Octet Transmit processing) ram a
int_ram_par(4)	internal RAM : CT (Cell Transmit)
int_ram_par(3)	internal RAM : UR (UTOPIA Receive) two cell buffer
int_ram_par(2)	internal RAM : UL (Upstream Loop) two cell buffer
int_ram_par(1)	internal RAM : DL (Downstream Loop) two cell buffer
int_ram_par(0)	internal RAM : UT (UTOPIA Transmit) two cell buffer

4.2.17 Extended Interrupt Status 2 Register (eis2)

Destructive read Address $1A_H$
Value after reset: 0000_H

15	8
Not used	

7	0
rts_overflow(7:0)	

rts_overflow(7:0) RTS buffer overflow port(7:0)

0 No RTS buffer overflow in clock recovery interface
1 RTS buffer overflow in clock recovery interface

Note: Only applicable for AAL ports (pcfN[p_atm] = 0) with SRTS enabled (pcfN[p_srts] = 1).

4.2.18 Extended Interrupt Status 3 Register (eis3)

Destructive read Address $1B_H$
Value after reset: 0000_H

15	8
Not used	

7	0
tim_set1_exp(7:0)	

tim_set1_exp(7:0) Timer set 1 expired timer(7:0)

0 No time-out
1 Time-out

4.2.19 Extended Interrupt Status 4 Register (eis4)

Destructive read Address $1B_H$
Value after reset: 0000_H

15	8
ocd_end(7:0)	
7	**0**
ocd_start(7:0)	

ocd_end(7:0) End of OCD (Out of cell delineation) state at port (7:0)
0 No event
1 ocd_end event occured

ocd_start(7:0) Start of OCD (Out of cell delineation) state at port (7:0)
0 No event
1 ocd_start event occured

Note: Only applicable for ATM ports (pcfN[p_atm] = 1).

4.2.20 Interrupt Status Register 2 (isr2)

Destructive read Address $1D_H$
Value after reset: 0000_H

15	8
Not used	
7	**0**
tim_set2_exp(7:0)	

tim_set2_exp(7:0) Timer set 2 expired timer(7:0)
0 No time-out
1 Time-out

4.3 Internal Configuration RAM's

The 3 internal 256 x 32 bit configuration RAM's (RAM1, RAM2 and RAM3) are used to assign the timeslots of the Framer Receive and Framer Transmit interfaces to ATM channels. For each port there are 32 entries. RAM1 is used to define the timeslots of the Framer Receive ports, and RAM2 and RAM3 are used to define the Framer Transmit ports

.

Word	Bit 31		0
255	Port 7	Slot 31	
224	Port 7	Slot 0	
223	Port 6	Slot 31	
64	Port 2	Slot 0	
63	Port 1	Slot 31	
32	Port 1	Slot 0	
31	Port 0	Slot 31	
0	Port 0	Slot 0	

Figure 24 Structure of internal configuration RAM's

For AAL ports with CES - Nx64 kbit/s service, the timeslots are grouped into channels containing N of the 32 timeslots. The first timeslot of the channel is referred to as the *AAL reference slot*. The other N-1 timeslots of the channel are called *AAL continuation slots*. Those timeslots of a port that do not belong to any channel are called *idle slots*.

For AAL ports with CES - unstructured service, there is no notion of timeslots. In this case it is only necessary to program slot 0 of the port as an AAL reference slot.

For ATM ports, ATM cells are mapped in one group of N timeslots. The first timeslot used is the reference slot, while the other used timeslots are continuation slots. The unused slots are idle slots.

To comply with ITU-T G.804 the following ATM cell mapping should be used :
- for E1 ports : timeslot 0 and 16 have to be programmed as ‘Idle Slot’, timeslot 1 is the ‘ATM Reference Slot’ and all other timeslots are ‘ATM Continuation Slots’.
- for T1 ports : timeslots 0, 4, 8, 12, 16, 20, 24 and 28 have to be programmed as ‘Idle Slot’, timeslot 1 is the ‘ATM Reference Slot’ and all other timeslots are ‘ATM Continuation Slots’.

It is however possible to define other ATM cell mappings, e.g. ATM cells in a 64 kbit/s channel.

The two LSB bits of a slot entry identify the slot type :

Slot Type	Bit 1	Bit 0
Idle	0	0
Continuation	1	0
Reference	X	1

Figure 25 Coding of Slot Type in internal configuration RAM’s

4.3.1 RAM1 : Receive Port Configuration

4.3.1.1 RAM1 : ATM Receive Reference Slot

Read/write Address 00200_H to $003FF_H$
Value after reset: Not applicable. RAM must be initialized via SW.

31						24
Not used						
23						**16**
Not used						
15						**8**
Not used						
7						**0**
ocd_start _intrpt	ocd_end _intrpt	go_hunt	delete_ idle_cells	x43_ descram -bling	channel_mode(1:0)	ref_slot = 1

ocd_start_intrpt Generate interrupt when OCD state starts
- 0 No interrupt generated
- 1 Interrupt generated

ocd_end_intrpt Generate interrupt when OCD state ends
- 0 No interrupt generated
- 1 Interrupt generated

go_hunt Go to hunt state
- 0 Cell delineation finite state machine normal operation
- 1 Cell delineation finite state machine forced in hunt state Only the transition 0 → 1 forces the hunt state. Counter (number of times SYNC state is left) is *not* incremented. ocd_start interrupt is *not* generated.

delete_idle_cells Delete idle/unassigned cells enable
- 0 Deletion of idle/unassigned cells disabled
- 1 Deletion of idle/unassigned cells enabled

x43_descrambling ATM cell payload descrambling enable
- 0 ATM cell payload descrambling disabled
- 1 ATM cell payload descrambling enabled

channel_mode(1:0) Channel mode

- 00 Inactive mode
- 01 Active mode (normal mode)
- 10 Standby mode
- 11 Active mode (normal mode)

ref_slot Reference slot indicator

- 1 This slot is a reference slot

Note: To allow IWE8 internal channel initialization, the channel_mode must remain inactive for at least 250 µsec *after* activation of the port (i.e. after setting pcfN[p_rx_act] = 1).

4.3.1.2 RAM1 : ATM Receive Continuation Slot

Read/write Address 00200_H to $003FF_H$
Value after reset: Not applicable. RAM must be initialized via SW.

31 … 24	23 … 16	15 … 8	7	6 … 1	0
Not used	Not used	Not used	Not used	ref_slot_nr(4:0)	cont_slot = 1	ref_slot = 0

ref_slot_nr(4:0) Reference slot number

- (4:0) Number of the reference slot

cont_slot Continuation slot indicator

- 1 This slot is a continuation slot

ref_slot Reference slot indicator

- 0 This slot is not a reference slot

4.3.1.3 RAM1 : AAL Receive Reference Slot

Read/write Address 00200_H to $003FF_H$
Value after reset: Not applicable. RAM must be initialized via SW.

31							24
next_slot_nr(4:0)					sdt_mfs	sdt_ double_ mfs	srts
23							**16**
subst-bpslct(1:0)		dcor	dcor_random_nr(4:0)				
15							**8**
aal0	part_fill(5:0)						band_ width (4)
7							**0**
band_width(3:0)				sdt	channel_mode(1:0)		ref_slot = 1

next_slot_nr(4:0) Next slot number
- X If pcfN[p_ces] = 1
- (4:0) Number of the second slot in the channel

sdt_mfs Start of structure pulse select
- X If [sdt] = 0 or pcfN[p_ces] = 1 or [aal0] = 1
- 0 Start of structure is frame pulse
- 1 Start of structure is multiframe pulse

sdt_double_mfs Start of structure double pulse select
- X If [sdt] = 0 or if pcfN[p_ces] = 1 or if [aal0] = 1
- 0 Start of structure is every pulse
- 1 Start of structure is every second pulse

srts srts enable
- X If pcfN[p_srts] = 0 or [aal0] = 1
- 0 srts disabled
- 1 srts enabled if pcfN[p_srts] = 1

Note: Only 1 channel per port may have [srts] set to 1.

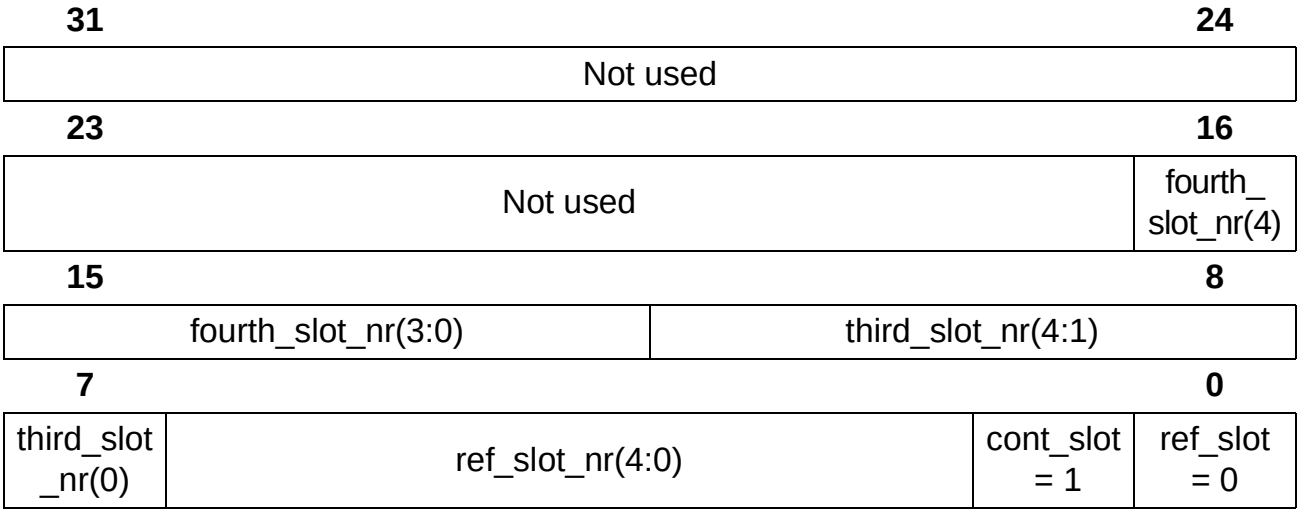
subst-bpslct Substitute byte-pattern select
- 00 Select byte-pattern 0, defined in bp10[bp0]
- 01 Select byte-pattern 1, defined in bp10[bp1]
- 10 Select byte-pattern 2, defined in bp32[bp2]
- 11 Select byte-pattern 3, defined in bp32[bp3]

dcor	Decorrelation circuit enable	
	0	Decorrelation circuit disabled
	1	Decorrelation circuit enabled
dcor_random_nr(4:0)	Decorrelation random Number	
	X	if [dcor] = 0
	(4:0)	Random value
aal0	AAL0 enable	
	0	AAL0 disabled (AAL1 is used)
	1	AAL0 enabled (instead of AAL1)
part_fill(5:0)	Partially filled cell filling level	
	< 4 or > 48	*Illegal* value, will be replaced by fully filled cells
	4 … 46(47)	Partially filled cells for AAL1 (AAL0)
	47	Fully filled cells for AAL1 (with SDT and pointer, cell may have only 46 user data octets)
	48	Fully filled cells for AAL0
band_width(4:0)	band_with = N - 1 (with N = number of timeslots for 1 channel)	
	0 … 31	For N = 1 to 32
	31	if pcfN[p_ces} = 1 the band_width should be all 1’s
sdt	Structured Data Transfer enable	
	X	If pcfN[p_ces] = 1 or [aal0] = 1
	0	SDT disabled
	1	SDT enabled
channel_mode(1:0)	Channel mode	
	00	Inactive mode
	01	Active mode (normal mode)
	10	Standby mode
	11	Substitute mode
ref_slot	Reference slot indicator	
	1	This slot is a reference slot

Note: To allow IWE8 internal channel initialization, all channels must remain in inactive mode at least 250 µsec *after* activation of the port (i.e. setting pcfN[p_rx_act] = 1).

4.3.1.4 RAM1 : AAL Receive Continuation Slot

Read/write Address 00200_H to $003FF_H$
Value after reset: Not applicable. RAM must be initialized via SW.



fourth_slot_nr(4:0) Fourth slot number
X If [band_width] < 3
(4:0) Number of the fourth slot in the channel

third_slot_nr(4:0) Third slot number
X If [band_width] < 3
(4:0) Number of the third slot in the channel

ref_slot_nr(4:0) Reference slot number
(4:0) Number of the reference slot

cont_slot Continuation slot indicator
1 This slot is a continuation slot

ref_slot Reference slot indicator
0 This slot is not a reference slot

4.3.1.5 RAM1 : ATM or AAL Receive Idle Slot

Read/write Address 00200_H to $003FF_H$
Value after reset: Not applicable. RAM must be initialized via SW.

31							24
Not used							
23							**16**
Not used							
15							**8**
Not used							
7							**0**
Not used						cont_slot = 0	ref_slot = 0

cont_slot Continuation slot indicator
1 This slot is not a continuation slot

ref_slot Reference slot indicator
0 This slot is not a reference slot

4.3.2 RAM2 : Transmit Port Configuration

4.3.2.1 RAM2 : ATM Transmit Reference Slot

Read/write Address 00400_H to $005FF_H$
Value after reset: Not applicable. RAM must be initialized via SW.

31			24
Not used			
23			**16**
Not used			
15			**8**
Not used			
7			**0**
Not used	x43_ scram-bli ng	channel_mode(1:0)	ref_slot = 1

x43_scrambling ATM cell payload scrambling enable
- 0 ATM cell payload scrambling disabled
- 1 ATM cell payload scrambling enabled

channel_mode(1:0) Channel mode
- 00 Inactive mode
- 01 Active mode (normal mode)
- 10 Standby mode
- 11 Active mode (normal mode)

ref_slot Reference slot indicator
- 1 This slot is a reference slot

Note: To allow IWE8 internal channel initialization, the channel_mode must remain inactive for at least 250 µsec *after* activation of the port (i.e. after setting pcfN[p_tx_act] = 1).

4.3.2.2 RAM2 : ATM Transmit Continuation Slot

Read/write Address 00400_H to $005FF_H$
Value after reset: Not applicable. RAM must be initialized via SW.

31			24
next_slot_nr(4:0) = 00000			Not used
23			**16**
Not used			
15			**8**
Not used			
7			**0**
Not used	ref_slot_nr(4:0)	cont_slot = 1	ref_slot = 0

next_slot_nr(4:0) Next slot number
00000 This field must be all 0 for ATM continuation slots

ref_slot_nr(4:0) Reference slot number
(4:0) Number of the reference slot

cont_slot Continuation slot indicator
1 This slot is a continuation slot

ref_slot Reference slot indicator
0 This slot is not a reference slot

4.3.2.3 RAM2 : AAL Transmit Reference Slot

Read/write Address 00400_H to $005FF_H$
Value after reset: Not applicable. RAM must be initialized via SW.

31						24
next_slot_nr(4:0)				Not used	snp_ check	sn_ check
23						**16**
sc_fast	sdt_mfs	sdt_oos_nr(1:0)	sdt_par	sdt_once	crv_en	mcp_ reinit
15						**8**
aal0	part_fill(5:0)					Not used
7						**0**
Not used			sdt	channel_mode(1:0)		ref_slot = 1

next_slot_nr(4:0) Next slot number

X If pcfN[p_ces] = 1

(4:0) Number of the second slot in the channel
If the current slot is the last slot in the channel (64 kbit/s channel) next_slot_nr must be equal to the current slot number (= ref_slot_nr).

snp_check SNP field check enable

X If [aal0] = 1 or [sn_check] = 0

0 SNP field check disabled

1 SNP field check enabled

sn_check SN field check enable

X If [aal0] = 1

0 SN field check disabled

1 SN field check enabled

sc_fast SC algorithm select

X If [aal0] = 1 or [sn_check] = 0

0 Standard SC algorithm enabled

1 Fast SC algorithm enabled

sdt_mfs — Start of structure pulse select

- X — If [aal0] = 1 or [sdt] = 0
- 0 — Start of structure is frame pulse
- 1 — Start of structure is multiframe pulse

sdt_oos_nr(1:0) — Number of SDT out of sync errors before re-initialization buffer

- X — If [aal0] = 1 or [sdt] = 0
- 00 — Re-initialize after 1 out of sync error
- 01 — Re-initialize after 2 out of sync error
- 10 — Re-initialize after 3 out of sync error
- 11 — Not allowed, IWE8 will not be able to re-initialize

sdt_par — SDT pointer parity check enable

- X — If [aal0] = 1 or [sdt] = 0
- 0 — SDT pointer parity check disabled
- 1 — SDT pointer parity check enabled

sdt_once — SDT pointer appears once in 8 cell cycle

- X — If [aal0] = 1 or [sdt] = 0
- 0 — All cells with CSI bit = 1 are supposed to contain a P format SAR-PDU payload.
- 1 — Only the first cell with CSI bit = 1 in a cycle of 8 cells is supposed to contain a P format SAR-PDU payload.

crv_en — Data to Clock Recovery interface enable (rts values and/or acm buffer filling levels)

- X — if pcfN[p_srts] = 0 or acfg[a_crv_en] = 0
- 0 — Data to Clock Recovery interface disabled
- 1 — Data to Clock Recovery interface enabled

Note: Only one channel per port may have crv_en set to 1.

mcp_reinit — Microprocessor forced reassembly buffer reinitialization

- 0 — Microprocessor forced reassembly buffer reinitialization disabled
- 1 — Microprocessor forced reassembly buffer reinitialization enabled
  The SW should set and reset this bit to continue proper operation.

aal0 — AAL0 enable

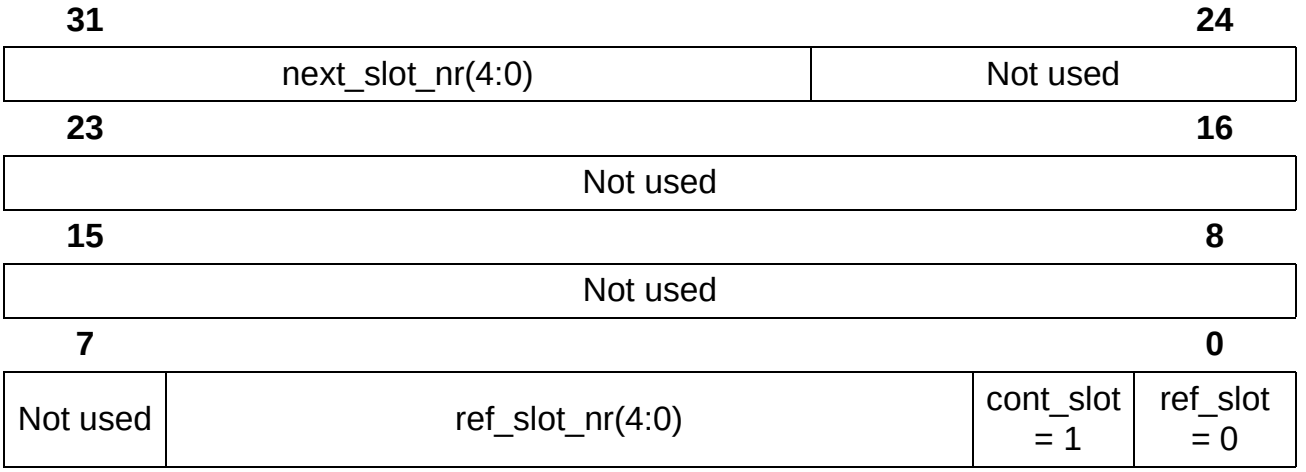
- 0 — AAL0 disabled (AAL1 is used)
- 1 — AAL0 enabled (instead of AAL1)

part_fill(5:0)	Partially filled cell filling level	
	< 4 or > 48	*Illegal* value, will be replaced by completely filled cells
	4 … 46(47)	Partially filled cells for AAL1 (AAL0)
	47	Completely filled cells for AAL1 (with SDT pointer some cells will have only 46 user data octets)
	48	Completely filled cells for AAL0
sdt	Structured Data Transfer enable	
	X	If pcfN[p_ces] = 1 or [aal0] = 1
	0	SDT disabled
	1	SDT enabled
channel_mode(1:0)	Channel mode	
	00	Inactive mode
	01	Active mode (normal mode)
	10	Standby mode
	11	Active mode (normal mode)
ref_slot	Reference slot indicator	
	1	This slot is a reference slot

Note: To allow IWE8 internal channel initialization, all channels must remain in inactive mode at least 250 µsec *after* activation of the port (i.e. setting pcfN[p_rx_act] = 1).

4.3.2.4 RAM2 : AAL Transmit Continuation Slot

Read/write Address 00400_H to $005FF_H$
Value after reset: Not applicable. RAM must be initialized via SW.



next_slot_nr(4:0) Next slot number

(4:0) Number of the next slot in the channel
If the current slot is the last slot of the channel next_slot_nr must be equal to the reference slot number.

ref_slot_nr(4:0) Reference slot number

(4:0) Number of the reference slot

cont_slot Continuation slot indicator

1 This is a continuation slot

ref_slot Reference slot indicator

0 This slot is not a reference slot

4.3.2.5 RAM2 : ATM or AAL Transmit Idle Slot

Read/write Address 00400_H to $005FF_H$
Value after reset: Not applicable. RAM must be initialized via SW.

31			24
Not used			
23			**16**
Not used			
15			**8**
Not used			idle_ bpslct(1)
7			**0**
idle_ bpslct(0)	Not used	cont_slot = 0	ref_slot = 0

idle_bpslct(1:0) Idle slot byte-pattern select
- 00 select byte-pattern 0, defined in bp10[bp0]
- 01 select byte-pattern 1, defined in bp10[bp1]
- 10 select byte-pattern 2, defined in bp32[bp2]
- 11 select byte-pattern 3, defined in bp32[bp3]

cont_slot Continuation slot indicator
- 0 This is not a continuation slot

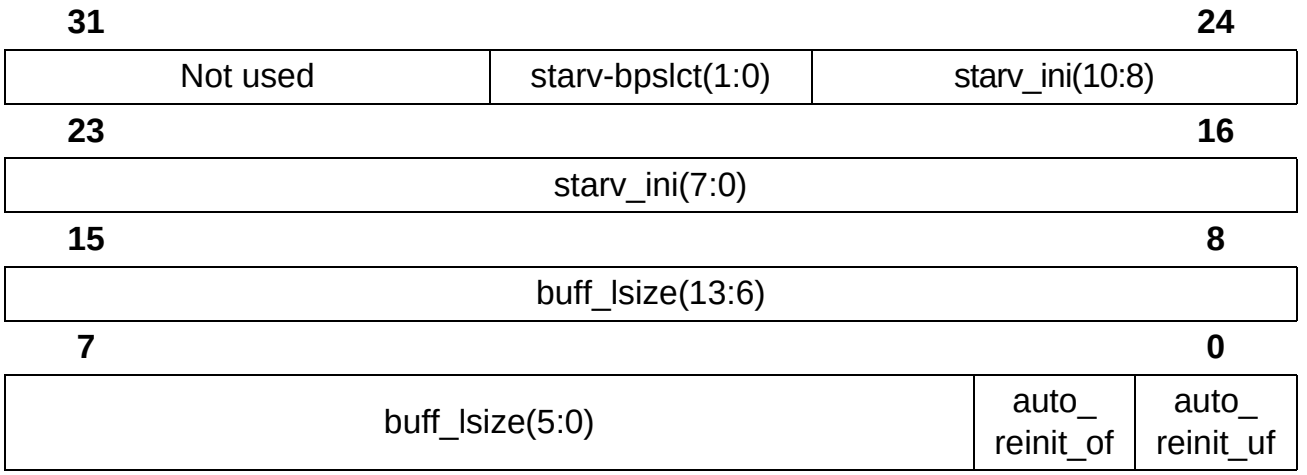
ref_slot Reference slot indicator
- 0 This slot is not a reference slot

4.3.3 RAM3 : Transmit Port Configuration Extended

RAM3 needs only to be programmed in the case of an 'AAL Transmit Reference Slot'. In all other cases the RAM3 entry is don't care.

4.3.3.1 RAM3 : AAL Transmit Reference Slot

Read/write Address 00600_H to $007FF_H$
Value after reset: Not applicable. RAM must be initialized via SW.



starv-bpslct(1:0) Starvation byte-pattern select
- 00 Select byte-pattern 0, defined in bp10[bp0]
- 01 Select byte-pattern 1, defined in bp10[bp1]
- 10 Select byte-pattern 2, defined in bp32[bp2]
- 11 Select byte-pattern 3, defined in bp32[bp3]

starv_ini(10:0) Number of starvation octets sent at reassembly buffer initialization (actual number of octets sent = starv_ini + 1 octet)

buff_lsize(13:0) Logical size of reassembly buffer in octets

auto_reinit_of automatic reassembly buffer reinitialization at overflow
- X If [aal0] =1
- 0 µP controlled reassembly buffer initialization
- 1 automatic reassembly buffer initialization

auto_reinit_uf automatic reassembly buffer reinitialization at underflow
- X If [aal0] = 1
- 0 µP controlled reassembly buffer initialization
- 1 automatic reassembly buffer initialization

4.4 External RAM

The IWE8 requires an external 64K × 32 bit RAM. A 33th bit is added for parity.

Figure 26 shows the structure of the external RAM.

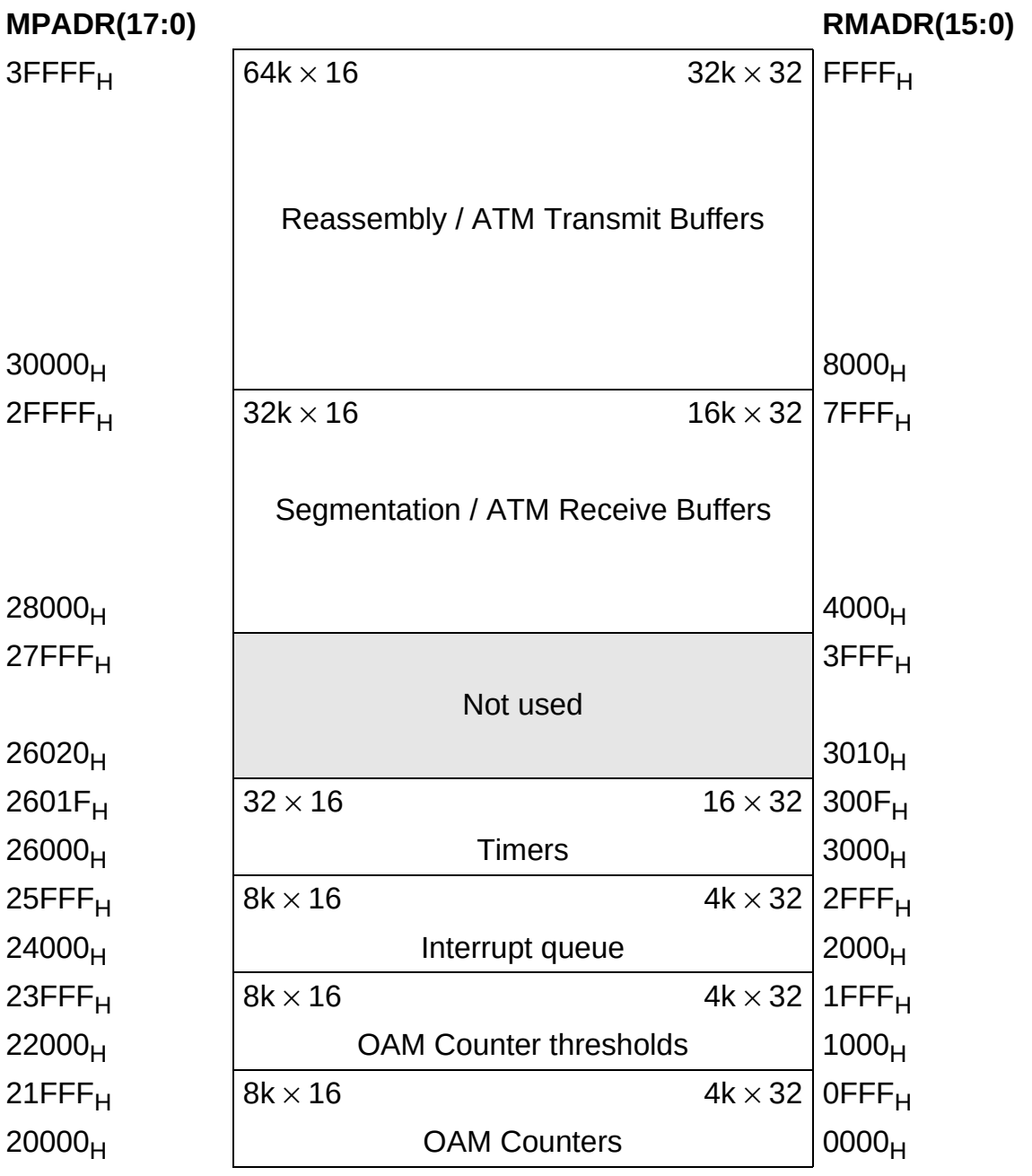


Figure 26 Structure of the IWE8 external RAM

4.4.1 OAM Counters

Memory size: 4k × 32 bits : 8 ports x 32 channels x 16 counters

RMADR		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
MPADR	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	0	0	0	0	Port_nr (3:0)			Channel_nr (4:0)					Counter_nr (3:0)				0

Table 23 OAM counters for ATM ports [1)]

Counter_nr	Counter contents
0 [2)]	Number of discarded cells due to output queue, ATM receive buffer or segmentation buffer overflow
1	Number of received cells with correctable HEC errors
2	Number of received cells with non-correctable HEC errors
3	Number of times cell delineation SYNC state is left, except when forced by the processor
4	Number of discarded cells due to ATM transmit buffer overflow
5	Not used
6	Not used
7	Not used
8	Not used
9	Not used
10	Not used
11	Not used
12	Not used
13	Not used
14	Not used
15	Not used

1) For ATM ports, the counters are located in channel_nr = 00000

2) Counter_nr 0 is common to all ports and is located in port_nr = 111 channel_nr = 11111

Table 24 OAM counters for AAL ports[1)]

Counter_nr	Counter contents
0 [2)]	Number of discarded cells due to output queue, ATM receive buffer or segmentation buffer overflow
1	Not used
2	Not used
3	Number of times SDT start of structure changes phase upstream (AAL1)
4	Number of discarded downstream cells (AAL1) or misinserted cells (AAL0) due to reassembly buffer overflow
5	Number of end of reassembly buffer overflow (AAL0 & AAL1)
6	Number of downstream cells with invalid SN/SNP (AAL1)
7	Number of SC out of sequence (AAL1)
8	Number of downstream ‘misinserted cells’ detected by SC algorithm (AAL1)
9	Number of downstream cells discarded by SC algorithm
10	Number of rejected SDT pointers due to parity error (AAL1)
11	Number of SC cycles with no SDT pointer field or more than one pointer field (AAL1)
12	Number of end of reassembly buffer underflow (AAL0 & AAL1)
13	Number of inserted starvation cells (AAL0 & AAL1) due to reassembly buffer underflow
14	Number of times ATM start of structure out of sync with port start of structure (AAL1)
15	Number of downstream ‘lost cells’ detected by SC algorithm (AAL1)

1) For AAL ports with CES-unstructured service, the counters are located in channel_nr = 00000

2) Counter_nr 0 is common for all ports and is located in port_nr = 111 channel_nr = 11111

The OAM counters are incremented when the channel_mode is active or standby, and when the corresponding enable bit in the catm or caal register is set.

The format of the counter entries is as follows :

31	30 ... 0
int_gen	count_value(30:0)

int_gen interrupt queue entry generated

0 no interrupt queue entry was generated for this counter
1 an interrupt queue entry was generated for this counter

Note: Only one interrupt queue entry per counter can be generated.

count_value(30:0) counter value

4000 maximum count_value
0000_H the counter will not increment beyond this value
count_value(30) = 1 indicates maximum counter_value

4.4.2 OAM Counter thresholds

Memory size: 4k × 32 bits : 8 ports x 32 channels x 16 counter thresholds

RMADR		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
MPADR	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	0	0	0	1	Port_nr (3:0)			Channel_nr (4:0)					Counter_nr (3:0)				0

The format of the counter threshold entries is as follows :

31	30 ... 0
thres_act	thres_value(30:0)

thres_act threshold active

0 counter threshold is not active
1 counter threshold is active

thres_value(30:0) threshold value

4000 thresholds beyond this value will never create an
0000_H interrupt queue entry as the counter stops at 4000 0000_H

4.4.3 Interrupt queue

Memory size: 4k × 32 bits

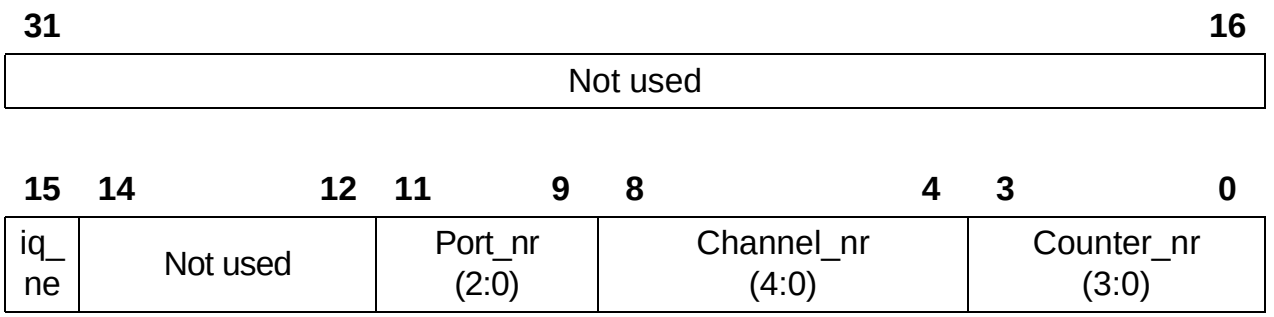
RMADR		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
MPADR	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	0	0	1	0	interrupt_queue_addr(11:0)												0

When the OAM function is disabled (register oamc[oam_act] = 0), the µP can read and write all addresses of the interrupt queue.

When the OAM function is enabled (register oamc[oam_act] = 1), the interrupt queue address lines to the external RAM RMADR11-0 are generated by the OAM function. For the µP, the interrupt queue address lines MPADR12-1 are don't care while reading the interrupt queue. The OAM function will automatically provide the first queue entry to the µP data bus.

Each interrupt queue entry identifies a particular OAM counter that has reached its threshold value. The counter is identified by its port_nr, channel_nr and counter_nr.

The format of the interrupt queue entries is as follows :



iq_ne interrupt queue not empty

0 interrupt queue is empty, no further entries

1 interrupt queue is not empty, further entries can be read

4.4.4 Timers

Memory size: 16 × 32 bit timers

RMADR		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
MPADR	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	0	0	1	1	0	0	0	0	0	0	0	0	timer_nr (3:0)				0

timer_nr Timer number

0..7 Timer set 2 : time-out generates an interrupt on MPIR2
8..15 Timer set 1 : time-out generates an interrupt on MPIR1

The format of the timer entries is as follows :

31 16	**15**	**14** **0**
Not used	timer_en	timer_value(14:0)

timer_en Timer enable

0 Timer disabled
1 Timer enabled

The SW should write an initial value in timer_value(14:0). If timer_en is set to 1, the timer_value will then be automatically decremented at equidistant intervals of 512 x 12 x T_{CLOCK} (i.e. 245.8 µS for a CLOCK of 25 Mhz). The timer_en bit can be used by the SW to pause the timer. When the timer expires, i.e. the timer value has reached all 0's, the IWE8 will automatically reset the timer_en bit to 0. The timer_value will decrement once more and stop at $7FFF_H$. An interrupt status bit will be set in isr1 for timer set 1 or in isr2 for timer set 2.

Note: Internal register bit oamc[tim_set1_en] = 0 will disable all timers in set 1.
Internal register bit time[tim_set2_en] = 0 will disable all timers in set 2.

4.4.5 Segmentation / ATM Receive Buffers

Memory size 16k × 32 bits : 8 ports x 32 channels x 4 cells x 16 doublewords

RMADR		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
MPADR	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	0	1	port_nr (2:0)			channel_nr (4:0)					cell_nr (1:0)		double_word (3:0)				0

For ATM ports the SW does not need to access the ‘ATM Receive Buffers’.

For AAL ports the ATM cell header to be used for each channel has to be programmed by the SW in the ‘Segmentation Buffer’ of the channel at the address given by :

101 & port_nr & channel_nr=reference_slot_nr & cell_nr=00 & double_word=0000

The Segmentation / ATM Receive Buffers is divided in 8 equal port-areas (1 area per port). Each port-area consists of 128 blocks of 16 Doublewords = 2.048 Doublewords.

The SW accesses only Doubleword 00 of cell number 0 of the packetising buffer (non-ATM payload). The SW should not access the packetising buffer (DW 01:15) or demapping buffer (DW 00:15) as the data changes continually.

ATM mode:

A cell is stored in a block of 16 Doublewords. Per port-area only the first 16 blocks are used.

Doubleword 00:4 ATM Header octets

d[31:28]:VCI [03:00]

d[27:25]:PTI [2:0]

d[24]:CLP

d[23:20]:VCI[11:08]

d[19:16]:VCI[07:04]

d[15:12]:VPI[03:00]

d[11:08]:VCI[15:12]

d[07:04]:GFC or VPI[11:08]

d[03:00]:VPI[07:04]

(HEC octet is not stored)

Doubleword 01: not used

Doubleword 02:13: cell payload

Doubleword 14:15: not used

Non-ATM mode:

A cell is stored in a block of 16 Doublewords or in a subblock of 8 Doublewords.

For CES mode: only the first 16 blocks of the port area are used.

For Nx64 Kbit/s: the port-area is divided into 32 equal block-groups of 4 blocks each. Each channel can occupy 1, 2 or 4 block-groups (4, 8 or 16 blocks). The first block-group is always the reference slot nr of the channel. The second, third and fourth block-groups used are always the number of the corresponding interface slots defining the channel

Doubleword 00:4 ATM Header octets (only cell number 0)

d[31:28]:VCI [03:00]

d[27:25]:PTI [2:0]

d[24]:CLP

d[23:20]:VCI[11:08]

d[19:16]:VCI[07:04]

d[15:12]:VPI[03:00]

d[11:08]:VCI[15:12]

d[07:04]:GFC or VPI[11:08]

d[03:00]:VPI[07:04]

(HEC octet is not stored)

Doubleword 01: 4 control octets

d[31:24]: don’t care

d[23]: AAL0

d[22]: SDT pointer field used

d[21:16]: cell filling level partially filled cells

d[15]: SDT offset parity

d[14:08]: SDT offset value

d[07]: CSI

d[06:04]: Sequence Count

d[03:01]: CRC-3

d[00]: Parity

If part_fill > 24 then a cell is stored in a block of 16 Doublewords

Doubleword 02:13 : cell payload

Doubleword 14:15: not used

If part_fill <= 24 then cell is stored in a subblock of 8 Doublewords

Doubleword 02:07 : cell payload.

4.4.6 Reassembly / ATM Transmit Buffers

Memory size 32k × 32 bits : 8 ports x 32 channels x 8 cells x 16 doublewords

RMADR		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
MPADR	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	1	port_nr (2:0)			channel_nr (4:0)					cell_nr (2:0)			double_word (3:0)				0

The SW does not need to access the ‘Reassembly or ATM Transmit Buffers’.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings and Recommended Operating Conditions

Table 25 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_{CC}	- 0.5 to 4.6	V
Input voltage	V_I	- 0.5 to V_{CC}+0.5	V
Output voltage	V_O	- 0.5 to V_{CC}+0.5	V
Storage temperature	T_{stg}	– 65 to 150	°C

Note: Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to "absolute maximum rating" conditions for extended periods may affect device reliability

Table 26 Recommended Operating Conditions

Parameter	Symbol	Limit Values		Unit
		Min	Max	
Supply voltage	V_{CC}	3.0	3.6	V
Input voltage	V_I	0	V_{CC}	V
Output voltage	V_O	0	V_{CC}	V
Input low voltage	V_{IL}	0	0.8	V
Input high voltage	V_{IH}	2.0	V_{CC}	V
Ambient temperature	T_A	0	70	°C

5.2 DC Characteristics

T_A = 0 to 70 °C , V_{CC} = 3.3 V ± 5 % , V_{SS} = 0 V

Table 27 DC Characteristics

Parameter	Symbol	Limit Value		Unit	Test Condition
		Min	Max		
Output low voltage	V_{OL}		0.4	V	I_{OL} = 4 mA , 8 mA [1]
Output high voltage	V_{OH}	V_{CC} - 0.6		V	I_{OH} = - 4 mA , - 8 mA [1]
Treshold voltage	V_T	0.8	2.0	V	
Low-level input current	I_{IL}		± 1	µA	$V_I = V_{IL(min)}$
High-level input current	I_{IL}		± 1	µA	$V_I = V_{IH(max)}$
High-impedance state output current	I_{OZ}		± 20	µA	
Input capacitance[2]	C_{IN}		10	pF	
Output capacitance[2]	C_{OUT}		15	pF	
Supply current	I_{CC}		375	mA	C_L = 50 pF F_{CLOCK} = 25 Mhz

[1] All Utopia output buffers are 8 mA.

[2] Not tested in production.

5.3 AC Characteristics

T_A = 0 to 70 °C , V_{CC} = 3.3 V ± 5 % , V_{SS} = 0 V

All inputs are driven to V_{IH} = 2.4 V for a logical “1”
and to V_{IL} = 0.4 V for a logical “0”

All outputs are measured at V_H = 2.0 V for a logical “1”
and at V_L = 0.8 V for a logical “0”

The AC testing input/output waveforms are shown below.

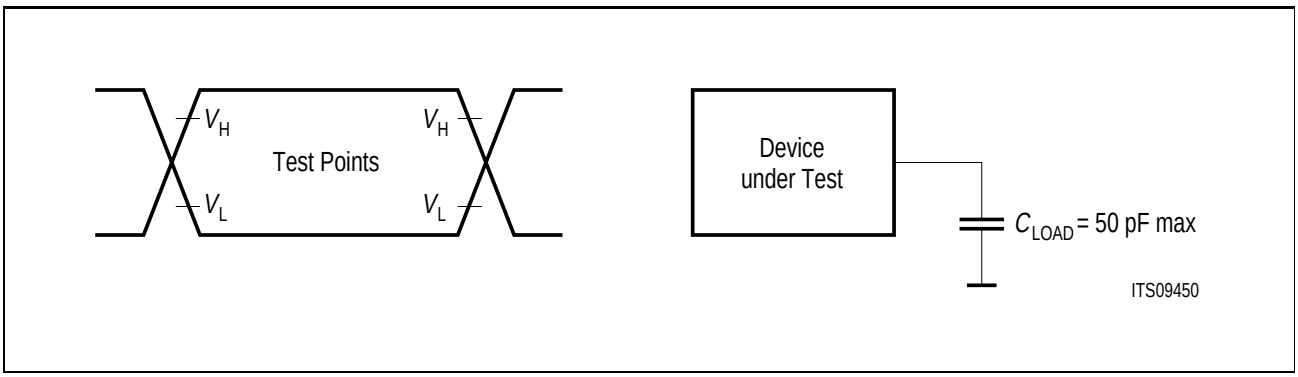


Figure 27
Input/Output waveform for AC measurements

5.3.1 Clock and reset interface

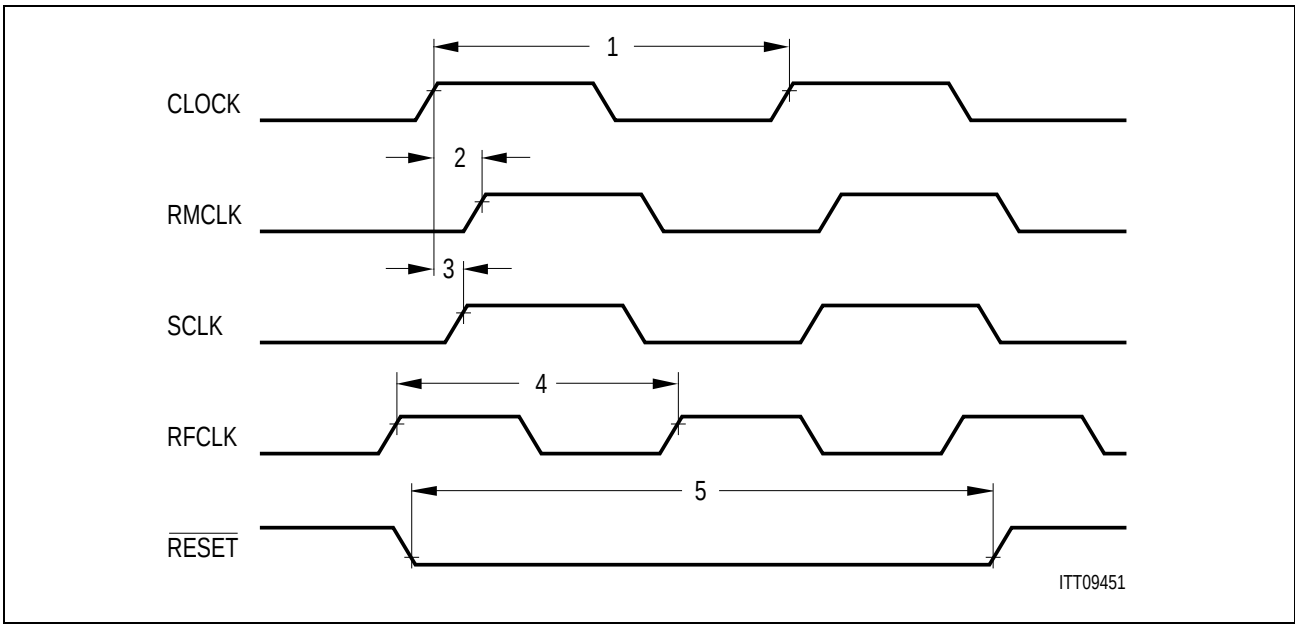


Figure 28
Clock and reset interface timing diagram

Table 28 Clock and reset interface AC timing characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{CLOCK} : Period CLOCK	38	40	T_{FRCLK} / 3 T_{FTCLK} / 3	ns
1A	F_{CLOCK} : Frequency CLOCK	3 xF_{FRCLK} 3 xF_{FTCLK}	25	26,3	Mhz
2	Delay CLOCK to RMCLK	2		12	ns
3	Delay CLOCK to SCLK	1		10	ns
4	T_{RFCLK} : Period RFCLK		T_{FRCLK} / 4 T_{FTCLK} / 4		ns
4A	F_{RFCLK} : Frequency RFCLK		4 xF_{FRCLK} 4 xF_{FTCLK}		Mhz
5	Pulse width $\overline{\text{RESET}}$ low	3 xT_{CLOCK}			

5.3.2 UTOPIA interface

UTOPIA receive interface

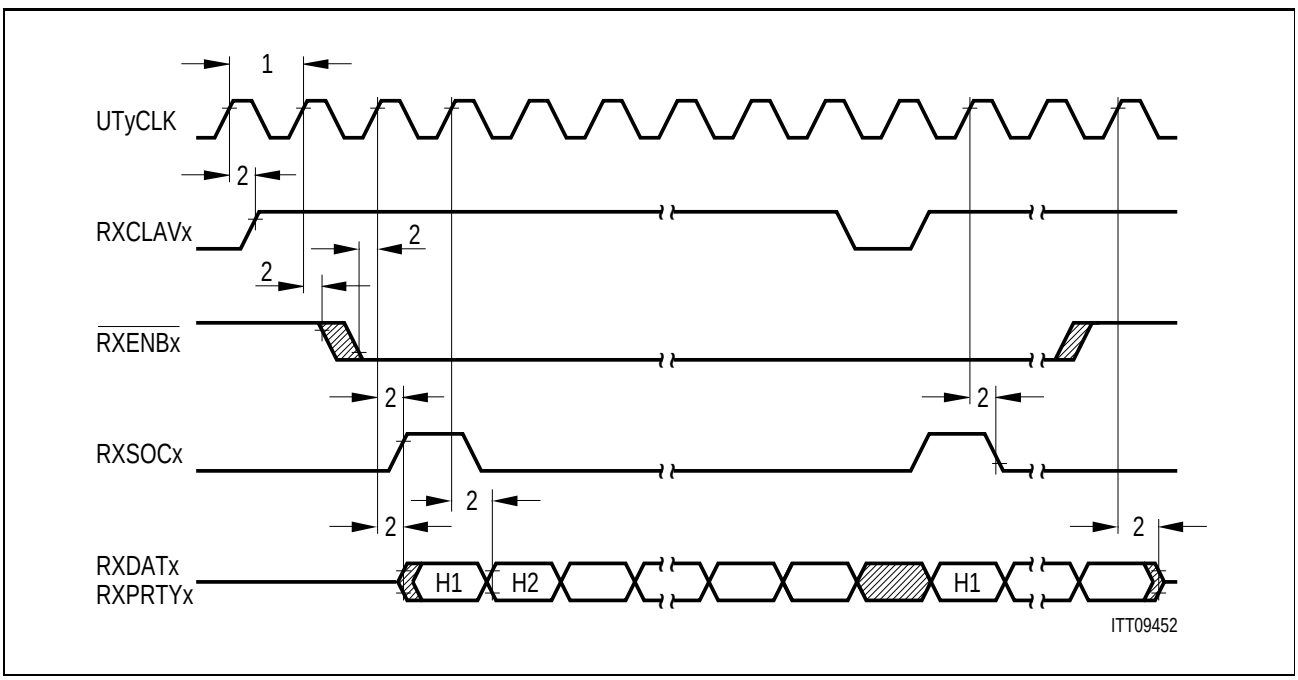


Figure 29
Utopia receive interface timing diagram

Table 29 Utopia receive interface AC timing characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{RXCLK} : Period RXCLK			40	ns
1A	F_{RXCLK} : Frequency RXCLK	0		25	Mhz
2	Delay RXCLK rising to RXCLAV, RXSOC, RXDAT and RXPTY	2		20	ns
3	Setup time $\overline{\text{RXENB}}$ before RXCLK rising	10			ns
4	Hold time $\overline{\text{RXENB}}$ after RXCLK rising	1			ns
5	Delay RXCLK rising to RXDAT and RXPTY low impedance	5		20	ns
6	Delay RXCLK rising to RXDAT and RXPTY high impedance	5		20	ns

UTOPIA transmit interface

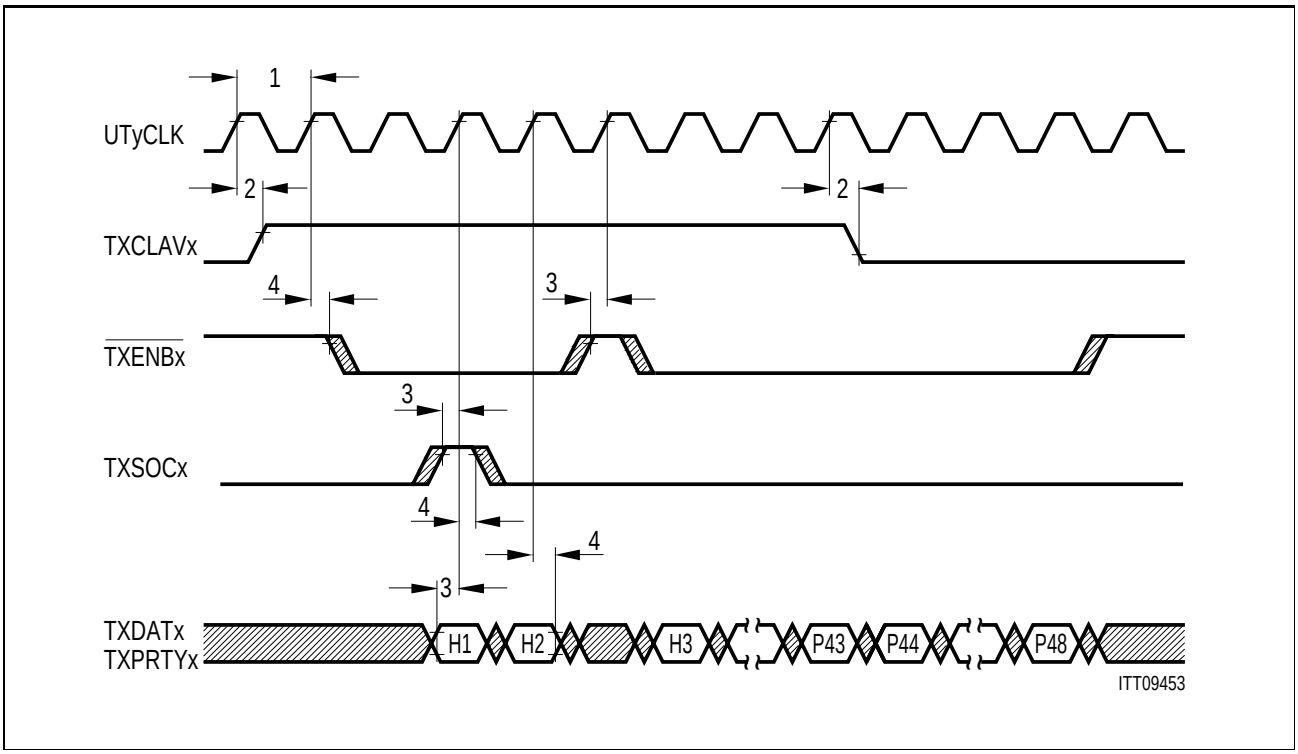


Figure 30
Utopia transmit interface timing diagram

Table 30 Utopia transmit interface AC timing characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{TXCLK} : Period TXCLK			40	ns
1A	F_{TXCLK} : Frequency TXCLK	0		25	Mhz
2	Delay TXCLK rising to TXCLAV	2		20	ns
3	Setup time $\overline{\text{TXENB}}$, TXSOC, TXDAT and TXPTY before TXCLK rising	10			ns
4	Hold time $\overline{\text{TXENB}}$, TXSOC, TXDAT and TXPTY after TXCLK rising	1			ns

5.3.3 RAM interface

The IWE8 has a fixed RAM interface cycle of 12 clock periods. A sequence of 6 consecutive read cycles (addresses AR1 to AR6), a dummy address cycle and 5 consecutive write cycles (addresses AW1 to AW5) is continuously repeated. The timing of $\overline{\text{RMADC}}$ and $\overline{\text{RMOE}}$ is always fixed as shown in figure 31. Whether the IWE8 actually reads data from the external RAM or writes data into the external RAM is controlled by the $\overline{\text{RMCS}}$ and $\overline{\text{RMWR}}$ signals. In the example shown in figure 31, data R1 and R3 are actually read by the IWE8, and data W1 and W3 are actually written into the extermal RAM.

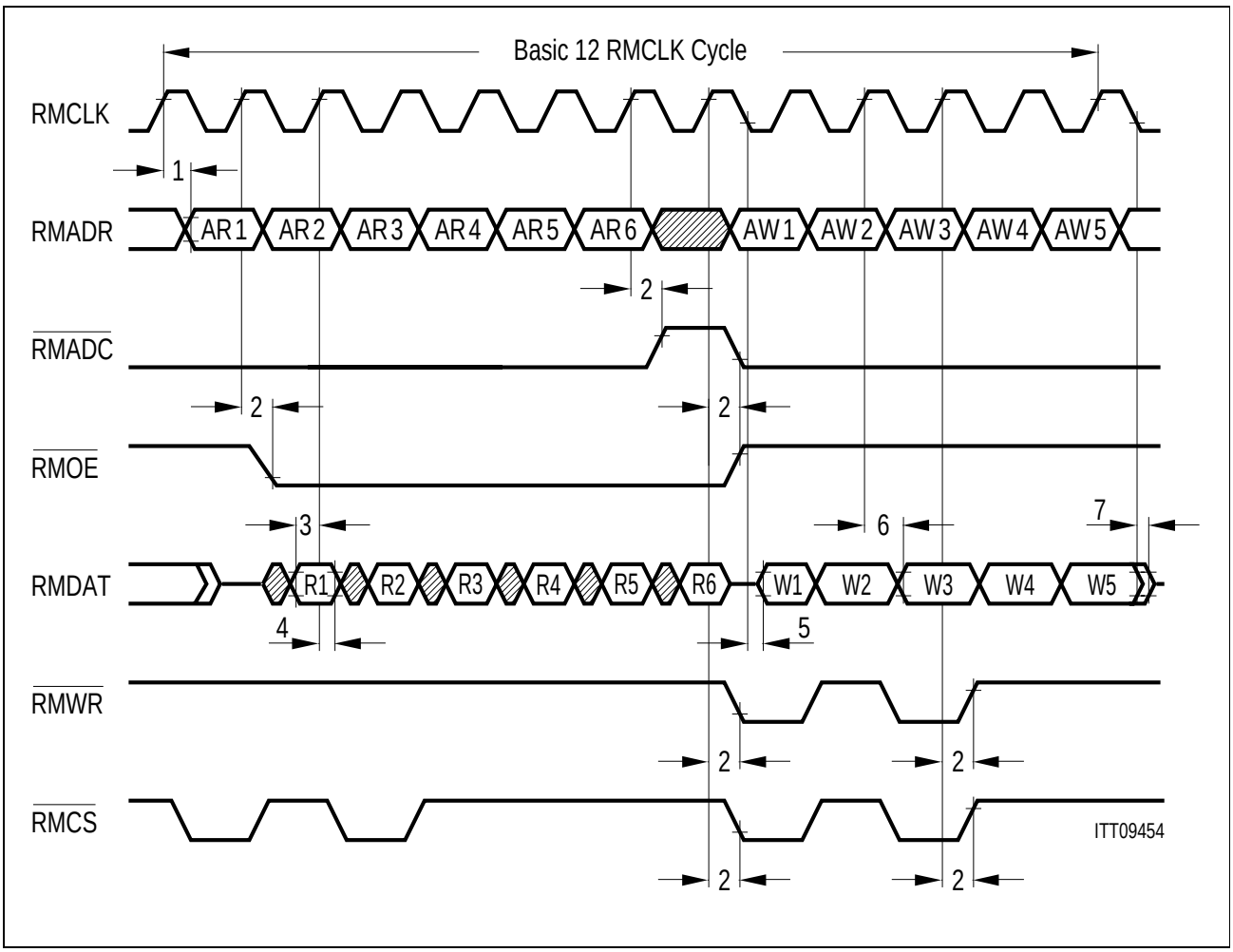


Figure 31
RAM interface timing diagram

Table 31 RAM interface AC timing characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	Delay RMCLK rising to RMADR	2		10	ns
2	Delay RMCLK rising to $\overline{\text{RMADC}}$, $\overline{\text{RMOE}}$, $\overline{\text{RMWR}}$, $\overline{\text{RMCS}}$	2		10	ns
3	Setup time RMDAT before RMCLK rising (all read cycles)	12			ns
4	Hold time RMDAT after RMCLK rising (all read cycles)	0			ns
5	Delay RMCLK falling to RMDAT low impedance (write cycle W1)	0		8	ns
6	Delay RMCLK rising to RMDAT (write cycles W2 to W5)	4		20	ns
7	Delay RMCLK falling to RMDAT high impedance (write cycle W5)	0		8	

5.3.4 Framer interface

Framer receive interface

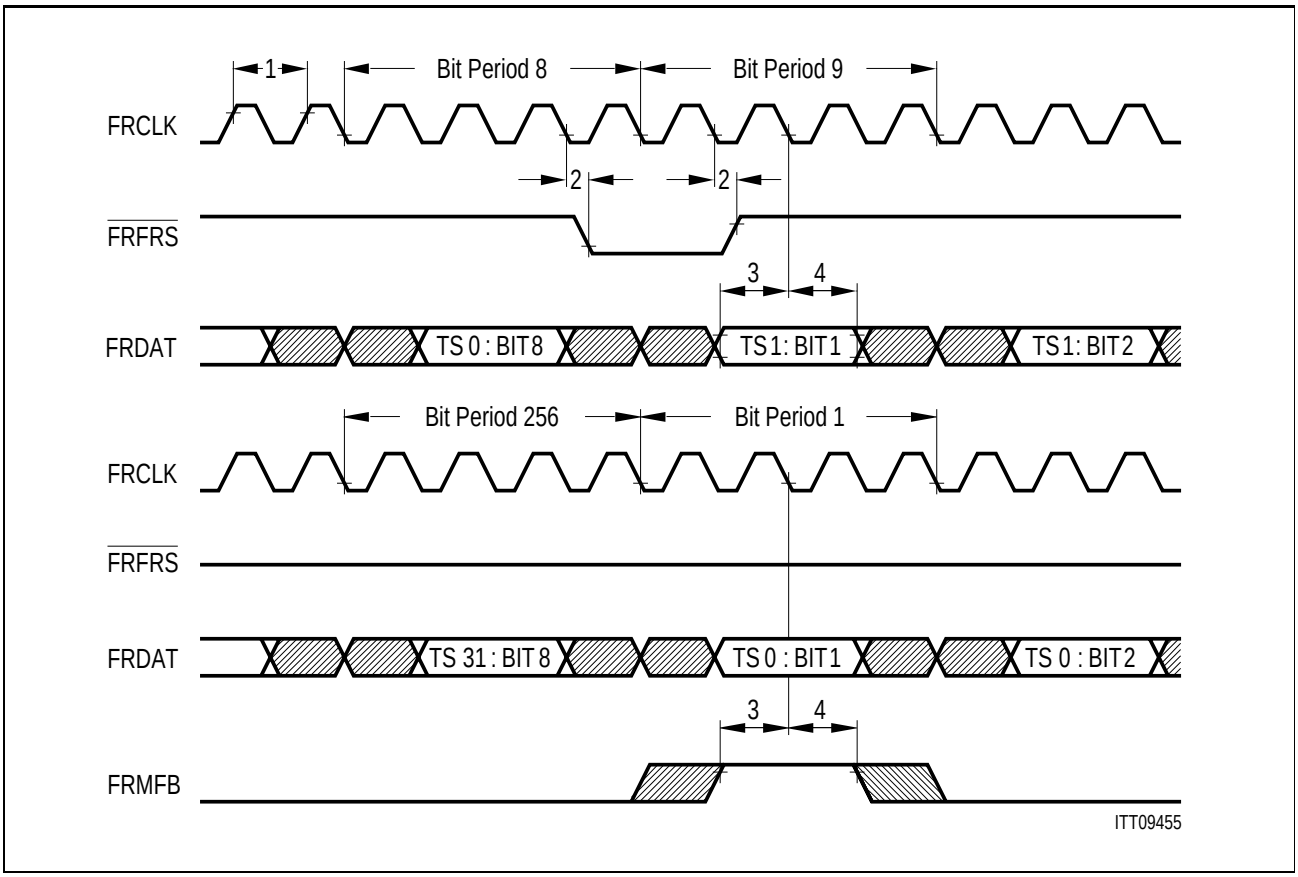


Figure 32
Framer receive interface timing diagram

Table 32 Framer receive interface AC timing characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{FRCLK} : Period FRCLK		122		ns
1A	F_{FRCLK} : Frequency FRCLK	*- 130 ppm*	8,192	*+130 ppm*	Mhz
2	Delay FRCLK falling to $\overline{FRFRS}$	3		20	ns

Table 32 Framer receive interface AC timing characteristics (cont'd)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
3	Setup time FRDAT and FRMFB before FRCLK falling (center of bit period)	150			ns
4	Hold time FRDAT and FRMFB after FRCLK falling (center of bit period)	150			ns

Framer transmit interface

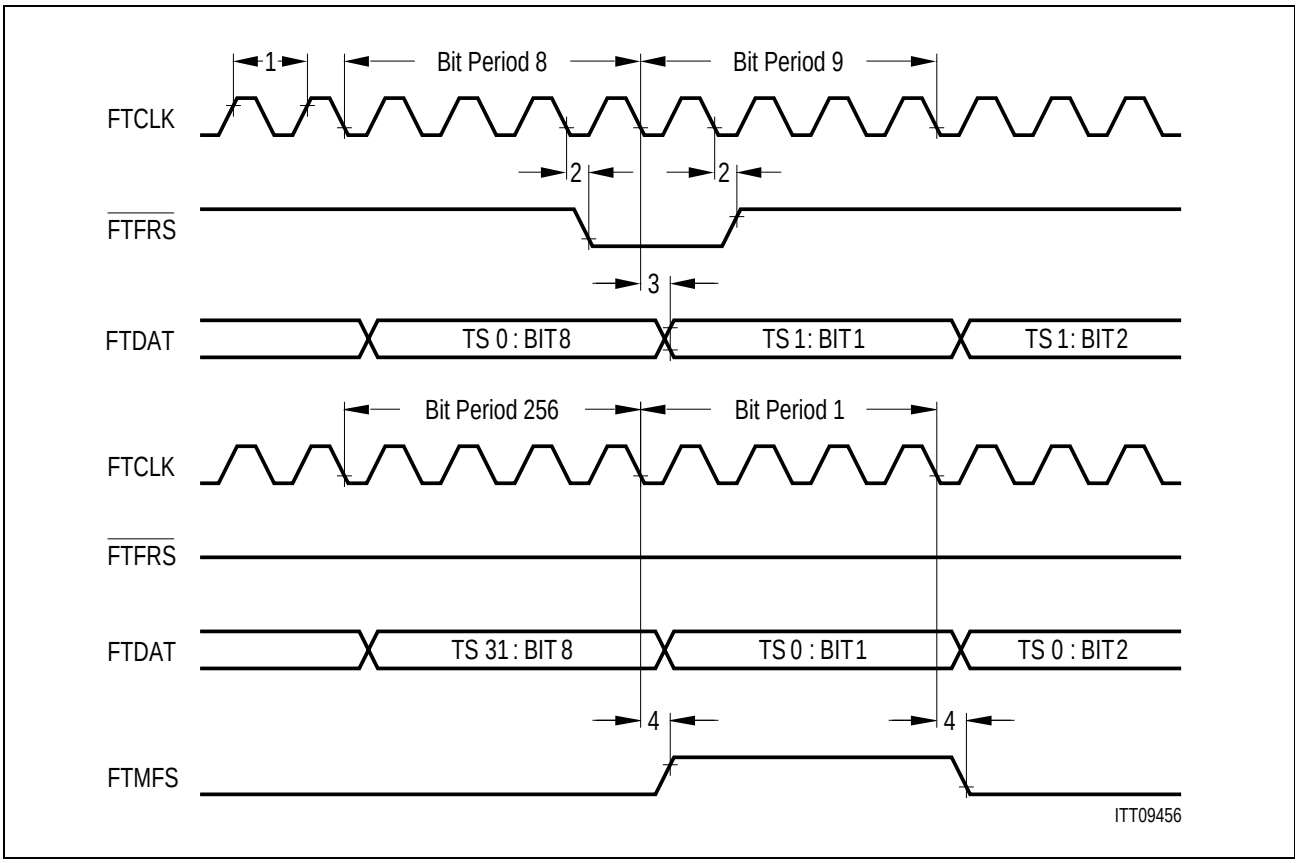


Figure 33
Framer transmit interface timing diagram

Table 33 Framer transmit interface AC timing characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{FTCLK} : Period FTCLK		122		ns
1A	F_{FTCLK} : Frequency FTCLK	*- 130 ppm*	8,192	*+130 ppm*	Mhz
2	Delay FTCLK falling to $\overline{FTFRS}$	3		20	ns
3	Delay FTCLK falling to FTDAT	3		20	ns
4	Delay FTCLK falling to FTMFB	3		20	ns

5.3.5 Microprocessor interface

Microprocessor write cycle

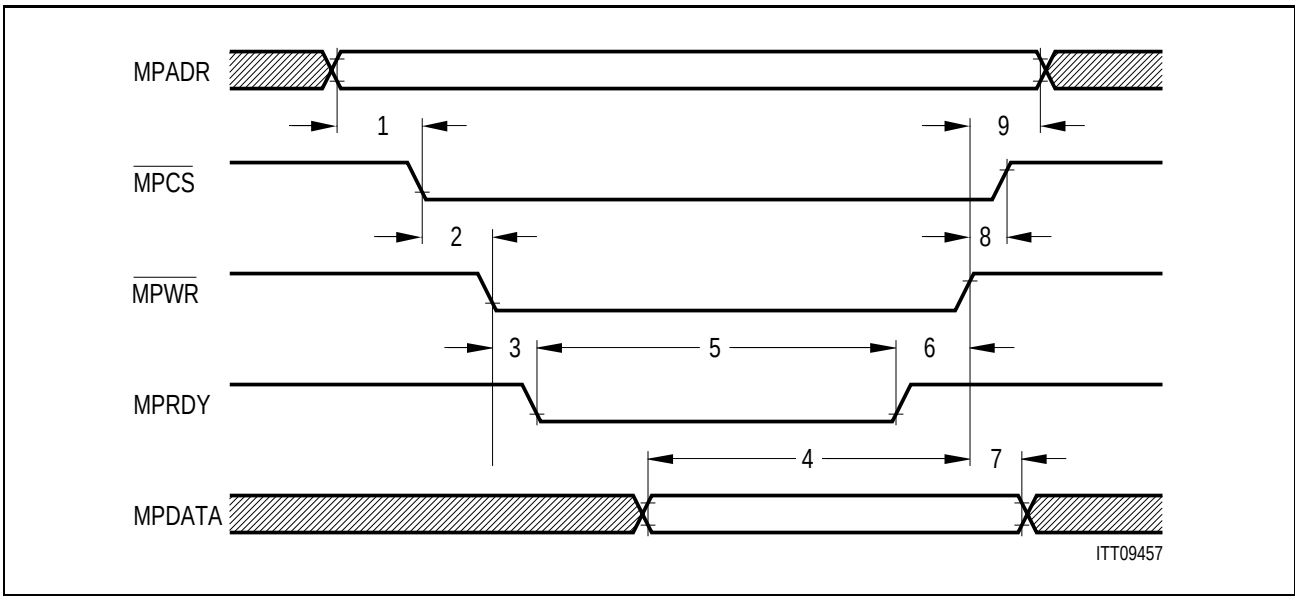


Figure 34
Microprocessor write cycle timing diagram

Table 34 Microprocessor write cycle AC timing characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	Setup time MPADR before $\overline{\text{MPCS}}$ low	0			ns
2	Setup time $\overline{\text{MPCS}}$ before $\overline{\text{MPWR}}$ low	0			ns
3	Delay MPRDY low after $\overline{\text{MPWR}}$ low	2		20	ns
4	MPDAT valid after $\overline{\text{MPWR}}$ low			2 x T_{clock}	ns
5	Pulse width MPRDY low	2 x T_{clock}		20 x T_{clock}	ns
6	MPRDY high to $\overline{\text{MPWR}}$ high	10			ns
7	Hold time MPDAT after $\overline{\text{MPWR}}$ high	5			ns
8	Hold time $\overline{\text{MPCS}}$ after $\overline{\text{MPWR}}$ high	5			ns
9	Hold time MPADR after $\overline{\text{MPWR}}$ high	5			ns

Microprocessor read cycle

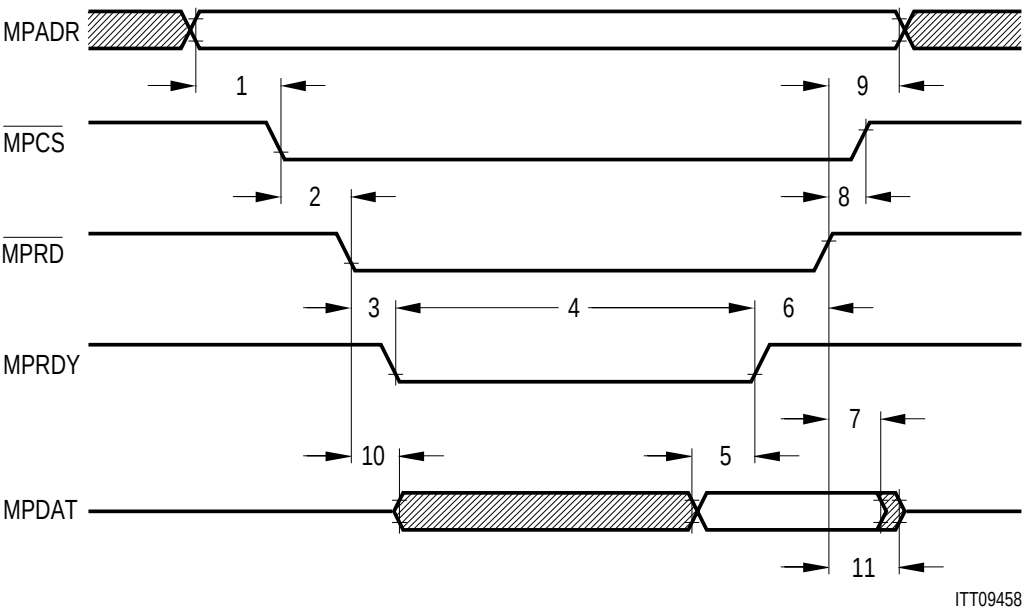


Figure 35
Microprocessor read cycle timing diagram

Table 35 Microprocessor read cycle AC timing characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	Setup time MPADR before $\overline{\text{MPCS}}$ low	0			ns
2	Setup time $\overline{\text{MPCS}}$ before $\overline{\text{MPRD}}$ low	0			ns
3	Delay MPRDY low after $\overline{\text{MPRD}}$ low	2		20	ns
4	Pulse width MPRDY low	2 x T_{clock}		20 x T_{clock}	ns
5	MPDAT valid before MPRDY high	10			ns
6	MPRDY high to $\overline{\text{MPRD}}$ high	10			ns
7	Hold time MPDAT after $\overline{\text{MPRD}}$ high	3			ns
8	Hold time $\overline{\text{MPCS}}$ after $\overline{\text{MPRD}}$ high	5			ns
9	Hold time MPADR after $\overline{\text{MPRD}}$ high	5			ns

Table 35 Microprocessor read cycle AC timing characteristics (cont'd)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
10	Delay $\overline{\text{MPRD}}$ low to MPDAT low impedance	4		20	ns
11	Delay $\overline{\text{MPRD}}$ high to MPDAT high impedance	5		20	ns

5.3.6 Clock Recovery interface

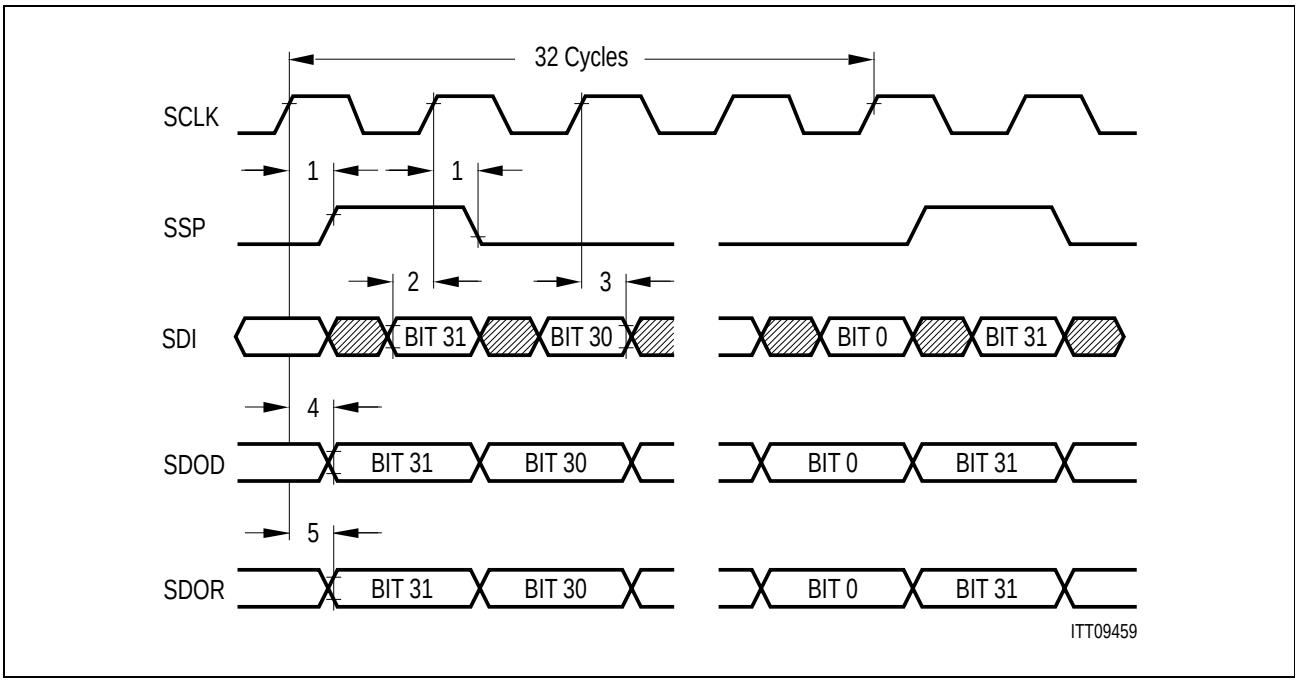


Figure 36
Clock recovery interface timing diagram

Table 36 Clock recovery interface AC timing characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	Delay SCLK rising to SSP	2		11	ns
2	Setup time SDI before SCLK rising	12			ns
3	Hold time SDI after SCLK rising	0			ns
4	Delay SCLK rising to SDOD	2		11	ns
5	Delay SCLK rising to SDOR	2		11	ns

5.3.7 Boundary-scan test interface

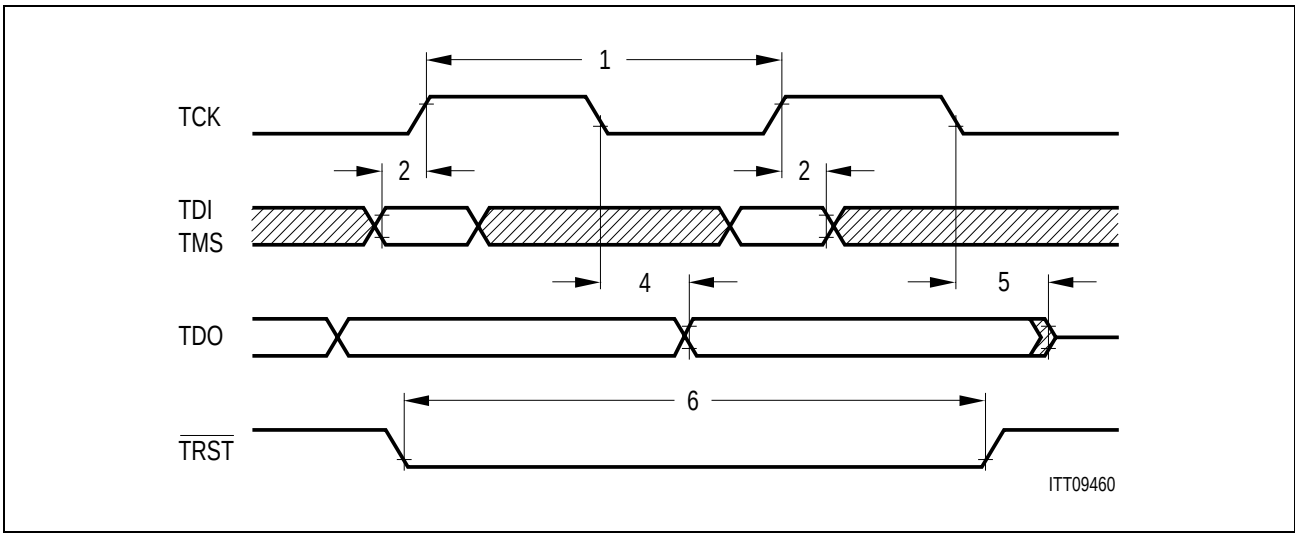


Figure 37
Boundary-scan test interface timing diagram

Table 37 Boundary-scan test interface AC timing characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{TCK} : Period TCK	160			ns
1A	F_{TCK} : Frequency TCK			6,25	Mhz
2	Setup time TMS, TDI before TCK rising	10			ns
3	Hold time TMS, TDI after TCK rising	10			ns
4	Delay TCK falling to TDO valid	0		30	ns
5	Delay TCK falling to TDO high impedance	0		30	ns
6	Pulse width $\overline{\text{TRST}}$ low	2 x T_{TCK}			ns

Device Identification register

31 28	27 12	11 1	0
Version	**Part-number**	**Manufacturer-ID**	
0000	1011 0000 1011 0100	0000 0010 111	1

Instruction register

Table 38 shows the instruction binary codes for the 4 bit instruction register.

Table 38 Boundary-scan instruction binary codes

Instruction	Code
EXTEST	0000
IDCODE	0001
HIGHZ	0100
SAMPLE/PRELOAD	0101
CLAMP	0111
BYPASS	1111

Boundary-scan register

Table 39 describes the Boundary-scan register. The register contains 272 cells numbered from 271 down to 0. Cell number 0 is located closest to TDO. The cells of type “input” cannot drive the on-chip system logic (the INTEST instruction is not implemented). The cells of type “control” will disable the corresponding outputs when a logic-1 is applied. The control cells are preset to a safe logic-1 during the TEST-LOGIC-RESET state of the TAP controller.

Table 39 Boundary-scan register

Nr	Name	Type
271	MPCS	input
270	MPWR	input
269	MPRD	input
268	MPDAT0	input
267	MPDAT1	input
266	MPDAT2	input
265	MPDAT3	input
264	MPDAT4	input
263	MPDAT5	input
262	MPDAT6	input
261	MPDAT7	input
260	MPDAT8	input
259	MPDAT9	input
258	MPDAT10	input
257	MPDAT11	input
256	MPDAT12	input
255	MPDAT13	input
254	MPDAT14	input
253	MPDAT15	input
252	MPDAT0	output
251	MPDAT1	output
250	MPDAT2	output
249	MPDAT3	output
248	MPDAT4	output
247	MPDAT5	output
246	MPDAT6	output
245	MPDAT7	output
244	MPDAT8	output
243	MPDAT9	output
242	MPDAT10	output

Nr	Name	Type
135	RMDAT24	input
134	RMDAT25	input
133	RMDAT26	input
132	RMDAT27	input
131	RMDAT28	input
130	RMDAT29	input
129	RMDAT30	input
128	RMDAT31	input
127	RMDAT32	input
126	RMDAT0	output
125	RMDAT1	output
124	RMDAT2	output
123	RMDAT3	output
122	RMDAT4	output
121	RMDAT5	output
120	RMDAT6	output
119	RMDAT7	output
118	RMDAT8	output
117	RMDAT9	output
116	RMDAT10	output
115	RMDAT11	output
114	RMDAT12	output
113	RMDAT13	output
112	RMDAT14	output
111	RMDAT15	output
110	RMDAT16	output
109	RMDAT17	output
108	RMDAT18	output
107	RMDAT19	output
106	RMDAT20	output

Table 39 Boundary-scan register (cont'd)

Nr	Name	Type
241	MPDAT11	output
240	MPDAT12	output
239	MPDAT13	output
238	MPDAT14	output
237	MPDAT15	output
236	MPDAT_CTRL	control
235	RFCLK	input
234	CLK	input
233	RESET	input
232	MPRDY	output
231	MPRDY_CTRL	control
230	MPIR1	output
229	MPIR1_CTRL	control
228	MPIR2	output
227	MPIR2_CTRL	control
226	MPADR0	input
225	MPADR1	input
224	MPADR2	input
223	MPADR3	input
222	MPADR4	input
221	MPADR5	input
220	MPADR6	input
219	MPADR7	input
218	MPADR8	input
217	MPADR9	input
216	MPADR10	input
215	MPADR11	input
214	MPADR12	input
213	MPADR13	input
212	MPADR14	input

Nr	Name	Type
105	RMDAT21	output
104	RMDAT22	output
103	RMDAT23	output
102	RMDAT24	output
101	RMDAT25	output
100	RMDAT26	output
99	RMDAT27	output
98	RMDAT28	output
97	RMDAT29	output
96	RMDAT30	output
95	RMDAT31	output
94	RMDAT32	output
93	RMDAT_CTRL	control
92	RMWR	output
91	RMWR_CTRL	control
90	RMCS	output
89	RMCS_CTRL	control
88	RMOE	output
87	RMOE_CTRL	control
86	RMADC	output
85	RMADC_CTRL	control
84	RMADR0	output
83	RMADR1	output
82	RMADR2	output
81	RMADR3	output
80	RMADR4	output
79	RMADR5	output
78	RMADR6	output
77	RMADR7	output
76	RMADR8	output

Table 39 Boundary-scan register (cont'd)

Nr	Name	Type
211	MPADR15	input
210	MPADR16	input
209	MPADR17	input
208	ITST0	input
207	E1/T1	input
206	ITST1	input
205	ITST2	input
204	OUTTR	input
203	ITST3	input
202	SDI	input
201	SCLK	output
200	SCLK_CTRL	control
199	SSP	output
198	SSP_CTRL	control
197	SDOR	output
196	SDOR_CTRL	control
195	SDOD	output
194	SDOD_CTRL	control
193	TXCLA	output
192	TXCLA_CTRL	control
191	TXENB	input
190	TXSOC	input
189	TXDAT0	input
188	TXDAT1	input
187	TXDAT2	input
186	TXDAT3	input
185	TXDAT4	input
184	TXDAT5	input
183	TXDAT6	input
182	TXDAT7	input

Nr	Name	Type
75	RMADR9	output
74	RMADR10	output
73	RMADR11	output
72	RMADR12	output
71	RMADR13	output
70	RMADR14	output
69	RMADR15	output
68	RMADR_CTRL	control
67	FTCLK0	input
66	FTCLK1	input
65	FTCLK2	input
64	FTCLK3	input
63	FTCLK4	input
62	FTCLK5	input
61	FTCLK6	input
60	FTCLK7	input
59	FRCLK0	input
58	FRCLK1	input
57	FRCLK2	input
56	FRCLK3	input
55	FRCLK4	input
54	FRCLK5	input
53	FRCLK6	input
52	FRCLK7	input
51	FRDAT0	input
50	FRDAT1	input
49	FRDAT2	input
48	FRDAT3	input
47	FRDAT4	input
46	FRDAT5	input

Table 39 Boundary-scan register (cont'd)

Nr	Name	Type
181	TXPRT	input
180	UTTR	input
179	TXCLK	input
178	RXSOC	output
177	RXSOC_CTRL	control
176	RXCLA	output
175	RXCLA_CTRL	control
174	RXDAT0	output
173	RXDAT1	output
172	RXDAT2	output
171	RXDAT3	output
170	RXDAT4	output
169	RXDAT5	output
168	RXDAT6	output
167	RXDAT7	output
166	RXDAT_CTRL	control
165	RXPRT	output
164	RXPRT_CTRL	control
163	RXENB	input
162	RXCLK	input
161	RMCLK	output
160	RMCLK_CTRL	control
159	RMDAT0	input
158	RMDAT1	input
157	RMDAT2	input
156	RMDAT3	input
155	RMDAT4	input
154	RMDAT5	input
153	RMDAT6	input
152	RMDAT7	input

Nr	Name	Type
45	FRDAT6	input
44	FRDAT7	input
43	FRMFB0	input
42	FRMFB1	input
41	FRMFB2	input
40	FRMFB3	input
39	FRMFB4	input
38	FRMFB5	input
37	FRMFB6	input
36	FRMFB7	input
35	FRFRS0	output
34	FRFRS1	output
33	FRFRS2	output
32	FRFRS3	output
31	FRFRS4	output
30	FRFRS5	output
29	FRFRS6	output
28	FRFRS7	output
27	FRFRS_CTRL	control
26	FTDAT0	output
25	FTDAT1	output
24	FTDAT2	output
23	FTDAT3	output
22	FTDAT4	output
21	FTDAT5	output
20	FTDAT6	output
19	FTDAT7	output
18	FTDAT_CTRL	control
17	FTMFS0	output
16	FTMFS1	output

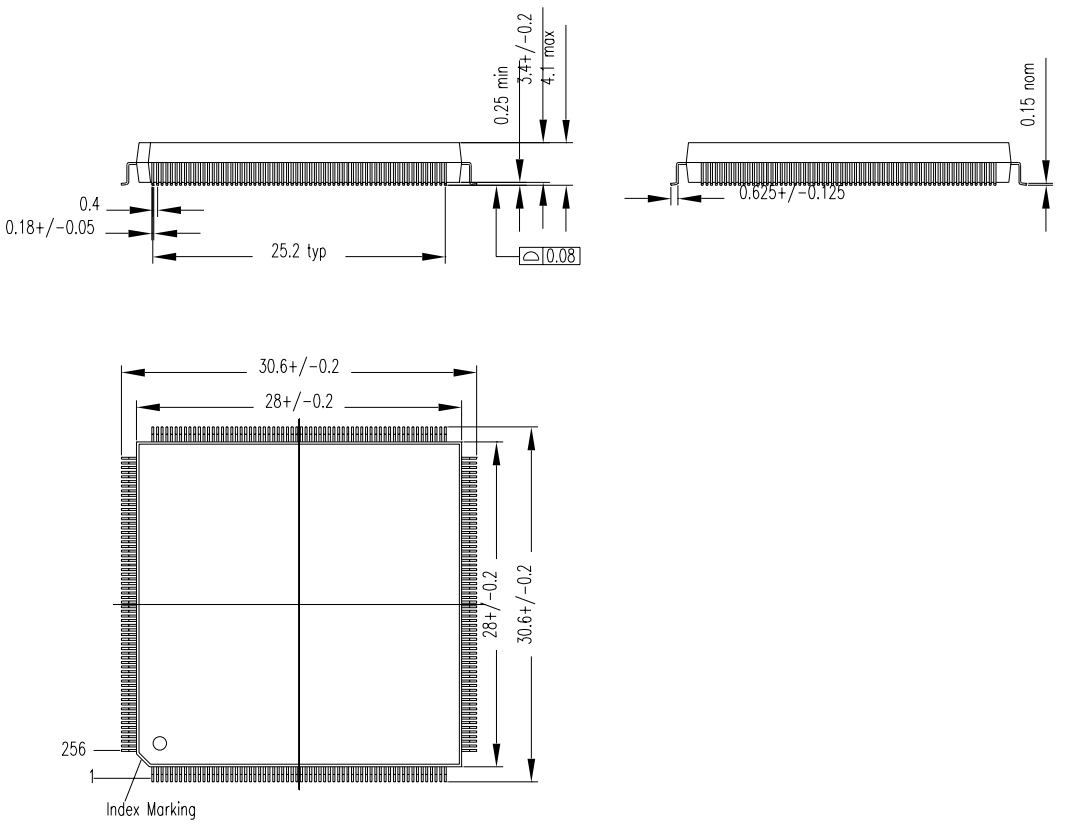
Table 39 Boundary-scan register (cont'd)

Nr	Name	Type
151	RMDAT8	input
150	RMDAT9	input
149	RMDAT10	input
148	RMDAT11	input
147	RMDAT12	input
146	RMDAT13	input
145	RMDAT14	input
144	RMDAT15	input
143	RMDAT16	input
142	RMDAT17	input
141	RMDAT18	input
140	RMDAT19	input
139	RMDAT20	input
138	RMDAT21	input
137	RMDAT22	input
136	RMDAT23	input

Nr	Name	Type
15	FTMFS2	output
14	FTMFS3	output
13	FTMFS4	output
12	FTMFS5	output
11	FTMFS6	output
10	FTMFS7	output
9	FTMFS_CTRL	control
8	FTFRS0	output
7	FTFRS1	output
6	FTFRS2	output
5	FTFRS3	output
4	FTFRS4	output
3	FTFRS5	output
2	FTFRS6	output
1	FTFRS7	output
0	FTFRS_CTRL	control

6 Package Outline

Plastic Package, P-MQFP-256
(Plastic Metric Quad Flat Package)



Packing Types
Package outlines for tubes, trays etc. are contained in our “Package Information” Data Book.

SMD = Surface Mounted Device

Dimensions in mm

7 Appendices

7.1 Initialization of IWE8

After hardware or software reset, all internal registers take the default values indicated in the register description. The internal configuration RAM's (RAM1, RAM2 and RAM3) and the external RAM are undefined after reset.

Table 40 General initialization of IWE8

Action	Register or RAM [field]	Typical Value
Check IWE8 version = 1.1, Check E1 or T1 mode	vers	E1 : $00C9_H$ T1 : 0089_H
Initialize internal RAM's	RAM1, RAM2, RAM3	$0000\ 0000_H$
Initialize external RAM	Ext RAM	$0000\ 0000_H$
Enable UTOPIA receive interface	acfg [a_ur_en]	1_B
Enable UTOPIA transmit interface	acfg [a_ut_en]	1_B
Change byte-patterns if required	bp32 [bp3,bp2] bp10 [bp1,bp0]	$FFFF_H$ $FFFF_H$

7.1.1 ATM mode ports

Table 41 Initialization of ATM mode ports

Action	Register or RAM [field]	Typical Value
Set port in ATM mode	pcfN [p_atm]	1_B
Change cell delineation parameters if required	atmc [alpha] [delta] [coset]	7655_H 0111_B 0110_B $0101\ 0101_B$
Change pattern of cells to be deleted if required	rxid [prg_rx_hd] [msk_rx_hd]	E1:0100_H T1:$00FE_H$ E1:$0000\ 0001_B$ T1:$0000\ 0000_B$ E1:$0000\ 0000_B$ T1:$1111\ 1110_B$
Change pattern of idle/unassigned cells to be transmitted if required	txid [prg_tx_hd] [prg_tx_pl]	$016A_H$ $0000\ 0001_B$ $0110\ 1010_B$

Table 41 Initialization of ATM mode ports (cont'd)

Action	Register or RAM [field]	Typical Value
Set counter thresholds in external RAM	Ext RAM (OAM counter thresholds)	8000 0003_H
Enable OAM counters for ATM ports	catm[cnt_atm_en]	1 1111_B
Initialize timers of set1 - disable timer - set timer for 4 msec (16 x 245 µs)	Ext RAM (timers) [timer_enable] [timer_value]	0000 0010_H 0_B 0010_H
Set OAM control register	oamc [tim_set1_en] [dest_read] [oam_act]	0007_H 1_B 1_B 1_B
Activate output queue overflow counter	acfg [a_ovf_cnt_en]	1_B
Unmask interrupts	imr1	1009_H
Define ATM Receive Idle Slots	RAM1(idle slots)	0000 0000_H
Define ATM Receive Reference Slot - en/disable interrupt at OCD start - en/disable interrupt at OCD end - go to HUNT state cell delineation - en/disable idle cell deletion - en/disable payload descrambler - channel_mode = inactive - ref_slot = 1	RAM1(1) [ocd_start_intrpt] [ocd_end_intrpt] [go_hunt] [delete_idle_cells] [x43_descrambling] [channel_mode] [ref_slot]	0000 $00D9_H$ 1_B 1_B 0_B 1_B 1_B 00_B 1_B
Define ATM Receive Continuation Slots - reference slot number = 1 - cont_slot = 1 - ref_slot = 0	RAM1(continuation slots) [ref_slot_nr] [channel_mode] [ref_slot]	0000 0006_H 00001_B 1_B 0_B
Define ATM Transmit Idle Slots	RAM2(idle slots)	0000 0000_H
Define ATM Transmit Reference Slot - en/disable payload scrambler - channel_mode = inactive - ref_slot = 1	RAM2(1) [x43_scrambling] [channel_mode] [ref_slot]	0000 0009_H 1_B 00_B 1_B
Define ATM Transmit Continuation Slots - reference slot number = 1 for G.804 - cont_slot = 1 - ref_slot = 0	RAM2(continuation slots) [ref_slot_nr] [cont_slot] [ref_slot]	0000 0006_H 00001_B 1_B 0_B

Table 42 Activation of ATM mode ports

Action	Register or RAM [field]	Typical Value
Activate transmit port	pcfN[p_tx_act]	1_B
Activate receive port	pcfN[p_rx_act]	1_B
Wait for 250 µs		
Set channel_mode to ‘Active’ in ‘ATM Transmit Reference Slot’	RAM2(1) [channel_mode]	01_B
Set channel_mode to ‘Active’ in ‘ATM Receive Reference Slot’	RAM1(1) [channel_mode]	01_B

7.1.2 AAL mode ports with unstructured CES

Table 43 Initialization of AAL ports with unstructured CES

Action	Register or RAM [field]	Typical Value
Set port in AAL mode	pcfN [p_atm]	0_B
Set port in unstructured CES mode	pcfN [p_ces]	1_B
Select clock recovery method e.g. SRTS only	pcfN [p_acm] pcfN [p_srts]	0_B 1_B
Enable clock recovery interface	acfg [a_crv_en]	1_B
Change dummy RTS if required	acfg [a_dummy_rts]	0000_B
Activate output queue overflow counter	acfg [a_ovf_cnt_en]	1_B
Set counter thresholds in external RAM treshold active and set to 3	Ext RAM (channel_nr = 0) (OAM counter thresholds)	8000 0003_H
Enable OAM counters for AAL ports all SDT related counters are disabled	caal[cnt_aal_en]	$B3F1_H$
Set OAM control register	oamc [tim_set1_en] [dest_read] [oam_act]	0003_H 0_B 1_B 1_B
Unmask interrupts	imr1	6001_H

Table 43 Initialization of AAL ports with unstructured CES (cont'd)

Action	Register or RAM [field]	Typical Value
Define AAL Receive Reference Slot	RAM1(0)	092F 5FF1$_H$
- next slot nr	[next_slot_nr]	0 0001$_B$
- SDT start of structure pulse select	[sdt_mfs]	0$_B$
- SDT start of structure double pulse	[sdt_double_mfs]	0$_B$
- enable SRTS	[srts]	1$_B$
- substitute byte-pattern select	[subst_bpslct]	00$_B$
- enable decorrelation circuit	[dcor]	1$_B$
- decorrelation random number e.g. 15	[dcor_random_nr]	0 1111$_B$
- disable AAL0	[aal0]	0$_B$
- partial cell filling (47 = fully filled cells)	[part_fill]	10 1111$_B$
- band_width	[band_width]	1 1111$_B$
- disable SDT	[sdt]	0$_B$
- channel_mode = inactive	[channel_mode]	00$_B$
- ref_slot = 1	[ref_slot]	1$_B$
Define AAL Transmit Reference Slot	RAM2(0)	0B82 4E01$_H$
- next slot nr	[next_slot_nr]	0 0001$_B$
- not used		0$_B$
- enable SNP check	[snp_check]	1$_B$
- enable SN check	[sn_check]	1$_B$
- choose fast SC algorithm	[sn_fast]	1$_B$
- SDT start of structure pulse select	[sdt_mfs]	0$_B$
- SDT out of sync before reinitialization	[sdt_oos_nr]	00$_B$
- SDT pointer parity check	[sdt_par]	0$_B$
- SDT pointer only once in 8 cells	[sdt_once]	0$_B$
- enable clock recovery downstream	[crv_en]	1$_B$
- microprocessor reassembly buffer init	[mcp_reinit]	0$_B$
- disable AAL0	[aal0]	0$_B$
- partial cell filling (47 = fully filled cells)	[part_fill]	10 1111$_B$
- not used		0 0000$_B$
- disable SDT	[sdt]	0$_B$
- channel_mode = inactive	[channel_mode]	00$_B$
- ref_slot = 1	[ref_slot]	1$_B$
AAL Transmit Reference Slot extended	RAM3(0)	0200 1003$_H$
- not used		000$_B$
- starvation byte-pattern select	[starv_bpslct]	00$_B$
- init starvation octets sent	[starv_ini]	512
- buffer logical size	[buff_lsize]	1024
- automatic buffer reinit at overflow	[auto_reinit_of]	1$_B$
- automatic buffer reinit at underflow	[auto_reinit_uf]	1$_B$

Calculation of reassembly buffer sizes.

Assume CDV = 1 ms , K = 2, MaxDelay = 4 ms , N = 32
Physical reassembly buffer size in CES mode : 256 cells
Starvation octets at initialization : starv_ini > K x N x CDV/125µs = 512
Buffer logical size : buff_lsize < MaxDelay x N / 125µs = 1024

Table 44 Activation of AAL mode ports with unstructured CES

Action	Register or RAM [field]	Typical Value
Activate transmit port	pcfN[p_tx_act]	1_B
Activate receive port	pcfN[p_rx_act]	1_B
Wait for 250 µs		
Set channel_mode to 'Active' in 'AAL Transmit Reference Slot'	RAM2(0) [channel_mode]	01_B
Set channel_mode to 'Active' in 'AAL Receive Reference Slot'	RAM1(0) [channel_mode]	01_B

7.1.3 AAL mode ports with N x 64 kbit/s basic service

As an example table 45 shows the initialization of a 2 x 64 kbit/s channel in an E1 port using frame slot 2 and 5, with partially filled cells of 8 octets transmitted in multiframe based SDT mode, using SRTS and ACM for clock recovery, using substitute mode in case of FRCLK clock failure and using no decorrelation.

Table 45 Initialization of AAL port with 2 x 64 kbit/s channel

Action	Register or RAM [field]	Typical Value
Set port in AAL mode	pcfN [p_atm]	0_B
Set port in N x 64 kbit/s mode	pcfN [p_ces]	0_B
Select clock recovery method e.g. ACM and SRTSy	pcfN [p_acm] pcfN [p_srts]	1_B 1_B
Enable clock recovery interface	acfg [a_crv_en]	1_B
Change dummy RTS if required	acfg [a_dummy_rts]	0000_B
Change emergency byte-pattern if required	acfg [a_emg_bpslct]	00_B
Activate output queue overflow counter	acfg [a_ovf_cnt_en]	1_B
Set counter thresholds in external RAM treshold active and set to 3	Ext RAM (channel_nr = 2) (OAM counter thresholds)	8000 0003_H
Enable all OAM counters for AAL ports	caal[cnt_aal_en]	$FFFF_H$

Table 45 Initialization of AAL port with 2 x 64 kbit/s channel (cont'd)

Action	Register or RAM [field]	Typical Value
Set OAM control register	oamc [tim_set1_en] [dest_read] [oam_act]	0003_H 0_B 1_B 1_B
Unmask interrupts	imr1	6001_H
Define AAL Receive Idle Slots	RAM1(idle slots)	$0000\ 0000_H$
Define AAL Receive Reference Slot - next slot nr = 5 - SDT start of structure pulse select - SDT start of structure double pulse - enable SRTS - substitute byte-pattern select - disable decorrelation circuit - decorrelation random number - disable AAL0 - partial cell filling (8 octets) - band_width (N-1 = 1) - enable SDT - channel_mode = inactive - ref_slot = 1	RAM1(2) [next_slot_nr] [sdt_mfs] [sdt_double_mfs] [srts] [subst_bpslct] [dcor] [dcor_random_nr] [aal0] [part_fill] [band_width] [sdt] [channel_mode] [ref_slot]	$2D00\ 1019_H$ $0\ 0101_B$ 1_B 0_B 1_B 00_B 0_B $0\ 0000_B$ 0_B $00\ 1000_B$ $0\ 0001_B$ 1_B 00_B 1_B
Define AAL Receive Continuation Slot - fourth slot number (don't care) - third slot number (don't care) - reference slot number = 2 - cont_slot = 1 - ref_slot = 0	RAM1(5) [fourth_slot_nr] [third_slot_nr] [ref_slot_nr] [channel_mode] [ref_slot]	$0000\ 000A_H$ $0\ 0000_B$ $0\ 0000_B$ $0\ 0010_B$ 1_B 0_B
Define AAL Transmit Idle Slots	RAM2 (idle slots)	$0000\ 0000_H$

Table 45 Initialization of AAL port with 2 x 64 kbit/s channel (cont'd)

Action	Register or RAM [field]	Typical Value
Define AAL Transmit Reference Slot	RAM2(2)	$2B6E\ 1004_H$
- next slot nr = 5	[next_slot_nr]	$0\ 0101_B$
- not used		0_B
- enable SNP check	[snp_check]	1_B
- enable SN check	[sn_check]	1_B
- choose standard SC algorithm	[sn_fast]	0_B
- SDT start of structure pulse select	[sdt_mfs]	1_B
- 2 SDT out of sync before reinitialization	[sdt_oos_nr]	10_B
- SDT pointer parity check	[sdt_par]	1_B
- SDT pointer only once in 8 cells	[sdt_once]	1_B
- enable clock recovery downstream	[crv_en]	1_B
- microprocessor reassembly buffer init	[mcp_reinit]	0_B
- disable AAL0	[aal0]	0_B
- partial cell filling (8 octets per cell)	[part_fill]	$00\ 1000_B$
- not used		$0\ 0000_B$
- ensable SDT	[sdt]	1_B
- channel_mode = inactive	[channel_mode]	00_B
- ref_slot = 1	[ref_slot]	1_B
Define AAL Transmit Continuation Slot	RAM2(5)	$1000\ 000A_H$
- next slot number = 2 (last slot)	[next_slot_nr]	$0\ 0010_B$
- reference slot number = 2	[ref_slot_nr]	$0\ 0010_B$
- cont_slot = 1	[channel_mode]	1_B
- ref_slot = 0	[ref_slot]	0_B
AAL Transmit Reference Slot extended	RAM3(2)	$0020\ 0200_H$
- not used		000_B
- starvation byte-pattern select	[starv_bpslct]	00_B
- init starvation octets sent	[starv_ini]	32
- buffer logical size	[buff_lsize]	128
- automatic buffer reinit at overflow	[auto_reinit_of]	0_B
- automatic buffer reinit at underflow	[auto_reinit_uf]	0_B

Calculation of reassembly buffer sizes :

Assume CDV = 1 ms , K = 2, MaxDelay = 8 ms , N = 2, Cell Fill = 8
Cells per block : 4 (see Table 20)
Physical reassembly buffer size : N x 8 x Cell Fill x Cells per block = 512 octets
Starvation octets at initialization : starv_ini > K x N x CDV/125µs = 32 octets
Buffer logical size: buff_lsize < MaxDelay x N / 125µs = 128 octets
Buffer logical size: buff_lsize > ((K x CDV) + SDTdelay)/AverageCellDistance) + 1
with FR = 16, Pmax = 2 x Cell Fill = 16 and N = 2
SDTdelay = 125µs (Fr + (Pmax/N)) = 3 ms
AverageCellDistance = 125µs x Cell Fill / N = 0.5 ms
buff_lsize > (2ms + 3 ms)/0.5ms + 1 = 11 cells = 88 octets

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7.3 Glossary

UTOPIA Transmit Interface (Downstream): Data is transferred from the ATM Layer to the PHY Layer (in this case the IWE8).

UTOPIA Receive Interface (Upstream): Data is transferred from the PHY Layer (in this case the IWE8) to the ATM Layer.

7.4 Acronyms

Acronyms	Meaning
AAL	ATM Adaptation Layer
ACM	Adaptive Clock Method
ATM	Asynchronous Transfer Mode
B-ISDN	Broadband - Integrated Services Digital Network
CBR	Constant Bit Rate
CDV	Cell Delay Variation
CES	Circuit Emulation Service
CLP	Cell Loss Priority
CRC	Cyclic Redundancy Check
CS	Convergence Sublayer
CSI	Convergence Sublayer Indication
DS1	Digital Signal 1 (1.544 Mbit/s) (=T1)
FALC	Framer And Line Interface Component
FIFO	First In, First Out Buffer
FS/DL	Frame Sync/Data Link
FSM	Finite State Machine
GFC	Generic Flow Control
HEC	Header Error Control
I/O	Input/Output
ITU	International Telecommunications Union
ITU-T	International Telecommunications Union - Telecommunications Standardization Sector
IWE8	Interworking Element component, PXB 4220, for 8 channels
LCD	Loss of Cell Delineation
LIC	Line Interface Card or Line Interface Circuit
LOS	Loss Of Signal
LSB	Least Significant Bit
MSB	Most Significant Bit
NIC	Network Interface Controller or Card

Acronyms	Meaning
NNI	Network-to-Network Interface
OAM	Operation, Administration, and Maintenance
OCD	Out of Cell Delineation
PDU	Protocol Data Unit
PHY	Physical
PTI	Payload Type Identifier
RTS	Residual Time Stamp
SAR	Segmentation And Reassembly
SARE	Segmentation And Reassembly Element, PXB 4110
SC	Sequence Count
SDT	Structured Data Transfer
SN	Sequence Number
SNP	Sequence Number Protection
SRTS	Synchronous Residual Time Stamp
SSRAM	Synchronous Static RAM
TAP	Test Access Port
TBD	To Be Defined
UDT	Unstructured Data Transfer
UNI	User-to-Network Interface
UTOPIA	Universal Test and Operations Physical Interface for ATM
VC	Virtual Channel
VCI	Virtual Channel Identifier
VP	Virtual Path
VPI	Virtual Path Identifier