

ICs for Communications

Joint Audio Decoder-Encoder for Analog Videophone
JADE AN

PSB 7230 V 1.2

Preliminary Data Sheet 2.97

T7230-XV12-P1-7600

PSB 7230, Preliminary Revision History 2.97	
Previous Releases:none	
Page	Subjects (changes since last revision)

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25\text{ °C}$ and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about “**Processing Guidelines**” and “**Quality Assurance**” for ICs, see our Product Overview “**ICs for Communications**”

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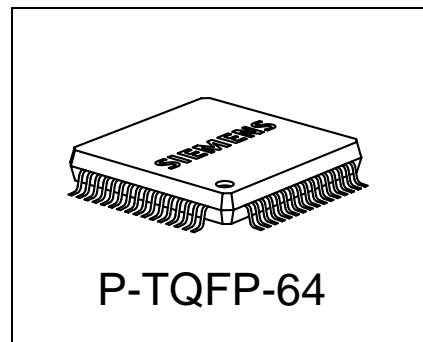
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1	Introduction	5
1.1	Feature List	5
1.2	Overview	7
1.3	Logic Symbol	9
1.4	Pin Configuration	10
1.5	Pin Description	11
1.6	Functional Block Diagram	16
1.7	System Integration	17
1.7.1	H.324 desktop videoconferencing solution for POTS	17
1.7.2	Low Cost H.324 desktop videoconferencing with software video	19
1.7.3	LAN videoconferencing	21
1.7.4	Standalone H.324/H.323 Videophone	22
1.7.5	Internet Telephone Access in Line Card	23
1.8	Board Layout	25
2	General Architecture and Functions	26
2.1	Architecture	26
2.2	Functions	28
2.2.1	Summary of the Functions	28
2.2.2	Audio Functions and Supplementary Features	28
3	Interfaces and Memory Organization	30
3.1	Interfaces	30
3.1.1	IOM-2 Interface	30
3.1.2	Serial Audio Interface	33
3.1.3	Parallel Host Interface	35
3.1.4	Clock Interface	36
3.2	Shared Memories	37
3.3	Directly Accessible Register Bank	39
3.3.1	Input/Output Registers	39
3.3.2	DSP/Host Com Area	42
3.4	Mailbox	46
4	Functional Blocks	49
4.1	Oscillator and Baud Rate Generator	49
4.2	Audio and Data Reception/Transmission	51
4.3	Serial Data Controller	61
4.4	IOM-2 Functions	65
4.4.1	Monitor Channel Protocol	66
4.4.2	C/I Channel	73
4.5	Programming Indirectly Accessible Registers	76

4.5.1	Programming via Parallel Host Interface (see also section 3.3.2)	76
5	Register Description	77
5.1	Interrupt Structure	77
5.2	Interrupt Status Registers	78
5.3	Indirectly Accessible Configuration and Control Registers	82
5.4	Serial Data Controller Registers	96
6	Firmware Features	110
6.1	Basic Functions	110
6.1.1	Firmware Version Number	110
6.1.2	Software Reset	112
6.2	Audio Interfaces	114
6.2.1	Compressed Audio Protocols and Control of JADE AN	115
6.2.1.1	Outband Control of JADE AN	116
6.2.1.2	Compressed Audio Protocol with Outband Control	131
6.2.1.3	Compressed Audio Protocol with Inband Control	133
6.2.2	Uncompressed Data Protocol	141
6.2.3	Audio Interface Timings	141
6.2.3.1	Uncompressed Data: Host IF Compressed Data: Host IF	141
6.2.3.2	Uncompressed Data: IOM IF Compressed Data: Host IF	148
6.2.3.3	Uncompressed Data: IOM IF Compressed Data: Serial Audio Interface (SAI)	159
7	Electrical Specification	162
7.1	Absolute Maximum Ratings	162
7.2	Operating Conditions	162
7.3	DC Characteristics	162
7.4	Capacitances	164
7.5	Oscillator Circuit	164
7.6	XTAL 1,2 Recommended typical crystal parameters	164
7.7	AC Characteristics	165
7.7.1	Testing Waveform	165
7.7.2	Parallel Host Interface Timing	166
7.7.3	IOM-2 Interface Timing	169
7.7.4	Serial Audio Interface Timing	172
8	Package Outline	176

1 Introduction**1.1 Feature List****Functions**

- G.723 V5.1 Compression/Decompression (6.3, 5.3 kbps)
- G.711 Compression/Decompression (64 kbps)
- Accepts/outputs uncompressed audio in 8-bit PCM A/μ law or 16-bit linear format
- Uncompressed/compressed audio switchable between different interface combinations (IOM[®]/Serial Audio Interface, IOM/Host, Host/Host)
- Inband controlled H.221/H.223 oriented audio protocol, e.g. for direct serial connection to Videocodec (VCP of 8x8 Inc., formerly IIT Inc.) as well as host based solutions
- Outband controlled audio protocol with optimized data rate
- Stable reaction on interrupt handshake timing violations of e.g. a slow host (Windows PC)
- Combined board-layout with other JADE versions in P-TQFP-100 package possible

System On-chip Functions

- One universal serial transparent data controller
- IOM-2 Monitor and C/I channels
- Generation of programmable system clock output

Interfaces

- 4-line IOM-2/PCM interface (programmable master or slave)
- 5-line Serial Audio Interface, e.g. for connection to Videocodec/H.221/223 processor
- Parallel 8-bit Host Interface

Control

- Programmable via Parallel Host Interface
- Operating parameters and mode settings via a register bank

Introduction

- Access to audio channels and serial transparent data controller from DSP or an external Host
- Interface to external software via a full-duplex 64-byte on-chip mailbox
- H.221/H.223 oriented inband configuration/mode switching

General

- Supply voltage: 3.0-3.6 V
- Additional 4.5 to 5.5 V supply for connection to 5-V systems without external components
- Ambient temperature range 0 °C to +70 °C
- P-TQFP-64 package

Type	Ordering Code	Package
PSB 7230 V1.2	Q67101-H6864	P-TQFP-64

1.2 Overview

The PSB7230 Joint Audio Decoder Encoder for Analog Videophones (JADE AN) is a device which implements voice compression algorithms using the Algebraic Code Excited Linear Prediction (ACELP) and the Multi-Pulse Maximum Likelihood Quantization (MP-MLQ) standard as defined in the ITU-T G.723 Recommendation. In addition G.711 PCM audio coding is also supported.

Thus, in G.723 mode it compresses the PCM (8 bit A-/μ-law) or 16 bit linear voice signal into 5.3 kbit/s (ACELP) or 6.3 kbit/s (MP-MLQ) bit stream, and vice versa. The implementation complies with the newest ITU-T C-code V5.1 (including the fallback version 4.1 without voice activity detection).

The JADE AN finds applications in

- ISDN Videophones (H.320)
- Analog Videophones (H.324)
- Networks (e.g. LANs) for packetized voice (H.323)
- Video Conference Systems
- Corporate Network voice concentrators, multiplexers and gateways
- Data-over-voice and Voice-over-data terminals.

Other potential application areas are:

- Networks (e.g. LANs) for packetized voice
- Digital Added Main-Line (DAML) & Digital Circuit Multiplication Equipment (DCME)
- Voice storage e.g. in PC based applications
- Message recording and distribution.

The interfaces of the JADE allow a seamless integration into IOM-2 based systems. After the circuit is set up in the proper mode of operation and parameter settings are programmed by a controlling software, the circuit runs independent of the rest of the system. Status and control information to/from the JADE can be transferred either inband the compressed audio data via the corresponding selected interface or outband using an 8-bit parallel host interface.

The audio frontend data can be exchanged either through the host interface or the IOM-2 interface. In the latter case the Siemens ARCOFI SP can be connected providing half-duplex handsfree or a Siemens ACE (acoustic echo canceller circuit) together with an ARCOFI BA providing full duplex handsfree.

The default configuration of the JADE is such, that in a videoconferencing system using the 8x8 (formerly IIT) VCP (Video Codec and Multimedia Communications Processor) the Siemens PSB7230 can work standalone without the need of external initialization. I.e., no host is needed in this case and the full communication is automatically started between the VCP and the Siemens PSB7230.

Introduction

The voice compression algorithms are implemented by an embedded 16-bit fixed point Digital Signal Processor with all memories internal and no external memory needed.

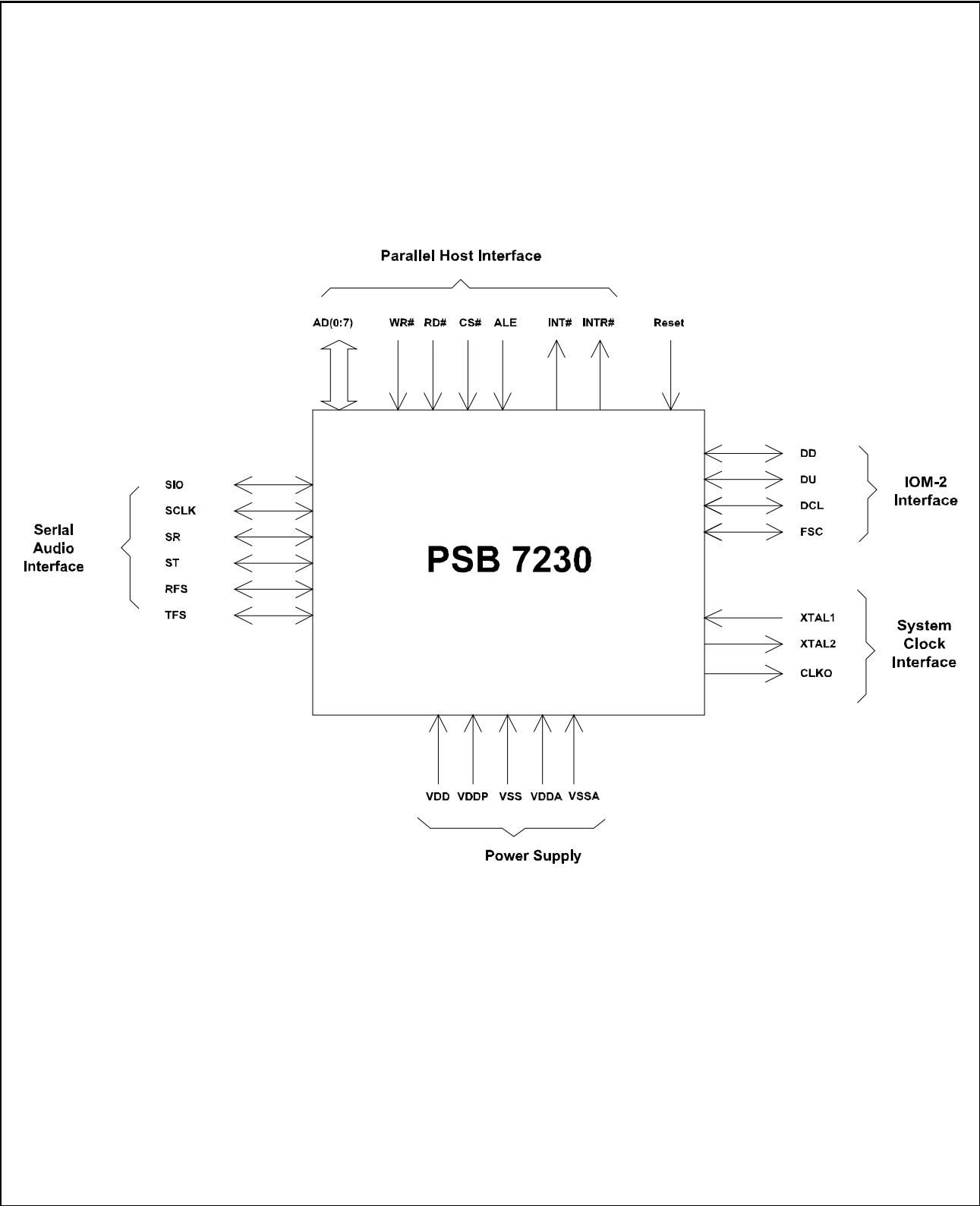
Integration of these and other features, as well as perfectly matched interfaces with other ICs allows for the implementation of highly optimized, low cost system solutions e.g. for Videophones, Data-over-voice and Channel Multiplexing equipment.

For system integration, a serial data channel is implemented which can be serviced by an attached host (or the on-chip DSP). System functions and communication between the chip and an external controller is supported by a full-duplex 64-byte on-chip mailbox communication memory.

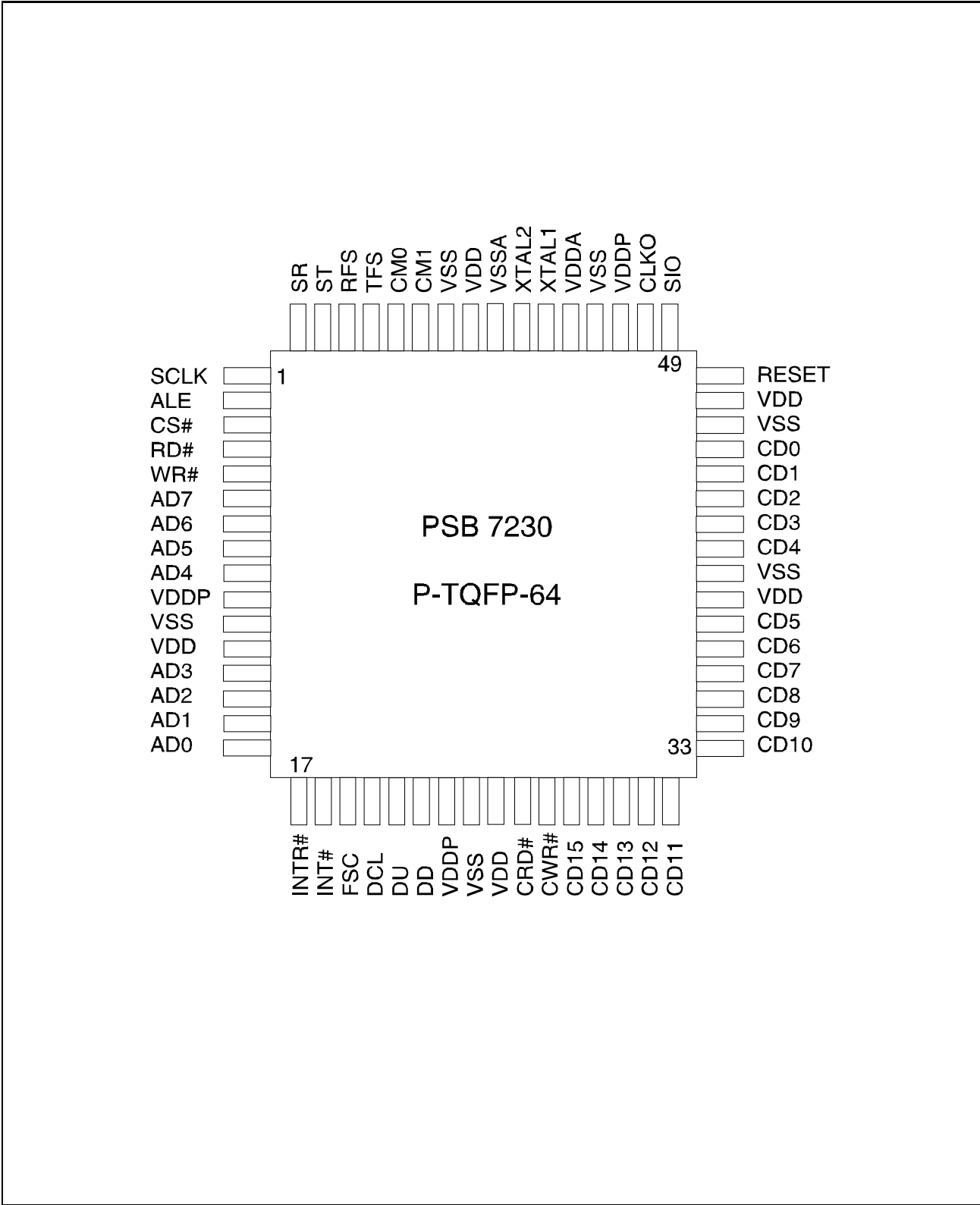
The circuit is offered in a Quad Flat Pack package with 64 pins (P-TQFP-64: size 10x10 mm, pitch 0.5 mm, height 1.4 mm).

Note: This Data Sheet gives a thorough description of the functions and hardware that forms the base of PSB 7230. It includes information that is not needed for the PSB 7230 as a 'ready to use plug and play' G.723/G.711 audio compression device.

1.3 Logic Symbol



1.4 Pin Configuration



1.5**Pin Description****Parallel Host Interface**

Pin No.	Symbol	Function	Descriptions
16	AD0	I/O	Address/Data Bus
15	AD1	I/O	
14	AD2	I/O	
13	AD3	I/O	
9	AD4	I/O	
8	AD5	I/O	
7	AD6	I/O	
6	AD7	I/O	
4	\overline{RD}	I	Read. This signal indicates a read operation.
5	\overline{WR}	I	Write. This signal indicates a write operation.
3	\overline{CS}	I	Chip Select.
2	ALE	I	Address Latch Enable. A "high" on this line indicates an address on AD(0:7).
17	\overline{INTR}	OD	Interrupt Real-time Interrupt output line for high priority interrupt status (Serial Audio Receive/Transmit, Serial Data Receive/Transmit data) to host
18	\overline{INT}	OD	Interrupt Request Interrupt output line for all other interrupt states.

Introduction**IOM-2 Interface**

Pin No.	Symbol	Function	Descriptions
22	DD	I/O/OD	Data Downstream on IOM-2/PCM interface.
21	DU	I/O/OD	Data Upstream on IOM-2/PCM interface.
20	DCL	I/O	Data Clock. Clock frequency is twice the data rate, or equal to the data rate.
19	FSC	I/O	Frame Sync. Marks the beginning of a physical IOM-2 or PCM frame.

Serial Audio Interface

Pin No.	Symbol	Function	Descriptions
1	SCLK	I/O	Serial Clock. Serial clock for SR and ST.
64	SR	I/O/OD	Serial Data Receive.
63	ST	I/O/OD	Serial Data Transmit.
62	RFS	I/O	Audio Receive Frame Sync.
61	TFS	I/O	Audio Transmit Frame Sync.

Introduction

System Clocks

Pin No.	Symbol	Function	Descriptions
54	XTAL1	I	Crystal In or Clock In. If a crystal is used, it is connected between XTAL1 and XTAL2. If a clock signal is provided (via an external oscillator), this signal is input via XTAL1. In this case the XTAL2 output is to be left non-connected. The XTAL1 input has to be 50% duty cycle and must not exceed the voltage range between V_{SSA} and V_{DDA} .
55	XTAL2	O	Crystal Out. Left unconnected if a crystal is not used.
50	CLKO	O	Clock Out. Output clock of frequency equal to the internal frequency divided by a programmable factor.

Test Interface (for production test only)

Pin No.	Symbol	Function	Descriptions
45	CD0	I/O	Test-Bus Data.
44	CD1	I/O	Is to be left NC if not used.
43	CD2	I/O	
42	CD3	I/O	
41	CD4	I/O	
38	CD5	I/O	
37	CD6	I/O	
36	CD7	I/O	
35	CD8	I/O	
34	CD9	I/O	
33	CD10	I/O	
32	CD11	I/O	
31	CD12	I/O	
30	CD13	I/O	
29	CD14	I/O	
28	CD15	I/O	

Introduction

Test Interface (for production test only) (cont'd)

Pin No.	Symbol	Function	Descriptions
26	\overline{CRD}	O	Test-Bus Read. Left NC if not used.
27	\overline{CWR}	O	Test-Bus Write. Left NC if not used.

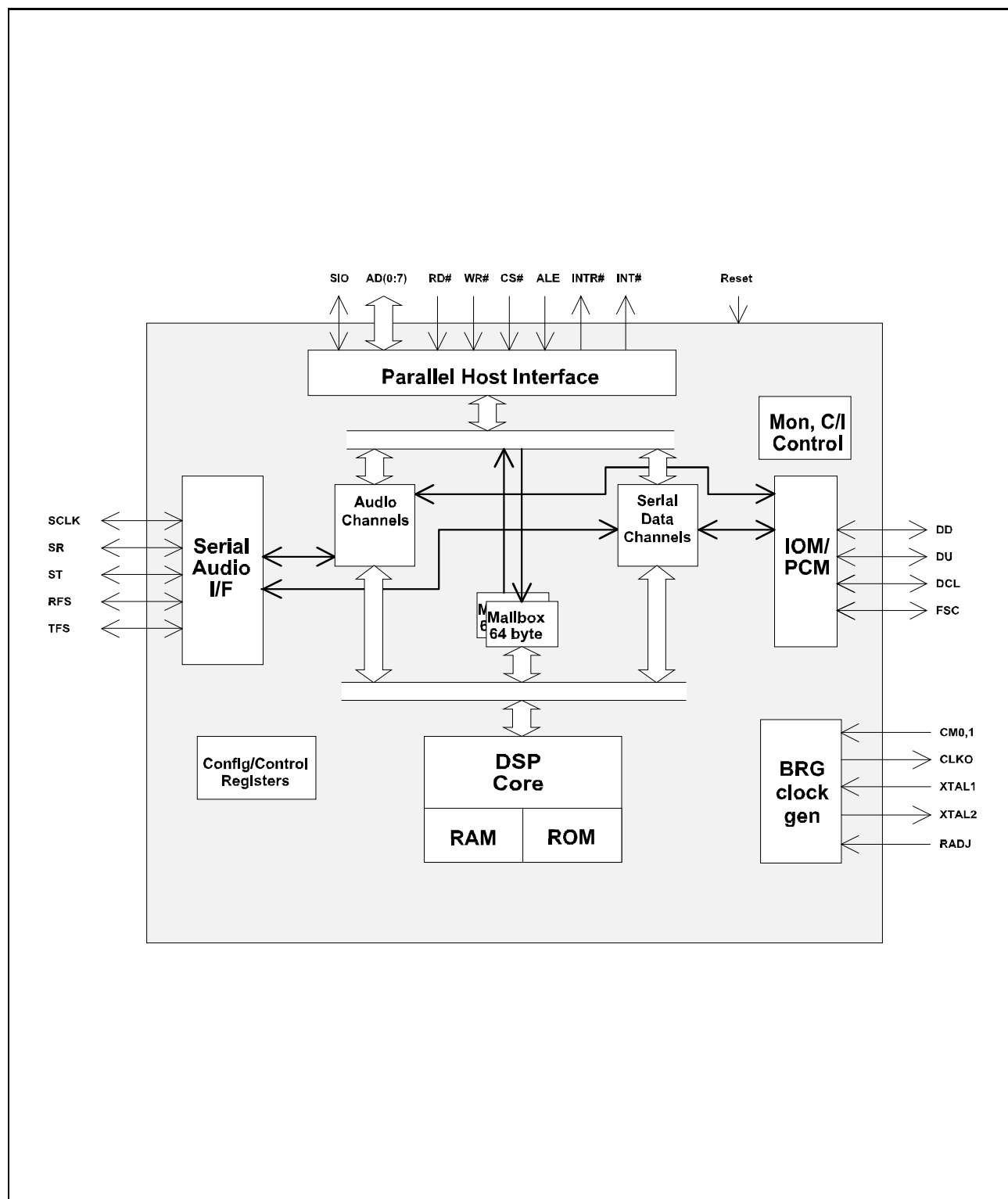
General Control

Pin No.	Symbol	Function	Descriptions
60	CM0	I	Test pin. Has to be connected to V_{DDP} or V_{SS} if not used
59	CM1	I	Test pin. Has to be connected to V_{DDP} or V_{SS} if not used
49	SIO	I/O	Serial I/O line When programmed as input, a rising or falling (selectable) edge on this line may generate a maskable interrupt \overline{INT} (host) or $\overline{INT1}$ (DSP). When programmed as output, its state is directly controlled by the DSP or the host.
48	RESET	I	Reset input. Reset time: >1 msec

Power Supply

Pin No.	Symbol	Function	Descriptions
11	V_{SS}		Ground (common to V_{DD} and V_{DDP})
24	V_{SS}		
40	V_{SS}		
46	V_{SS}		
52	V_{SS}		
58	V_{SS}		
12	V_{DD}		Positive power supply voltage (3.0-3.6 V)
25	V_{DD}		
39	V_{DD}		
47	V_{DD}		
57	V_{DD}		
10	V_{DDP}		Positive power supply voltage (4.5-5.5 V) for external interfaces
23	V_{DDP}		
51	V_{DDP}		
56	V_{SSA}		Separate Ground (0V) for Clock Generation Unit.
53	V_{DDA}		Separate positive power supply voltage (3.0-3.6 V) for Clock Generation Unit.

1.6 Functional Block Diagram



Detailed description see chapter 2.

1.7 System Integration

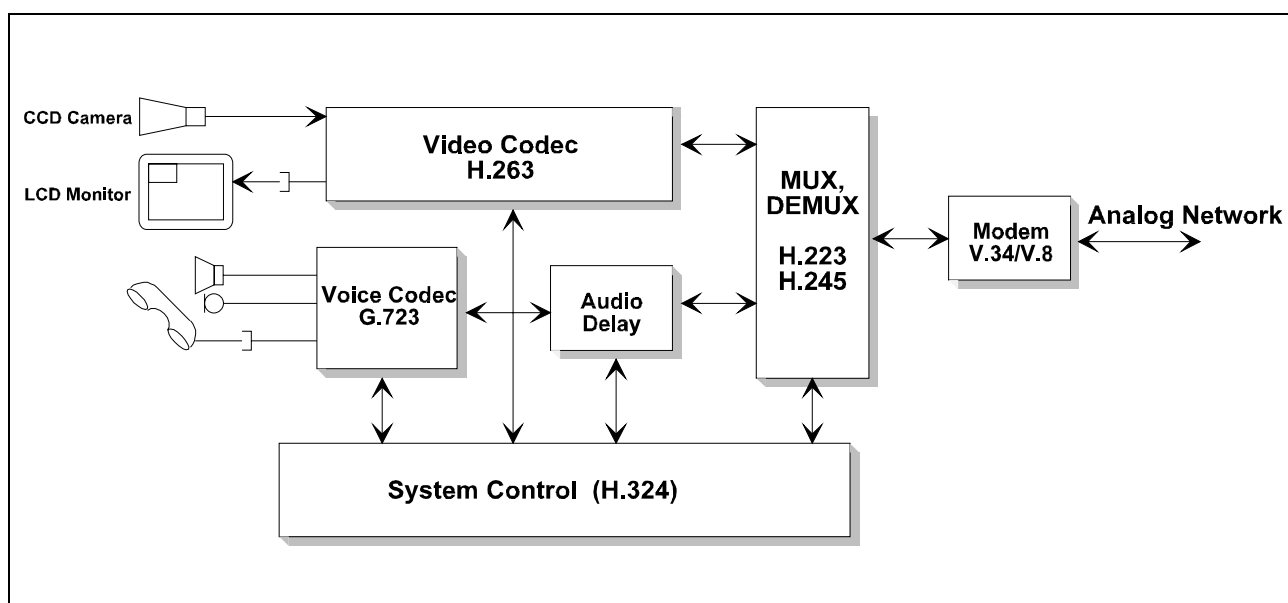
Example of integration in videophones for analog telephone line:

The first example represents a low-cost solution for a desktop stand-alone videophone that connects to an analog telephone line.

The analog telephone line can carry up to 28.8 kbps using a V.34 modem or 33.6 kbps using a V.34bis modem.

The general aspects of videotelephony over analog telephone lines are covered by ITU-T H.324 recommendations. The video is compressed according to the H.263 recommendation.

The compressed video and audio signals are multiplexed together with additional control information into a single communication link. The multiplexing is specified by the H.223 recommendation (see figure below).

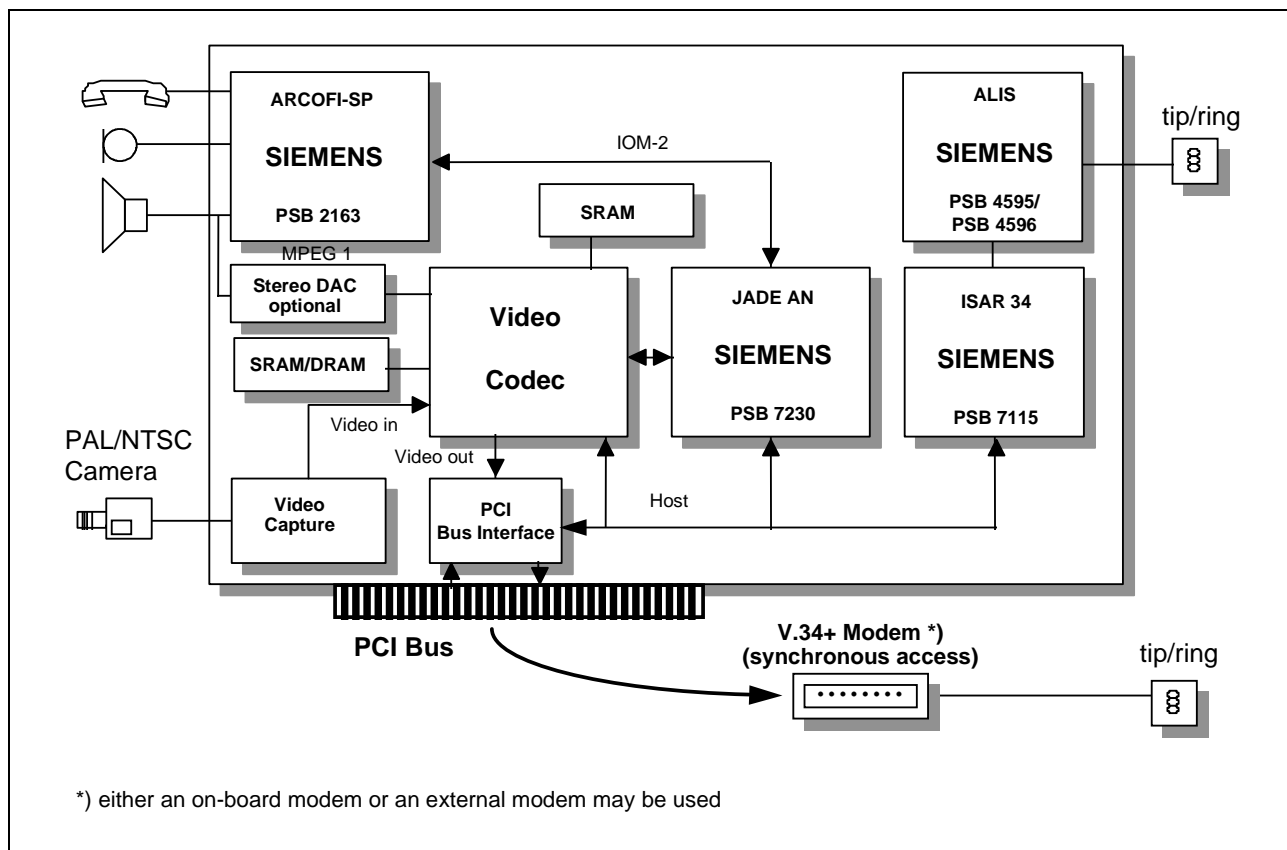


In order to make the best possible use of the total bandwidth and obtain the best possible video quality, the audio should require only a small fraction of the total data rate. This is made possible by using parametric compression techniques such as ACELP (5.3 kbps) or MP-MLQ (6.3 kbps). Above all, the corresponding norm (G.723) is an internationally adopted standard, so that compatibility between equipment from different manufacturers is ensured.

1.7.1 H.324 desktop videoconferencing solution for POTS

An H.324 desktop videoconferencing solution for POTS (plain old telephone system) line as a PCI card for commercial PC's is shown in the following figure:

Introduction



The connection to the POTS line can be done either by an on-board modem or an external V.34+ modem that is capable of synchronous data transfer. In the case of the modem on board, the videophone can be regarded as an add-on modem feature.

The JADE AN and the video codec chip (e.g. the Video Communication Processor "VCP" from 8x8 Inc.) constitute the heart of the videophone.

Both (together with the modem) are connected to the PC via a PCI Bus Interface (e.g. the "VPIC" of 8x8 Inc.).

The JADE AN compresses/decompresses audio according to the ITU-T standards G.723 (5.3 and 6.3 kbps) and G.711 (used in e.g. LAN applications) and runs a fully inband controlled protocol on the interface to the video codec. It receives/transmits uncompressed audio via the IOM-2 interface from/to the ARCOFI-SP. The JADE AN is setup for this application automatically after a hardware reset, so no additional initialization by a host is required. Since the JADE AN has all its memories on chip, no external SRAM needs to be connected.

The ARCOFI-SP (Audio Ringing Codec Filter) is a hands-free codec for 3.1 kHz voice which performs detection and elaborate balancing of the received and transmitted audio to suppress undesirable effects due to acoustical feedback of the signal from the remote

Introduction

subscriber. The quality obtained is very close to that of echo-free full duplex conferencing.

The video is captured by a PAL/NTSC camera and digitized and demodulated e.g. by a standard SAA7110 which is directly connected to the video processor. Alternatively, a digital camera may be used, which can be connected directly to the video processor.

The video processor compresses and decompresses video according to the ITU-T standards H.263 and multiplexes/demultiplexes video, audio and data according to H.223. The video processor uses DRAMs and SRAMs to store data and program code.

The H.223 multiplexed data stream is either sent via the PCI interface to an external V.34+ modem or via host or IOM-interface to an on-board modem (e.g. Siemens ISAR-34 (PSB7115) and ALIS (PSB 4595/4596)). The modem must be able to work in synchronous mode, i.e. the H.223 multiplexed data shall be applied directly to the V.34+ synchronous data pump. When an external, non-integrated V.34+ modem is utilized, control between the modem and the terminal shall be via ITU-T V.80.

For the on-board modem the ISAR-34 constitutes the data pump transferring the data with 33.6 kbps in both directions.

The ALIS chipset substitutes the conventional codec and DAA circuit. Since the it is a programmable solution, it can be configured by software to fit the approval requirements of all different countries, thus one hardware solution can be produced for all markets over the world. The decoupling between line and modem is done by capacitors instead of transformers, thus offering very small size and low cost implementations.

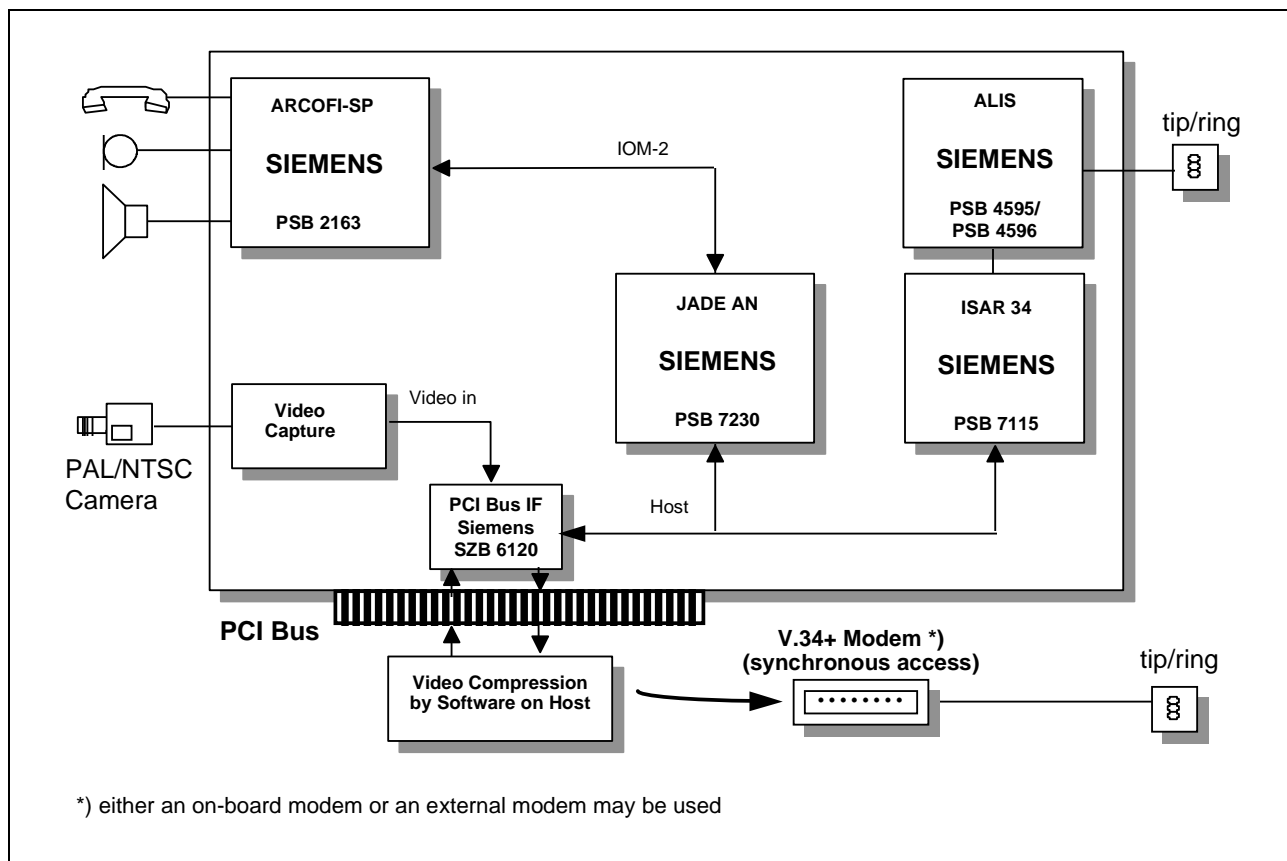
To achieve "lip synchronization", the audio may be delayed with respect to the video. This is necessary because of the higher transmission delay caused by the video signal, due to the elaborate H.263 video compression. A delay of approximately 0.5 seconds is enough in most practical cases. To make maximum use of the existing memory in the system, the delay is performed by the video processor with its external RAMs.

When decoding MPEG bitstreams, the audio D/A conversion is provided by a stereo audio DAC.

1.7.2 Low Cost H.324 desktop videoconferencing with software video

A low-cost solution of the previous board does the video encoding/decoding in software on the host. See the following figure for low-cost H.324 desktop videoconferencing:

Introduction



The V.34+ modem can be either on board, thus building a modem with additional videophone functionality, or an existing external modem can be used. For a description of the ISAR-34 data pump and the ALIS programmable codec and DAA worldwide solution see section 1.7.1.

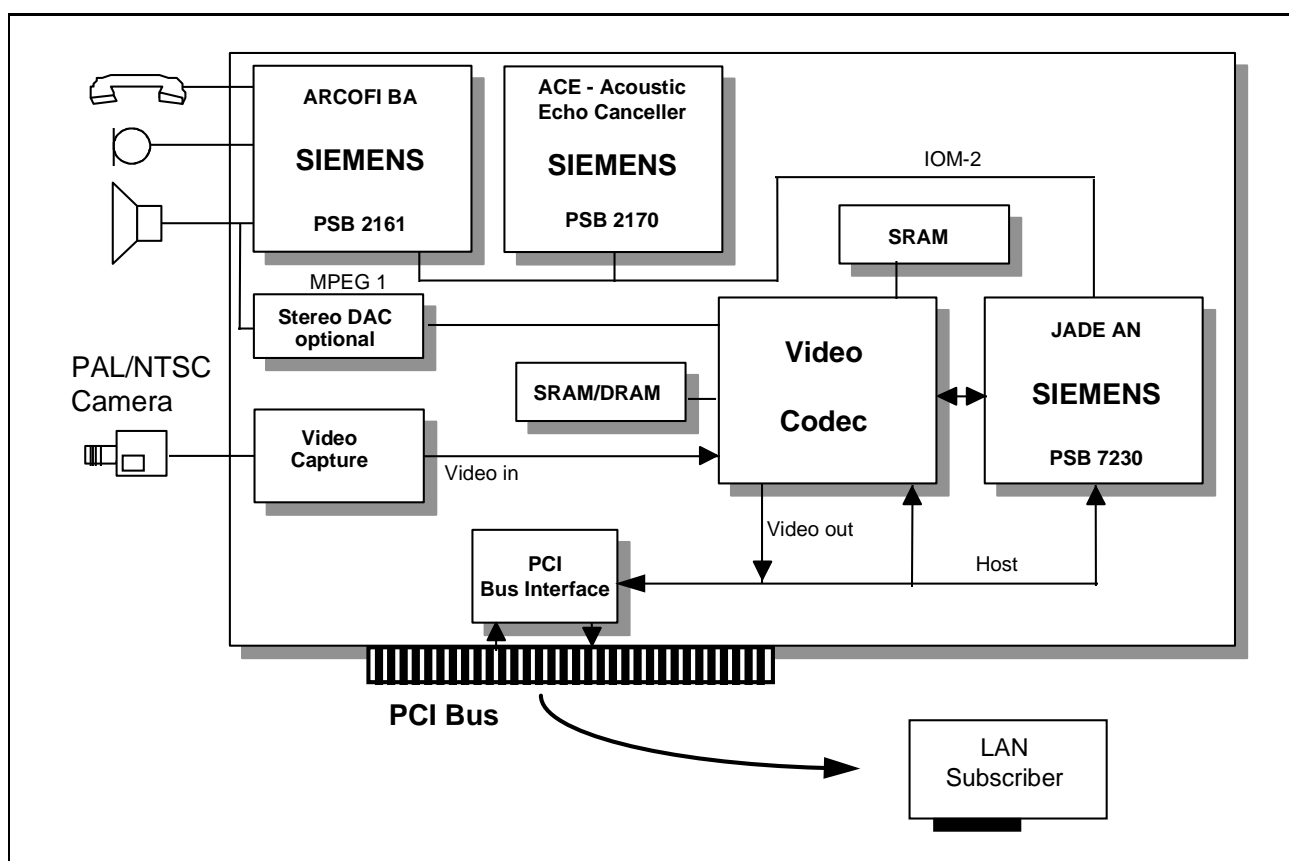
The audio compression is done by the JADE AN, thus providing high quality audio without noise or gaps when the operating system of the host processor is busy. For example when opening a DOS-Shell in a Microsoft Windows operating system, the JADE AN enables the system to have continuous audio without gaps or clicks.

As said, the video compression is done by the host processor, e.g. in a Microsoft Netmeeting system.

The Siemens SZB6120 PCI bus interface is compliant with PCI spec. 2.1. It has a glueless interface to video digitizers (e.g. SAA7110, SAA7111) and a DMA transfer of video bitstreams, thus enabling frame grabbing function. The JADE AN and the V.34+ modem are connected to the guest bus of the SZB6120.

1.7.3 LAN videoconferencing

For videoconferencing over LAN, usually high bandwidth is available, thus resulting in an advantage of hardware videocoding versus software video coding. In addition, high audio quality with acoustic echo cancellation is requested. See the following figure for a LAN videoconferencing board:



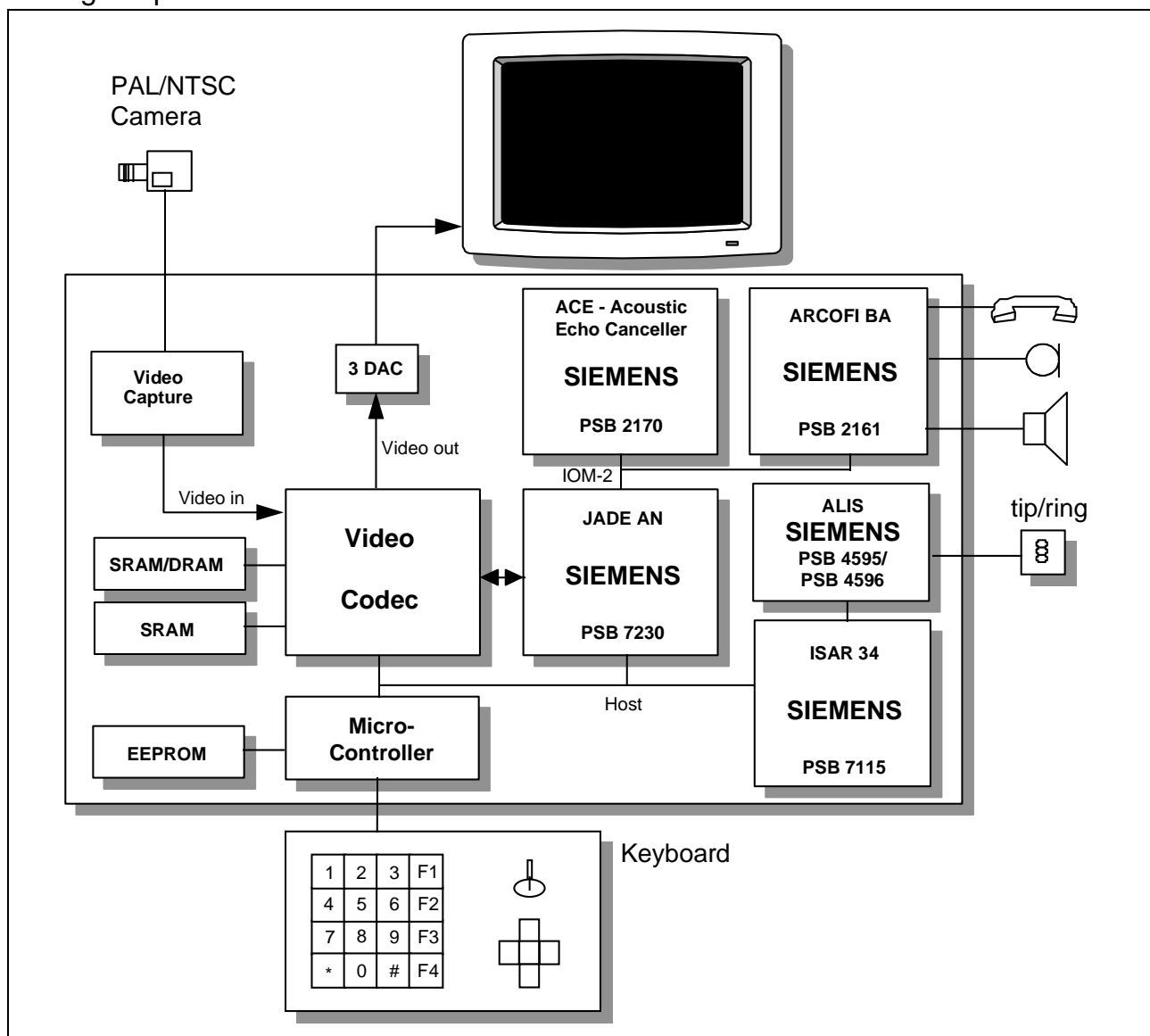
Since the line connection is off-board, all kinds of connections (ISDN H.320, POTS H.324 or LAN H.323) can be used with a single board. The LAN standard H.323 implements a correction mechanism for non-guaranteed quality of service, thus enabling also videoconferencing via Internet.

The audio input/output in this example is done via the Siemens ARCOFI BA (PSB 2161) and the Siemens ACE (PSB 2170), an acoustic echo canceller which implements two different algorithms (switchable) for minimum delay and maximum performance.

An MPEG playback possibility is optional in this example and can be skipped to reduce costs.

1.7.4 Standalone H.324/H.323 Videophone

The following example shows an H.324 (or H.323) standalone videophone solution for analog telephone line:



Compared to a PCI plug-in card a microcontroller, keypad and screen need to be added for a standalone videophone.

The initialization and keyboard control is done by the microcontroller. It substitutes the tasks of the host processor in the previous examples.

The screen (e.g. standard CCD device) is connected directly to the video codec via a 3 DAC.

The multiplexing of the video and audio bitstreams (H.223 or H.225) can be either done by the video codec or the microcontroller.

Introduction

For a description of the ISAR-34 data pump and the ALIS programmable codec and DAA worldwide solution see section 1.7.1.

The other components are already known from the previous examples, so please refer to the above descriptions for details.

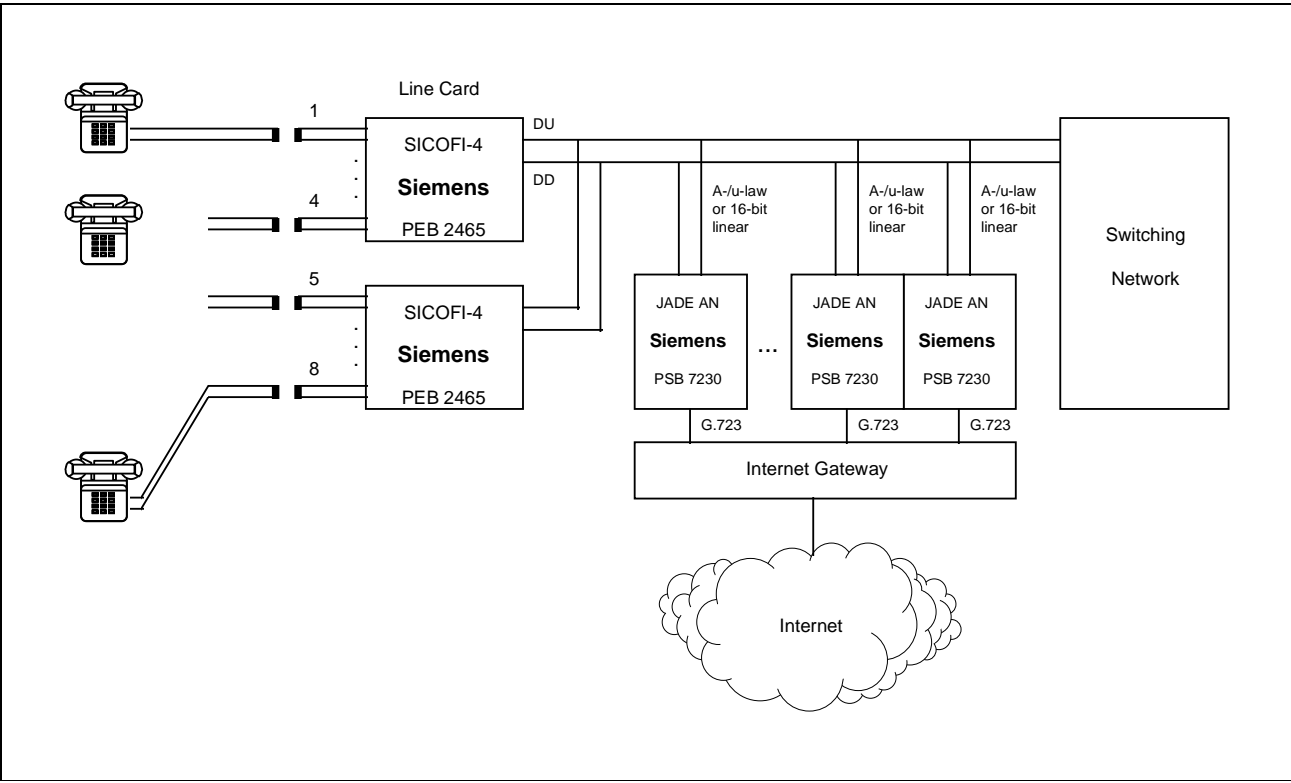
1.7.5 Internet Telephone Access in Line Card

The following figure shows an internet telephone access implemented in an analog line card of a common tip/ring line. There is no need for the user to buy a special internet telephone. With his old equipment he can use the internet for rate-reduced calls to overseas or to connect to a "true" internet telephone. At the beginning or even before a new call the user may select between the "standard" tarif via the switching network and a "reduced rate" tarif transferring speech via a packetized network such as internet.

Since the JADE AN does the voice compression/decompression complying to ITU-T G.723 standard, it can connect to any other telephone using the same standard (e.g. Microsoft Netmeeting).

The example below shows a line card with 8 subscribers. The number of JADE AN to connect to the internet may be selected between 1 and 8 - depending on the statistical usage of this kind of connection.

Alternatively, an internet access with voice compression can also be implemented in the switching network. This may offer an even better statistical distribution, thus optimizing the number of gateways needed.



Introduction

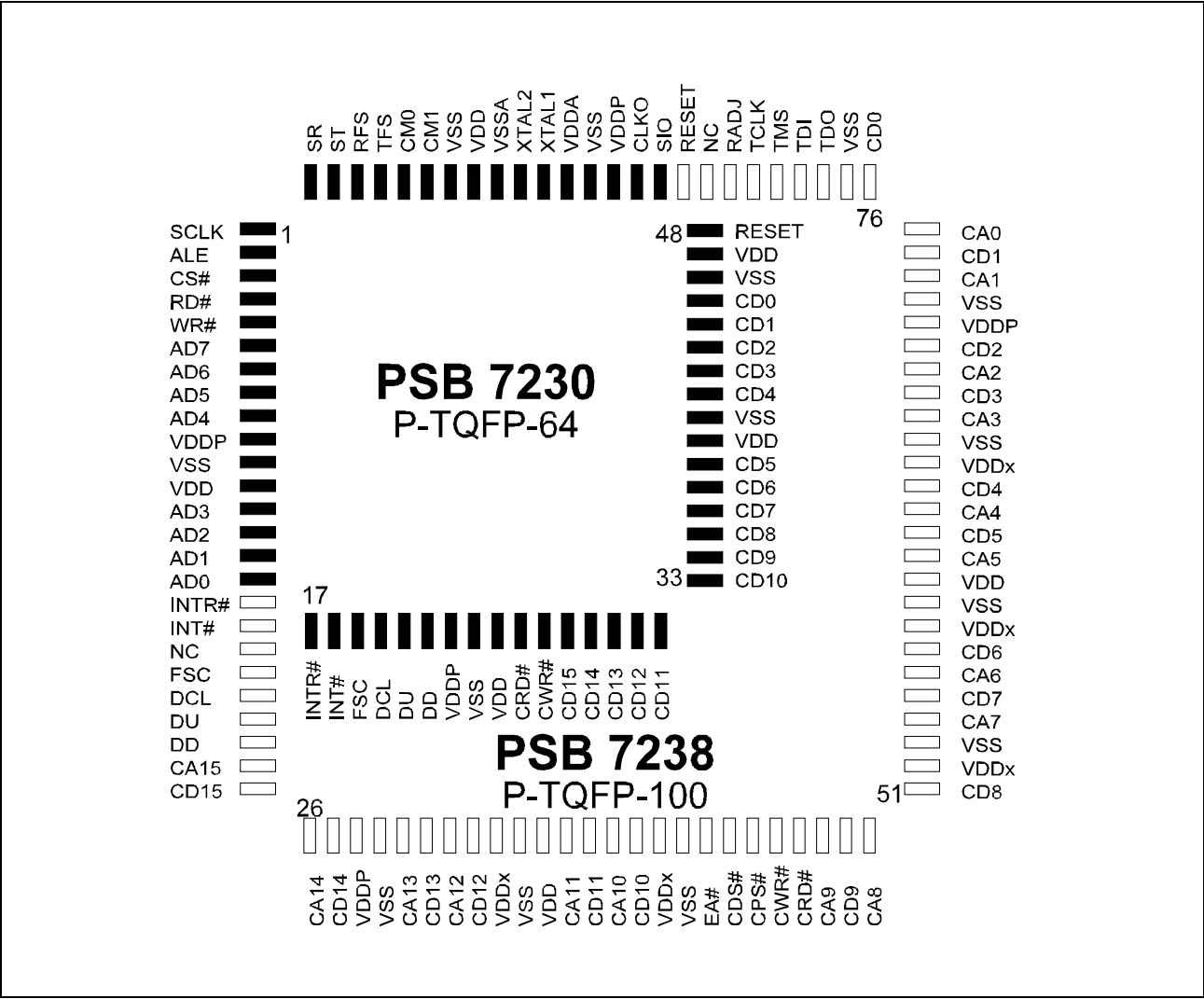
The same principle may also be used for ISDN lines, thus connecting common ISDN telephones to internet phones like Microsoft Netmeeting or using the internet for rate-reduced overseas connections.

Reference Board Designs:

For Reference board designs containing the mentioned components please contact Siemens.

1.8 Board Layout

The PSB 7230 offers the possibility of a combined and space optimized board layout with other JADE versions like PSB 7280 (JADE: G.711, G.722, G.728) and PSB 7238 (JADE MM: G.711, G.722, G.728, G.723) which are offered in P-TQFP-100 package. Thus, one board layout can be designed for multiple applications (POTS videophone, ISDN videophone, multimode videophone for ISDN and POTS). As an example, the combined board layout of JADE AN and JADE MM 1.2 is shown in the following figure:



The pins 1-16 and 49-64 of the P-TQFP-64 package are compatible with the 100-pin package of JADE and JADE MM like shown in the figure. This layout is also available in the "JADE Analog with Echo Cancelling Test Board", JANET (SIPB 7282), which is available from Siemens.

General Architecture and Functions

2 General Architecture and Functions

2.1 Architecture

The following figure shows a sketch of the PSB 7230 architecture with its most important functional modules.

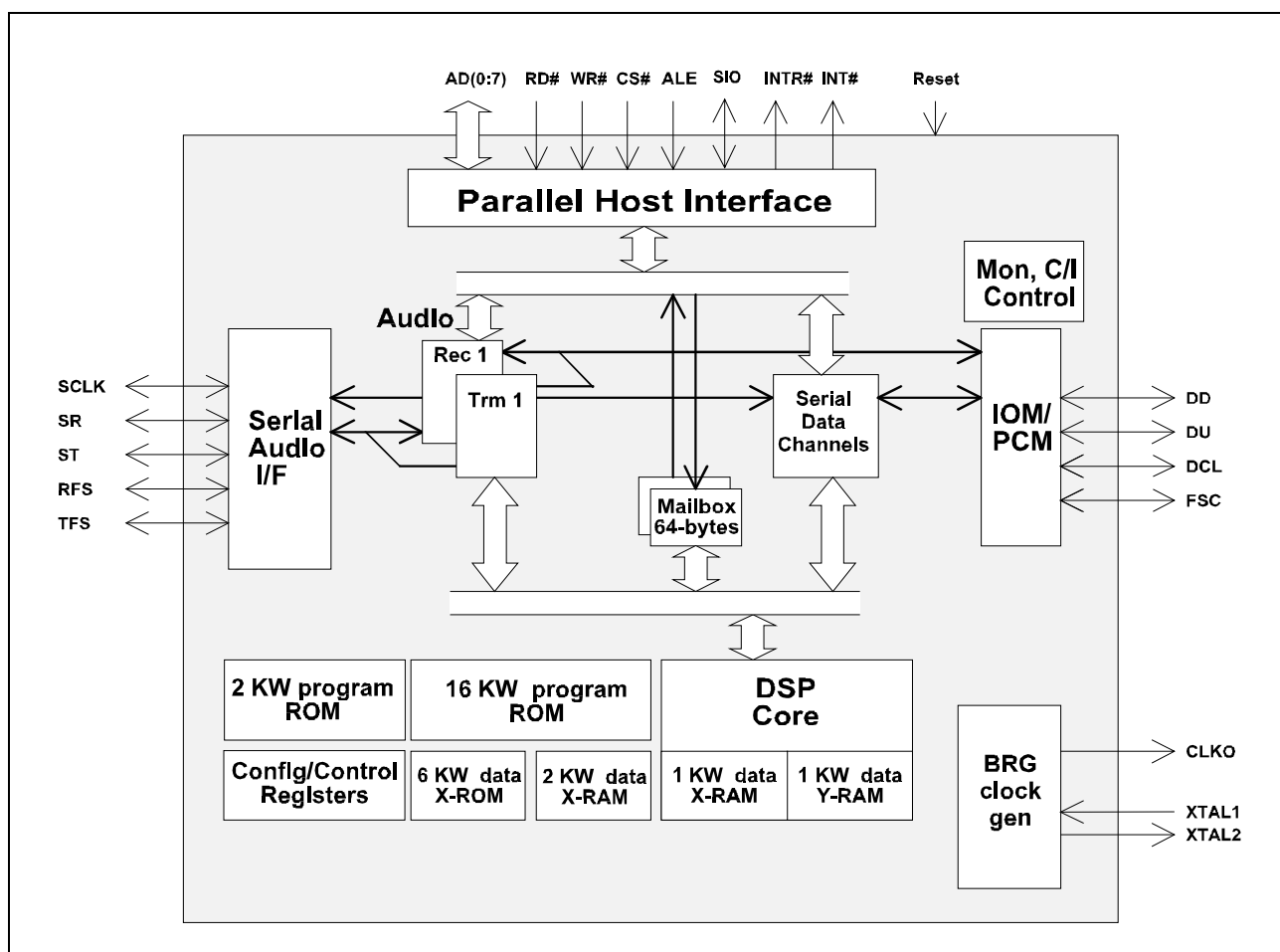


Figure 1

The audio processing of the PSB 7230 is based on a 16-bit fixed point DSP core, **SPCF (Signal Processor Core Fast)**.

The **Clock Generator** is responsible for generating the internal clocks for the SPC. A **Baud Rate Generator** provides an output clock of programmable rate.

The **Parallel Host Interface** is used to control the circuit through an associated host via interrupt handshake procedures. Alternatively, the circuit can be controlled via the Serial Audio Interface, thus enabling stand-alone applications to be implemented. Communication between the Host, if used, and the DSP is interrupt supported, via a full-duplex 64-byte on-chip **Communication Memory Mailbox**.

General Architecture and Functions

One receive and one transmit audio channel are provided. They are input/output on the **ISDN Oriented Modular** (IOM-2) or the **Serial Audio Interface** (SAI) interfaces in individually programmable time-slots. These channels are accessed from the DSP and/or the Parallel Host Interface.

The **Serial Data Controller** channels can be serviced by the DSP or the Parallel Host Interface. The serial data for the serial data controller is located in programmable time-slots on IOM-2 and/or SAI.

2.2 Functions

2.2.1 Summary of the Functions

The main functions implemented by the PSB 7230 are:

- G.723 V5.1 Compression/Decompression (6.3, 5.3 kbps)
- G.711 Compression/Decompression (64 kbps)
- Accepts/outputs uncompressed audio 8-bit PCM A/μ law or 16-bit linear format
- Uncompressed/compressed audio switchable between different interface combinations (IOM/Serial Audio Interface, IOM/Host, Host/Host)
- Inband controlled H.221/H.223 oriented audio protocol, e.g. for direct serial connection to Videocodec (VCP of 8x8 Inc., formerly IIT Inc.)
- Outband controlled audio protocol with optimized data rate
- Stable reaction on interrupt handshake timing violations of e.g. a slow host (Windows PC)

Details about these functions are given in **section 2.2.2**.

For more details on the hardware (necessary for a better understanding of some of the topics described in the present chapter), please refer to the other chapters of this Data Sheet.

2.2.2 Audio Functions and Supplementary Features

General

The uncompressed/compressed audio is applied to the interfaces as follows:

Uncompressed Audio:

IOM-2 (transparent)

IOM-2 (transparent)

Host IF (interrupt handshake protocol)

Compressed Audio:

SAI (H.221/223 oriented audio protocol or transparent)

Host IF (interrupt handshake protocol with minimized interrupt load for the host)

Host IF (interrupt handshake protocol)

"Transparent" means that data is received/transmitted in a time-slot without protocol.

1. Full duplex G.711 encoding/decoding of one audio channel

Audio coding according to ITU-T G.711 recommendation using Pulse Code Modulation (PCM, 64 kbps). A logarithmic function is used for coding of 8 KHz audio samples, thus offering a nearly constant S/N over the whole amplitude range. Two different laws are defined known as A- and μ -law.

2. Full duplex G.723 encoding/decoding of one audio channel

Audio coding according to ITU-T G.723 recommendation using Multipulse Maximum Likelihood Quantization (MP-MLQ, 6.3 kbps) or Algebraic Code Excited Linear Prediction (ACELP, 5.3 kbps). The high pass filter and the postfilter of the G.723 may be independently switched on or off. The implementation complies with the newest ITU-T C-Code V5.1 and contains Voice Activity Detection (VAD), Comfort Noise Generation (CNG) and Discontinuous Transmission (DTX).

3. Serial H.221/223 oriented audio protocol.

The PSB 7230 supports a serial H.221/223 oriented inband controlled audio protocol for direct connection to a Videocodec (e.g. VCP of 8x8 Inc.), which means the control data for compression mode, volume etc. is sent in a header preceeding the compressed data. This protocol provides an outband synchronization of the audio bit streams by using block structures for the compressed audio data.

Interfaces and Memory Organization

3 Interfaces and Memory Organization

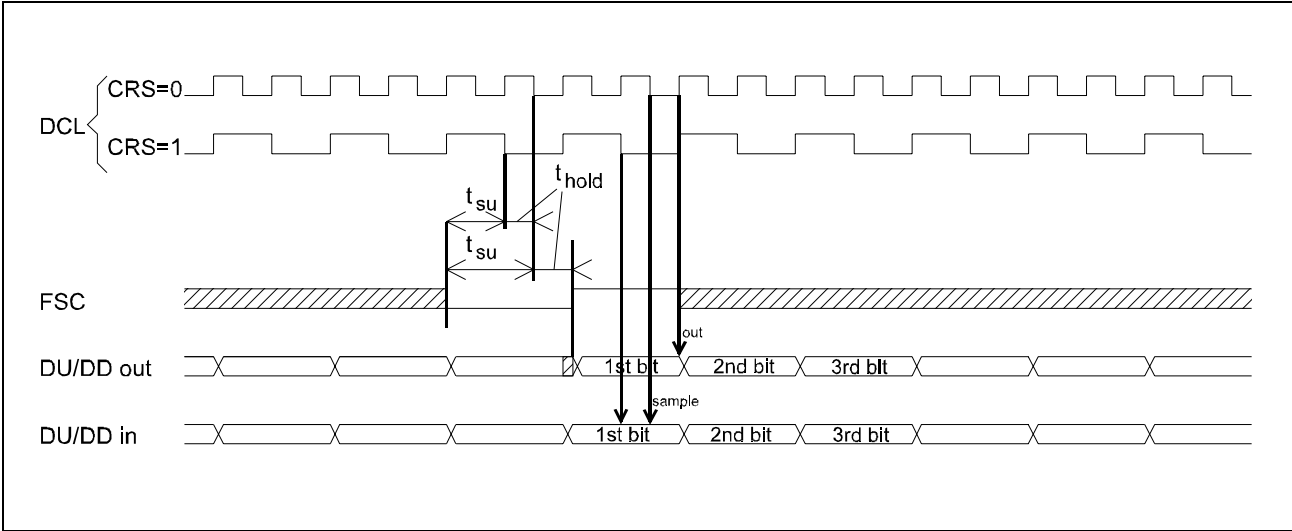
3.1 Interfaces

3.1.1 IOM-2 Interface

Electrical interface

The IOM-2 interface is a 4-wire interface with two data lines (DD and DU, programmable open drain or push-pull), a data clock line (DCL input/output) and a frame sync signal (FSC input/output). The data clock is by default equal to twice the data rate ("Double rate"). However, DCL may be set equal to the data rate ("Single rate") by programming. In terminal applications, the bit rate on the interface is normally 768 kbit/s, in line card applications it is 2048 kBit/s (for details, see IOM-2 Interface Reference Guide). However, the data rate may be different (between 16 kbit/s and 4.096 Mbit/s and the DCL rate correspondingly between 16 kHz and 4.096 MHz), since the interface can be considered as a general purpose TDM (Time-Division Multiplex) highway.

The total number of time slots on the interface is not explicitly programmed: instead, the FSC signal (at repetition rate 8 kHz) always marks the TDM physical frame beginning. See figure below for both IOM clock rates (CRS=0/1).



Interfaces and Memory Organization

DCL	Bits on DU/DD are clocked out with the rising edge of DCL and latched in with the falling edge of DCL. Frequency 16 kHz to 4.096 MHz.
FSC (8 kHz)	Marks the beginning of the physical frame on DU and DD. The first bit in the frame is output after the rising edge of FSC. The first bit in the frame is latched in with the first falling edge after FSC has gone "high" if CRS=1, or after the second edge (at 3/4) if CRS=0.

Interfaces and Memory Organization
Channels

The following channels may be programmed on the IOM-2 interface: one receive audio channel, one transmit audio channel, one Monitor channel, two C/I channels, one receive and one transmit data channel:

Audio receive channel	Independently programmable on DD or DU, with programmable locations (start at bit 1...512) and lengths (1...32 bits) w.r.t. FSC
Audio transmit channel	
Monitor channel	Programmable on DD(in)/DU(out) or DD(out)/DU(in), with programmable time-slot (3rd byte in multiplex 0, ..., 15) after FSC
Two C/I channels	Programmable on DD(in)/DU(out) or DD(out)/DU(in), with programmable length (4 or 6 bits) and position (4th byte in multiplex 0, ..., 15) after FSC
Data receive and transmit channels	Independently programmable on DD or DU, with programmable locations (start at bit 1...512) and lengths (1...256 bits) w.r.t. FSC

The transfer of voice samples is performed with the help of an interrupt with repetition rate 8 kHz derived from the FSC signal. A double-buffered register is provided for each channel, accessible from the DSP and from the parallel host interface. The double buffered register ensures that enough time is always provided for reading and writing data before an overflow/underflow occurs, independent of the location of the time-slots. Alternatively, the audio samples can be transferred between the DSP or Host and IOM-2 by using an interrupt generated when a programmable number (1...32) of bits are shifted out (number independent of the time-slot length on the line).

Outside the time slots where transmission takes place the DU and DD lines are in high impedance.

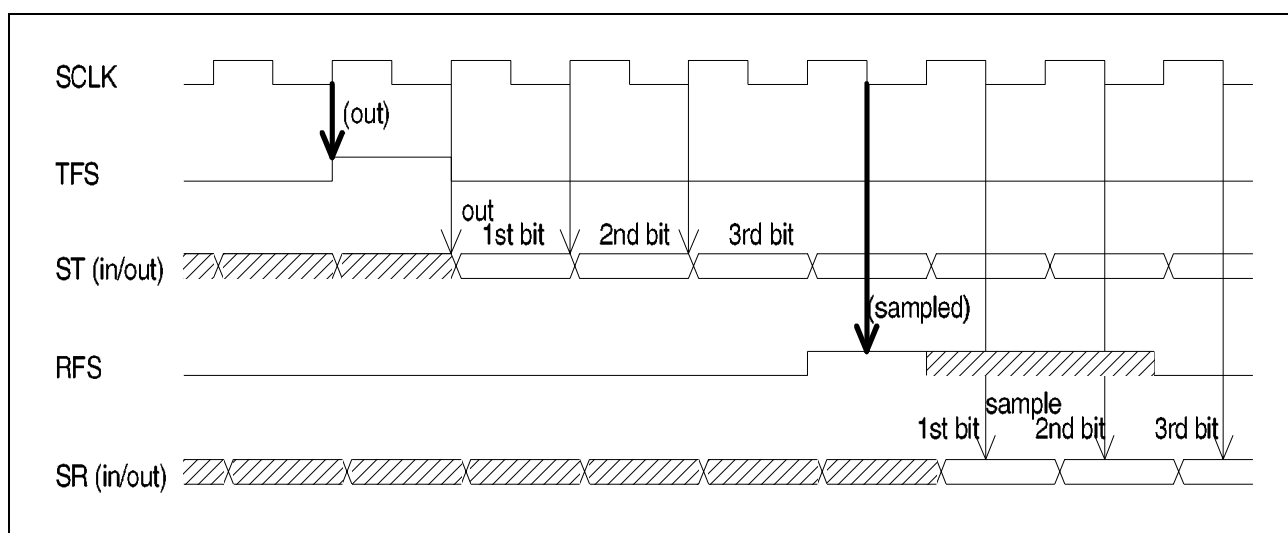
Interfaces and Memory Organization

3.1.2 Serial Audio Interface

The Serial Audio Interface is a generic 5-line serial interface with the following lines:

SCLK	Serial bit clock	Input or Output
SR	Serial Receive	Input/Output
ST	Serial Transmit	Input/Output
RFS	Receive Frame Sync	Input or Output
TFS	Transmit Frame Sync	Input or Output.

The following figure shows an example where RFS is input and TFS is output.



Interfaces and Memory Organization

SCLK Input or output

Bits on SR/ST are clocked out with the rising edge of SCLK and latched in with the falling edge of SCLK. When SCLK is programmed as output, it is derived from a programmable baud rate generator.

RFS Input or output

Marks the beginning of the physical frame on SR.

When input: Sampled with a falling edge of SCLK

When output: Clocked out with the rising or falling edge of SCLK
(duration = 1 SCLK period).
Repetition rate (continuous mode) or number of
pulses (burst mode) is programmable

TFS Input or output

Marks the beginning of the physical frame on ST.

When input: Sampled with a falling edge of SCLK

When output: Clocked out with the rising or falling edge of SCLK
(duration = 1 SCLK period).
Repetition rate (continuous mode) or number of
pulses (burst mode) is programmable

SCLK is derived from the chip-internal DSP clock via a programmable baud rate generator (division factor 1, 2, 3, ..., 1024).

The Receive Frame Sync (RFS), when programmed as output, has two selectable modes of operation:

- In the **continuous mode** (CONT=1), pulses are continuously generated, separated by a distance $16 \cdot (\text{PRD} + 1)$ bits from each other, where PRD=0, ..., 255.
- In the **burst mode** (CONT=0), pulses are generated upon command a programmable number of times (REP+1: 1, ..., 1024), spaced 16 bits apart from each other.

The same applies to TFS when it is an output.

Interfaces and Memory Organization**Channels**

Audio receive and transmit channels	Independently programmable on SR, ST, DU or DD with programmable locations (start at bit 1...512) and lengths (1...32 bits) with respect to RFS/TFS
Data receive and transmit channels	Independently programmable on SR, ST, DU or DD with programmable locations (start at bit 1...512) and lengths (1...256 bits) with respect to RFS/TFS

3.1.3 Parallel Host Interface

A multiplexed address/data bus on the host interface is provided, with control signals \overline{CS} , \overline{WR} , \overline{RD} , ALE.

3.1.4 Clock Interface

The chip internal clock is derived from a crystal connected across XTAL1,2 or from an external clock input via pin XTAL1. The internal frequency is directly input via XTAL1(,2). When using a crystal, a 28.416 MHz crystal swinging at its basic harmonic has to be connected to XTAL1,2.

The clock mode pins CM(1-0) have no function in JADE AN, nevertheless they maybe connected to either V_{SS} or V_{DDP} for compatibility reasons (combined board layout, see section 1.8) with other JADE devices.

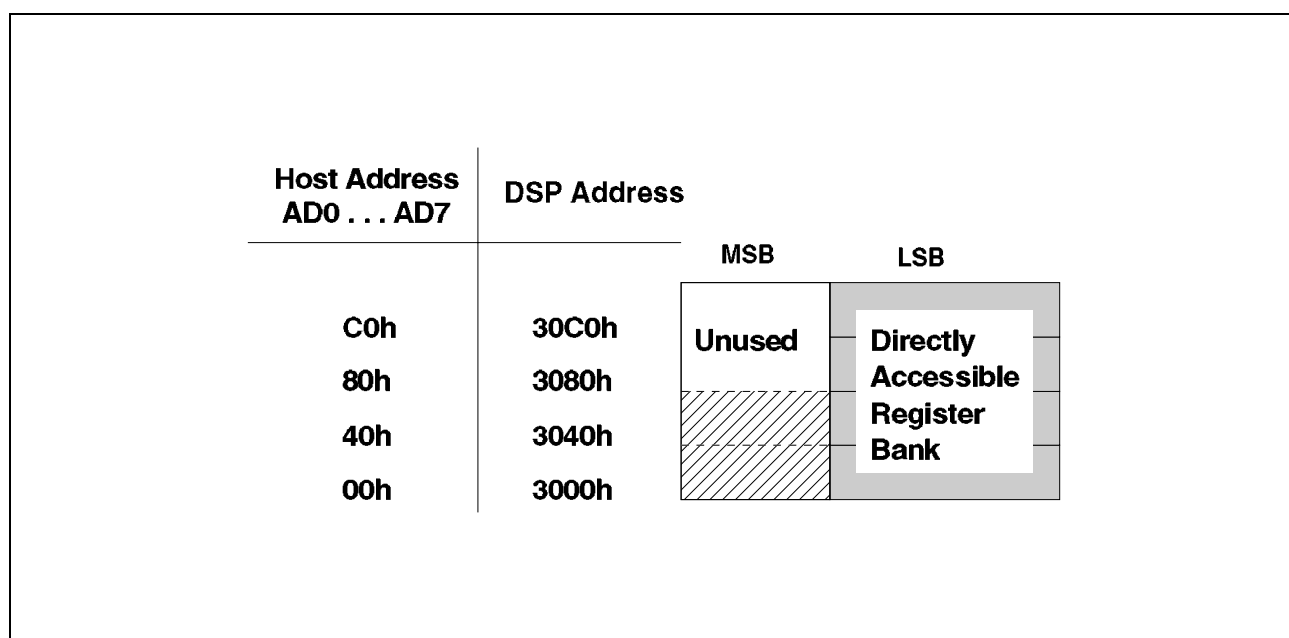
After Reset the pin CLK0 outputs the buffered XTAL1 frequency (28.416 MHz). Alternatively, CLK0 can be programmed to output the frequency of a programmable divider (CKOS bit in register 2002h). Thus, a clock of frequency equal to the internal clock divided by a programmable baud rate factor (1, 2, 3,..., 2^{19}) can be generated.

3.2 Shared Memories

Note: The absolute addresses for the different internal register banks and memories are given here and in the rest of this Data Sheet both as seen from the host **and** from the embedded DSP, the latter information being included for the sake of completeness only.

Directly Accessible Register Bank (DARB)

The Host accesses directly via its 8-bit address bus the so-called **Directly Accessible Register Bank (DARB)** located between DSP addresses 3000_H and 30FF_H.



This area is in turn divided into four blocks of 64 bytes each according to their functions:

1. Locations for reading and writing samples "in real time" from/to the serial interfaces (IOM-2 and Serial Audio Interface) - **Input/Output area**
2. Area for communication between the host and the embedded DSP, for programming parameters and reporting status conditions - **DSP/Host Com area**
3. Register bank for Serial Data Controller - accessed by host if HHA1 (Configuration bit) is "1" - **SDATA**
4. Reserved for future expansion.

See figure below.

Host	DSP	MSB	LSB
C0h	30C0h	Unused	Reserved
80h	3080h		SDATA
40h	3040h		DSP/Host Com
00h	3000h		Input/Output

Not all the addresses in each of these 64-byte areas are used. The functions of the register banks are detailed in the following paragraphs.

3.3 Directly Accessible Register Bank

3.3.1 Input/Output Registers

This area contains the locations for receiving/transmitting real-time audio and data between the serial interfaces (IOM-2 and Serial Audio Interface) and the Host (or embedded DSP).

The PSB 7230 implements one receive and one transmit audio channel, denoted RC1 and XC1, respectively. Further, one receive and one transmit channel is provided to access the serial data receiver input data and the serial data transmitter output, respectively, called HR1 and HX1.

Transfer of audio samples is interrupt supported, whereby two possibilities are provided:

- interrupt status generated after a programmable number of bits (1, ..., 32) have been shifted in/out;
- interrupt indicating the start of a physical frame (normally at 8 kHz, either from FSC, RFS or TFS frame sync pulses): in this case the number of significant bits depends on the time-slot length programmed for that channel on the line (DU/DD/SR/ST).

The interrupt statuses may generate a maskable interrupt on the high priority interrupt lines $\overline{\text{INTR}}$ (Host) and/or INT0 (embedded DSP), respectively.

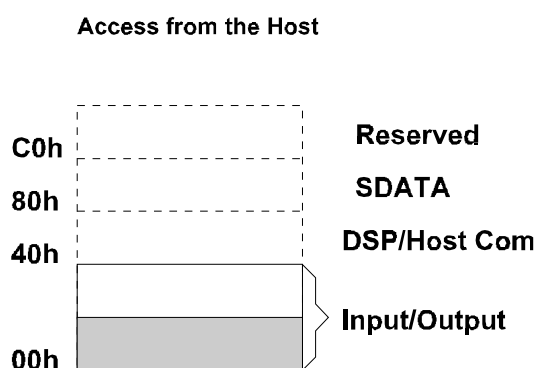
RC1, XC1, HR1, HX1 channel registers are located in the address range $00_{\text{H}}-3\text{F}_{\text{H}}$ for the Host, and in the memory mapped area $3000_{\text{H}}-303\text{F}_{\text{H}}$ for the DSP. The register banks for the Host and the DSP are physically separate from each other. The read registers and write registers are physically separate.

The addresses for these registers are such that a 32-bit sample can be accessed from the DSP via only two 16-bit read/write operations (16-bit data bus). From the Host, the access is byte by byte (8-bit data bus).

List of registers:

- RC1: 32-bit register for audio receive channel 1 (read)
- XC1: 32-bit register for audio transmit channel 1 (write)
- HRR1: 32-bit register for reading data from Data Receiver input shift register
- HRW1: 32-bit register for writing data to be loaded into Data Receiver input
- HXR1: 32-bit register for reading data from Data Transmitter output
- HXW1: 32-bit register for writing data to Data Transmitter output shift register

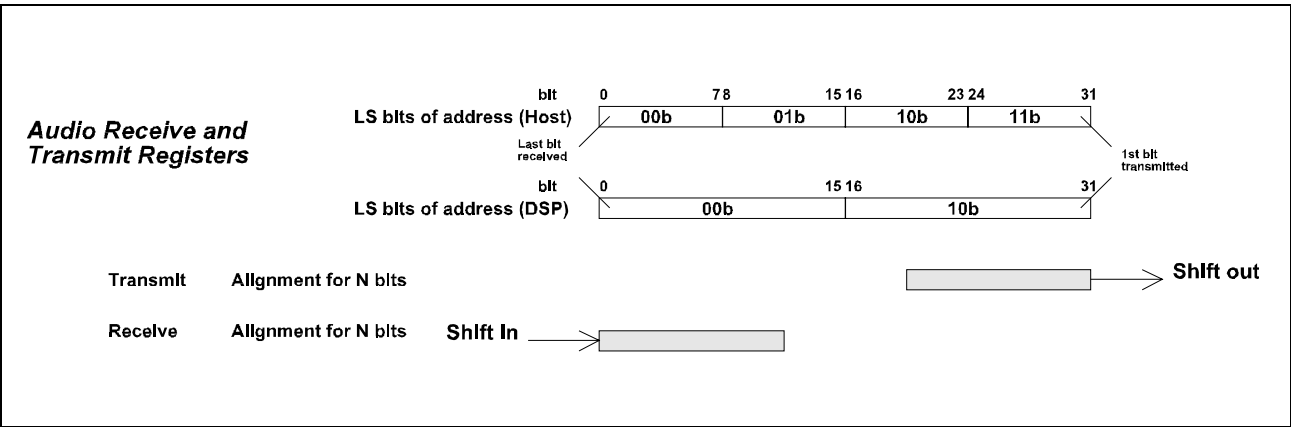
Memory map:



Host Address A0 - A7	Host Write	Host Read
17h	HXW1 (31:24)	HXR1 (31:24)
16h	HXW1 (23:16)	HXR1 (23:16)
15h	HXW1 (15:8)	HXR1 (15:8)
14h	HXW1 (7:0)	HXR1 (7:0)
13h	HRW1 (31:24)	HRR1 (31:24)
12h	HRW1 (23:16)	HRR1 (23:16)
11h	HRW1 (15:8)	HRR1 (15:8)
10h	HRW1 (7:0)	HRR1 (7:0)
	.	.
03h	XC1 (31:24)	RC1 (31:24)
02h	XC1 (23:16)	RC1 (23:16)
01h	XC1 (15:8)	RC1 (15:8)
00h	XC1 (7:0)	RC1 (7:0)

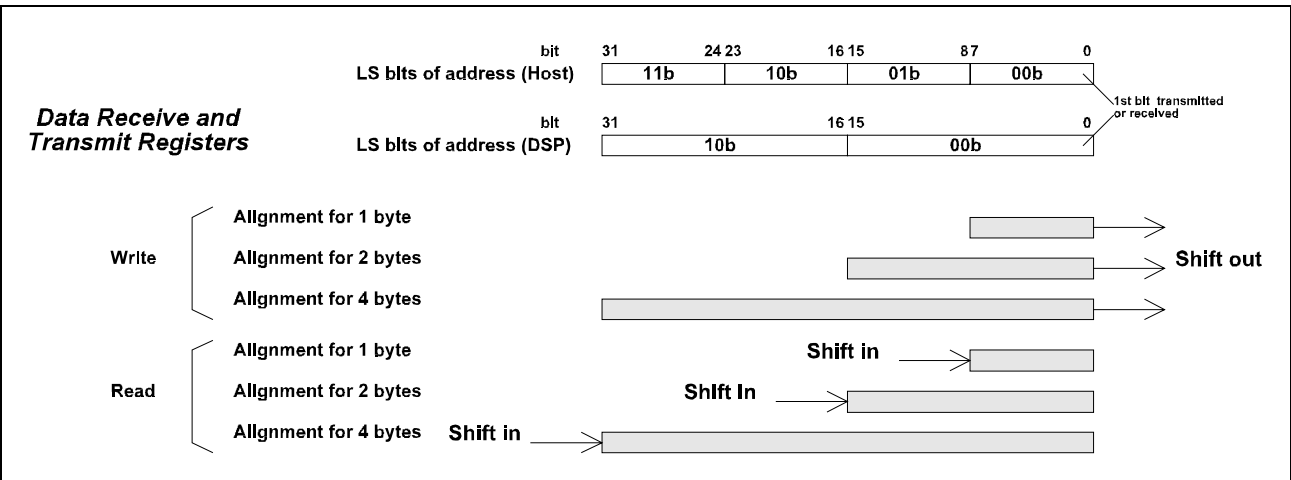
Alignment of data for Audio channel:

The most significant bit is always the first bit received/transmitted. Therefore, if audio is processed in units of N bits (N programmable between 1 and 32), the alignment of the data for receive and transmit audio channels in the registers is as shown in the **figure below**.



Alignment of data for serial Data channel:

In the serial data controller the reception/transmission of most significant or least significant bit can be selected by control switches (RMSB, XMSB). Nevertheless, for serial data communication, the convention is that the least significant bit of user data is received/transmitted first. In order to have an identical format for the data in the serial controller input/output registers as in the FIFOs, the data is aligned in the registers as shown below (the available options for data unit sizes when pre/postprocessing data are: 1, 2 or 4 bytes).



3.3.2 DSP/Host Com Area

The DSP/Host communication area contains the registers to support hardware and software interrupts and special purpose registers that support communication between the embedded DSP and the Host, in particular for indirect programming of the Configuration and Control registers from the host (**see figure below**).

DSP (16 bit)			Host (8 bit)		
DSP Address	DSP Write	DSP Read	Host Address A0 - A7	Host Write	Host Read
3076h MSB 3076h LSB 3074h MSB 3074h LSB 3072h MSB	Acknowledge registers		FFh	reserved	reserved
			FEh		
	Interrupt Mask registers	Interrupt registers	77h	Acknowledge registers	
			76h		
	Acknowledge register		75h	Interrupt Mask registers	Interrupt registers
3070h MSB 3070h LSB	Interrupt Mask registers	Interrupt registers	74h	Acknowledge register	
			73h		
			71h	Interrupt Mask registers	Interrupt registers
			70h		
			6Ch	reserved	reserved
3061h 3060h	Control DSP->Host MSB	Control Host->DSP MSB	6Ah	reserved	reserved
	Control DSP->Host LSB	Control Host->DSP LSB	61h	Control Host->DSP MSB	Control DSP->Host MSB
			60h	Control Host->DSP LSB	Control DSP->Host LSB
			58h		
3058h	IND Int. Status	INDB		INDB	IND Int. Status
3050h					
			50h	INH Int. Status	INHB
			4Ch	Mallbox I/O write (vIrt)	Mallbox I/O read (vIrt)
			4Ah	Mallbox write address	Mallbox write address
3041h 3040h			48h	Mallbox read address	Mallbox read address
	Reg Data DSP->Host	Reg Data Host->DSP	41h	Reg Data Host->DSP	Reg Data DSP->Host
			40h	Conf/Cont Reg Address	

The functions of these registers are described below.

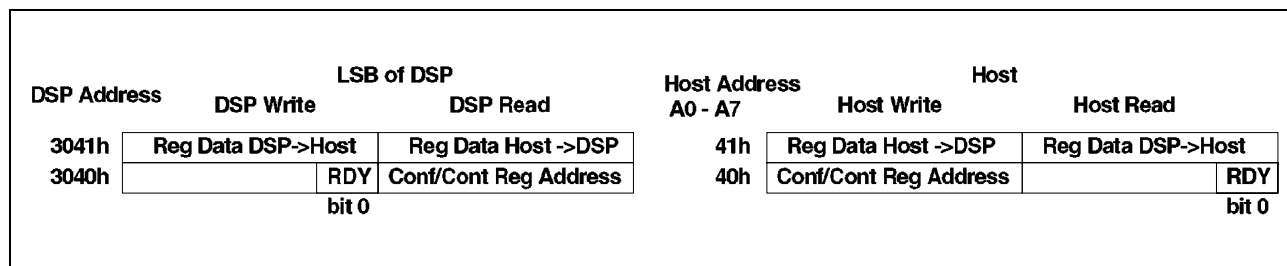
Indirect Access to Configuration and Control Registers

Writing of hardwired registers (Configuration and Control registers) in the DSP memory (from 2000_H to 203F_H) can be effected through the Parallel Host Interface.

For the last case two directly accessible locations are provided in the DSP/Host Com area (Host addresses 40_H and 41_H). A write operation in the first of these registers with

a command (read/write) and a 6-bit address offset will cause the DSP to read or write a configuration/control register in address space 2000_H - $203F_H$. The second location (Host address 41_H) contains the data read/written from/to the requested location.

The procedure is described in the following figure.



For reading a register from address $(2000_H + a5:0)$	<p>Host writes byte: 1 0 a5 a4 a3 a2 a1 a0 to address 40_H. This causes RDY bit to be set to 0. Internally, an RACC interrupt status (INT1 line) is generated to the DSP.</p> <p>Firmware: DSP reads address 3040_H, recognizes a "read" access (most significant bit = 1), fetches data from $(2000_H + a5:0)$, writes into 3041_H and sets RDY bit (address $3040_H/40_H$) to "1". After polling RDY bit to be "1", the host can read the data from 41_H, and access 40_H for another operation.</p>
For writing a register at address $(2000_H + a5:0)$	<p>Host writes data into address 41_H. Host writes byte: 0 0 a5 a4 a3 a2 a1 a0 to address 40_H. This causes RDY bit to be set to 0. Internally, an RACC interrupt status (INT1 line) is generated to the DSP.</p> <p>Firmware: DSP reads address 3040_H, recognizes a "write" access (most significant bit = 0), fetches data from 3041_H, writes it into $(2000_H + a5:0)$, and sets RDY bit (address $3040_H/40_H$) to "1". After polling RDY bit to be "1", the host can access 40_H for another operation.</p>

Software Interrupts

For communication between the host software and the DSP software, the soft interrupt registers IND (from DSP to Host) and INH (from Host to DSP) can be used.

Interrupt from Host to DSP

A write operation by the Host to address 50_H (INH) causes a maskable INH interrupt status to be generated on INT1 to the DSP, and the Interrupt Host Busy bit INHB (address 50_H , readable by host) to be set to "1". Having recognized an INH interrupt status, the DSP (firmware) reads address 3050_H (INH). This read operation automatically resets the HINT interrupt status bit in the DSP Interrupt Status Register for INT1 (address 3074_H). The INHB bit can be written by the DSP again to "0" to indicate that it is ready to accept a new interrupt from the host, which it would usually (but not necessarily) do after it has read the INH register. The 16-bit Control register located at $60/61_H$ ($3060/3061_H$) may contain additional information for the DSP to read after an INH interrupt. Please refer to the specific interface procedures for details.

Interrupt from DSP to Host

For a soft interrupt from the DSP to the host, the procedure is identical. In this case, the soft interrupt is a maskable interrupt on line \overline{INT} . The interrupt vector is written by the DSP in address 3058_H (IND). Simultaneously, the Interrupt DSP Busy bit INDB (address 58_H , writable by host) is set to "1". Having recognized an IND interrupt status, the host reads address 58_H (IND), which automatically resets the DINT interrupt status bit in the Host Interrupt Status Register for \overline{INT} (address 75_H). The INDB bit can be written by the host again to "0" to indicate that it is ready to accept a new interrupt from the DSP. The 16-bit Control register located at $60/61_H$ ($3060/3061_H$) may contain additional information for the host to read after an IND interrupt. Please refer to the specific interface procedures for details.

Registers pertaining to the Mailbox

The function of these host registers is described in detail in the next section.

Hardware Interrupt Registers

In the following the interrupts for the Host are listed, as well as, for completeness, those for the embedded DSP.

The interrupts are grouped so that the high priority interrupt statuses may cause a maskable interrupt on \overline{INTR} ("Interrupts Real-time" for Host) and/or INT0 (DSP), and the lower priority interrupt statuses on \overline{INT} (Host) and/or INT1 (DSP).

High priority interrupts ($\overline{INTR}/INT0$):

FSC, RFS, TFS

BFUL1, BEMP1, BFHR1, BFHX1

Lower priority interrupts ($\overline{INT}/INT1$):

SAIN

SDATA

HINT (to DSP) or DINT (to Host)

RACC (to DSP only)

MDR, MER, MDA, MAB, CIC1, CIC2

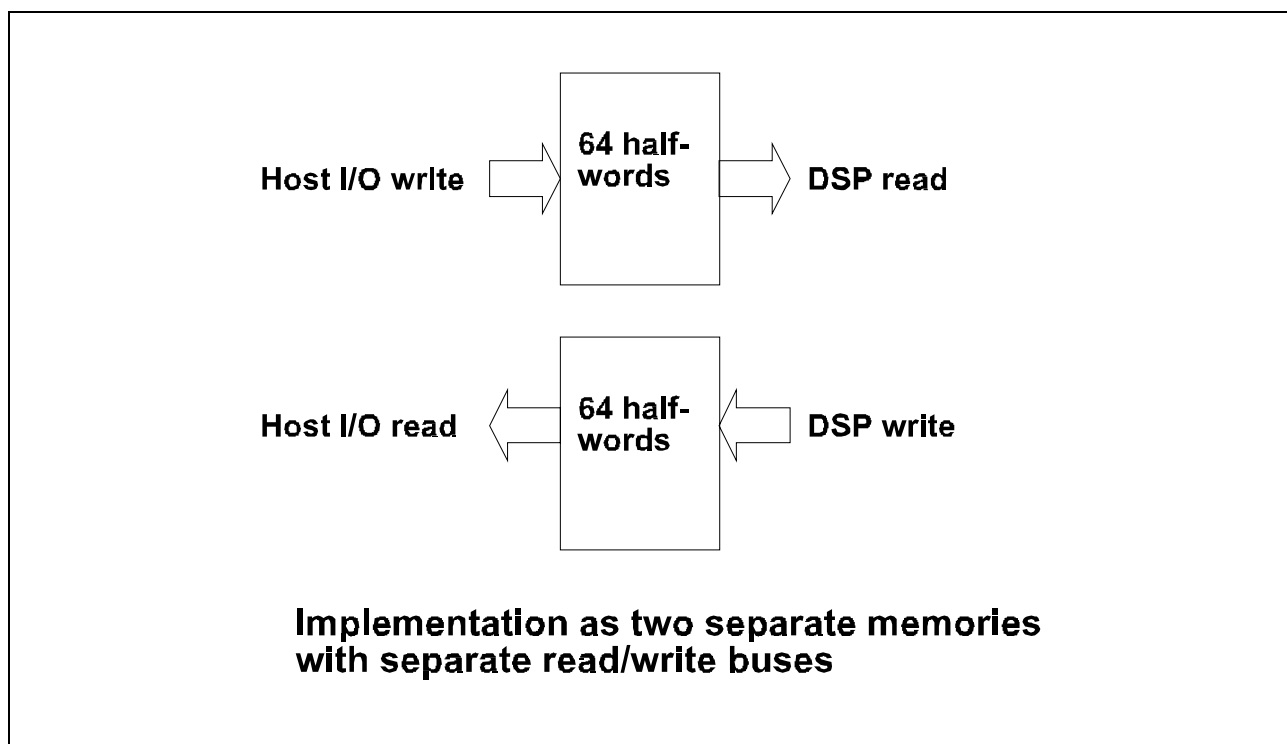
The active level of $\overline{\text{INTR}}$ and $\overline{\text{INT}}$ lines is "low", of INT0 and INT1 "high".

The interrupt line will remain active as long as an interrupt status (if unmasked) is not explicitly acknowledged, or the cause of the interrupt status has not been removed.

The registers for the interrupt status as well as the Configuration and Control registers (from address 2000_H upwards) are described in detail in **section 5**.

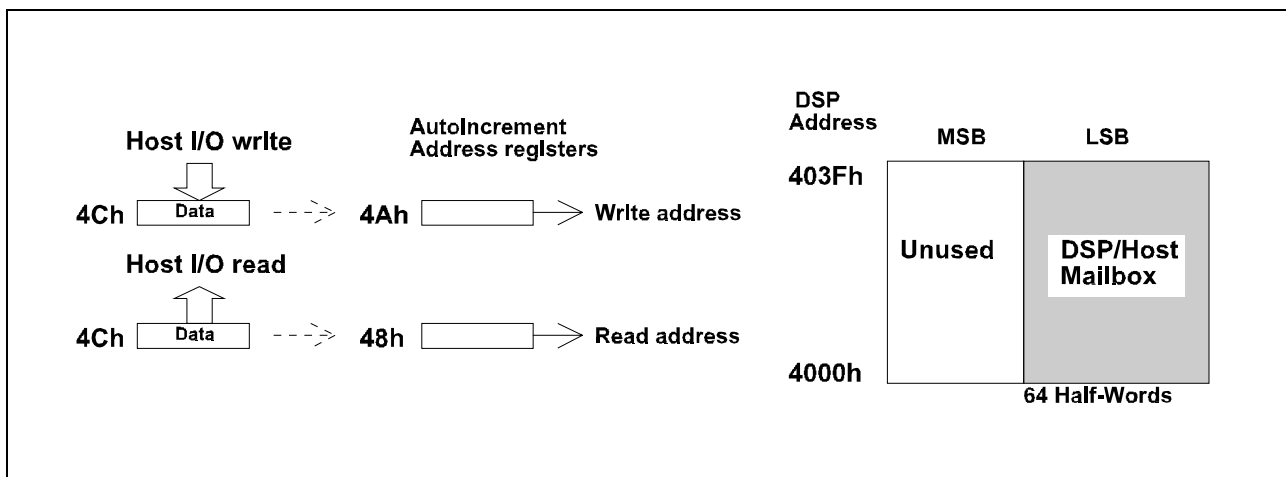
3.4 Mailbox

The Mailbox is implemented as physically two separate 64-byte memory blocks. Only least significant bytes are used. One is read-only by the DSP and write-only by the host, the other is write-only by the DSP and read-only by the host.



Since the two memories are totally independent, data transfer from host to DSP can take place simultaneously with data transfer from DSP to host (full duplex operation).

The Mailbox is seen from the host as an I/O device. Thus, to read or write a byte in the Mailbox, the host accesses a single location (separate for read and for write Mailbox). The address is given by an address register directly programmable by the host. This address is autoincremented every time an access by the host to the Mailbox I/O address is performed. Thus, for sequential, fast access, the Mailbox is seen as a 64-byte, full duplex FIFO. For random accesses to the Mailbox the Host has to reprogram the address register(s). This is summarized in the **following figure**.



I/O access from the host to the Mailbox (Summary):

Read

Host programs the desired start address (00_H to 3F_H) into address register 48_H.

Loop:

A read access from Host to 4C_H gives the data from the current location in the read Mailbox pointed to by the address register in 48_H.

The address register is autoincremented.

Go to Loop.

Write

Host programs the desired start address (00_H to 3F_H) into address register 4A_H.

Loop:

A write access from Host to 4C_H writes the data into the current location in the write Mailbox pointed to by the address register in 4A_H.

The address register is autoincremented.

Go to Loop.

(In the case of overflow, the address register 48_H or 4A_H wraps around to 00_H.)

Software handling of communication via Mailbox:

To indicate that data is ready to be read by the host/DSP, the DSP/host may use a general purpose 8-bit interrupt register located in the Host/DSP Comm section of the Directly Accessible Register Bank (DARB), associated with a 16-bit soft command and status word in the same area. This protocol is implemented in software. The same applies for indicating to the host/DSP that data has been read, in other words, the memory in one direction is free. See Example below for using the Mailbox involving a handshake protocol between the DSP and the Host.

Simultaneous read/write is not prohibited by hardware, but a handshake mechanism (via IND/INH software interrupt registers with optional Control Data) is implemented in software.

Procedure from Host to DSP (example):

Host:

Write Mailbox (1 to 64 bytes) if free (released by DSP)

Write word in Control register (60-61_H) (e.g. number of bytes in Mailbox)

Write 8-bit vector in INH

Internally, this causes an INT1 interrupt to DSP, which recognizes a "soft interrupt" (firmware)

DSP: services INT1 and acknowledges by writing an 8-bit vector in IND

Host:

Read IND

Jump into routine pointed to by IND: "Mailbox release"

Write further data, etc.

4 Functional Blocks

4.1 Oscillator and Baud Rate Generator

Clocking modes:

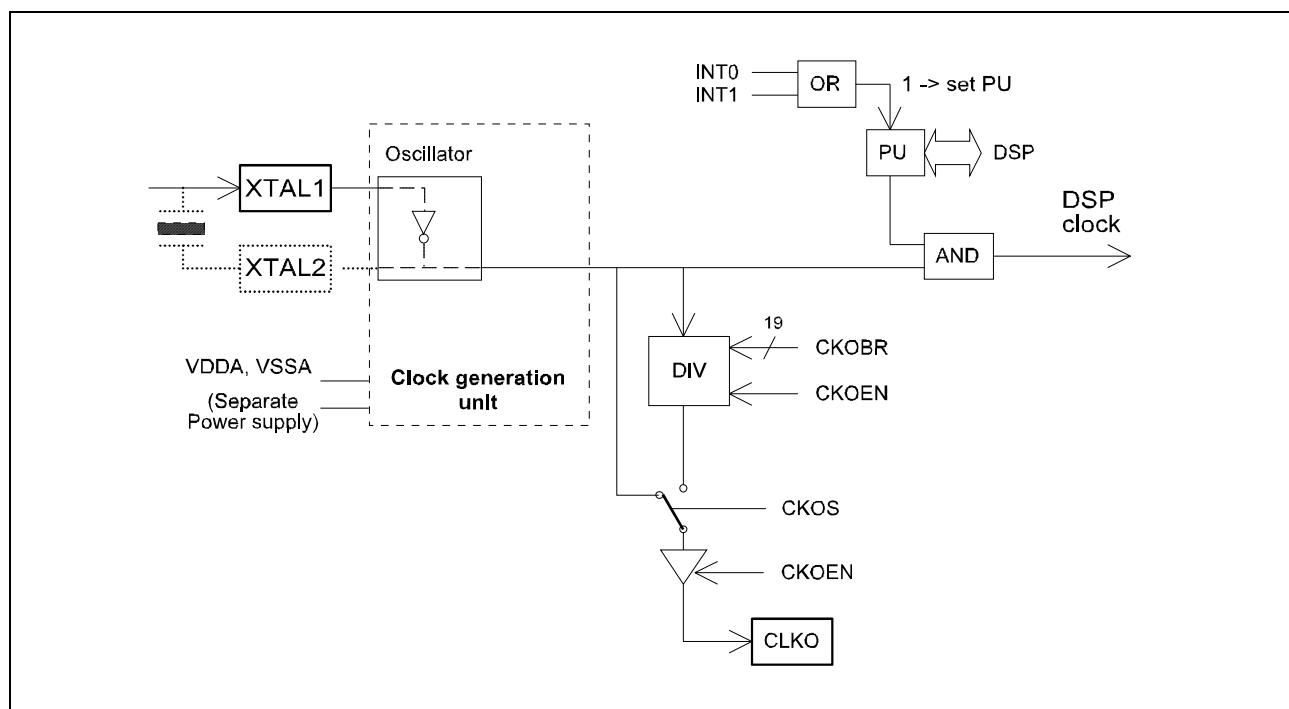
The Clock Generator generates the internal master clock derived from an input clock (or crystal) on pins XTAL(1:2).

Because of integrated decoupling capacitors, DC components of the input frequency on XTAL(1:2) are filtered out. Consequently, for a crystal input (nearly a sinusoid), an internal clock of nearly 50 % duty cycle results.

The internal frequency is directly input via XTAL1(,2). When using a crystal, a 28.416 MHz crystal swinging at its basic harmonic has to be connected to XTAL1,2.

For the clock generation unit a separate supply voltage pin (V_{DDA}) and a separate ground pin (V_{SSA}) are provided.

The block diagram of the clock circuitry is shown in the **figure below**.



For a proper initialization the required total length of the RESET is 1 msec.

Note: After a hardware reset, the JADE firmware needs to initialize its internal memories and interfaces. The time to do this is less than 10 msec. The user must take care to access the JADE only after this initialization phase is completed, i.e. 10 msec after the hardware reset.

Functional Blocks

Power-down:

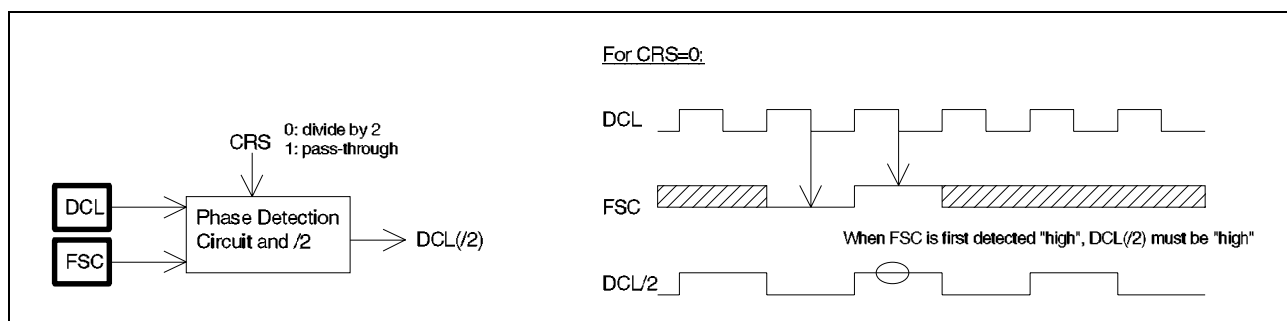
The actual chip internal clock ("DSP clock") is gated with the PU bit in the General Configuration/Control register. Thus, when PU is set to "0" (either via the host or the DSP), clock distribution is stopped and the DSP is disabled. In this mode the power consumption is minimum (software power-down). Only an interrupt to the DSP (on INT0 or INT1) can restart the DSP clock.

The oscillator is not affected by the PU bit, but it is always active. Because of the reset procedure above, the initial state of the PU bit is "1".

IOM-2 Clocks:

The IOM-2 clocking is either provided by separate timing inputs DCL and FSC, independent of the other clocks, or maybe generated by the JADE itself (CGEN bit in register 202Bh). When generated by the JADE, only double rate clocking in TE mode (DCL=1.536 MHz, FSC=8 KHz) is supported.

When input, the DCL clock frequency is either equal to the data rate on DD/DU (if Clock Rate Select bit CRS=1) or twice the bit rate (if CRS=0, default value after Reset). In the last case it is ensured that the internal IOM-2 bit clock has a phase such that output bits on DD/DU are correctly clocked out (**see figure below**).

**CLKO:**

After Reset the auxiliary clock output CLKO outputs the buffered XTAL1 frequency (28.416 MHz). Alternatively, CLKO can be programmed (via CKOS bit in register 2002h) to output a frequency obtained from the DSP clock via a programmable baud rate generator (baud rate factor 1, 2, 3, ..., 2^{19}).

The wide range for the division factor for the CLKO output allows also for the possibility to use it as a time marker (period on the order of 10 ms to synchronize another device to the PSB 7230 time base).

4.2 Audio and Data Reception/Transmission

The PSB 7230 supports a total of four independent serial I/O-channels:

- one receive and one transmit audio channel, and
- one receive and one transmit data channel (pertaining to the serial Data controller).

The four channels are transferred between the DSP and/or the Parallel Host Interface and one of the serial interface lines: DD or DU (IOM-2), or SR or ST (Serial Audio Interface SAI). The capacity of each channel is individually determined by programming the time-slot length on the selected serial interface line.

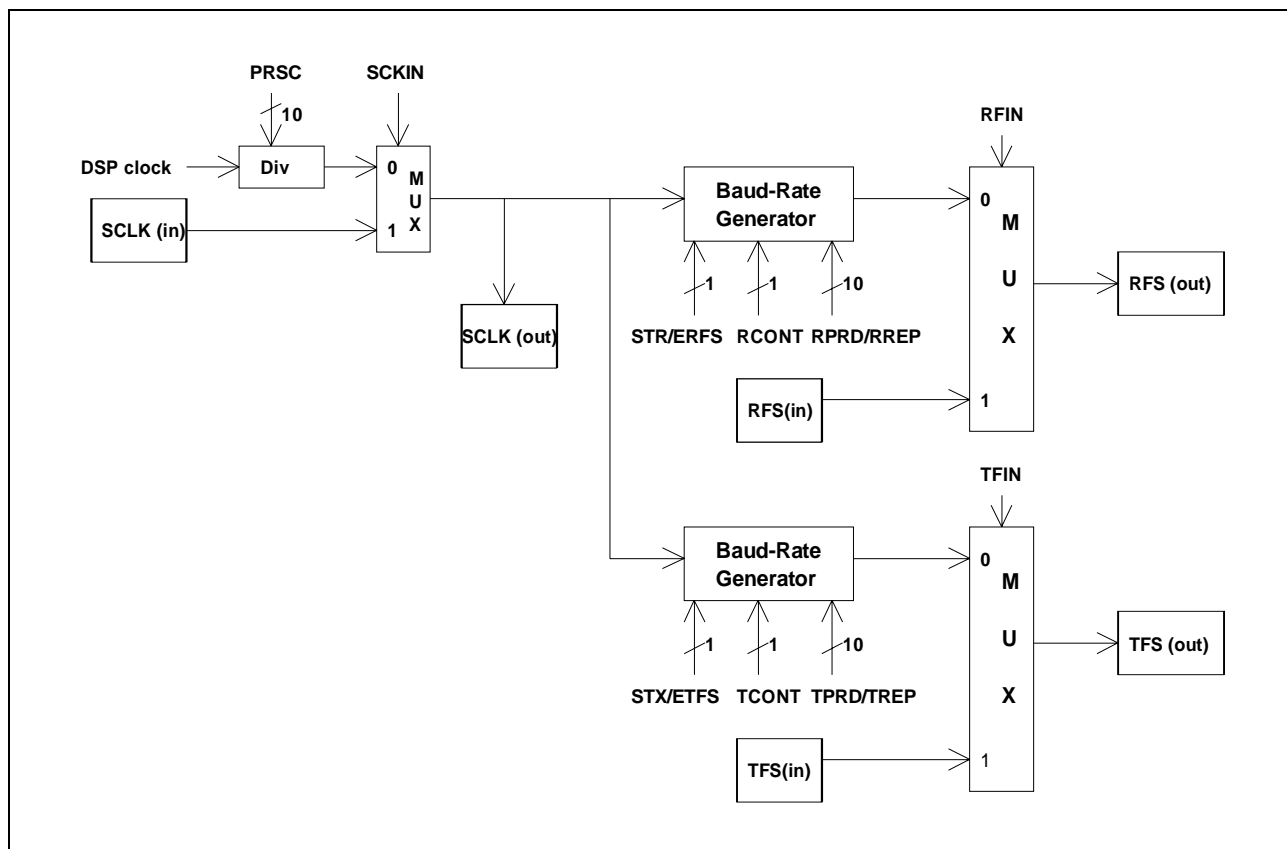
Timing Generation

The selection of the line for each of the channels is performed via SLIN1,0 (00: DU; 01: DD; 10: SR; 11: ST). The timing logic is driven by the bit clock and frame synchronization signals corresponding to the selected line. These are:

DCL(/2) and FSC	for DD and DU
SCLK and RFS	for SR
SCLK and TFS	for ST.

The IOM-2 timing signals can be input or output of the PSB 7230, i.e. the circuit is a slave or master with respect to the IOM-2 interface. The selection is done by the CGEN bit in register 202Bh.

The timing on the SAI lines SR and ST is either input or output. In the case where the timing is internally generated (i.e. the PSB 7230 functions as SAI master for SR and/or ST), a schematic diagram of the generation logic is shown in the **figure below**.



For the frame sync signal RFS and/or TFS, two basic modes of operation are provided:

Case 1:

If control bit RCONT=1, pulses on RFS are continuously and periodically generated if ERFS (Enable RFS generation control bit in data controller register bank) is set to "1", of one bit period length and spaced $(PRD+1) \cdot 16$ bits apart, where $PRD=0, 1, \dots, 31$.

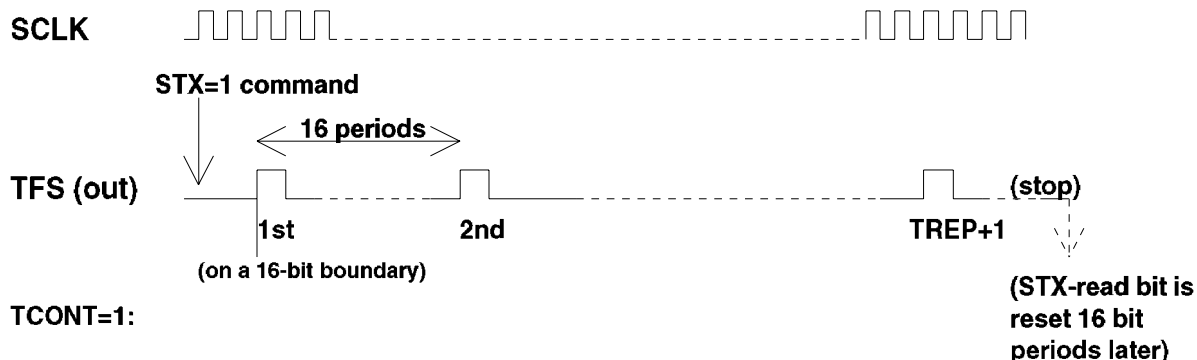
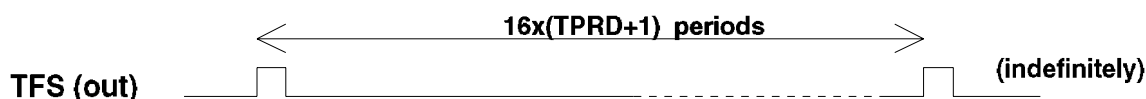
Note: (It suffices that the ERFS bits in the serial Data Controller register bank is set to "1" in order for pulses to be generated.)

Case 2:

If RCONT=0, a burst of $REP+1$ pulses on RFS is generated, of one bit period duration and spaced 16 bit periods apart when a start command is issued by setting the STR bit to "1". REP takes the a value in the range 0 to 1,023.

Note: (It suffices that the STR command in the serial Data Controller register bank is issued in order for the generation of pulses start.)

The same applies for TFS (control bits are ETFS and STX).

Example for TFS:**For TFIN=0****TCONT=0:****TCONT=1:****While ETFS=1:**

The uses of these modes are as follows:

Case 1:

When the timing is input, or when it is internally generated with TCONT=1, the interface can be used as a general Time-Division Multiplex highway with time-slots of programmable lengths and locations for audio and data.

Case 2:

When the timing is output with TCONT=0, the interface is typically used to transfer messages or blocks of compressed or uncompressed audio or data, preceded by a header of control information pertaining to the transferred data block and synchronous to it. The blocks can be received and transmitted using the serial Data Controller. An application of this mode of operation is the synchronous transfer of H.221/223 oriented data between the PSB 7230 and an attached VCP Videocodec.

Audio Channel Transfer

As mentioned in **section 3**, all the serial channels (1 receive audio, 1 transmit audio, and one full-duplex transparent data channel) can be transferred between one of the serial interfaces and the DSP or the host in a flexible manner.

The interface to each of the audio channels is a 32-bit wide shift register. In receive direction, when the shift register is filled to a programmable level (up to 32 bits), the whole 32-bit shift register is loaded into the receive channel read register set accessible from the DSP and from the host. Simultaneously, a maskable interrupt status is set. Similarly, in the transmit direction, transmit channel data is loaded from the write register pertaining to that channel (either from DSP or host register, as selected via a control bit) into the transmit shift register when a selectable number of bits have been shifted out.

The buffering of up to 32 bits reduces the reaction time of the DSP software.

As an alternative to this, the audio channel data can also be loaded from the shift register to the DSP/host registers (receive direction) and from the DSP/host registers into the shift register (transmit direction) at the occurrence of the frame sync pulse. In this case the number of significant bits in the registers is determined by the time-slot length programmed on the receive/transmit line. The DSP/host has 125 μ s to read/write the register while new data is assembled or the contents of the shift register are transmitted, during the following frame. (This option could be used for DSP software synchronized on the 8 kHz time base).

The audio channel registers, each of length 2 words/4 bytes, are (**see section 3**):

RC1	Receive channel 1
XC1	Transmit channel 1

The relevant parameters for controlling the transfer of the audio channels are (independent for each channel):

EN	Enable channel
LMOD	Load Mode (either once per frame, or after LBIT bits have been received/transmitted)
LBIT	Load Bits. Gives the number of bits (1 to 32) to be loaded, in multiples of the physical time-slot length.

The maskable interrupt status bits for controlling the transfer are:

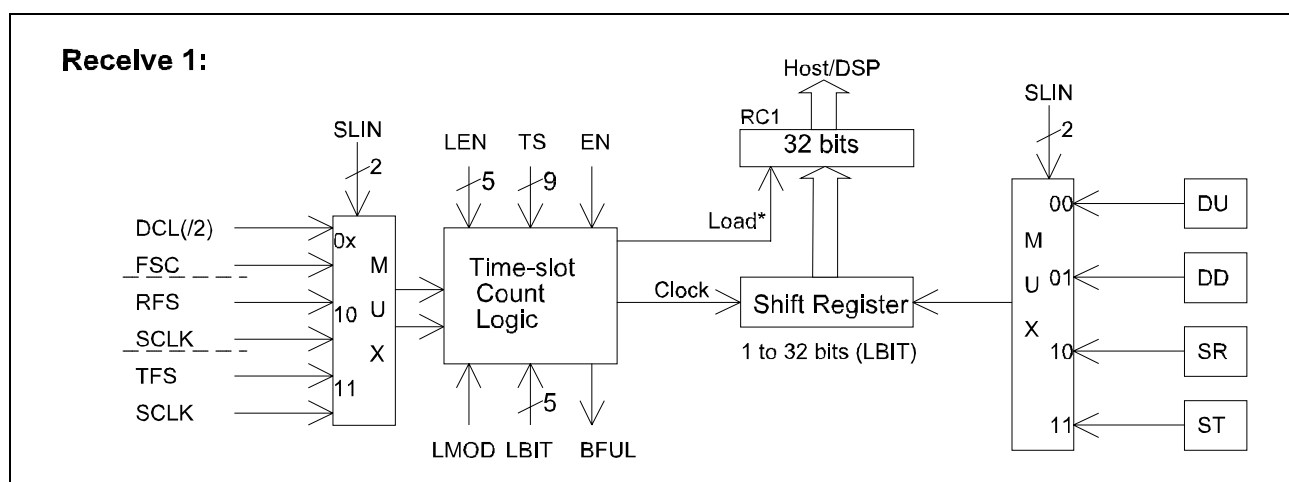
BFUL	Buffer full (RC1)
BEMP	Buffer empty (XC1)

or optionally:

FSC Frame Sync interrupt (FSC)
RFS Frame Sync interrupt (RFS)
TFS Frame Sync interrupt (TFS).

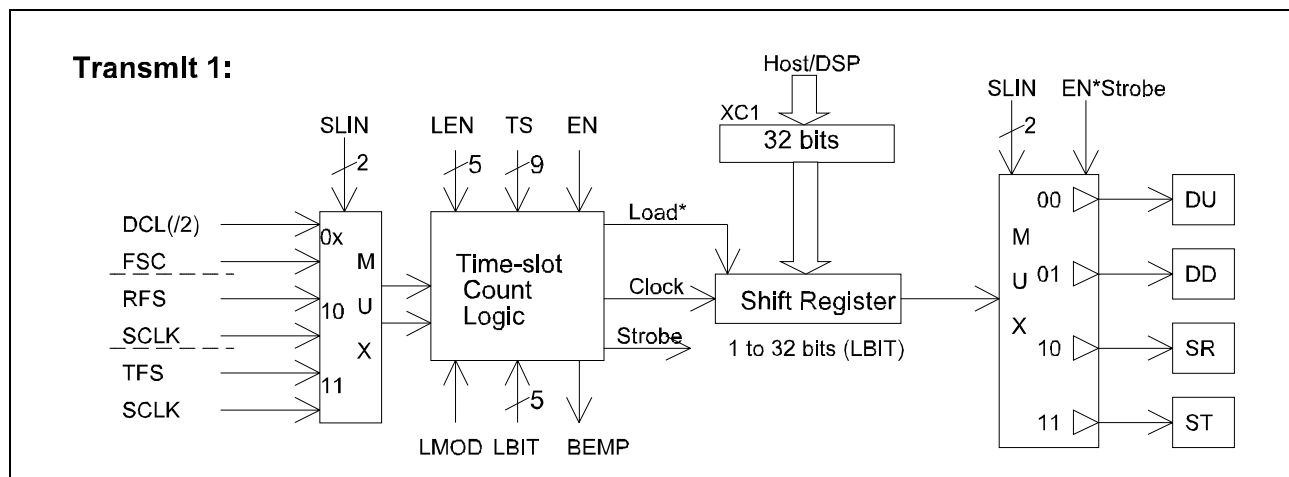
In addition, the control bit HXA1 controls whether the audio transmit channel is loaded into the shift register from the XC1 register accessible from the DSP (HXA=0) or from the host (HXA=1).

The block diagrams for the receive and transmit audio channels are shown in the following figures.



* Load: Generated

- after detection of sync pulse (before sync pulse interrupt) if LMOD=0,
- or when LBIT bits (1 to 32) have been shifted into shift register, but before BFUL interrupt, if LMOD=1.



*Load: Generated

- after detection of sync pulse (before sync pulse interrupt) if LMOD=0,
- or when LBIT bits (1 to 32) have been shifted out from shift register, but before BEMP interrupt, if LMOD=1.

Caption to the Figures:

In receive direction, the input data is loaded from the shift register into DSP accessible read registers and simultaneously into (physically separate) host accessible read registers.

In the transmit direction, data is loaded into the shift register from the transmit channel register accessible from the DSP (if HXA=0) or the register accessible from the host (if HXA=1). The control bit HXA1 is provided for this purpose.

Serial Data Channel Transfer

The interface between the input of the serial data receiver and the DSP or host, and between the output of the transmitter and DSP or host is in each case a 32-bit long shift register.

In receive direction, when the shift register from the serial line is filled to a programmable level (1, 2 or 4), the whole 32-bit shift register is loaded into the HRR1 read register accessible from the DSP and from the host. Simultaneously, the contents of the HRW1 write register is loaded to the data receiver input, after which a maskable interrupt status is generated. If the data in HRR1 is to be pre-processed, the HRW1 register should be written before the next 1, 2 or 4 bytes (programmable) have been shifted into the shift register.

Similarly, in the transmit direction, after 1, 2 or 4 bytes (programmable) are available from the data transmitter output, they are loaded into the HXR1 read register accessible by the DSP and the host. The contents of the HXW1 write register is loaded into the serial output shift register. If the data in HXR1 is to be post-processed, the HXW1 register should be written before the next 1, 2 or 4 bytes (programmable) have been shifted out.

In receive direction, the data from the shift register is loaded into DSP accessible read registers and simultaneously into (physically separate) host accessible read registers. Data to the data receiver is loaded from the transmit channel register accessible from the DSP (if HHR=0) or the register accessible from the host (if HHR=1). The control bit HHR1 is provided for this purpose.

The serial data channel registers, each of length 2 words/4bytes, are (**see section 3**):

HRR1	Data Receive Read 1
HRW1	Data Receive Write 1

HRR1	Data Receive Read 1
HXR1	Data Transmit Read 1
HXW1	Data Transmit Write 1

The relevant parameters for controlling the transfer of the serial data channels are:

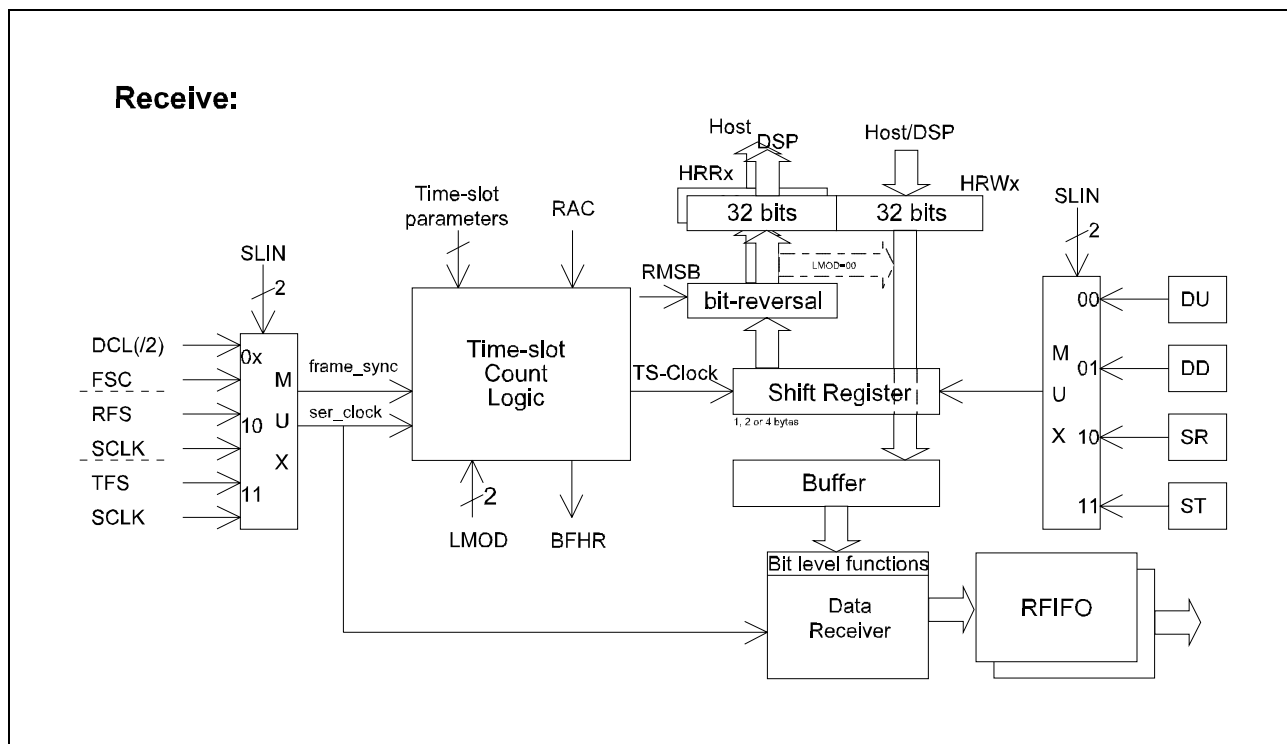
LMOD(1:0)	Load Mode (access byte by byte without delay, or access in 1, 2 or 4 byte units with a corresponding serial data delay)
HHR	Access to serial data receiver input from DSP (HHR=0) or from host (HHR=1)
HHX	Access to serial data output shift register from DSP (HHX=0) or from host (HHX=1).

The access right to the receiver and transmitter input/output from the DSP or the host (determined bits HHR1 and HHX1) is independent of who is allowed to service the data controller (determined by bits HAH1).

The maskable interrupt status bits for controlling the transfer are:

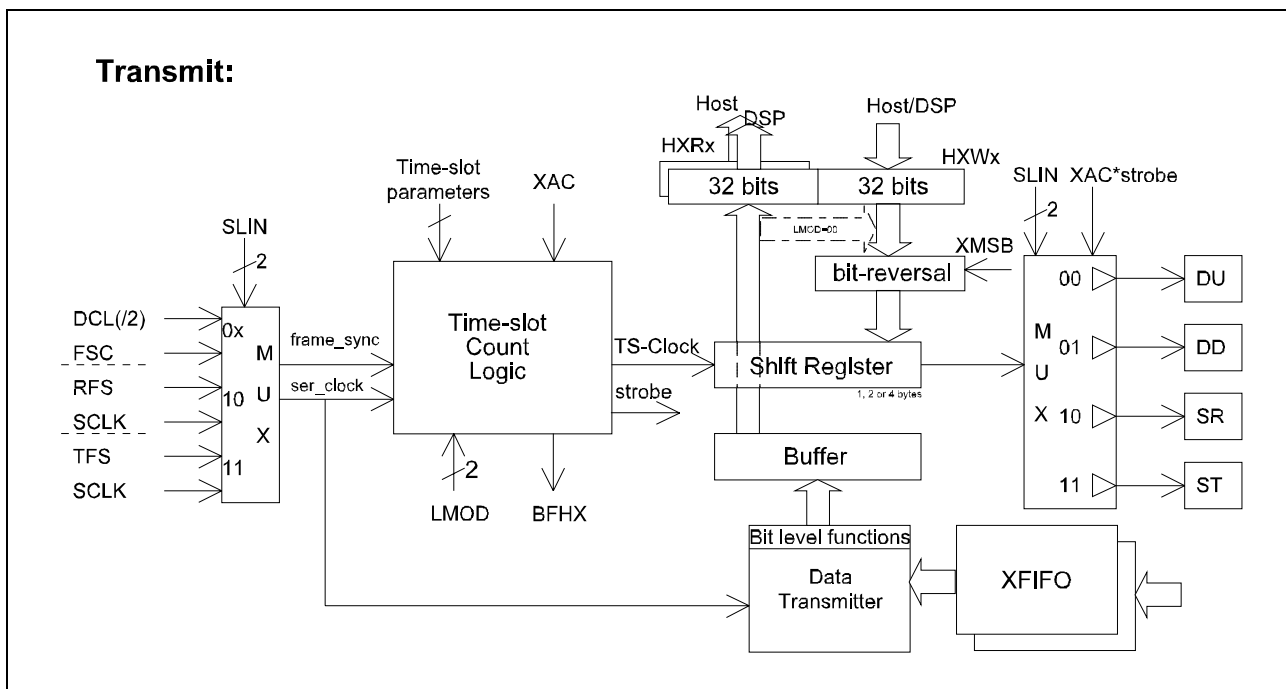
BFHR	Buffer full for data receiver (new data can be read from HRR and written into HRW)
BFHX	Buffer full for data transmitter (new data can be read from HXR and written into HXW)

The block diagrams for the receive and transmit data Controller channels are shown in the **following figures**.



Caption to the Figure:

The data from the shift register is loaded into DSP accessible read registers and simultaneously into (physically separate) host accessible read registers. Data to the receiver is loaded from the transmit channel register accessible from the DSP (if HHR=0) or the register accessible from the host (if HHR=1). The control bit HHR1 is provided for this purpose.



Caption to the Figure:

The data from the data transmitter is loaded into DSP accessible read registers and simultaneously into (physically separate) host accessible read registers. Data is loaded into the shift register from the transmit channel register accessible from the DSP (if HHX=0) or the register accessible from the host (if HHX=1). The control bit HHX1 is provided for this purpose.

The access right to the receiver and transmitter input/output from the DSP or the host (determined bit HHR1 and HHX1) is independent of who is allowed to service the data controller (determined by bits HAH1).

Note on Time-Slots of Data Communication Controller

If a time-slot is still active (either in receive or transmit direction) when a new frame sync pulse is detected, the programmed length of the time-slot is not reduced but the time-slot remains active until its end. However, the time-slot count logic for the new frame starts immediately at the detection of the new frame sync pulse. A new time-slot can start immediately after the currently active time-slot has been closed, thus permitting a permanent reception or transmission ("time-slot length" = "distance between two consecutive frame sync's").

The case where "time-slot length" > "distance between two consecutive frame sync's" should not occur.

Note on Latency of Serial Data

When a data receiver is enabled (via bit RAC), it is clocked with the serial interface clock even outside the selected time-slot. However, the logic at the input of the data receiver is only clocked with the serial clock during the selected time-slot. Consequently, N bits are loaded into HRR register from the serial line after N clock edges inside the selected time-slot (N is equal to 8, 16 or 32 depending on LMOD). Similarly, data from HRW register is loaded into data receiver only after a certain number of clock edges inside the selected time-slot have occurred. The latency (delay) of received data from the input pin to the data FIFO is given in the following as a function of LMOD ("clocks" means the number of clock edges inside the active time-slot:

LMOD=00	9 clocks
LMOD=01	17 clocks
LMOD=10	33 clocks
LMOD=11	65 clocks.

These latencies have to be taken into account in systems where the serial clock is not continuous but is immediately disabled after the last serial data bit is clocked into the input register.

The same latencies apply in the case of the data from the output of the data transmitter to the serial output pin.

4.3 Serial Data Controller

The internal serial data controller of the PSB 7230 can be independently serviced

- either via the Parallel Host Interface
- or by the DSP (SPC).

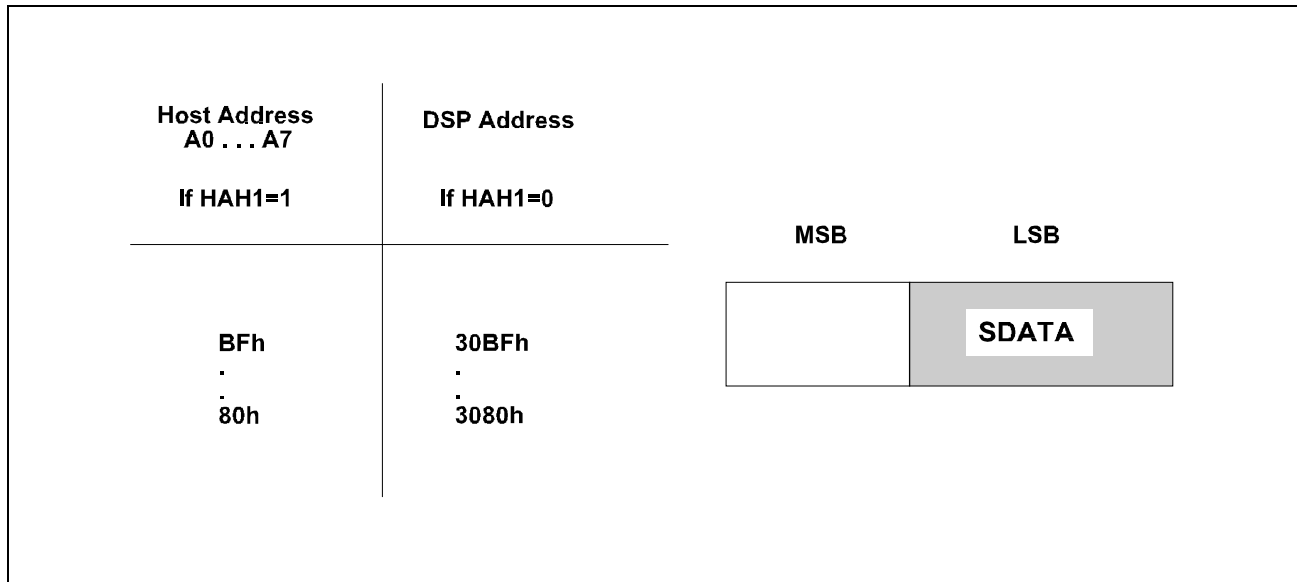
Important Notes:

1. From the point of view of the end user/system manufacturer, only the servicing of the data controller via the host is of relevance, since the servicing via the DSP is done by on-chip firmware invisible to the end user.
2. If the packet oriented protocol on the Serial Audio Interface used in videophone applications with the VCP (from 8x8, Inc.) videocodec is needed, the data controller is serviced by the on-chip firmware, in other words, it cannot be accessed by the host. Only in protocols (see section 6.2) with the compressed data stream via host interface the serial data controller is available for host usage.

The servicing of the data controller via the host and via the embedded DSP are exclusive of each other. The access to the register banks of the data controller is determined by the "Data Controller Access from Host" bit HAH1:

- When HAHx is 0, the SPC is allowed to access the data register bank, and the Host interface bus is disconnected from the data controller;
- When HAHx is "1", the Host is allowed to access the data register bank, and the SPC data bus is disconnected from the data controller.

The address space of the data controllers for the Host interface bus and for the SPC data bus is shown in the **following figure (see also section 5: Data Controller Register Description)**:



The received data is stored in the receive FIFO so that byte alignment in the FIFO corresponds to byte alignment in the serial time-slot (if the length of the time-slot is a multiple of 8 bits). Similarly, in transmit direction the byte alignment in the FIFO corresponds to the time slot boundaries in the transmit time-slot, if its length is a multiple of 8 bits. When the transmit FIFO is empty, idle ("1") is transmitted during the active time-slot. Outside the selected time-slot, the output line is in "high impedance" state.

Details on the operation of the serial data receiver

The data receive FIFO size is 2×32 bytes. One half of the FIFO is connected to the receiver shift register while the second half is accessible from the controlling software.

The status bits pertaining to the data receiver are:

RPF	Receive Pool Full 32 bytes of a frame have arrived in the receive FIFO. The frame has not yet been completely received.
RFO	Signifies that data has been lost because no room was available in RFIFO.

The data receiver is controlled by the following bits:

RAC	Receiver Active When RAC is set to "1", storage of bytes in the receive FIFO starts time-slot aligned (if the receive time-slot length is a multiple of 8 bits).
RMC	Receive Message Complete Acknowledges a previous RPF status. Frees the FIFO pool for the next received frame or part of a frame.
RRES	Receiver Reset Resets the data receiver, which goes into an idle state (RAC cleared), clears the receive FIFO.

Details on the Operation of the serial data Transmitter

The transmit FIFO size is 2*32-bytes. One half is connected with the transmit shift register while the other half is accessible via the controlling software.

The interrupt status bits pertaining to the data transmitter are:

XPR	Transmit Pool Ready One data block may be entered into the transmit FIFO.
ALLS	All Sent. When "1", indicates that the last bit has been transmitted and that the XFIFO is empty.

The following status bits are provided:

XDOV	Transmit Data Overflow Indicates that more than 32 bytes have been written into the transmit FIFO
------	--

The data transmitter is controlled by the following bits:

XAC	Transmitter Active In transparent mode, when XAC is set to "1", transmission of bytes from the transmit FIFO starts time-slot aligned (if the transmit time-slot length is a multiple of 8 bits).
XF	Transmit Frame Initiates transmission of an entire frame, or part of one (up to 32 bytes).
XRES	Transmitter Reset. Resets the data transmitter, clears the transmit FIFO and generates an XPR status after the command has been completed.

After up to 32 bytes have been written to the FIFO, transmission is started by issuing the XF command. The data controller requests another data block by an XPR interrupt status if there are no more than 32 bytes in the FIFO. To this the software responds by writing another pool of data and issuing a transmit command XF for that data. If transmission of earlier data (or of a previous frame) is still underway when a new transmission command XF is issued, software access to the FIFO is blocked until the first transmission is completed (**see figure**).

If the transmit FIFO runs out of data, the host will be advised by a Transmit Data Unterrun (XDU) interrupt status.

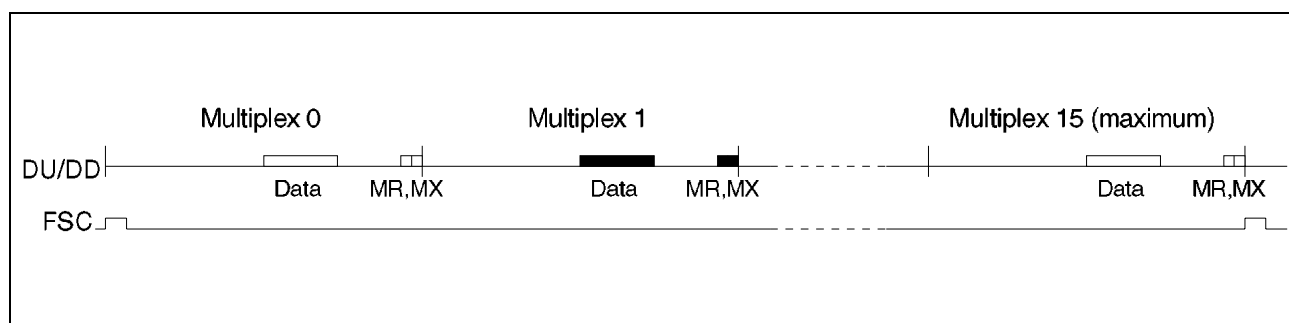
4.4 IOM-2 Functions

The IOM-2 functions supported by the PSB 7230 are:

- Layer 1 functions in terms of the frame structure supporting any number n of 4-byte multiplexes ($n=1, \dots, 16$), the number is implicitly determined by the DCL clock (see section 2)
- One Monitor channel of programmable location
- Two C/I channels.

See figure below.

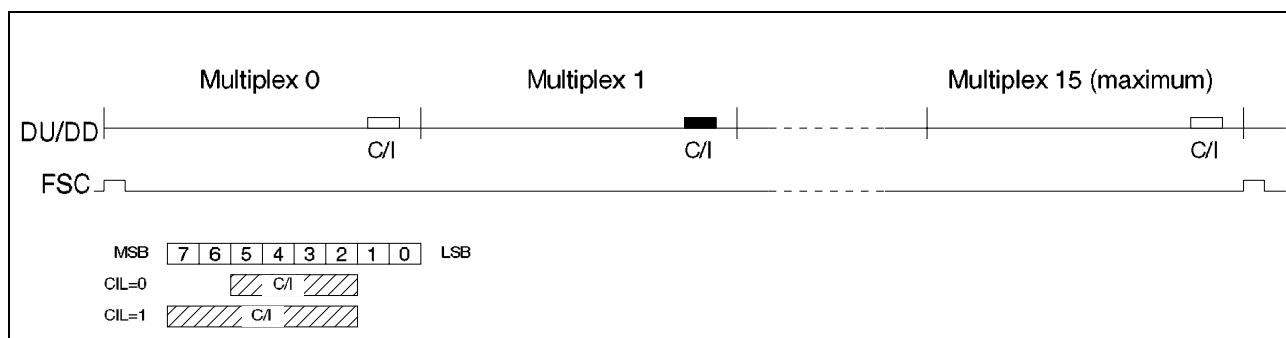
Monitor Channel



Parameters:

- SLIN=0: Monitor transmit data on DU, receive data on DD
- SLIN=1: Monitor transmit data on DD, receive data on DU
- CH(0:3): Monitor channel in 3rd byte of multiplex 0, ..., 15 (common to receive and transmit channel) (CH(0:3)=0001 in the example)

C/I Channels (2 independent channels)



Parameters:

- SLIN=0: C/I channel transmit data on DU, receive data on DD
- SLIN=1: C/I channel transmit data on DD, receive data on DU
- CH(0:3) C/I channel in 4th byte of multiplex 0, ..., 15, common for receive and transmit channel (CH(0:3)=0001 in the example)
- CIL: C/I channel length is 4 bits (0) or 6 bits (1)
- DLL: Double last look yes (1) or no (0)

4.4.1 Monitor Channel Protocol

Use of Monitor Channel

In the case where a *local host* is present, the Monitor channel may be used e.g. for data exchange between the local host and another controller attached to the IOM-2 bus. For this purpose the basic Monitor channel protocol as explained in this section is sufficient.

Note: The Monitor channel protocol is not implemented **on-chip** on the PSB 7230. The Monitor channel protocol has to be implemented via the host: this allows the implementation of data exchange with a remotely located controller.

General Description of Monitor Channel Protocol

The Monitor channel consists of 8 bits for the Monitor Data channel (MON) and 2 bits for the flow control (MX and MR). The transmitter controls the Monitor Data channel and the MX bit on one line while evaluating the condition of the MR bit on the other line. The receiver evaluates the MX bit of one line and latches its Monitor Data value. It controls the MR bit of the other line. The Monitor channel protocol is shown in the figure below.

The hardware performs reception and transmission of Monitor channel messages (packets) byte by byte under software control.

The received and transmitted Monitor channel bytes are stored in the Monitor Data Transmit (MONX) register and Monitor Data Receive (MONR) register, respectively.

The software controls the monitor channel via two control bits in the Monitor channel Control Register:

MRE	Monitor channel Receiver Enable
MRC	MR bit Control
MXC	Monitor channel Transmitter Control.

The Monitor channel status is reported to the software via four bits in the Monitor channel Status register:

MDR	Monitor channel Data Received
MER	Monitor channel End of Reception
MDA	Monitor channel Data Acknowledged
MEA	Monitor End of Acknowledgement
MAB	Monitor channel Abort.

Inactivity

The transmitter indicates its inactivity with the idle state of the MX bit (1) and by transmitting the value FF_H (or high impedance) in the Monitor Data channel. The receiver responds to this inactivity via the idle (1) condition of the MR output bit.

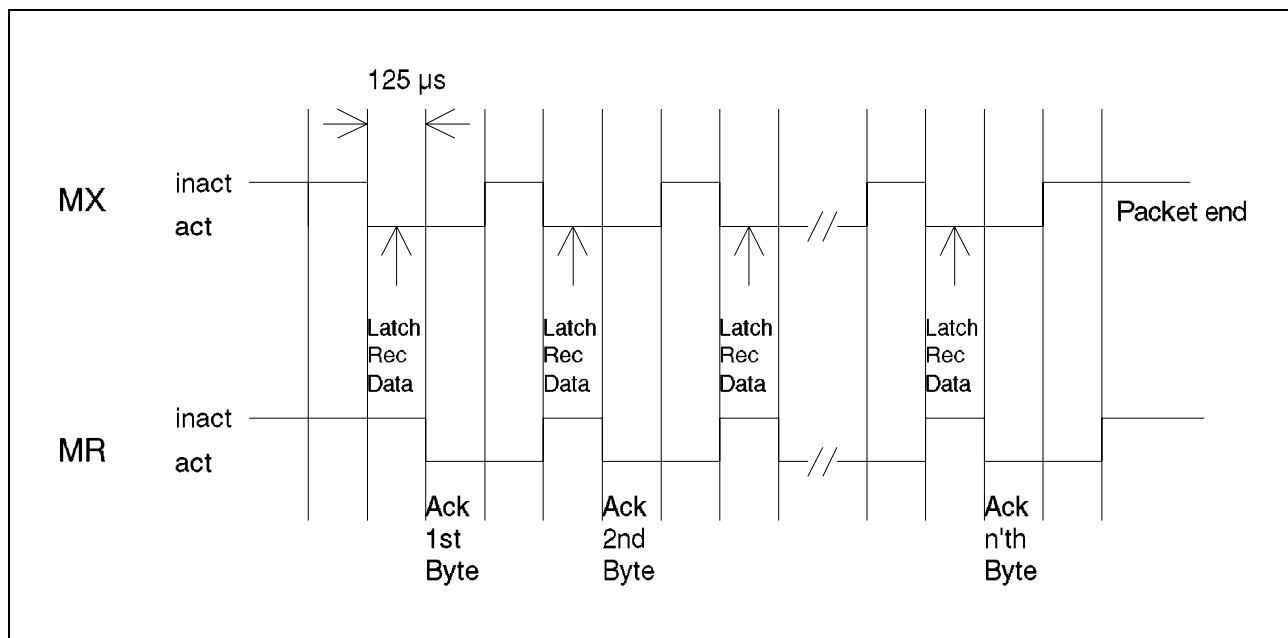
Monitor packet transfer

The message transfer starts when the transmitter transmits the value of the first byte of the Monitor Data channel and sets the MX bit to its active state (0). The MX bit remains active until the receiver acknowledges the data or the transmitter software aborts the transmission. The receiver recognizes the change of the MX bit to the active state and latches the contents of the Monitor Data channel. Since the Monitor channel address is always transmitted as the first byte of a message, all receiving devices compare (per hardware or software) the first value with their own address. If a device recognizes its address it acknowledges the data by changing its MR bit to the active state (0).

The transmitter recognizes this change and can now transmit the next byte of the message. This is done by transmitting the value in the Monitor Data channel and setting the MX bit to the inactive, idle (1) state for one frame and then changing it back to the active (0) state. The receiver recognizes the transition of MX from the inactive to the active state and latches the contents of the Monitor Data channel.

The receiver acknowledges the data transfer by setting the MR bit to the inactive (1) state for one frame and then back to the active (0) state. This procedure is repeated until all the data is transferred. Once the receiver has acknowledged the last value the transmitter switches its MX bit and the Monitor channel into the idle (1) state. The receiver recognizes this idle state after it has received two consecutive frames with an idle MX bit and will then set its own MR bit in the idle (1) state.

The transmitter recognizes the change of the MR bit and indicates the idle condition after the second frame. If the receiver wants to abort a transmission, then it will set its MR bit into an idle (1) condition. The transmitter recognizes the abort condition after the second frame with an idle MR bit and switches its MX bit and the Monitor Data channel to idle.



Note: For simplification of the diagram the states of MX and MR are shown as "0" or "1" during the entire 125-μs frame without regard to the bit positions they actually occupy.

Software handling of Monitor channel transmission

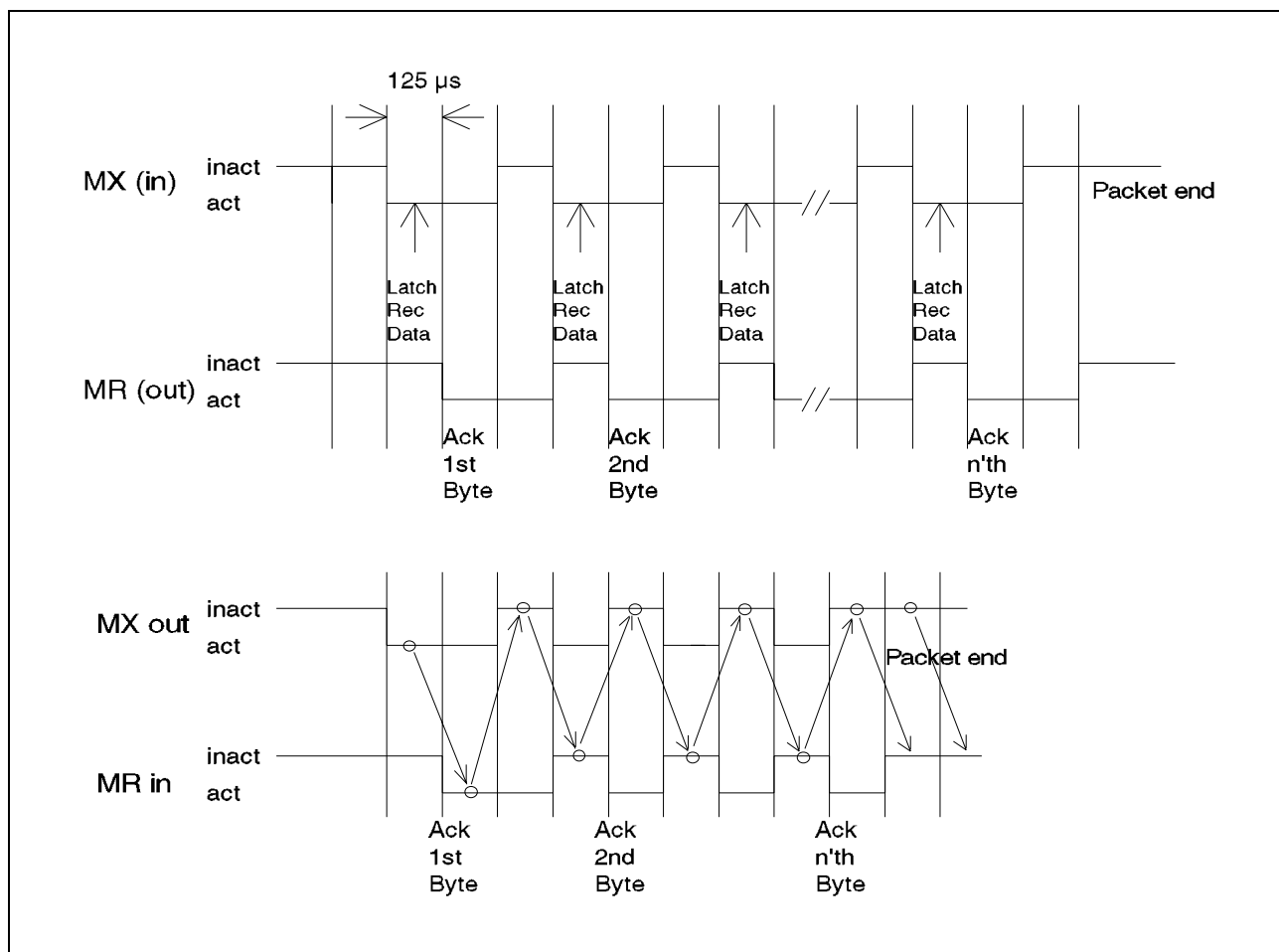
The idle state of the transmitter is maintained when the MXC (Monitor channel Transmit Control) bit is 0. In order to transmit the first byte, its value is written into the MONX (Monitor channel Transmit) Register. After the MXC bit is set to 1, the Monitor channel hardware sends the byte from MONX and controls the MX bit accordingly (MX:1→0). When the hardware detects the acknowledgment from the other end (received MR bit=0), it will set the MDA (Monitor Data Acknowledged) bit. When this is detected by the software, it writes the next byte in MONX register. This byte is sent and the MX bit controlled accordingly. The acknowledgment by the other end is again indicated by the MDA status bit. This procedure is repeated until all the data is transmitted. After the last MDA status the software sets the MXC bit back to 0 and the transmit channel including the MX bit returns to the idle state.

If an abort request from the receiving end is detected by the hardware, the MAB (Monitor channel Abort) status bit is set.

In the PSB 7230 the Monitor channel transmitter implements the so-called **Maximum speed** option of this protocol, whereby the acknowledgment of every byte (except the first) by the receiving end is anticipated. This means that an MDA interrupt status is generated as soon as the received MR bit is detected to go from 0 to 1. Transmission of the next byte is started as soon as the software has reacted to this interrupt. Thus a maximum transfer speed of 32 kbit/s can be obtained.

Each data byte is transmitted at least twice (only twice if the receiver is fast enough so that the transmitter works at maximum speed), namely once when MX is 1, and once when MX is 0 in the next frame. The only exception is the first byte, which is transmitted in three consecutive frames (where MX=1, 0, 0, respectively).

In order for the transmitter to recognize that the receiver has correctly acknowledged the last byte, the interrupt status MEA is set after the received MR bit is received at 1 in two consecutive frames (interrupt status different from MAB). The condition for generating an MEA interrupt status is the **recognition of a MR=0, 1, 1 sequence when MXC=0**.



The top figure shows the general case, the bottom figure the maximum speed case.

Software handling of Monitor channel reception

The receiver of the Monitor channel is controlled via the MRE bit. As long as the MRE bit is zero, no evaluation of the received MX bit is done. If the MRE bit is set to 1, then the Monitor channel hardware waits for a start of a Monitor packet. When the start of a packet is recognized with a Monitor byte matching monitor receive address, acknowledgement can be enabled by the software by setting the MR Control bit MRC

to 1. The hardware performs acknowledgement by setting the transmitted MR bit to 0. Upon the reception of the next byte the hardware sets the MDR status bit. When the Monitor byte is read from the MONR register, this byte is acknowledged via transmit MR=0. Every new byte is similarly indicated by the MDR status, and acknowledged after a read of the MONR register. If the hardware recognizes the end of a packet, it indicates this via the MER status (MRE=1).

The receiver of the PSB 7230 does not perform a double-last-look check on the received data (i.e. compare the data received while MX=0 with the data in the previous frame with MX=1).

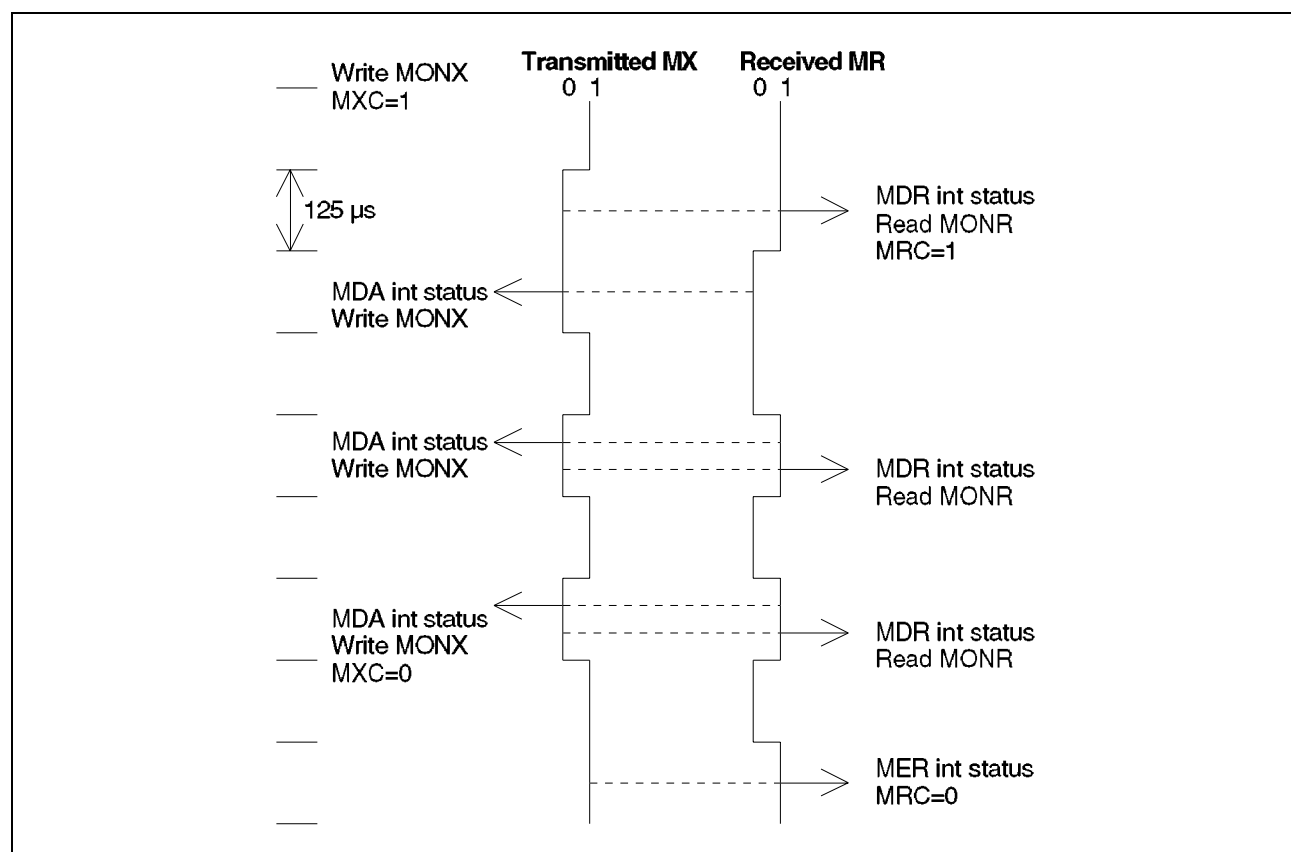
When MRC=0, it is made sure that the receiver only receives the first byte of a packet and does not latch any further bytes in MONR until the beginning of the next packet.

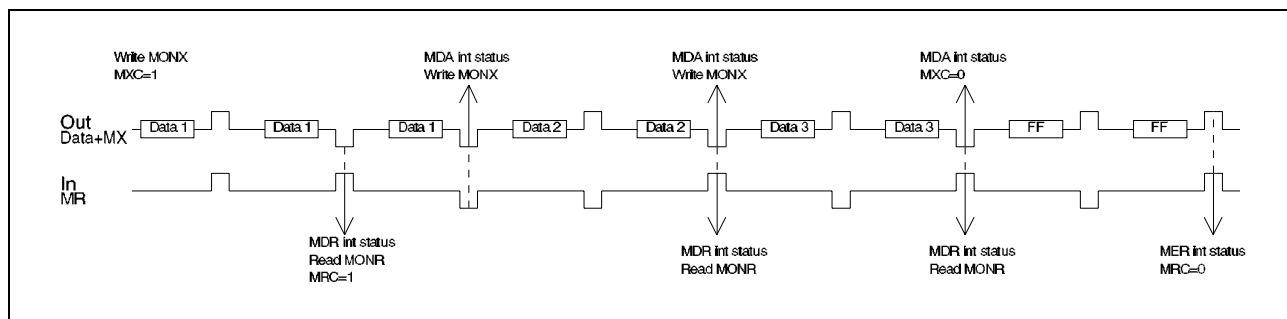
Thus the conditions for latching the first byte of a packet is:

(MRE=1) & (MX=0 after having been 1 in at least two consecutive frames).

Any further bytes are latched into MONR only if:

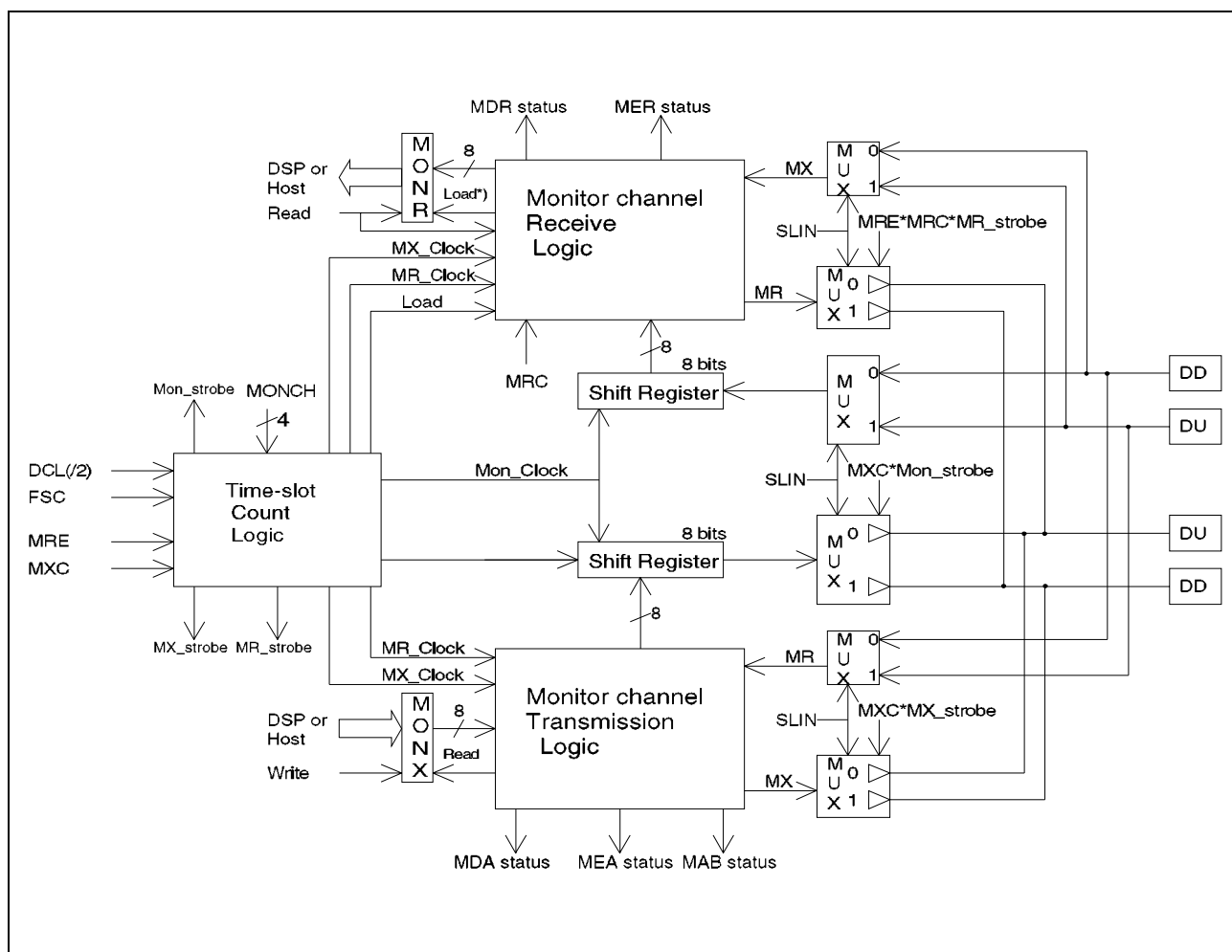
(MRE*MRC=1) & (previously received byte has been read from MONR register) & (MX=0).





Monitor Channel Data Transfer

A hardware model of the Monitor channel is shown below.



*) MRC has to be "1" and MONR has to be read before any new value from the same packet is loaded into MONR. Thus, while MRC=0, only the first byte of a packet is loaded into MONR.

4.4.2 C/I Channel

The two C/I channels are controlled via the C/I Transmit (CIX) and C/I Receive (CIR) registers, the C/I channel Enable (CIEN) and the C/I Change (CIC) interrupt status bit.

In addition, an Awake (AWK) control bit is provided. When this bit is set to "1", the output line is unconditionally "low" until AWK is set to "0" again. This bit is used in ISDN terminal applications to "wake up" the IOM-2 interface, i.e. to require clocking to be generated on DCL and FSC by an upstream circuit – typically an ISDN S-Bus Access Controller ISAC-S.

When the AWK bit is set to "0", the output line is released only after the next FSC pulse has been detected, to avoid sending an invalid code in the outgoing C/I channel. The same applies for the CIEN bit, which is also synchronized with the FSC signal. C/I data reception and processing begins only after the first FSC pulse following a transition of CIEN to 1. AWK overrides any data normally transmitted during the C/I time-slot even if CIEN=1. When CIEN (synchronized with FSC) is "0" and AWK (synchronized with FSC) is "0", the outgoing C/I channel is permanently in high-impedance state.

The block diagram of the C/I channel handler is shown below.

In the receive direction, a change is recognized either using Double Last Look (DLL=1) or not (DLL=0).

Without Double Last Look

A change in received C/I channel is recognized after a new value is recognized once.

The new value is loaded into CIR for the DSP to read, and a CIC interrupt status is generated.

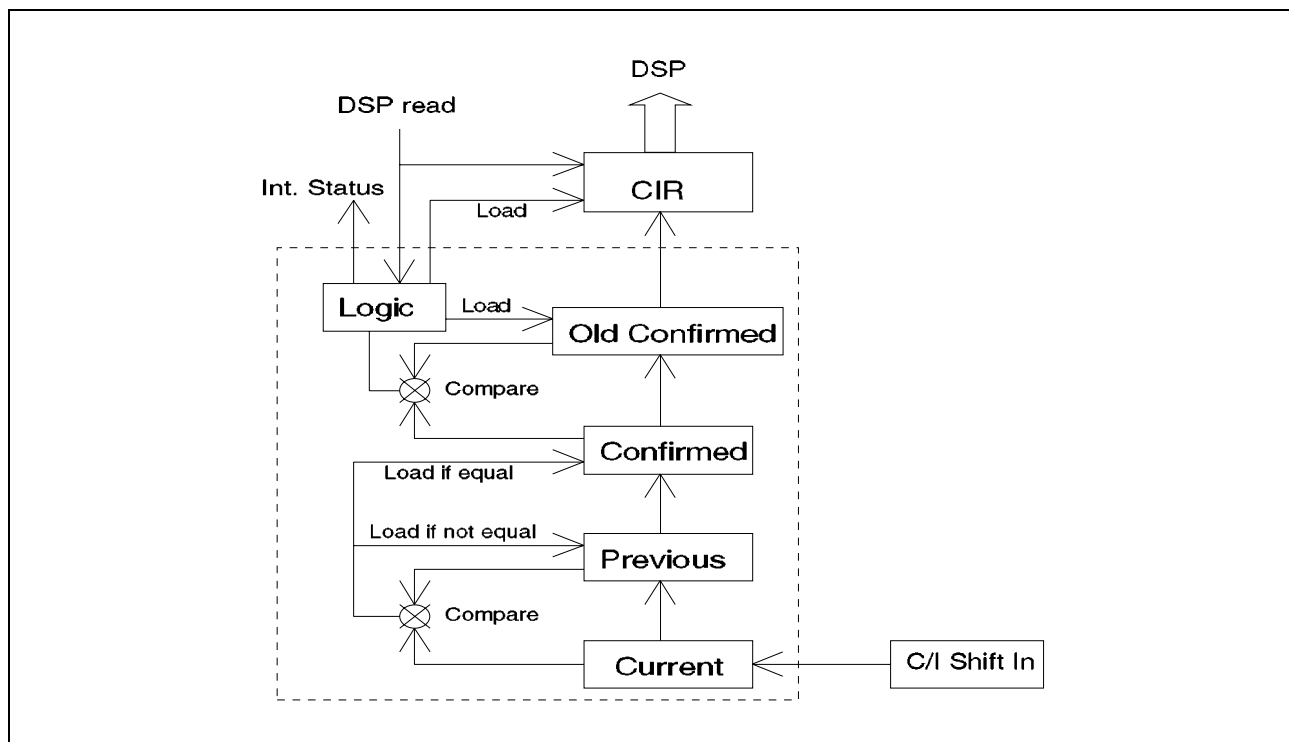
If further changes in receive C/I code take place before a previous changed value in CIR has been read, the changed values are not loaded in CIR.

When the first changed value is read by the DSP, the latest changed value is loaded in CIR and a CIC interrupt status is generated anew. Any possible changes that occurred between the first and the latest are thus lost.

With Double Last Look

A change in received C/I is recognized after a new value is detected in two consecutive frames.

This is shown in the figure below.



Algorithm:

"Current" is compared to "Previous":

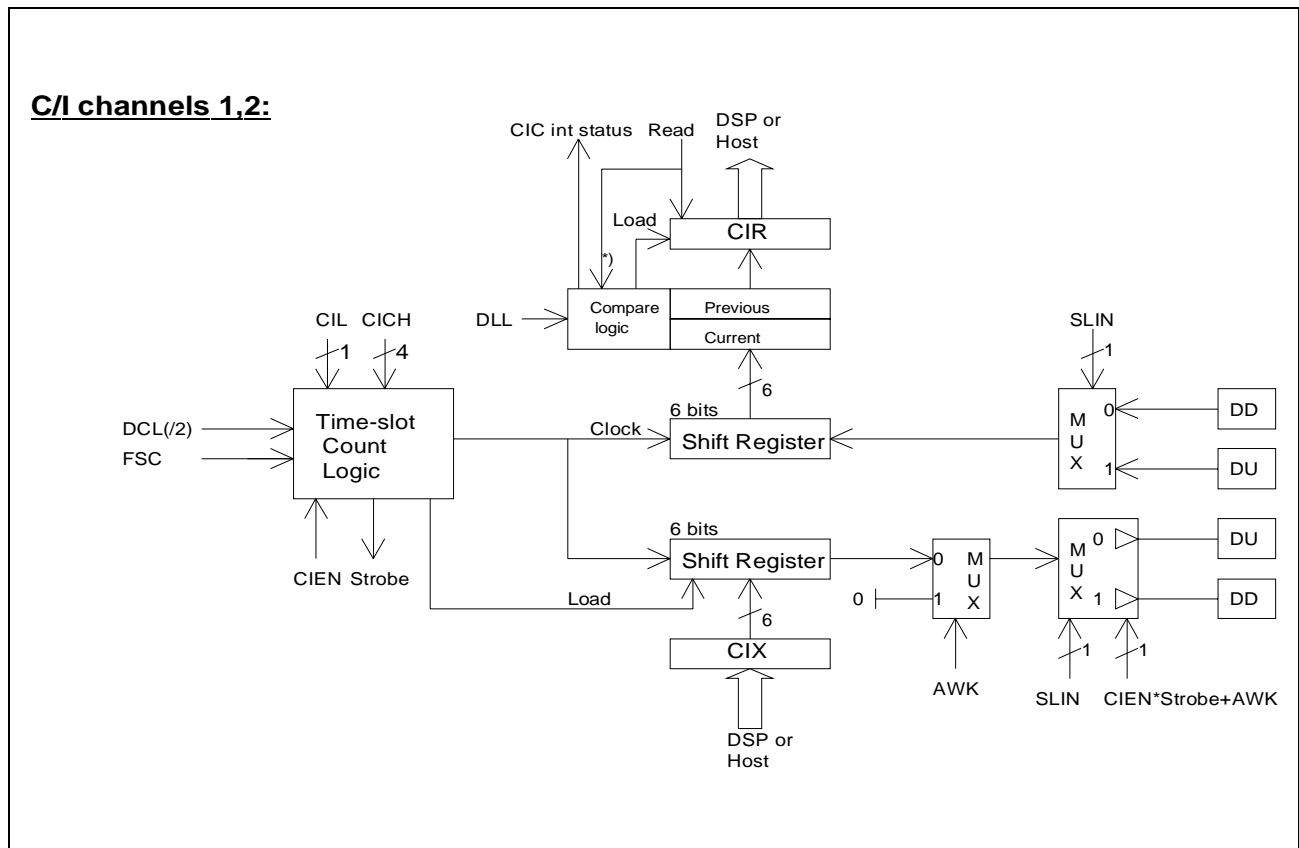
- If they are not equal, "Current" is loaded into "Previous", and a new comparison is performed in the next frame. No further actions are taken.
- If they are equal, the new value takes the place of "Confirmed". "Confirmed" is compared to "Old Confirmed":
 - If they are equal, no actions are taken.
 - If they are not equal, "Confirmed" is copied to "Old Confirmed".

If CIR register has been read, "Old Confirmed" is compared to CIR:

- If they are equal, no actions are taken.
- If they are not equal, "Old Confirmed" is copied to CIR and a CIC interrupt status is generated.

C/I Channel Data Transfer

The block diagram of the C/I channel handler is shown below.



*) Read of the old changed value is the condition of loading of a new changed value. Thus, when several changes occur before the first changed value has been read, only the first and the last change are available.

4.5 Programming Indirectly Accessible Registers

Registers in the memory mapped (DSP X-data RAM) area from 2000_H upwards are read and written:

- via the Parallel Host Interface by using two registers (Conf/Cont Reg Address Register at address $40_H / 3040_H$ and Conf/Control Reg Data Register at address $41_H / 3041_H$)

4.5.1 Programming via Parallel Host Interface (see also section 3.3.2)

For writing a Configuration/Control register (addresses 2000_H - $203F_H$), the host writes in the Data register the data byte to be written and in the Address register the write command:

Bit 7								Bit 0
0	0	A5	A4	A3	A2	A1	A0	

where $A(5:0)$ gives the offset of the register to be written. This causes an RACC (Register Access) interrupt status to the DSP. The DSP software transfers the Data byte to the requested address $2000_H + A(5:0)$ and writes the RDY bit (least significant bit of address $40_H/3040_H$) to "1" again (which was set to "0" by hardware at the time of writing of the Address register). By sensing the state of bit RDY the host is able to start a new access to Address and Data registers when the DSP is ready.

For reading a Configuration/Control register (addresses 2000_H - $203F_H$), the host writes in the Address register the read command:

Bit 7								Bit 0
1	0	A5	A4	A3	A2	A1	A0	

where $A(5:0)$ gives the offset of the register to be read. This causes a RACC (Register Access) interrupt status to the DSP. The DSP software transfers the contents of the requested address $2000_H + A(5:0)$ into the Data register and writes the RDY bit to "1".

5 Register Description

5.1 Interrupt Structure

As explained in **section 3**, the interrupt statuses are grouped on two interrupt lines, "high priority" and "low priority" interrupts, respectively. They are:

High Priority Interrupts ($\overline{\text{INTR}}$)

FSC, RFS, TFS

BFUL1, BEMP1, BFHR1, BFHX1

Lower Priority Interrupts ($\overline{\text{INT}}$):

SAIN

SDATA

DINT

MDR, MER, MDA, MEA, MAB, CIC1, CIC2

Corresponding interrupt status register exist for the internal DSP.

The interrupt status registers are physically separate for the Host and for the DSP. Thus, when an interrupt status is generated, the interrupt status bit is set in both registers.

The interrupt status disappears from the interrupt status register when the cause of the interrupt status is removed by the software, or the interrupt is explicitly acknowledged.

Whenever possible, an interrupt status is made to disappear when the cause of that interrupt status is removed (example: in/out audio data channel interrupts), in order to spare the explicit writing of an acknowledge register address. In other cases the interrupt statuses are explicitly acknowledged by writing a "1" in a virtual acknowledge register. The only exception to this are the interrupt statuses of the data controller, which are cleared by reading the interrupt status register of the respective controller.

The interrupt status bits (with the exception of the data controller interrupt status) have individual mask bits which have no influence on the setting of the interrupt status bits, but only on the generation of the interrupt on the interrupt line. When the mask bit is 0, the generation of the interrupt for the corresponding interrupt status on line $\overline{\text{INTR}}$ or $\overline{\text{INT}}$ is prevented.

5.2 Interrupt Status Registers

Register Map for Host Interrupts

Host Interrupt Status for $\overline{\text{INTR}}$:

	Bit 7						Bit 0
71 _H	FSC	RFS	TFS				

	Bit 7						Bit 0
70 _H	BFUL1	0	BEMP1	0	BFHR1	BFHX1	0

FSC	FSC detected
RFS	RFS detected
TFS	TFS detected
BFUL1	Receive channel sample of programmable length (1...32 bits) available in RC1
BEMP1	Transmit channel sample of programmable length (1...32 bits) can be written in XC1
BFHR1	Data receiver shift register can be read and/or written (1, 2 or 4 bytes) in HR1
BFHX1	Data transmitter shift register can be read and/or written (1, 2 or 4 bytes) in HX1

Interrupt Mask Registers:

	Bit 7							Bit 0
71 _H	FSC	RFS	TFS					
	Bit 7							Bit 0
70 _H	BFUL1		BEMP1		BFHR1	BFHX1		

A "0" in a bit position masks the corresponding interrupt (default value, i.e. after Reset). The mask bit affects only the generation of the interrupt, but not the interrupt status bit from being set.

Acknowledge Register:

	Bit 7							Bit 0
73 _h	FSC	RFS	TFS					

The interrupt status bit is reset when the host writes a "1" in the corresponding bit position.

The other interrupt status bits are reset when the input/output registers are read or written:

- BFUL1 Reset when RC1 (any of 00-03_H) is read
- BEMP1 Reset when XC1 (any of 00-03_H) is written
- BFHR1 Reset when HRR1 (any of 10-13_H) is read
- BFHX1 Reset when HXR1 (any of 14-17_H) is read

Host Interrupt for $\overline{\text{INT}}$:

	Bit 7							Bit 0
75 _H	0	0	0	SAIN		DINT	SDATA	0

	Bit 7						Bit 0	
74 _H	MDR	MER	MDA	MEA	MAB		CIC1	CIC2

SAIN Serial Audio Input Interrupt (from SIO line)

DINT Software interrupt from DSP

SDATA Interrupt from serial data Controller

MDR Monitor Channel Data Received

MER Monitor Channel End of Reception

MDA Monitor Channel Data Acknowledged

MEA Monitor End of Acknowledgment

MAB Monitor Channel Abort Request

CIC1 C/I Channel 1 Change

CIC2 C/I Channel 2 Change.

Interrupt Status Mask Register:

	Bit 7						Bit 0	
75 _H				SAIN		DINT	SDATA	

	Bit 7						Bit 0	
74 _H	MDR	MER	MDA	MEA	MAB		CIC1	CIC2

A "0" in a bit position masks the corresponding interrupt (default value, i.e. after Reset). The mask bit affects only the generation of the interrupt, but not the interrupt status bit from being set. Undocumented mask bits must be always set to "0".

Acknowledge Register:

	Bit 7						Bit 0	
77 _H				SAIN				

	Bit 7						Bit 0	
76 _H		MER	MDA	MEA	MAB			

The interrupt status bit is reset when the host writes a "1" in the corresponding bit position. The other interrupts are acknowledged as follows:

- DINT Reset when IND Int. Status register is read
- SDATA Reset when serial data Controller interrupt register is read
- MDR Reset when MONR register is read
- CIC1 Reset when CIR1 register is read
- CIC2 Reset when CIR2 register is read.

Note: Since no direct access to the MONR, CIR1 and CIR2 registers for the host is allowed (these registers are in the Configuration and Control Register area 2000_H upwards), they are read using the procedure via Address and Data registers as deccribed in **section 2** – in principle giving the host the possibility to handle the Monitor and C/I channels via the DSP.

5.3 Indirectly Accessible Configuration and Control Registers

Summary:

Addr	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2000 _H	Chip Version Nr					VN3	VN2	VN1	VN0
2001 _H	Reserved	LDMEM	CAEN	DSPMEM	DACC	NRW3	NRW2	NRW1	NRW0
2002 _H	General Config	PU	CRS	CKOEN	CKOS	ODS	CKOBR18	CKOBR17	CKOBR16
2003 _H	CLKO Baud Rate2	CKOBR15	CKOBR14	CKOBR13	CKOBR12	CKOBR11	CKOBR10	CKOBR9	CKOBR8
2004 _H	CLKO Baud Rate1	CKOBR7	CKOBR6	CKOBR5	CKOBR4	CKOBR3	CKOBR2	CKOBR1	CKOBR0
2005 _H	SAI Mode	SODS					SCKIN	PRSC9	PRSC8
2006 _H	SCLK Baud Rate	PRSC7	PRSC6	PRSC5	PRSC4	PRSC3	PRSC2	PRSC1	PRSC0
2007 _H	RFS Mode	RFIN	RCONT	RFE				RREP9	RREP8
2008 _H	RFS Per/Rep Rate	RREP7	RREP6	RREP5	RPRD4/ RREP4	RPRD3/ RREP3	RPRD2/ RREP2	RPRD1/ RREP1	RPRD0/ RREP0
2009 _H	TFS Mode	TFIN	TCONT	TFE				TREP9	TREP8
200A _H	TFS Per/Rep Rate	TREP7	TREP6	TREP5	TPRD4/ TREP4	TPRD3/ TREP3	TPRD2/ TREP2	TPRD1/ TREP1	TPRD0/ TREP0
200B _H	SIO Config						SAIO	SOUT	SINTC
200C _H		0		0	0	0	0	0	0
200D _H		0	0	0	0	0	0	0	0
200E _H		0		0	0	0	0	0	0
200F _H		0	0	0	0	0	0	0	0
2010 _H	Data Cntr Access							HAH1	0
2011 _H	Rec Audio Ch1 Cfg	EN	SLIN1	SLIN0	LEN4	LEN3	LEN2	LEN1	LEN0
2012 _H	Rec Audio Ch1 TS	TS8	TS7	TS6	TS5	TS4	TS3	TS2	TS1
2013 _H	Rec Audio Ch1 Mode	TS0	LMOD	LBIT4	LBIT3	LBIT2	LBIT1	LBIT0	
2014 _H		0	0	0	0	0	0	0	0
2015 _H		0	0	0	0	0	0	0	0
2016 _H		0	0	0	0	0	0	0	
2017 _H	Tx Audio Ch1 Cfg	EN	SLIN1	SLIN0	LEN4	LEN3	LEN2	LEN1	LEN0
2018 _H	Tx Audio Ch1 TS	TS8	TS7	TS6	TS5	TS4	TS3	TS2	TS1

Addr	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2019 _H	Tx Audio Ch1 Mode	TS0	LMOD	LBIT4	LBIT3	LBIT2	LBIT1	LBIT0	HXA
201A _H		0	0	0	0	0	0	0	0
201B _H		0	0	0	0	0	0	0	0
201C _H		0	0	0	0	0	0	0	0
201D _H	SDATA Ser Rec Path				SLIN1	SLIN0	LMOD1	LMOD0	HHR
201E _H	SDATA Ser Tx Path				SLIN1	SLIN0	LMOD1	LMOD0	HHX
201F _H					0	0	0	0	0
2020 _H					0	0	0	0	0
2021 _H	Mon Ch Config				SLIN	MONCH3	MONCH2	MONCH1	MONCH0
2022 _H	Mon Ch Cntr						MRE	MRC	MXC
2023 _H	IC Mon Channel Id	MAD7	MAD6	MAD5	MAD4	MAD3	MAD2	MAD1	MAD0
2024 _H	Monitor Tx/Rec	MONR7/ MONX7	MONR6/ MONX6	MONR5/ MONX5	MONR4/ MONX4	MONR3/ MONX3	MONR2/ MONX2	MONR1/ MONX1	MONR0/ MONX0
2025 _H	C/I Ch Mode					CIEN1	AWK1	CIEN2	AWK2
2026 _H	C/I Ch 1 Config		SLIN	CICH3	CICH2	CICH1	CICH0	CIL	DLL
2027 _H	C/I Ch 2 Config		SLIN	CICH3	CICH2	CICH1	CICH0	CIL	DLL
2028 _H									
2029 _H	C/I Channel 1			CIR5/ CIX5	CIR4/ CIX4	CIR3/ CIX3	CIR2/ CIX2	CIR1/ CIX1	CIR0/ CIX0
202A _H	C/I Channel 2			CIR5/ CIX5	CIR4/ CIX4	CIR3/ CIX3	CIR2/ CIX2	CIR1/ CIX1	CIR0/ CIX0
202B _H	IOM Config								CGEN

Note:

VN(3:0)	Read only (hardwired)
MONR	A read of MONR acknowledges MDR interrupt status (for Host and for DSP)
CIR	A read of CIR acknowledges the C/I Change CIC int status (for Host and for DSP)

Description of Configuration and Control Registers

Unless otherwise indicated, all register bits are initialized to "0" after a hardware reset. During the initialization phase the firmware does a re-programming on the following registers of the configuration/control block to setup the default configuration for the communication with a video-processor (see section 6.2.3.3), i.e. the hardware reset values given in the register description below are overwritten by the following values:

Address	Data	Description
2006 _H	1B _H	SCLK Baud Rate = 28.416 MHz / 28 = 1.01 MHz
2011 _H	8F _H	Receive Uncompressed Audio: DU line, 16 bit linear
2012 _H	10 _H	Position of first bit in time slot: 32
2013 _H	42 _H	Interrupt generated after 2 samples of 16 bits stored
2017 _H	AF _H	Transmit Uncompressed Audio: DD line, 16 bit linear
2018 _H	10 _H	Position of first bit in time slot: 32
2019 _H	42 _H	Interrupt generated after 2 samples of 16 bits stored
201D _H	10 _H	SDATA receiver connected to SR line
201E _H	18 _H	SDATA transmitter connected to ST line

When read, register bits that are not in use (or reserved for future use) are not defined, i.e. their value may be either "0" or "1".

Chip Version Number Register

Read

Address 2000_H

Value after reset: 00_H

VN(3-0)

Version Number of Chip

Reserved Register

Read/Write

Address 2001_H

Value after reset: 00_H

LDMEM

Reserved.

CAEN

Reserved.

DSPMEM

Reserved.

DACC Reserved.
 NRW(3-0) Reserved.

General Configuration Register**Read/Write****Address 2002_H**Value after reset: B0_H

PU	Power Up	
	0	The DSP clock is turned off. It can be started again with a DSP interrupt
	1	Normal operation This is the value of PU after a hardware reset.
CRS	Clock Rate Select	
	0	Input DCL is twice the bit rate on IOM-2
	1	Input DCL is equal to the bit rate on IOM-2
CKOEN	CLKO Enable	
	0	CLKO disabled (output high-impedance), CLKO generator initialized and idle.
	1	Enables generation of CLKO (value during and after Reset)
	Note: When PU is "0" and CKOEN is "0", all outputs and input/outputs of the PSB7238 are in the high-impedance state.	
CKOS	Source clock for CLKO output pin	
	0	Internal DSP system clock is input for divider connected to CLKO
	1	CLKO outputs the buffered XTAL1 clock, may be used to clock e.g. additional JADEs (value during and after Reset)
ODS	Open drain select for IOM DU and DD lines:	
	0	DD and DU are Open Drain (Reset value)
	1	DD and DU are Push-Pull
CKOBR (18-16)	Most significant bits of baud rate division factor for CLKO output from DSP clock	

CLKO Baud Rate Registers

Read/Write

Address 2003_H/2004_H

Value after reset: 00_H

CKOBR(15-0) Less significant bits of baud rate division factor for CLKO output from DSP clock

Serial Audio Interface Signal Register

Read/Write

Address 2005_H-200A_H

Value after reset: 00_H

SODS Serial Audio Interface Open Drain Select for SR and ST line

0 SR and ST are push-pull (Reset value)

1 SR and ST are open drain

SCKIN Serial Clock In

0 SCLK is an output

1 SCLK is input

PRSC(9-0) Prescaler

SCLK is derived from the DSP clock by division through PRSC+1 (1 to 1024), PRSC must be ≥ 3 (division by four) if HDLC1/2 or Audio Channel 1/2 are connected to the serial audio interface and SCLK is programmed as an output

RFIN RFS In

0 RFS is an output

1 RFS is input

RCONT Continuous generation of RFS pulses

0 A number of pulses (spaced 16-bit periods from each other) equal to RREP+1 (1, ..., 1024) is generated upon an STR command (see serial data controller register description)

1 When ERFS bit is "1" (see serial data controller register description), continuous pulses on RFS are generated, spaced RPRD+1 (1, ..., 32) 16-bit words from each other.

RFE RFS Clock Edge

	0	When RFS is generated by the PSB 7238 (=output), it changes its state at the rising edge of the SCLK clock
	1	When RFS is generated by the PSB 7238 (=output), it changes its state at the falling edge of the SCLK clock.
RPRD(4-0)/	Period of RFS pulse generation	
RREP(9-0)	Number of repetition of pulses When RCONT=0, RREP(9-0) gives the number of pulses (RREP+1) to be generated, spaced 16 bits apart (up to 1024 pulses). When RCONT=1, RPRD(4-0) gives the spacing of continuously generated pulses in 16-bit word increments (up to 32).	
TFIN	TFS In	
	0	TFS is an output
	1	TFS is input
TCONT	Continuous generation of TFS pulses	
	0	A number of pulses (spaced 16-bit periods from each other) equal to TREP+1 (1, ..., 1024) is generated upon an STX command (see serial data controller register description)
	1	When ETFS bit is "1" (see serial data controller register description), continuous pulses on TFS are generated, spaced TPRD+1 (1, ..., 32) 16-bit words from each other.
TFE	TFS Clock Edge	
	0	When TFS is generated by the PSB 7238 (=output), it changes its state at the rising edge of the SCLK clock
	1	When TFS is generated by the PSB 7238 (=output), it changes its state at the falling edge of the SCLK clock.
TPRD(4-0)/	Period of TFS pulse generation	
TREP(9-0)	Number of repetition of pulses When TCONT=0, TREP(9-0) gives the number of pulses (TREP+1) to be generated, spaced 16 bits apart (up to 1024 pulses). When TCONT=1, TPRD(4-0) gives the spacing of continuously generated pulses in 16-bit word increments (up to 32).	

SIO Configuration Register**Read/Write****Address 200BH**

Value after reset: 00H

SAIO	Serial Audio Interrupt line In/Out
0	SIO line is an input
1	SIO line is an output
SOUT	Serial Audio Out value. If SAIO=1 (SIO is output), value of SIO line (clocked out with the rising edge of SCLK)
SINTC	Serial Audio Interrupt Configuration
0	If SIO is programmed as input (SIO=0), a falling edge on SIO causes an interrupt, if unmasked
1	If SIO is programmed as input (SIO=0), a rising edge on SIO causes an interrupt, if unmasked.

Data Controller Access Register **Read/Write** **Address 2010_H**
 Value after reset: 00_H

HAH1	Host Access to serial data Controller
0	The DSP services the data controller (register set including FIFOs is inaccessible from Host)
1	The Host services the data controller (register set including FIFOs is inaccessible from DSP).
This bit determines the access to the register area of the data controller; it is independent of the HHR and HHX bits which determine the access from DSP or Host to the serial data input and output, respectively.	

Receive Audio Channel 1 **Read/Write** **Address 2011_H-2013_H**
 Value after reset: 00_H

EN	Enable
If inactive (0), no clock is generated for this channel, must be set to 0 during configuration of receive audio channel 1	
SLIN(1-0)	Select Line

	00	Channel time-slot on DU (frame sync FSC, clock DCL or DCL/2)
	01	Channel time-slot on DD (frame sync FSC, clock DCL or DCL/2)
	10	Channel time-slot on SR (frame sync RFS, clock SCLK)
	11	Channel time-slot on ST (frame sync TFS, clock SCLK)
LEN(4-0)	Length of channel time-slot Channel time-slot length in bits = LEN+1 (1, ..., 32 bits)	
TS(8-0)	Time slot position Position of first bit of time-slot from frame sync (0, ..., 511)	
LMOD	Load Mode	
	0	Sample of length LEN+1 loaded into read register (from frame-1) at the occurrence of frame sync
	1	(LBIT+1)*(LEN+1) bits are loaded into read register when ready (for software to be accessed via a "Buffer Full" interrupt status)
LBIT(4-0)	Load Bits Number of bits in aggregates of (LEN+1) loaded into read register when ready, if LMOD=1. The number of bits loaded is equal to (LBIT+1)*(LEN+1), the corresponding interrupt status is BFUL1. Note: Since the number of bits is 32 maximum, the value of the product (LBIT+1)*(LEN+1) shall not exceed 32.	

Transmit Audio Channel 1**Read/Write Address 2017_H-2019_H**Value after reset: 00_H

EN	Enable If inactive (0), no clock is generated for this channel, and the channel is in high impedance, must be set to 0 during configuration of transmit audio channel 1
SLIN(1-0)	Select Line
	00 Channel time-slot on DU (frame sync FSC, clock DCL or DCL/2)
	01 Channel time-slot on DD (frame sync FSC, clock DCL or DCL/2)

	10	Channel time-slot on SR (frame sync RFS, clock SCLK)
	11	Channel time-slot on ST (frame sync TFS, clock SCLK)
LEN(4-0)	Length of channel time-slot	
	Channel time-slot length in bits = LEN+1 (1, ..., 32 bits)	
TS(8-0)	Time slot position	
	Position of first bit of time-slot from frame sync (0, ..., 511)	
LMOD	Load Mode	
	0	Sample of length LEN+1 loaded from write register into shift register (for frame+1) at the occurrence of frame sync
	1	When shift register is about to become empty ((LBIT+1)*(LEN+1) bits shifted out), it is loaded from write register (for software to be accessed via a "Buffer Empty" interrupt status)
LBIT(4-0)	Load Bits	
	Number of bits in aggregates of (LEN+1) loaded into output shift register when ready, if LMOD=1. The number of bits loaded is equal to (LBIT+1)*(LEN+1), the corresponding interrupt status is BEMP1.	
	Note: Since the number of bits is 32 maximum, the value of the product (LBIT+1)*(LEN+1) shall not exceed 32.	
HXA	Host Transmit Access	
	0	Channel originates from DSP
	1	Channel originates from Host

Serial Data Channel Receive Path Register Read/Write Address 201D_H

Value after reset: 00_H

SLIN(1-0)	Select Line	
	00	Channel on DU (frame sync FSC, clock DCL or DCL/2)
	01	Channel on DD (frame sync FSC, clock DCL or DCL/2)
	10	Channel on SR (frame sync RFS, clock SCLK)
	11	Channel on ST (frame sync TFS, clock SCLK)
LMOD(1-0)	Load Mode	

	00	When shift register contains one byte, it is loaded into data receiver as soon as possible (and, in addition, to DSP/Host read register for monitoring)
	XX	When shift register contains n bytes (XX=01:n=1; XX=10:n=2; XX=11: n=4), the contents is loaded into DSP and Host read register, DSP or Host (cf. HHR1 bit) write register is loaded into data receive buffer, and read DSP or Host read register is loaded into DSP or Host write register (for software to be accessed via a "Buffer Full" interrupt status)
HHR		Host Data Receiver Access
	0	DSP has access to modify data receiver input (monitoring from host still possible)
	1	Host has access to modify data receiver input (monitoring from DSP still possible)

Serial Data Channel Transmit Path Register Read/Write Address 201E_H

Value after reset: 00_H

SLIN(1-0)	Select Line
	00 Channel on DU (frame sync FSC, clock DCL or DCL/2)
	01 Channel on DD (frame sync FSC, clock DCL or DCL/2)
	10 Channel on SR (frame sync RFS, clock SCLK)
	11 Channel on ST (frame sync TFS, clock SCLK)
LMOD(1-0)	Load Mode
	00 When shift register is about to become empty, it (as well as DSP and Host read registers) is loaded from data transmitter
	XX When shift register contains n bytes (XX=01:n=1; XX=10:n=2; XX=11: n=4), the contents is loaded into DSP and Host read register, DSP or Host (cf. HHR bit) write register is loaded into data receive buffer, and read DSP or Host read register is loaded into DSP or Host write register (for software to be accessed via a "Buffer Empty" interrupt status)
HHX	Host Data Transmitter Access

- 0 DSP has access to modify data transmitter output (monitoring of data output from host still possible)
- 1 Host has access to modify data receiver input (monitoring of data output from DSP still possible)

Monitor Channel Configuration Register Read/Write Address 2021_H

Value after reset: 00_H

- SLIN Select Line
- 0 Receive channel on DD, transmit channel on DU
 - 1 Receive channel on DU, transmit channel on DD
- MONCH(3-0) Monitor Channel position
- Monitor channel (same time-slot for receive and transmit direction)
located in the 3rd byte of multiplex MONCH (0 to 15)

Monitor Channel Control Register Read/Write Address 2022_H

Value after reset: 00_H

- MRE Monitor channel Receive Enable
- 0: Receive Monitor channel inactive
 - 1: Receive Monitor channel active
- MRC MR bit Control
- 0: No acknowledgement is sent in response to a received byte. When MRE=1 and MRC=0, only the first byte of a packet can be received, further bytes (in the case that the first byte is acknowledged by another IC) are not loaded into MONR
 - 1: Acknowledgement via MR bit is enabled, acknowledgement takes place after MONR is read
- MXC Monitor Transmit Control
- 0: Transmit Monitor channel inactive (high impedance)
 - 1: Monitor channel transmission enabled

Monitor Channel Address (IC Identification) Read/Write Address 2023_HValue after reset: 00_H

MAD Monitor Address
Programmable from host (if present).

Monitor Channel Transmit/Receive Register Read/Write Address 2024_HValue after reset: 00_H

MONX Monitor Transmit Register (write)
Value of Monitor byte to be transmitted

MONR Monitor Receive Register (read)
Value of received Monitor Channel byte. A read of this register enables
the automatic acknowledgement of the received byte.

C/I Channel Mode Register Read/Write Address 2025_HValue after reset: 00_H

CIEN1,2 C/I Channel 1,2 Enable

0: Transmission of C/I channel disabled (channel in high impedance)

1: Transmission of C/I channel enabled. When CIEN is changed, the change takes effect only after the next rising edge of FSC is detected, in order to prevent sending an "illegal" code in the C/I channel. One should avoid changing the state of CIEN just when a rising edge on FSC is expected.

AWK1,2 Awake for C/I channel 1,2

0: C/I channel normal operation

- 1: A "low" is unconditionally sent on the line programmed for C/I transmit channel.
- Note:** When AWK is set to "1", the line (DD or DU) is immediately pulled low (non-synchronously with clock). When AWK is set to "0", the line is "set free" only after the next rising edge of FSC is detected. One should avoid setting AWK to "0" just when a rising edge on FSC is expected.

C/I Channel 1, 2 Configuration RegistersRead/WriteAddress 2026_H/2027_H

Value after reset: 00_H

SLIN	Select Line
0	Receive channel on DD, transmit channel on DU
1	Receive channel on DU, transmit channel on DD
CICH(3-0)	C/I Channel position
	C/I channel (same time-slot for receive and transmit direction) located in the 4th byte of multiplex CICH (0 to 15)
CIL	C/I Channel Length
0:	4 bits
1:	6 bits
DLL	Double Last Look
0:	No double last look
1:	C/I channel change confirmed only after two consecutive identical values are received

C/I Channel 1 Transmit/Receive RegisterRead/WriteAddress 2029_H

Value after reset: 00_H

CIX	C/I Channel Transmit
	Value of transmitted C/I channel
CIR	C/I Channel Receive (read)
	Value of received C/I channel

C/I Channel 2 Transmit/Receive Register **Read/Write** **Address 202A_H**

Value after reset: 00_H

- CIX C/I Channel Transmit
Value of transmitted C/I channel
- CIR C/I Channel Receive (read)
Value of received C/I channel

IOM Configuration Register **Read/Write** **Address 202B_H**

Value after reset: 00_H

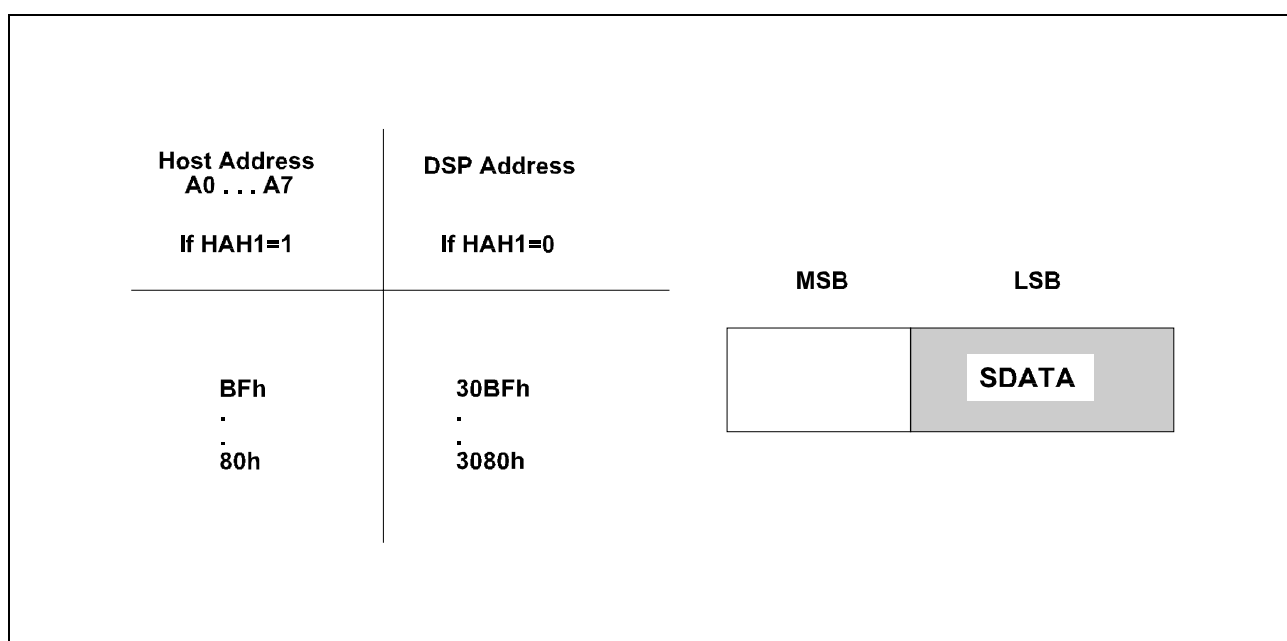
- CGEN Clock Generation for IOM-2 interface (TE mode)
 - 0 FSC and DCL are inputs (Reset value)
 - 1 FSC and DCL are outputs (DCL=1.536 MHz, FSC=8 KHz)

5.4 Serial Data Controller Registers

As mentioned previously, the addresses for the Data Controller registers are given here for the DSP for completeness only, since they are only relevant for the on-chip firmware.

The access to the register banks of the data controller is determined by the "Data Controller Access from Host" bit HAH1:

- When HAH1 is 0, the DSP is allowed to access the Data Controller register bank, and thus to service the data controller.
- When HAH1 is "1", the Host is allowed to service the data controller.



In the following tables the addresses are relative to the base address 80_H. In each row, the upper line lists the read values, the lower the write values of the corresponding register.

Byte address offset	Read Write	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00 _H . 1F _H	RFIFO XFIFO								
20 _H	STAR XCMD	XDOV XF	- -	XCEC XRES	RCEC -	- -	- -	STR -	STX STX
21 _H									

Byte address offset	Read Write	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
22 _H	MODE MODE	1 -	RAC RAC	XAC XAC	TLP TLP		- -	ERFS ERFS	ETFS ETFS
23 _H									
24 _H									
25 _H	- RCMD	- RMC	- RRES	- -	- -	- -	- -	- STR	- -
26 _H	CCR0 CCR0	PU PU	- -	- -	- -	- -	- -	RMSB RMSB	XMSB XMSB
27 _H	CCR1 CCR1	RCS0 RCS0	RSCO RSCO	RFDIS RFDIS	XCS0 XCS0	TSCO TSCO	XFDIS XFDIS	- -	- -
28 _H	TSAR TSAR	TSR5 TSR5	TSR4 TSR4	TSR3 TSR3	TSR2 TSR2	TSR1 TSR1	TSR0 TSR0	RCS2 RCS2	RCS1 RCS1
29 _H	TSAX TSAX	TSX5 TSX5	TSX4 TSX4	TSX3 TSX3	TSX2 TSX2	TSX1 TSX1	TSX0 TSX0	XCS2 XCS2	XCS1 XCS1
2A _H	RCCR RCCR	RCC7 RCC7	RCC6 RCC6	RCC5 RCC5	RCC4 RCC4	RCC3 RCC3	RCC2 RCC2	RCC1 RCC1	RCC0 RCC0
2B _H	XCCR XCCR	XCC7 XCC7	XCC6 XCC6	XCC5 XCC5	XCC4 XCC4	XCC3 XCC3	XCC2 XCC2	XCC1 XCC1	XCC0 XCC0
2C _H	ISR IMR	- -	RPF RPF	RFO RFO	XPR XPR	- -	ALLS ALLS	- -	- -

Unless otherwise indicated, all register bits are initialized to "0" after a hardware reset.

During the initialization phase the firmware does a re-programming on the following registers of the serial data controller to setup the default configuration for the communication with a video-processor (see section 6.2.3.3):

Address	Data	Description
30A2 _H	80 _H	Transparent Mode
30A5 _H	40 _H	Receiver Reset
30A6 _H	83 _H	Power Up, MSB first for Receiver and Transmitter
30AA _H	0F _H	Receiver: 16 bit time-slot
30AB _H	0F _H	Transmitter: 16 bit time-slot
30AC _H	50 _H	Interrupt Enable for RPF and XPR

When read, register bits that are not in use (or reserved for future use) are not defined, i.e. their value may be either "0" or "1".

Receive FIFO	RFIFO	Read	Address 00-1F_H
---------------------	--------------	-------------	----------------------------------

The serial data receive FIFO size is 2*32 bytes. One half of the FIFO is connected to the receiver shift register while the second half is accessible to the controlling processor.

Transmit FIFO XFIFO Write Address 00-1F_H

The transmit FIFO size is 2*32 bytes. One half is connected with the transmit shift register while the other half is accessible to the controllig processor.

Status Register STAR Read Address 20_H

	Bit 7							Bit 0
STAR	XDOV	-	XCEC	RCEC	-	-	STR	STX

- XDOV

Transmit Data Overflow
Indicates that more than 32 bytes have been written into the transmit FIFO.
- XCEC

Transmitter Command Executing
If "1", a command is currently executed by the transmitter and no further command may be written into the XCMD register. When "0", a new command may be entered into XCMD.
- RCEC

Reveiver Command Executing
If "1", a command is currently executed by the receiver and no further command may be written into the RCMD register. When "0", a new command may be entered into RCMD.

- STR** Status of generation of RFS pulses
Only valid when RFIN=0 (RFS pulses internally generated) and used if RCONT bit in RFS mode register is =0.
A "1" indicates that generation of pulses as a result of a previous STR command is still on-going; STR is reset to "0" 16 bit periods after the last RFS pulse has been generated.
This function may be used in connection with the data controller when a predefined number of data units (e.g. words) are received, clocked by RFS pulses.
- STX** Status of generation of TFS pulses
Only valid when TFIN=0 (TFS pulses internally generated) and used if TCONT bit in TFS mode register is =0.
A "1" indicates that generation of pulses as a result of a previous STX command is still on-going; STX is reset to "0" 16 bit periods after the last TFS pulse has been generated.
This function may be used in connection with the data controller when a predefined number of data units (e.g. words) are to be transmitted, clocked by TFS pulses.

Transmit Command Register XCMD

(Write)

Address 20_H

	Bit 7							Bit 0	
XCMD	XF			XRES					STX

XF Transmit Frame

Initiates transmission of a pool of data (up to 32 bytes).

XRES Transmitter Reset.

When XAC=1, this command resets the data transmitter, clears the transmit FIFO and generates an XPR status after the command has been completed.

When XRES is issued while XAC=0, this command initializes in addition the time-slot count logic for this channel.

STX	Start command for TFS generation
-----	----------------------------------

Only valid when TFIN=0 (TFS pulses internally generated) and used if TCONT bit in TFS mode register is =0.

When TCONT=0, when STX is set, exactly TREP(9-0) pulses of one bit duration and spaced 16 bit periods from each other are generated. When STX command is given, generation of pulses starts at the next possible 16-bit boundary.

This function may be used in connection with the data controller when a predefined number of data units (e.g. words) are transmitted, clocked by TFS pulses.

Mode Register MODE Read/Write Address 22_H

	Bit 7						Bit 0	
MODE	1/-	RAC	XAC	TLP			ERFS	ETFS

RAC	<p>Receiver Active</p> <p>Sets the receiver in an active state.</p> <p>Note: When RAC is set to "1", storage of bytes in the receive FIFO starts time-slot aligned (if the receive time-slot length is a multiple of 8 bits).</p>
XAC	<p>Transmitter Active</p> <p>When XAC is set to "1", transmission of bytes from the transmit FIFO starts time-slot aligned (if the transmit time-slot length is a multiple of 8 bits).</p> <p>When XAC=0, the time-slot assigned to the transmitter is in high impedance.</p>
TLP	<p>Test Loop</p> <p>When "1", output of the data controller is connected to input (i.e. what is transmitted is simultaneously received). The loop is transparent.</p>
ERFS	<p>Enable RFS generation</p> <p>Only valid when RFIN=0 (RFS pulses internally generated) and used if RCONT bit in RFS mode register is =1.</p> <p>When RCONT=1, an ERFS value of "1" enables the generation of RFS pulses of one bit duration and spaced RPRD+1 (1, ..., 32) 16-bit words from each other. Pulses are generated indefinitely until ERFS is set to "0" again.</p>
ETFS	<p>Enable TFS generation</p> <p>Only valid when TFIN=0 (TFS pulses internally generated) and used if TCONT bit in TFS mode register is =1.</p> <p>When TCONT=1, an ETFS value of "1" enables the generation of TFS pulses of one bit duration and spaced TPRD+1 (1, ..., 32) 16-bit words from each other. Pulses are generated indefinitely until ETFS is set to "0" again.</p>

Receive Command Register RCMD Write Address 25_H

	Bit 7						Bit 0	
RCMD	RMC	RRES					STR	

- RMC

Receive Message Complete
Acknowledges a previous RPF status. Frees the FIFO pool for the next received frame or part of a frame.
- RRES

Receiver Reset
When RAC=1, this command resets the data receiver and clears the receive FIFO.
When RRES is issued while RAC=0, this command initializes in addition the time-slot count logic for this channel.
- STR

Start command for RFS generation
Only valid when RFIN=0 (RFS pulses internally generated) and used if RCONT bit in RFS mode register is =0.
When RCONT=0, when STR is set, exactly RREP(9-0) pulses of one bit duration and spaced 16 bit periods from each other are generated. When STR command is given, generation of pulses starts at the next possible 16-bit boundary.
This function may be used in connection with the data controller when a predefined number of data units (e.g. words) are received, clocked by RFS pulses.

Channel Configuration Register 0 CCR0 Read/Write Address 26_H

	Bit 7						Bit 0	
CCR0	PU						RMSB	XMSB

PU	Power Up Power down (0) or power up (1).
RMSB	Receive MSB first When RMSB=0, the least significant bit of a byte in the receive FIFO is the bit first received (normal mode in serial data communication protocols). When RMSB=1, the most significant bit of a byte in the receive FIFO is the first bit received.
XMSB	Transmit MSB first When XMSB=0, the least significant bit of a byte in the transmit FIFO is the bit first transmitted (normal mode in serial data communication protocols). When XMSB=1, the most significant bit of a byte in the transmit FIFO is the first bit transmitted.

Channel Configuration Register 1 CCR1

Read/Write

Address 27_H

	Bit 7						Bit 0	
CCR1	RCS0	RSCO	RFDIS	XCS0	TSCO	XFDIS		

- RCS0

Receive Clock Shift 0
Together with RCS2 and RCS1 in TSAR, determines the clock shift relative to the frame synchronization signal. A clock shift of 0...7 is programmable.
- XCS0

Transmit Clock Shift 0
Together with XCS2 and XCS1 in TSAX, determines the clock shift relative to the frame synchronization signal. A clock shift of 0...7 is programmable.
- RSCO

Receive Time-slot Continuous
When RSCO is equal to one, the time-slot capacity (normally given by register RCCR, between 1 and 256 bits) is "infinity". This means that the time-slot will be always "active" so that data can be permanently received if RAC=1.
If RFDIS=0, and if the time-slot count logic has been reset (by issuing RRES while RAC=0), time-slot logic can start operation and thus "activate" a time-slot only after the first frame sync pulse is detected (i.e. on FSC, RFS, or TFS, whichever has been selected). The time-slot offset register TSAR + bit RCS0 mark the instant when the "infinite" time-slot will be activated after the first frame sync pulse has occurred. If RFDIS=1, reception can start immediately, without the necessity to wait for the first frame sync pulse.
- RFDIS

Receive Frame Sync Disregard
When RFDIS is "1", the time-slot generation logic disregards frame syncs. In particular, if RSCO=1 and RFDIS=1, receive time-slot is immediately considered as permanently "active", and remains activated as long as this condition prevails.

- TSCO** Transmit Time-slot Continuous
 When TSCO is equal to one, the time-slot capacity (normally given by register XCCR, between 1 and 256 bits) is "infinity". This means that the time-slot will be always "active" so that data can be permanently transmitted if XAC=1.
 If TFDIS=0, and if the time-slot count logic has been reset (by issuing XRES while XAC=0), time-slot logic can start operation and thus "activate" a time-slot only after the first frame sync pulse is detected (i.e. on FSC, RFS, or TFS, whichever has been selected). The time-slot offset register TSAX + bit XCS0 mark the instant when the "infinite" time-slot will be activated after the first frame sync pulse has occurred. If TFDIS=1, transmission can start immediately, without the necessity to wait for the first frame sync pulse.
- TFDIS** Transmit Frame Sync Disregard
 When TFDIS is "1", the time-slot generation logic disregards frame syncs. In particular, if TSCO=1 and TFDIS=1, transmit time-slot is immediately considered as permanently "active", and remains activated as long as this condition prevails.

Time-Slot Assignment Receive TSAR Read/Write Address 28_H

	Bit 7						Bit 0	
TSAR	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0	RCS2	RCS1

- TSR** Time-Slot Receive
 Selects one of up to 64 possible time-slots (00h-3F_H) in which data is received. TSR gives the location of the time-slot in octets (granularity=octet). The bits RCS(2-0) give the exact starting point of the time-slot with one-bit precision. In other words, the time-slot position with respect to the frame sync is given by (TSR*8+RCS). The length of the time-slot is given by RCC(7-0).
- RCS** Receive Clock Shift
 Together with RCS0, RCS1 and RCS2 mark the start of the time-slot with one-bit granularity.

Time-Slot Assignment Transmit TSAX Read/Write Address 29_H

	Bit 7						Bit 0	
TSAX	TSX5	TSX4	TSX3	TSX2	TSX1	TSX0	XCS2	XCS1

TSX Time-Slot Transmit
Selects one of up to 64 possible time-slots (00h-3F_H) in which data is transmitted. TSX gives the location of the time-slot in octets (granularity=octet). The bits XCS(2-0) give the exact starting point of the time-slot with one-bit precision. In other words, the time-slot position with respect to the frame sync is given by (TSX*8+XCS). The length of the time-slot is given by XCC(7-0).

XCS Transmit Clock Shift
Together with XCS0, XCS1 and XCS2 mark the start of the time-slot with one-bit granularity.

Receive Channel Capacity Register RCCR Read/Write Address 2A_H

	Bit 7						Bit 0	
RCCR	RCC7	RCC6	RCC5	RCC4	RCC3	RCC2	RCC1	RCC0

RCC Receive Channel Capacity
Defines the number of bits in the receive time-slot.
Number of bits = RCC +1 (1...256 bits/time-slot).

Transmit Channel Capacity Register XCCR Read/Write Address 2B_H

	Bit 7						Bit 0	
XCCR	XCC7	XCC6	XCC5	XCC4	XCC3	XCC2	XCC1	XCC0

XCC Transmit Channel Capacity
Defines the number of bits in the transmit time-slot.
Number of bits = XCC + 1 (1...256 bits/time-slot).

Interrupt Status Register	ISR	Read	Address 2C_H
----------------------------------	------------	-------------	-------------------------------

	Bit 7							Bit 0
ISR		RPF	RFO	XPR		ALLS		

RPF Receive Pool Full
32 bytes have been received and can be read from the FIFO.

RFO	Receive Frame Overflow
	Signifies that data has been lost because no room was available in RFIFO.

XPR Transmit Pool Ready
One data block may be entered into the transmit FIFO.

ALLS All Sent.
When "1", indicates that the last bit has been transmitted and that the XFIFO is empty.

Interrupt Mask Register IMR Write Address 2C_H

A "0" in a bit position (status after reset) masks the corresponding bit in ISR.



6 Firmware Features

This section describes the features and protocols of the on-chip ROM-based firmware. After a hardware reset, the firmware starts automatically initializing the internal memories and setting up the JADE AN in its default configuration.

Note on "Reset Time": The initialization time after reset is guaranteed to be less than 10 msec. The user must take care to access the JADE AN only after this initialization phase is completed, i.e. 10 msec after the hardware reset.

In the description of the register blocks (see sections 5.3 and 5.4) the hardware reset values are listed separately from the values which are re-initialized by the firmware setup, which is done during these first 10 msec. The default interface configuration programmed by the firmware is described in section 6.2.3.3.

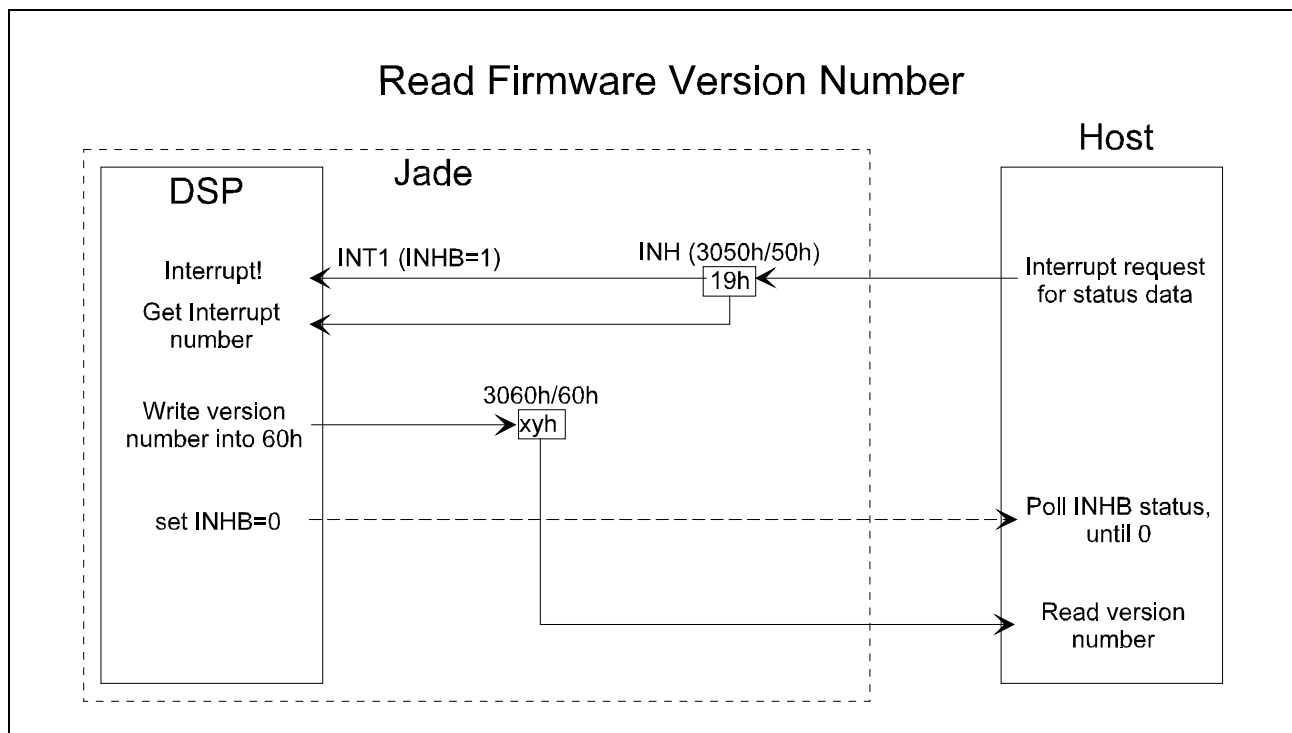
In the case one does not want to use the default configuration, a re-programming of the configuration-/control-registers can be done 10 msec after the reset.

Note on "Polling Host": The firmware features are using interrupt handshakes via the registers INH (Host write to 50h) and IND (Host read from 58h). A polling host should not directly poll the IND interrupt status register 58h, but the DINT bit in INT# interrupt status register 75h. This bit always shows whether an interrupt from the DSP has been generated or not, independently of the corresponding mask register. The mask register only decides whether an interrupt at INT# line is generated. After having recognized an IND interrupt status, the polling host may read out the register 58h to get the interrupt number.

6.1 Basic Functions

6.1.1 Firmware Version Number

To obtain the version number of the on-chip firmware, the following interrupt handshake procedure has to be implemented by a host:



The following steps are executed:

1. The host generates an interrupt to the JADE by writing value 19h into INH interrupt status register at address 50h.
2. The JADE writes the firmware version number into communication register accessible from the host at address 60h and resets the INHB bit to 0.
3. The host checks the INHB bit and as soon as it reads a "0" it may get the version number from register 60h. *)

*) The INHB=0 polling is not supported in some previous JADE versions (older than JADE 2.2 and JADE MM 1.2). Thus, if also these versions need to be identified by reading the version number, this can be obtained by waiting for 1 msec instead of polling the INHB=0 condition. For the JADE versions supporting the INHB=0 it is ensured that the INHB=0 condition becomes true in less than 1 msec.

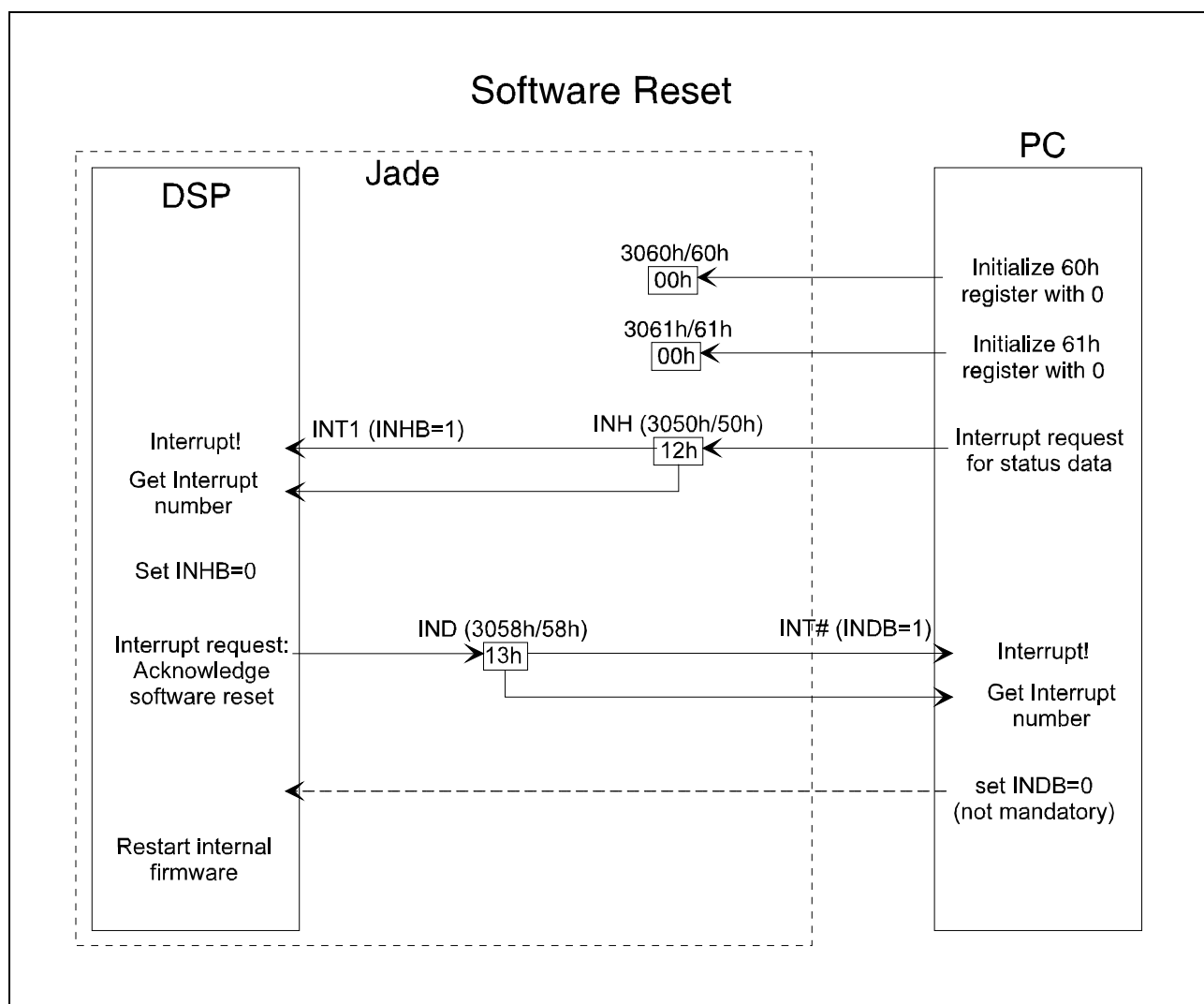
The version number of JADE AN 1.2 is: **xyh = A2h**

Thus the "xyh" in the picture above has to be substituted by this number.

6.1.2 Software Reset

A software reset is used to re-initialize the JADE AN without resetting the hardware. This means that e.g. not the whole configuration/control register area is reset, but only the firmware initialization (see sections 5.3 and 5.4) is executed.

See figure below:



The following steps are executed:

1. The host initializes the control registers 60h and 61h by writing a "0" into it.
2. The host generates an interrupt to the JADE by writing value 12h into INH interrupt status register at address 50h

Firmware Features

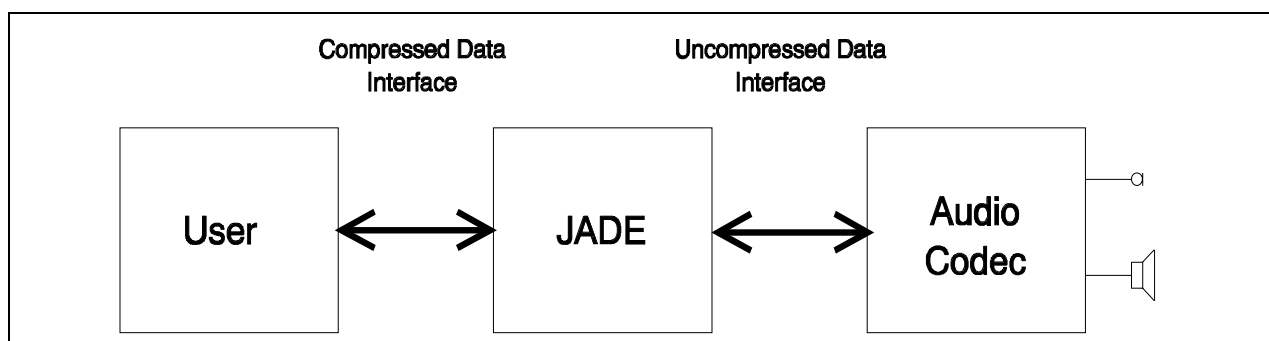
3. The JADE resets the INHB bit and acknowledges the reception by generating an interrupt at INT# line to the host by writing a value 13h into IND interrupt status register at address 58h.
4. The host may reset the INDB as a reaction to the JADE interrupt. This step is not mandatory and may be skipped.
5. The JADE restarts its internal firmware beginning with the initialization phase.

For the restart of the internal firmware the JADE AN needs the same initialization time like after a hardware reset. So, the user should wait for 10 msec before it accesses the JADE AN again.

6.2 Audio Interfaces

In order to cover a wide range of applications, the JADE AN offers a variety of different interface combinations and protocols for the uncompressed/compressed data exchange.

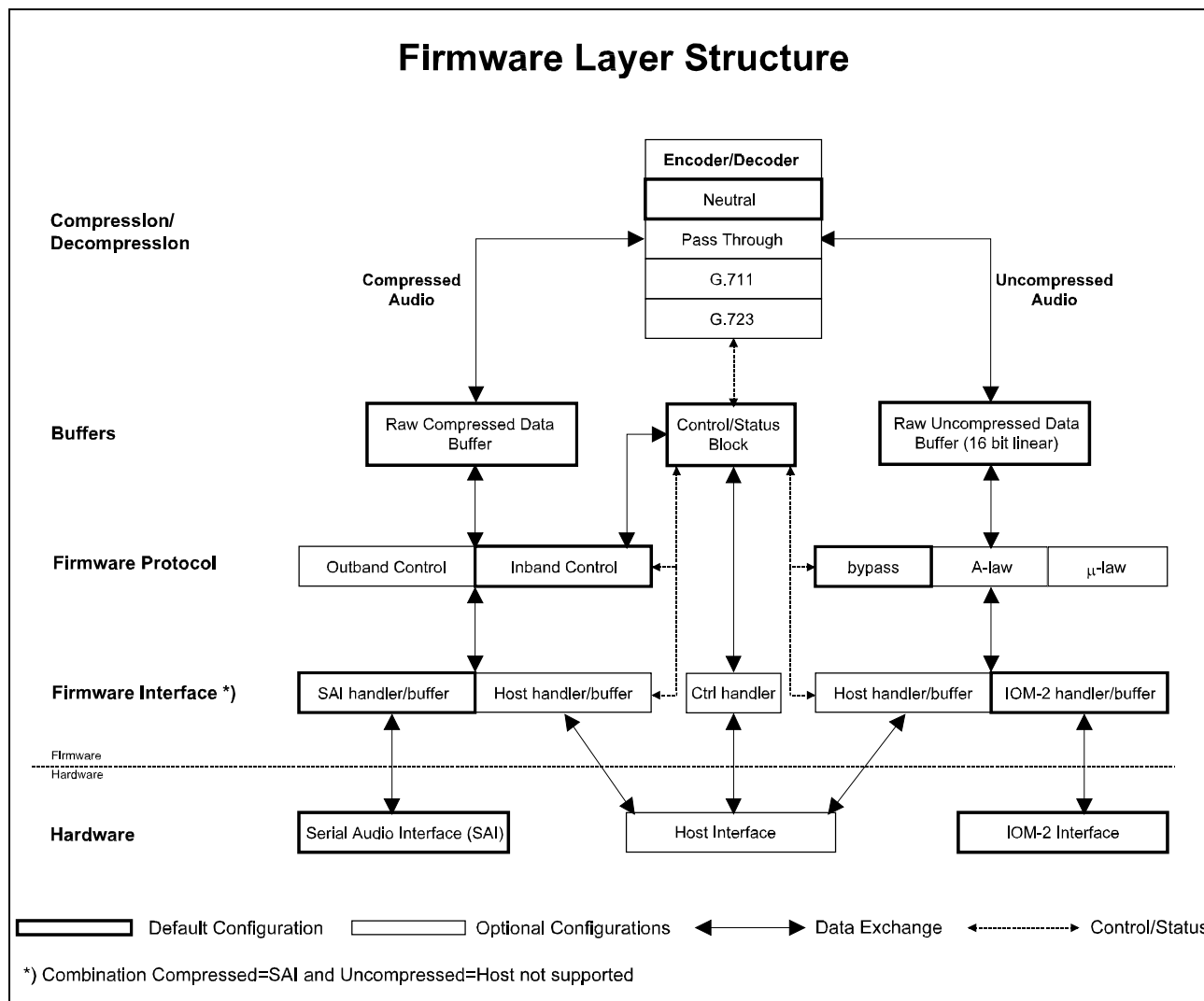
The basic interfacing is like in the figure below:



Two interfaces are necessary, one for compressed audio connected to a User and one for uncompressed audio connected to a Codec.

By switching the compressed/uncompressed data stream to different hardware interfaces (Host, IOM, Serial Audio Interface), the JADE AN is able to support standalone solutions using a video processor (compressed data provided on Serial Audio Interface) as well as Host systems (e.g. software video coders using the Host Interface for the compressed data) or offline audio compression (compressed and uncompressed audio exchanged through Host Interface).

See the following figure for the firmware layer structure and the corresponding structure of the description:



The audio interface description is split up into two basic parts:

In the first part the "Firmware Protocol" (data format, data packet size) and mode control (inband or outband) are described (sections 6.2.1 and 6.2.2) which are independent of the selected hardware-interface combination.

In the second part the "Firmware Interface" combinations for uncompressed and compressed audio, i.e. the individual timings and handshake procedures for the selected hardware-interface combination are described (section 6.2.3).

6.2.1 Compressed Audio Protocols and Control of JADE AN

In the following sections the protocols for the exchange of compressed audio data between the JADE AN and a user are described.

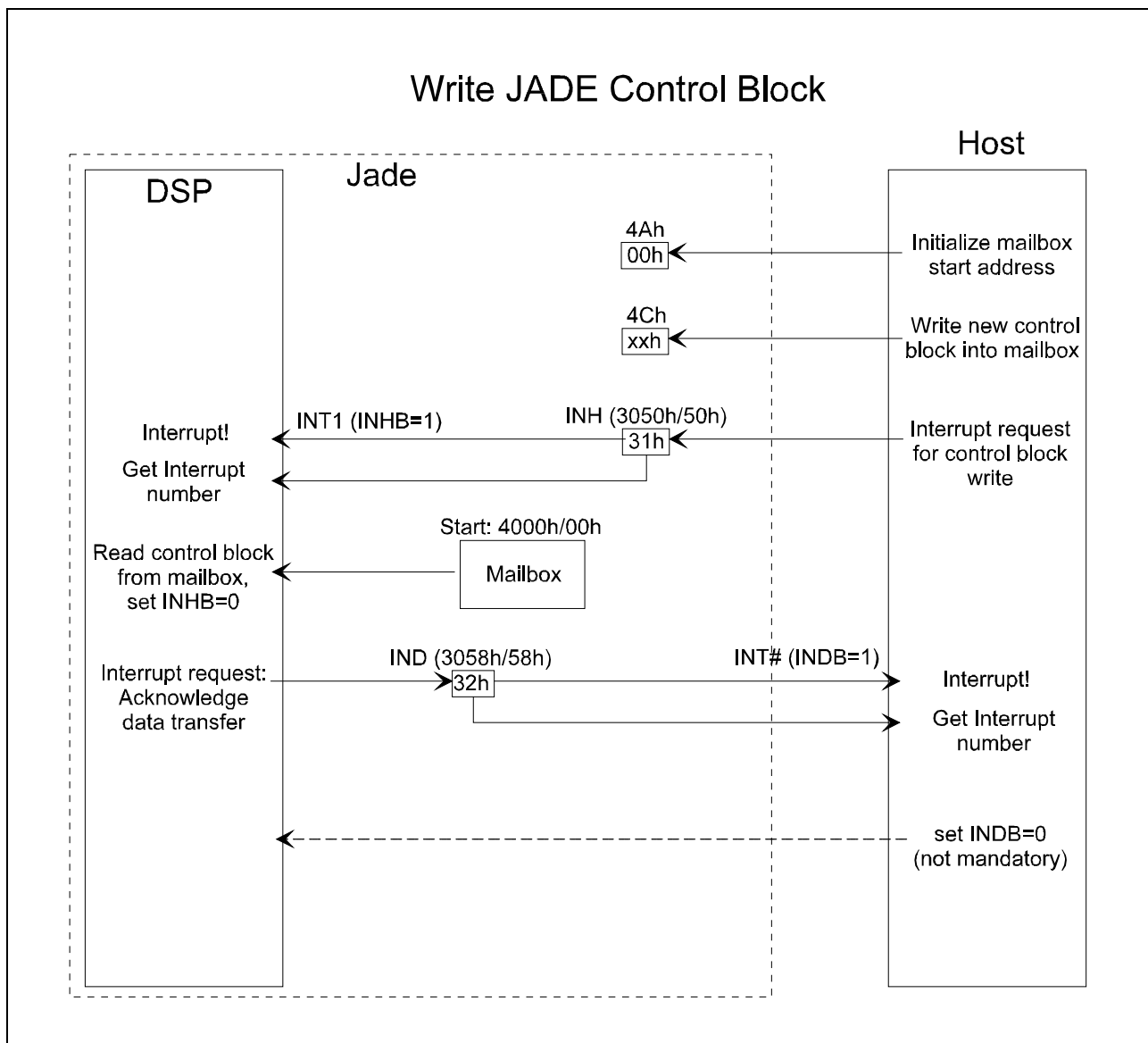
6.2.1.1 Outband Control of JADE AN

All times that are given in this chapter refer to realtime processing of a 10 msec frame length of the audio data, which is the default setting of the JADE AN. When doing offline processing (compressed and uncompressed data exchanged through the host), the delay times in this chapter have to be substituted by the corresponding number of frames. For example, a delay time of 30 msec corresponds to three frames of audio data exchange when doing offline processing.

The host may change the JADE AN operating mode by sending a command block, and the JADE AN will send back a status block, if requested by the host. Command and status blocks consist of 8-bit words.

To exchange command and status blocks, the host initiates an interrupt handshake procedure.

See the figure below for the host writing a new control block to the JADE AN:



The following steps are executed:

1. The host writes new control block into JADE mailbox using the procedure described in section 3.4.
2. The host generates an interrupt to the JADE by writing value 31h into INH interrupt status register at address 50h.

Firmware Features

1. The host writes new control block into JADE mailbox using the procedure described in section 3.4.
3. The JADE reads the new control block from the mailbox, resets the INHB bit and acknowledges the reception by generating an interrupt at INT# line to the host by writing a value 32h into IND interrupt status register at address 58h.
4. The host may reset the INDB as a reaction to the JADE interrupt. This step is not mandatory and may be skipped.

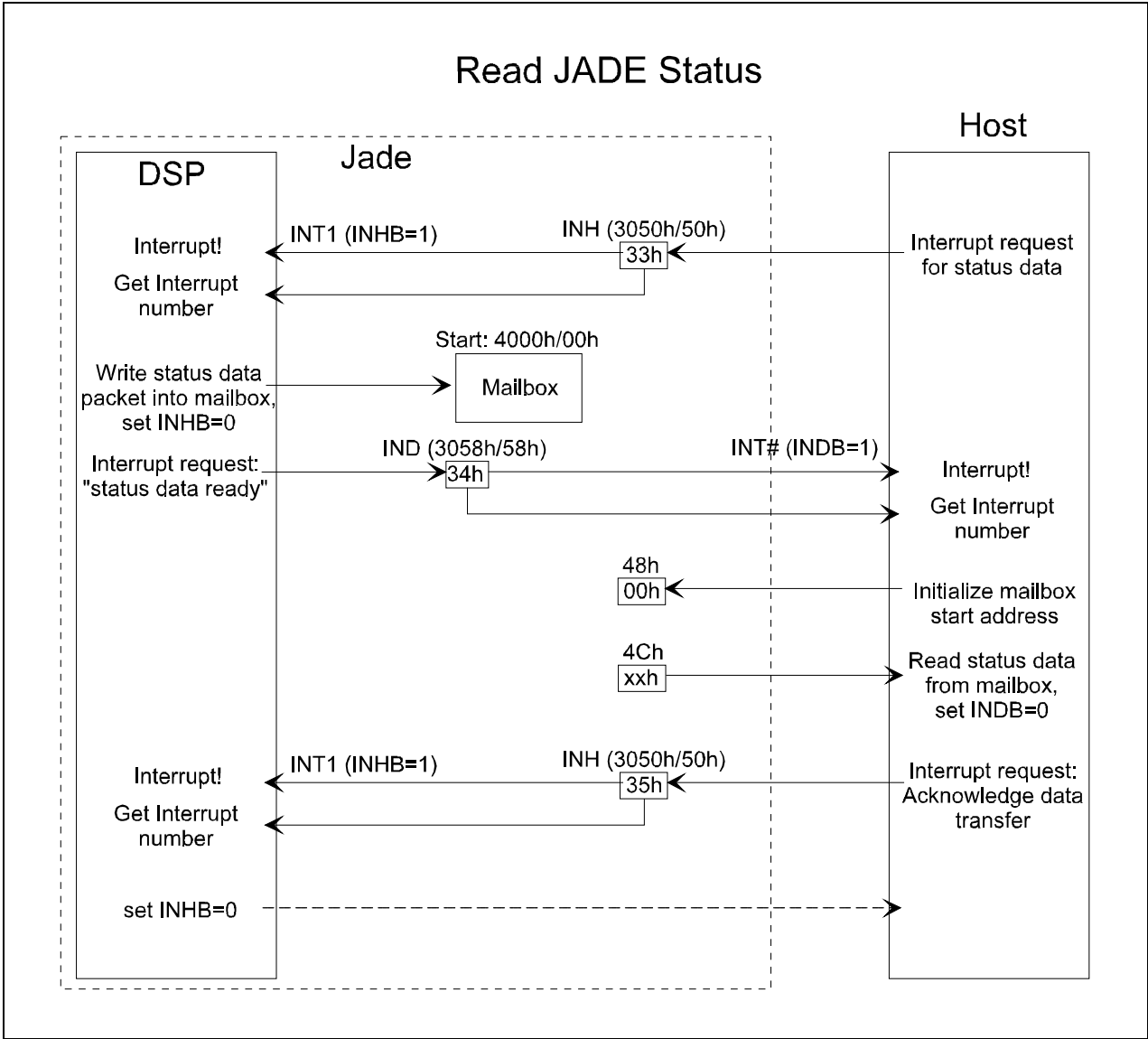
Any changes to the current operating mode of the JADE AN take effect on the next input data packets, i.e. when a 10 msec frame length is selected, the next 10 msec packet of uncompressed data will be compressed using the new settings and the next 10 msec packet of compressed data will be decompressed using the new settings, too.

Due to internal buffering, a three stages pipeline appears in the JADE AN (input, compression/decompression, output). Each stage takes as long as determined by the frame length (default: 10 msec). For that reason, a mode switch affecting the input data of the JADE AN has to go through the whole pipeline before the output data reports the new settings. This results in a delay of three times the frame length (default: 30 msec) between the host requesting a new mode setting and the JADE AN delivering the first packet of data compressed/decompressed with these new settings and reporting the new settings in the status data block.

Note on "Control Block Change": To change the control block data, the host must first set the mode to neutral (see MODE register description below) for at least four frames (default: 40 msec). Although the MODE word is part of the control block, it can be changed to neutral at any time. The switch to neutral mode before doing other changes to the control block is required to clear up the JADE's pipeline and make sure it does not have to process two different modes at once in the same pipeline. Following the neutral mode command, the host may transfer the control block with the new settings.

Some bits in the control block don't require this procedure (volume change, ...). These are especially indicated in the description of the control block (see below).

See the figure below for the host reading the current status data block from the JADE AN:



The following steps are executed:

1. The host generates an interrupt to the JADE by writing value 33h into INH interrupt status register at address 50h.
2. JADE writes the current status data into the mailbox, resets the INHB bit and generates an interrupt at INT# line to the host by writing a value 34h into IND interrupt status register at address 58h.
3. The host reads the status data from the mailbox using the procedure described in section 3.4 and may reset the INDB bit. The reset of the INDB bit is not mandatory and may be skipped. The host acknowledges the transfer by writing a value 35h into INH interrupt status register at address 50h and by that generating an interrupt to the JADE.
4. The JADE resets the INHB bit.

The structure of the control and status data blocks is identical. The host writes the control block to change the settings of the JADE AN and reads the status block to evaluate the current settings of the JADE AN.

The control/status block is organized in 8-bit words and has the following structure:

	(MSB)				(LSB)			
CTRL	PSEL	ISEL1	ISEL0	FLEN	0	0	0	1
UDF	0	0	0	UDF1	UDF0	0	1	0
G723C	<u>HP723</u>	<u>PF723</u>	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
MODE	EM3	EM2	EM1	EM0	DM3	DM2	DM1	DM0
OPT1	<u>I</u>	0	0	<u>P1</u>	<u>P0</u>	<u>L2</u>	<u>L1</u>	<u>L0</u>
OPT2	0	0	Re1	Re0	Rd1	Rd0	<u>e</u>	<u>d</u>
EVOL	<u>EV7</u>	<u>EV6</u>	<u>EV5</u>	<u>EV4</u>	<u>EV3</u>	<u>EV2</u>	<u>EV1</u>	<u>EV0</u>
DVOL	<u>DV7</u>	<u>DV6</u>	<u>DV5</u>	<u>DV4</u>	<u>DV3</u>	<u>DV2</u>	<u>DV1</u>	<u>DV0</u>

Underlined bits: Unless otherwise indicated, the host has to switch the MODE to neutral for at least four frames (default: 40 msec) before it can change the control block. Only the underlined bits may also be changed on the fly disregarding that rule. After Reset, the JADE AN is automatically in the neutral mode, so changes to the control block can be

Firmware Features

done immediately after the JADE AN has finished its initialization phase (see section 6.2.3).

Mailbox Address 00_H

Value after reset: C1_H

	(MSB)							(LSB)
CTRL	PSEL	ISEL1	ISEL0	FLEN	0	0	0	1

- PSEL

Protocol Select

0

Outband controlled protocol selected, see current section.

1

Inband controlled protocol selected, see section 6.2.1.3.

- ISEL(1-0)

Interface Select

00

Uncompressed audio: Host IF
Compressed data: Host IF

01

Uncompressed audio: IOM IF
Compressed data: Host IF

10

Uncompressed audio: IOM IF
Compressed data: Serial Audio IF

11

Reserved

- FLEN

Frame Length

0

10 msec frame length selected. The data packet size of compressed and uncompressed audio is determined by the frame length.

1

Reserved

Mailbox Address 01_H

Value after reset: 1A_H

	(MSB)							(LSB)
UDF	0	0	0	UDF1	UDF0	0	1	0

Firmware Features

UDF(1-0)	Uncompressed Data Format (independent of the selected audio compression).		
00	Reserved		
01	G.711 A-Law		
10	G.711 μ -Law		
11	16 bit uncompressed audio		

Mailbox Address 02_H

Value after reset: C0 _H		(MSB)		(LSB)			
G723C	<u>HP723</u>	<u>PF723</u>	0	0	0	0	0

HP723	G.723 High Pass Filter On/Off.		
0	High Pass Filter Off		
1	High Pass Filter On		
PF723	G.723 Postfilter On/Off.		
0	Postfilter Off		
1	Postfilter On		

Mailbox Address 03_H

Value after reset: 00 _H		(MSB)		(LSB)			
	0	0	0	0	0	0	0

Mailbox Address 04_H

Value after reset: 00 _H		(MSB)		(LSB)			
------------------------------------	--	-------	--	-------	--	--	--

Firmware Features

MODE	EM3	EM2	EM1	EM0	DM3	DM2	DM1	DM0
------	-----	-----	-----	-----	-----	-----	-----	-----

EM(3-0), DM(3-0)	Audio modes for encoder (EM(3-0)) and decoder (DM(3-0)).							
	0 _H	Neutral mode, no compressed audio data is exchanged						
	1 _H	Pass-through 8 KHz sampled data, not available when Host/Host is selected as interface combination for compressed/uncompressed data.						
	2 _H	G.711 8 KHz sample rate A-law encoding/decoding						
	3 _H	G.711 8 KHz sample rate μ -law encoding/decoding						
	4 _H	Reserved.						
	5 _H	Reserved.						
	6 _H	G.723 8 KHz sample rate MP-MLQ (6.3 kbps) or ACELP (5.3 kbps) coding						

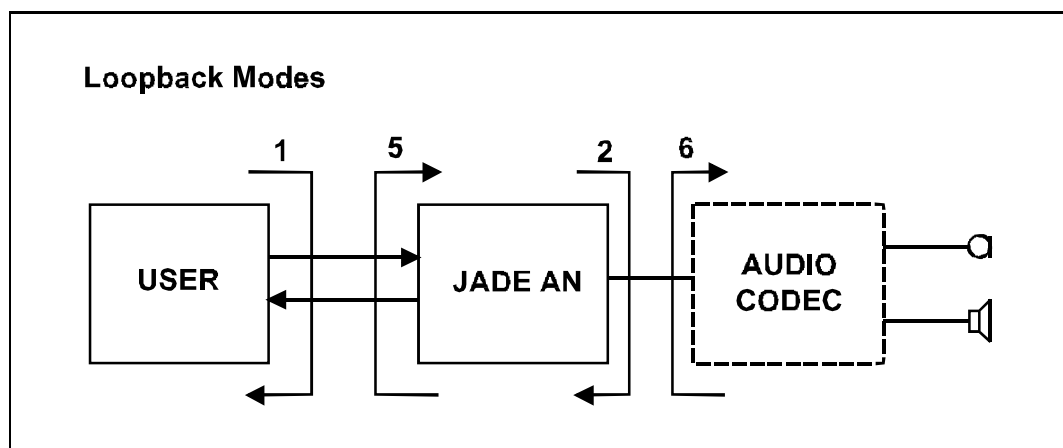
Mailbox Address 05_H

Value after reset: 00 _H								
	(MSB)					(LSB)		
OPT1	I	0	0	P1	P0	L2	L1	L0

I	Data is invalid. If I is set then the compressed data in this packet was missing or had errors. The data words in this packet are still sent to avoid buffer problems.							
	0	Data is valid						
	1	Data is invalid						

Firmware Features

- P(1-0)** Part number of the data in this packet. Allows the natural period of the data to be 10 to 40 msec. For G.723 takes on the values 0, 1 or 2 corresponding to the first, second or third part of a 30 msec data packet. Is always 0 for the other modes.
- Note:** To avoid the updating of these bits by the user in each frame when operating in G.723 mode, the JADE AN auto-increments the P-bits. Nevertheless, the user has to take care that G.723 encoder and decoder are running synchronously, i.e. the part number of the received and transmitted packet in one 10 msec frame must be identical for control and status. For that, after switching to G.723 mode the user has first to wait for valid packets (i.e. wait for $I=0$) and second to read the P(1-0) status bits to synchronize the data stream transmitted to the JADE AN correspondingly, i.e. if the user receives a status value of 2 from the JADE AN, it also has to transmit a part 2 packet in the current 10 msec frame.
- The P(1-0) control block bits sent by a user are ignored by the JADE AN when operating in G.723 mode. This is to avoid collisions between the host and the auto-increment mechanism in the JADE AN.
- 00 First part of compressed audio packet (G.723: part 1/3)
 - 01 Second part of compressed audio packet (G.723: part 2/3)
 - 10 Third part of compressed audio packet (G.723: part 3/3)
 - 11 Fourth part of compressed audio packet (G.723: reserved)
- L(2-0)** Loopback modes, used for testing the audio subsystem.



- 000 No loopback (default)
- 001 Send received compressed data back to the user as encode data
- 010 Encode the decoded user data

Firmware Features

- 011 Reserved
- 100 Reserved
- 101 Decode the encoded audio input data
- 110 Send the digital ADC output to the DAC input
- 111 Reserved

Mailbox Address 06_H

Value after reset: 00_H

(MSB)

(LSB)

OPT2	0	0	Re1	Re0	Rd1	Rd0	e	d
------	---	---	-----	-----	-----	-----	---	---

Re(1-0),
Rd(1-0)

When the encode mode is G.723 the Re bits give the desired encoding method:

- 00 high rate, don't use silence suppression
- 01 high rate, use silence suppression
- 10 low rate, don't use silence suppression
- 11 low rate, use silence suppression

Rd is the same as the above, but indicates the mode of the data in this packet. It is the same as the corresponding bits of the G.723 packet data.

e

Encoding mute enable. After switching, a ramping function is implemented to avoid audible clicks.

- 0 Encoding Mute disabled
- 1 Encoding Mute enabled

d

Decoding mute enable. After switching, a ramping function is implemented to avoid audible clicks.

- 0 Decoding Mute disabled
- 1 Decoding Mute enabled

Mailbox Address 07_H

Value after reset: 00_H

Firmware Features

	(MSB)							(LSB)
EVOL	<u>EV7</u>	<u>EV6</u>	<u>EV5</u>	<u>EV4</u>	<u>EV3</u>	<u>EV2</u>	<u>EV1</u>	<u>EV0</u>

EV(7-0) Encoder Volume.

00_H- Adjusts the gain on the analog input. Realized by multiplying the
FF_H encoder input samples with (EV(7-0)+1)/256, i.e. 00_H is the
minimum and FF_H the maximum volume.

Mailbox Address 08_H

Value after reset: 00_H

	(MSB)							(LSB)
DVOL	<u>DV7</u>	<u>DV6</u>	<u>DV5</u>	<u>DV4</u>	<u>DV3</u>	<u>DV2</u>	<u>DV1</u>	<u>DV0</u>

DV(7-0) Decoder Volume.

00_H- Adjusts the gain on the analog output. Realized by multiplying
FF_H the decoder output samples with (DV(7-0)+1)/256, i.e. 00_H is the
minimum and FF_H the maximum volume.

Control Pipeline

Like stated before, there is a delay of three times the frame length (default: 30 msec) between the transfer of a new control block from the host to the JADE AN and the new settings being reported in the status data (transferred from the JADE AN to the host) due to the internal buffering pipeline of the JADE AN.

The following table shows the pipeline behaviour switching from neutral to G.711 and vice versa.

Note: The encoder data is input through the uncompressed interface and output through the compressed interface. The decoder data is input through the compressed interface and output through the uncompressed interface. The "#Data Bytes" (see table below) transferred together with the control/status information refers only to the compressed interface!

Firmware Features

Control/Status pipeline for G.711 (identical for Pass-Through):

Packet# (10 msec)	Control (User to JADE AN)			Status (JADE AN to User)			Comment
	MODE	OPT1*	#Data Bytes	MODE	OPT1	#Data Bytes	
1.	00	00	0	00	00	0	Neutral status after Reset
2.	22	00	0	00	00	0	Command: G.711 A-law encode & decode
3.	22	00	80	00	00	0	First G.711 A-law encoded data to JADE AN
4.	22	00	80	00	00	0	
5.	22	00	80	22	00	80	First G.711 A-law en-/decoded data from JADE AN
6.	22	00	80	22	00	80	
7.	00	00	80	22	00	80	Command: Neutral Mode (at least 4 times), last G.711 data to JADE AN
8.	00	00	0	22	00	80	
9.	00	00	0	22	00	80	Last G.711 A-law en-/decoded data from JADE AN
10.	00	00	0	00	00	0	4th neutral packet, next can change mode
11.	33	05	0	00	00	0	Command: G.711 μ -law with Loop 5
12.	33	05	80	00	00	0	First (dummy) G.711 μ -law encoded data to JADE AN
13.	33	05	80	00	00	0	
14.	33	05	80	33	05	80	First G.711 μ -law en-/decoded data from JADE AN
15.	33	05	80	33	05	80	
16.	00	00	80	33	05	80	Command: Neutral Mode, last G.711 data to JADE AN
17.	00	00	0	33	05	80	
18.	00	00	0	33	05	80	Last G.711 μ -law en-/decoded data from JADE AN
19.	00	00	0	00	00	0	4th neutral packet, next can change mode
20.	02	00	0	00	00	0	Command: G.711 A-law decoder only

Firmware Features

Packet# (10 msec)	Control (User to JADE AN)			Status (JADE AN to User)			Comment
	MODE	OPT1*	#Data Bytes	MODE	OPT1	#Data Bytes	
21.	02	00	80	00	00	0	First G.711 A-law encoded data to JADE AN
22.	02	00	80	00	00	0	
23.	02	00	80	02	00	0	First G.711 A-law decoded data from JADE AN
24.	02	00	80	02	00	0	
25.	00	00	80	02	00	0	Command: Neutral Mode, last G.711 data to JADE AN
26.	00	00	0	02	00	0	
27.	00	00	0	02	00	0	Last G.711 A-law decoded data from JADE AN
28.	00	00	0	00	00	0	4th neutral packet, next can change mode

The pipelining is identical for the 8 KHz pass-through mode.

In G.723 the natural frame length of 30 msec is split up into three 10 msec packets to fit into the interface structure of the other audio modes. These packets are numbered by the P(1-0) bits (in OPT1 for outband control, OPTIONS for inband control) taking on the values 0, 1 or 2 for the first, second or third part of a 30 msec frame, respectively.

When entering G.723 mode the pipelining is similar to the above listing, but the first G.723 packets from the JADE AN will be invalid (indicate by MSB of OPT1). As mentioned above for synchronisation of input and output packets one has to wait for valid packets from the JADE.

When in G.723 mode, mode changes will be recognized by the JADE with the beginning of the first 10 msec packet. Thus, the control block for a mode change request should be transmitted to the JADE during the previous 3rd packet exchange. After an exit from G.723 encoder has been requested, the P(1-0) counter will no longer reflect the packet numbers even during the phase of draining the JADE internal pipeline. See the example below for details (high rate without voice activity detection used in this example, behaviour for the other modes is similar):

Firmware Features

Control/Status pipeline for G.723:

Packet# (10 msec)	Control (User to JADE AN)			Status (JADE AN to User)			Comment
	MODE	OPT1*	#Data Bytes	MODE	OPT1	#Data Bytes	
1.	00	00	0	00	00	0	Neutral status after Reset
2.	66	00	0	00	00	0	Command: G.723 high rate encode & decode
3.	66	00	8	00	00	0	First (dummy) G.723 encoded data to JADE AN for G.723 decoding
4.	66	00	8	00	00	0	
5.	66	90	8	66	90	8	First (invalid) G.723 en-/decoded data from JADE AN
6.	66	80	8	66	80	8	
7.	66	88	8	66	88	8	
8.	66	90	8	66	90	8	
9.	66	00	8	66	00	8	Part 0 of valid G.723 encoded frame to/from JADE AN
10.	66	08	8	66	08	8	Part 1 of 30 msec frame
11.	66	10	8	66	10	8	Part 2 of 30 msec frame
12.	66	00	8	66	00	8	Part 0 of 30 msec frame
13.	66	08	8	66	08	8	Part 1 of 30 msec frame
14.	00	10	8	66	10	8	Part 2 of 30 msec frame, Command: Neutral Mode, last G.723 data to JADE AN
15.	00	00	0	66	00	8	
16.	00	00	0	66	00	8	Last G.723 en-/decoded data from JADE AN
17.	00	00	0	00	00	0	4th neutral packet, next can change mode
18.	60	00	0	00	00	0	Command: G.723 high rate encode
19.	60	00	0	00	00	0	
20.	60	00	0	00	00	0	

Firmware Features

Packet# (10 msec)	Control (User to JADE AN)			Status (JADE AN to User)			Comment
	MODE	OPT1*	#Data Bytes	MODE	OPT1	#Data Bytes	
21.	60	00	0	60	90	8	First (invalid) G.723 encoded data from JADE AN
22.	60	00	0	60	80	8	
23.	60	00	0	60	88	8	
24.	60	00	0	60	90	8	
25.	60	00	0	60	00	8	Part 0 of valid G.723 encoded frame from JADE AN
26.	60	00	0	60	08	8	Part 1 of 30 msec frame
27.	60	00	0	60	10	8	Part 2 of 30 msec frame
28.	60	00	0	60	00	8	Part 0 of 30 msec frame
29.	60	00	0	60	08	8	Part 1 of 30 msec frame
30.	00	00	0	60	10	8	Part 2 of 30 msec frame, Command: Neutral Mode
31.	00	00	0	60	80	8	Invalid G.723 data from JADE AN internal pipeline
32.	00	00	0	60	00	8	Last G.723 encoded data from JADE AN
33.	00	00	0	00	00	0	4th neutral packet, next can change mode
34.	06	00	0	00	00	0	Command: G.723 high rate decode
35.	06	00	8	00	00	0	Part 0 of valid G.723 encoded frame to JADE AN
36.	06	08	8	00	00	0	Part 1 of 30 msec frame
37.	06	10	8	06	00	0	Part 2 of 30 msec frame, first G.723 decoded data from JADE AN
38.	06	00	8	06	00	0	Part 0 of 30 msec frame
39.	06	08	8	06	00	0	Part 1 of 30 msec frame
40.	00	10	8	06	00	0	Part 2 of 30 msec frame, Command: Neutral Mode, last G.723 data to JADE AN
41.	00	00	0	06	00	0	

Firmware Features

Packet# (10 msec)	Control (User to JADE AN)			Status (JADE AN to User)			Comment
	MODE	OPT1*	#Data Bytes	MODE	OPT1	#Data Bytes	
42.	00	00	0	06	00	0	Last G.723 decoded data from JADE AN
43.	00	00	0	00	00	0	4th neutral packet, next can change mode

*: P(1-0) bits are autoincremented in outband controlled mode. Thus, OPT1 does not need to be explicitly written for each 10 msec packet! If P(1-0) bits are written to the JADE which don't match the corresponding status bits, they will be ignored.

#Data Bytes means the number of compressed data bytes transmitted from the User to the JADE AN or from the JADE AN to the User, respectively. The uncompressed data is exchanged constantly with 80 samples in 10 msec (8 kHz).

6.2.1.2 Compressed Audio Protocol with Outband Control

To minimize the bandwidth on the compressed audio interface, an outband controlled protocol is implemented in the JADE AN. This means that the mode settings for the JADE AN are usually done before audio data exchange is started using the procedure described in section 6.2.1.1. During audio data transfer the JADE AN keeps its current mode settings and only compressed audio is exchanged.

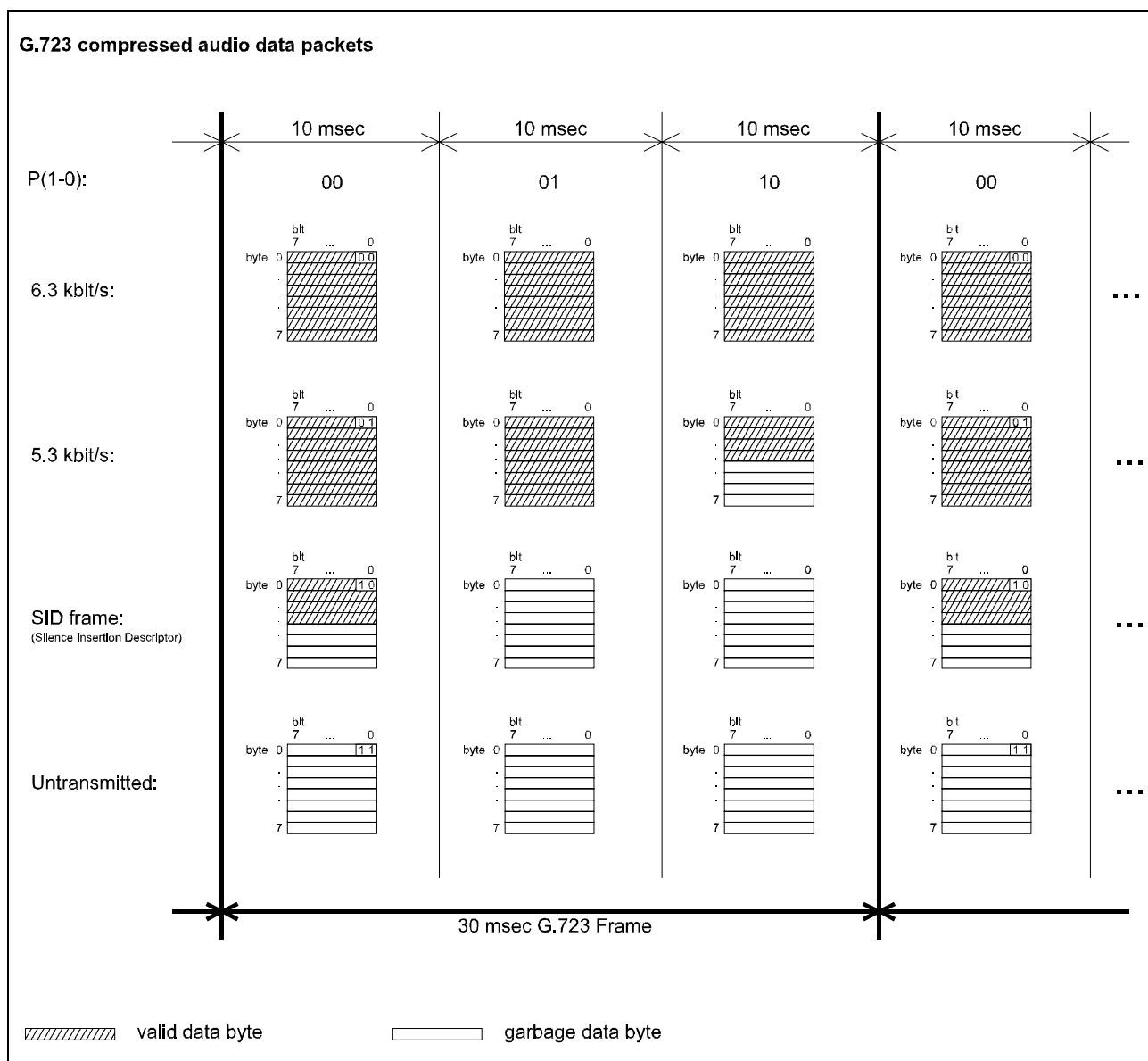
The size and format of the 10 msec compressed data packets is summarized in the table below for the various operating modes:

Compression Mode	Compressed data packet size in bytes	Valid bits per byte ¹⁾
Neutral	0	0
8 KHz pass-through *)	160	8
G.711	80	8
G.723, 6.3 kbit/s	8	8 ²⁾
G.723, 5.3 kbit/s	8	8/0 ²⁾
G.723, Silence Insertion Descriptor (SID) packets	8	8/0 ²⁾
G.723, untransmitted packets	8	0 ²⁾

Firmware Features

- 1) Always the most significant bits of a byte are valid and the least significant bits are ignored.
- 2) All different G.723 packets are transmitted with the same number of bytes which is determined by the 6.3 kbit/s mode. This is to make the protocol simple, not to minimize the data rate. Please refer to the drawing below for details.
- *) The 8 KHz pass-through mode is not available when Host/Host is selected as interface combination for compressed/uncompressed data.

In G.723 mode the natural frame size of 30 msec is split up into three 10 msec packets. To simplify the protocol handling all different G.723 modes are transmitted with the same data rate. Please refer to the following figure for sub-frame numbering with P(1-0) bits and valid bytes per packet in the corresponding G.723 packets:



Firmware Features

The two LSB's of the first byte inside a 30 msec frame determine the kind of frame that is currently being transmitted (see also figure above):

G.723 Mode	Supported in ITU-T C-Code Version:	Bit (1-0) of first Byte	Comment
G.723, 6.3 kbit/s	4.1, 5.0, 5.1	00	6.3 kbit/s Mode standard packet
G.723, 5.3 kbit/s	4.1, 5.0, 5.1	01	5.3 kbit/s Mode standard packet
G.723, Silence Insertion Descriptor (SID) packets	5.0, 5.1	10	Silence packet with filter coefficients, same for 6.3 and 5.3 kbit/s mode
G.723, untransmitted packets	5.0, 5.1	11	Silence packet without any data, same for 6.3 and 5.3 kbit/s mode

Note: Independently of the interface selection for the compressed audio, always the most significant bit of the most significant byte is transferred first, e.g. when using pass-through modes, the 16-bit samples are split up into two bytes and the most significant bit of the most significant byte is transferred first (big endian).

6.2.1.3 Compressed Audio Protocol with Inband Control

The following paragraph describes an H.221/H.223 oriented protocol which transfers the control information inband with the compressed audio data.

The user sends commands and data, and the provider sends status and data. Commands and data or status and data are grouped into blocks of 16-bit words.

Between the user and the JADE AN one data packet is transferred each way every 10 msec. The packet, that is transferred from the video processor to the JADE AN - called "command data" - consists of eight command words followed by the appropriate number of data words for the current speech algorithm:

Command Data Structure

Firmware Features

0	Command header word
1	Checksum of words 2-7
2	Set mode
3	Set options
4	Set volume
5-7	Reserved for future expansion
8+	Compressed data; 0, 4, 40 or 80 words (1 word = 16 bit)

The header of the command data packet describes the JADE AN operation modes in effect for data in the next packet. **See “Commands” section** below for a detailed description of the above command words.

The packet that is transferred from the JADE AN to the video processor - called “status data” - consists of eight status words followed by the appropriate number of data words for the current speech algorithm:

Status Data Structure

0	Status header word
1	Capabilities
2	Mode status
3	Options status
4	Volume status
5	Error conditions
6-7	Reserved for future expansion
8+	Compressed data; 0, 4, 40 or 80 words (1 word = 16 bit)

The compressed data is between 0 and 80 words long depending on which of the decoding/encoding modes is active (neutral, G.723, G.711 or 8 KHz samples pass-through). The most significant byte of a word is received/transmitted first.

The G.723 compressed data framing is identical with the outband controlled mode, see section 6.2.1.2 for details.

Firmware Features

A header bit can indicate that the current compressed data is invalid. This means that it is not decoded and instead the sound from a previous packet is repeated. By that a simple interpolation of the speech signal is achieved to avoid an audible click.

The size of the command and data packets is the following (header excluded):

Mode	Compressed Words (Bytes)
Neutral	0 (0)
G.723	4 (8)
G.711	40 (80)
8 KHz pass-through *)	80 (160)

*) The 8 KHz pass-through mode is not available when Host/Host is selected as interface combination for compressed/uncompressed data.

The communication between user and JADE AN starts in the neutral mode. To initiate transfer of speech data, the user sends a command data structure set to the desired compression mode(s) in a neutral size packet. The mode change affects the JADE's input pipeline stage in the next 10 msec period. This means that if the decode mode changes, the next packet from the user will change in size (corresponding to the new decode mode), while if the encode mode changes, the third packet from the JADE AN will be affected (packets from the JADE AN represent the output stage of the pipeline). As a general rule, any changes to the current operating mode or options (volume, mute, etc.) transferred to the JADE AN from the user take effect on the input captured on the next 10 msec boundary.

Note on "Mode Changes": To change compression modes, the user must first send four neutral mode command packets. The first neutral mode command will be in a full-size packet per the current operating mode, while the following neutral mode command packet does only contain the 8 words header. Four neutral packets are required to clear the JADE's pipeline. During that time the JADE AN will reorganize its memory (if required) and re-initialize internal variables.

When a mode change is requested by the user without sending four neutral packets before, the JADE AN may not work stable.

Commands:

Firmware Features

The following section defines the commands which are sent from the user to the JADE AN. Any changes in mode affects the input pipeline stage in the next 10 msec time slot.

1. Command header word:

0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	1
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

2. Checksum:

The sum of the six following words (regarded as signed 16 bit values) in the command header. If the checksum is wrong, no modes or options are changed, and an error status is sent back in the next status header.

3. Set Mode:

x	x	x	x	x	x	x	x	EM3	EM2	EM1	EM0	DM3	DM2	DM1	DM0
---	---	---	---	---	---	---	---	-----	-----	-----	-----	-----	-----	-----	-----

Audio modes for encoder (EM0:3) and decoder (DM0:3). The following modes are defined:

RESET	special full word definition of the command mode. Reset is defined as 0xFFFF and returns the JADE to its power on default state
0	Neutral mode, only command and status header information is exchanged
1	Pass-through 16-bit linear 8 KHz sampled data
2	G.711 8 KHz sample rate A-law encoding/decoding
3	G.711 8 KHz sample rate μ -law encoding/decoding
6	G.723 8 KHz sample rate MP-MLQ (6.3 kbps) or ACELP (5.3 kbps) coding

4. Set Options:

I	x	x	P1	P0	L2	L1	L0	x	x	Re1	Re0	Rd1	Rd0	e	d
---	---	---	----	----	----	----	----	---	---	-----	-----	-----	-----	---	---

d decoding mute enable (1) and disable (0). After switching, a ramping function is implemented to avoid audible clicks

e encoding mute enable (1) and disable (0). After switching, a ramping function is implemented to avoid audible clicks

Re(1-0), When the encode mode is G.723 the Re bits give the desired encoding
Rd(1-0) method:

- 00 high rate, don't use silence suppression
- 01 high rate, use silence suppression
- 10 low rate, don't use silence suppression
- 11 low rate, use silence suppression

Rd is the same as the above, but indicates the mode of the data in this packet. It is the same as the corresponding bits of the G.723 packet data.

L(2-0) Loopback modes, used for testing the audio subsystem. The following loops are implemented:

- 000 No loopback (default)
- 001 Send received compressed data back to the user as encode data
- 010 Encode the decoded user data
- 011 Reserved
- 100 Reserved
- 101 Decode the encoded audio input data
- 110 Send the digital ADC output to the DAC input
- 111 Reserved

Firmware Features

P(1-0) Part number of the data in this packet. Allows the natural period of the data to be 10 to 40 msec. For G.723 takes on the values 0, 1 or 2 corresponding to the first, second or third part of a 30 msec data packet. Is always 0 for the other modes.

Note: When in G.723 mode, the user has to take care that G.723 encoder and decoder are running synchronously, i.e. the part number of the received and transmitted packet in one 10 msec frame must be identical for control and status.

I Data is invalid. If I is set then the compressed data in this packet was missing or had errors. The data words in this packet are still sent to avoid buffer problems.

5. Set Volume

EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----

Adjusts the gain on the analog input and output. Realized by multiplying the encoder samples with $(EV(7-0)+1)/256$ and the decoder samples with $(DV(7-0)+1)/256$, i.e. for maximum volume, the samples are not affected and for minimum volume they are divided by 256.

Status:

The following section defines the status information that is sent from the JADE AN to the user. The status packet contains information about the current output pipeline stage, i.e. the modes used to generate the data in the status packet itself.

1. Status header word:

0	1	0	0	1	0	0	0	0	0	0	0	1	1	1	1
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Firmware Features

2. Capabilities:

C	S	0	0	0	0	0	0	0	0	M	0	0	μ	A	P
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

- P

Pass-through mode available (1) or not (0)
- A

G.711 - 8 KHz sample rate A-law coding available
- μ

G.711 - 8 KHz sample rate μ-law coding available
- M

G.723 - 8 KHz sample rate MP-MLQ (6.3 kbps) or ACELP (5.3 kbps) coding available
- S

Symmetry required.
The JADE AN reports a 1 indicating the standards used for encoding must be the same as for decoding. Asymmetry is allowed for neutral mode mixed with any other mode and mixed G.711 A-/μ-law, i.e. A-law encoder and μ-law decoder or vice versa.
- C

Codec connected to the JADE AN (1) or not (0). Default is 1.

3. Mode Status:

x	x	x	x	x	x	x	x	EM3	EM2	EM1	EM0	DM3	DM2	DM1	DM0
---	---	---	---	---	---	---	---	-----	-----	-----	-----	-----	-----	-----	-----

Report the audio mode or operation as defined in the command mode word above for the data that is in this packet.

4. Options Status:

I	x	x	P1	P0	L2	L1	L0	x	x	Re1	Re0	Rd1	Rd0	e	d
---	---	---	----	----	----	----	----	---	---	-----	-----	-----	-----	---	---

Firmware Features

Report the audio mode or operation per the bits as defined in the command options word above for the data in this packet.

5. Volume Status:

EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----

Report the gain on the analog input and output. Defined as in the command volume word above, i.e. 0 is the minimum volume, and 255 is the maximum.

6. Error Conditions:

E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
-----	-----	-----	-----	-----	-----	----	----	----	----	----	----	----	----	----	----

Set in response to an error, either in the command sequence or an internal error. All zero indicates no error.

Bit	Error Condition
0	Invalid checksum
1	Invalid audio mode
2	Invalid loopback mode
3	Hardware error
4	Packet timing error
5	IOM-Host Mode (section 6.2.3.2): interrupt service from host has been delayed by more than 160 msec

6.2.2 Uncompressed Data Protocol

The uncompressed data protocol is quite simple. The default configuration is 8 KHz sampling rate and 16-bit linear data. The data format can be selected to be either 16-bit linear or 8-bit PCM (G.711 A-/μ-law). For a 10 msec framing the size of the uncompressed data (in bytes) is listed in the table below:

	16-bit linear	G.711 A-/μ-law
8 KHz sampling rate	160	80

Note: Independently of the interface selection for the uncompressed audio, always the most significant bit of the most significant byte is transferred first, e.g. 16-bit linear samples are split up into two bytes and the most significant bit of the most significant byte is transferred first (big endian).

6.2.3 Audio Interface Timings

In this chapter the timings and/or interrupt handshake procedures are described for the different hardware interface selections (Host/Host, IOM/Host, IOM/Serial Audio Interface).

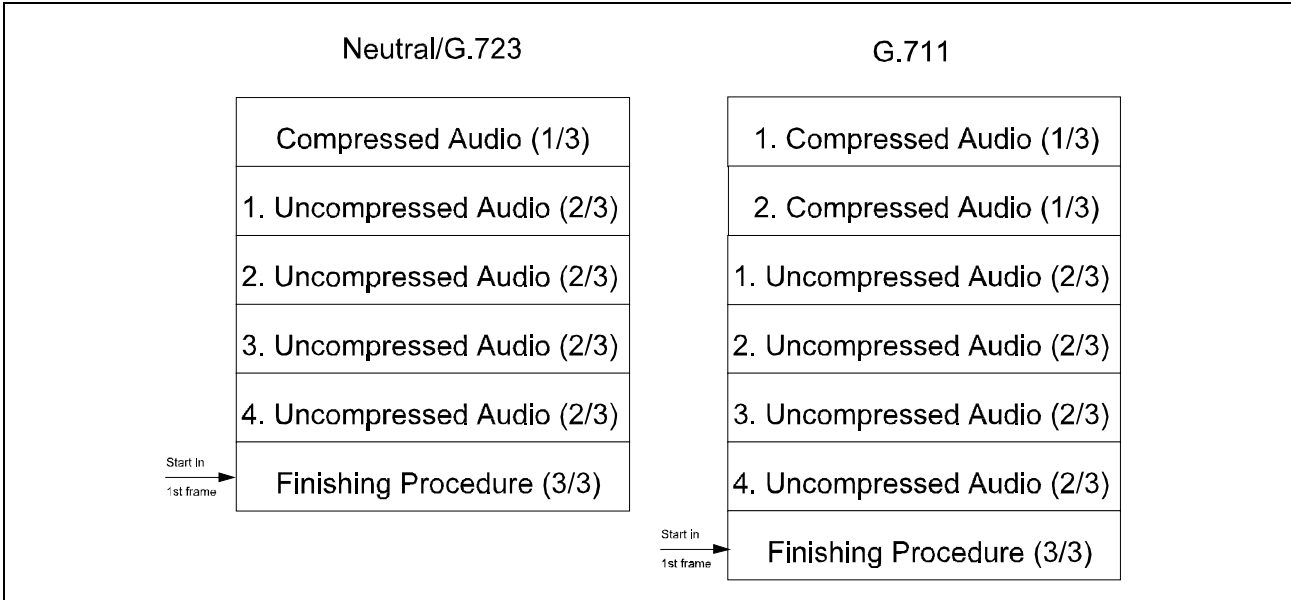
After a hardware reset the firmware automatically does all necessary initializations for the IOM/Serial Audio Interface combination described in section 6.2.3.3. The other interface combinations can be configured by configuring the control block (see section 6.2.1.1).

Note: After a hardware reset, the JADE AN firmware needs to initialize its internal memories and interfaces. The time to do this is less than 10 msec. The user must take care to access the JADE AN only after this initialization phase is completed, i.e. 10 msec after the hardware reset.

6.2.3.1 Uncompressed Data: Host IF
 Compressed Data: Host IF

This interface combination is used for offline processing of audio (ISEL(1-0)=00). I.e. the compression can be done faster than realtime, because the JADE AN is in each mode able to process audio *at least* in realtime. This definitely also depends on the capabilities of the host processor to provide a fast interrupt service to the handshake procedure described below. The most complex algorithm is G.723, in this mode the maximum possible speed is only slightly faster than realtime, because almost all of the computational power of the JADE AN is needed to compress the audio. The 8 KHz pass-through mode is not available with this interface combination.

The basic structure of data exchange between the Host and the JADE AN is shown in the following figure:



The picture shows the sequence of basic handshake procedures for one 10 msec frame. Basically, in both cases there are three blocks: The compressed audio exchange (basic procedure 1/3), the uncompressed audio exchange (basic procedure 2/3) and the finishing procedure (basic procedure 3/3).

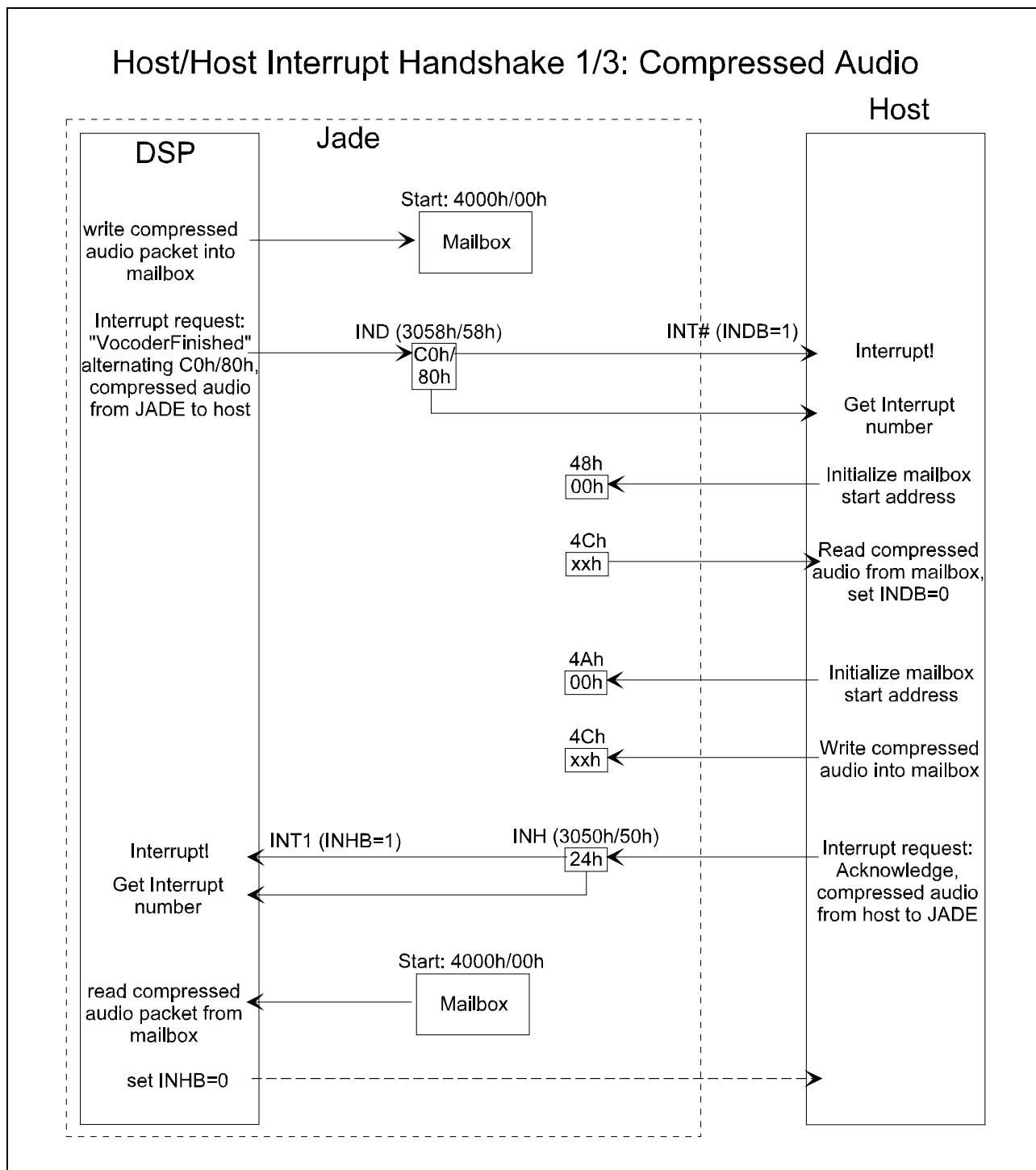
The compressed audio exchange (1/3) is executed only once (G.723) or twice (G.711) in a 10 msec frame. In the G.711 mode the mailbox cannot transfer the full data packet (80 or 96 bytes, depends on whether outband or inband control is selected) at once. Only for this mode the interrupt handshake procedure (1/3) is executed twice in one time frame. With the first run 64 bytes are transmitted in each direction, with the second run 16 bytes (outband control) or 32 bytes (inband control) are transmitted.

With the uncompressed audio handshake (2/3), 2.5 msec of uncompressed data are exchanged (20 samples at 8 KHz). This results in a four times repetition of this block to collect 10 msec of uncompressed data for the next frame.

Finally, a finishing handshake (3/3) is executed, which acknowledges the audio data exchange, offers the possibility to the host to request for other interrupt services and starts the next frame.

Note: The first time frame after the Host/Host interface has been setup starts with the last part of the finishing handshake procedure (3/3), see figure and table below.

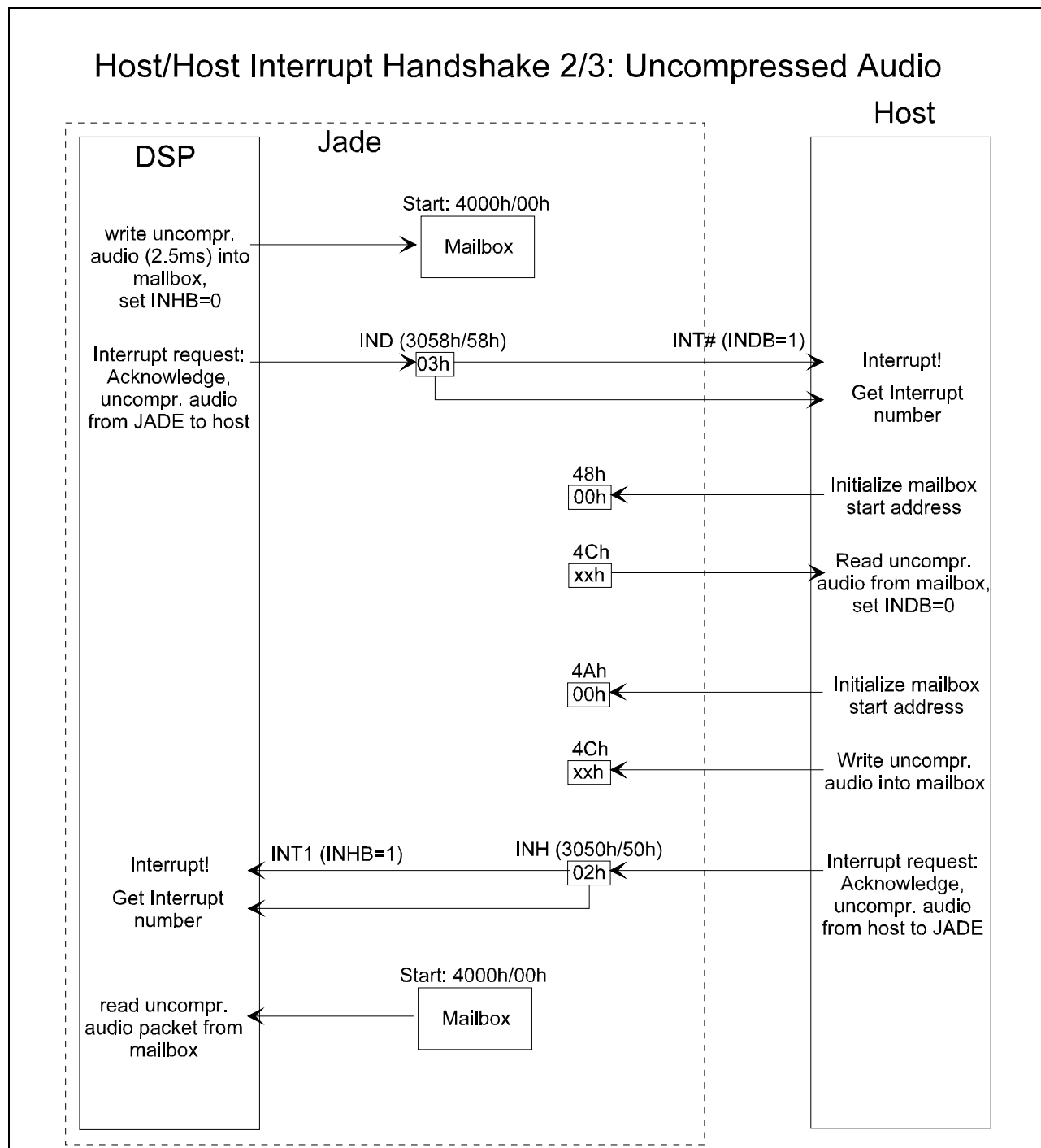
For the handshake procedure of the compressed audio see figure below:



This procedure is (nearly) identical with the interrupt handshake when in IOM/Host mode (see section 6.2.3.2) and the following steps are performed:

1. The JADE writes one frame of encoded audio data into the mailbox (most significant byte first).
2. The JADE generates a "VocoderFinished" interrupt at INT# line to the host by writing a value C0h or 80h (toggling) into IND interrupt status register at address 58h. The value of this interrupt is each time toggling between C0h and 80h to ensure that a polling host can consider a new "VocoderFinished". For an interrupt driven host one should just connect both numbers to the same interrupt service routine.
3. The host reads the compressed audio frame from the mailbox using the procedure described in section 3.4 and may reset the INDB bit. The reset of the INDB bit is not mandatory and may be skipped.
4. The host writes the compressed audio frame for the decoder into the mailbox using the procedure described in section 3.4.
5. The host generates an interrupt to the JADE by writing value 24h into INH interrupt status register at address 50h.
6. The JADE reads the compressed audio data from the mailbox and acknowledges the reception by resetting the INHB bit.

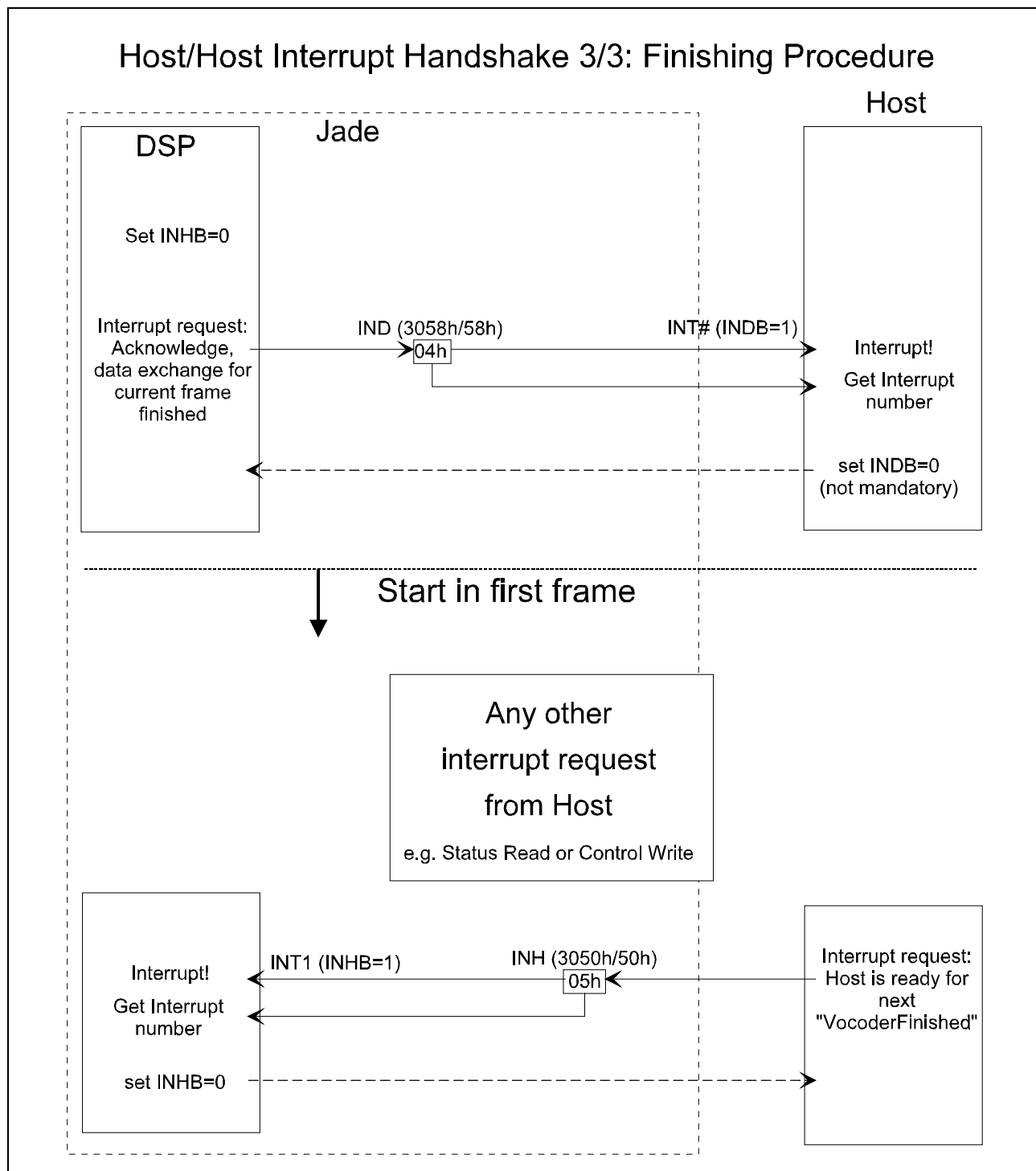
In the following, four 2.5 msec packets of uncompressed audio data are exchanged. See figure below for the handshake procedure:



The following steps are executed:

1. The JADE writes a packet of uncompressed audio (2.5 msec) into the mailbox (most significant byte first).
2. The JADE generates an interrupt at INT# line to the host by writing a value 03h into IND interrupt status register at address 58h.
This interrupt acknowledges the previous INH interrupt (either from the compressed data transfer or from the last uncompressed data transfer) and requests the current uncompressed data exchange.
3. The host reads the uncompressed audio from the mailbox using the procedure described in section 3.4 and may reset the INDB bit. The reset of the INDB bit is not mandatory and may be skipped.
4. The host writes a packet of uncompressed audio (2.5 msec) into the mailbox using the procedure described in section 3.4.
5. The host generates an interrupt of the JADE by writing value 02h into INH interrupt status register at address 50h.
6. The JADE reads the uncompressed audio data from the mailbox.

After the above procedure has been repeated four times, the finishing procedure is executed (see figure below):



The following steps are executed:

1. The JADE generates an interrupt at INT# line to the host by writing a value 04h into INH interrupt status register at address 50h.
2. The host may reset the INDB as a reaction to the JADE interrupt. This step is not mandatory and may be skipped.
3. **Start point in first frame**
At this point, the host can request other interrupts, like Read Status or Write Control Block (see section 6.2.1.1).
The number of interrupts and the time to execute them is not limited by the JADE, but dedicated by the host itself. The host may request interrupts as long as it has not executed the next step of this table.
4. The host generates an interrupt to the JADE by writing value 05h into INH interrupt status register at address 50h.
By that, the host indicates that it is ready to exchange the next frame of data.
5. The JADE resets the INHB bit.

With this procedure the handling of one frame of data is finished and the next frame is started beginning with the exchange of the compressed audio (procedure 1/3).

When starting the above protocol, it begins at the point marked with "Start in first frame". This is to enable the host to have control of the real start time, so the host first has to generate a "Host Ready" interrupt (INH=05h) before the host will start with the exchange of the compressed audio (procedure 1/3). After that, the Host/Host handshake procedure is executed cyclically.

6.2.3.2 **Uncompressed Data: IOM IF** **Compressed Data: Host IF**

The JADE AN can provide the uncompressed audio via the IOM interface while exchanging the compressed audio through the host interface (ISEL(1-0)=01).

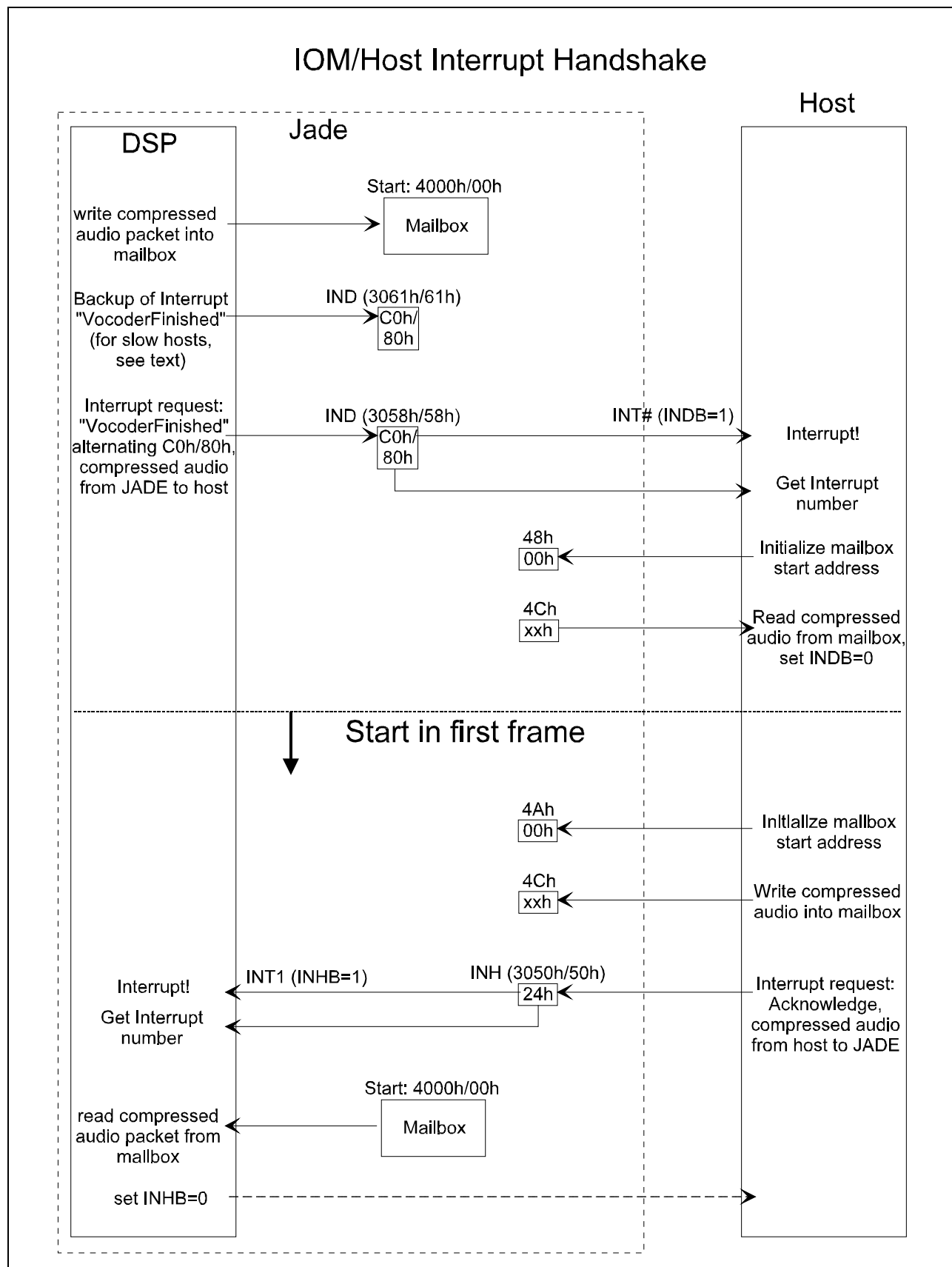
After switching to IOM/Host interface combination by programming the ISEL(1-0) bits in the control block, an initialization phase is executed by the JADE AN in which the internal firmware re-programs the configuration/control registers like in the default configuration (see section 5.3) to setup the IOM interface for the communication with the analog front end (AFE). This initialization phase is < 10 msec.

Firmware Features

The IOM Interface is in TE mode (double DCL clock) and IC1/2 channels are selected for the 16 bit linear data transfer between the JADE AN and the analog front end (AFE). The DD line is output of the JADE AN, DU is input to the JADE AN.

This configuration may be changed by the host by just overwriting the corresponding registers after the default initialization has been completed.

An interrupt handshake protocol is implemented for the data exchange on the host interface. The basic timing for this protocol is determined by the uncompressed data rate at the IOM interface. See figure below for the interrupt handshake procedure:



The following steps are performed:

1. The JADE writes one frame of encoded audio data into the mailbox (most significant byte first).
2. The JADE writes a backup of the "VocoderFinished" interrupt number performed in the next step into the host accessible register 61h. This is only used for detection of a missed interrupt when a slow host is connected, see text below.
3. The JADE generates a "VocoderFinished" interrupt at INT# line to the host by writing a value C0h or 80h (toggling) into IND interrupt status register at address 58h. The value of this interrupt is each time toggling between C0h and 80h to ensure that a polling host can consider a new "VocoderFinished". For an interrupt driven host one should just connect both numbers to the same interrupt service routine.
4. The host reads the compressed audio frame from the mailbox using the procedure described in section 3.4 and may reset the INDB bit. The reset of the INDB bit is not mandatory and may be skipped.
5. **Start point in first frame**
The host writes the compressed audio frame for the decoder into the mailbox using the procedure described in section 3.4.
6. The host generates an interrupt to the JADE by writing value 24h into INH interrupt status register at address 50h.
7. The JADE reads the compressed audio data from the mailbox and acknowledges the reception by resetting the INHB bit.^{1), 2)}

¹⁾ To keep the interrupt load for the host as small as possible, the JADE AN does not generate an acknowledge interrupt. It is guaranteed, that the INH interrupt 24h is serviced within a time of 125 μ sec, so if the host sends the interrupt 24h soon enough, it is guaranteed, that the interrupt handshake procedure is completed before the next "VocoderFinished" from the JADE AN appears. So, in this case the host does not need to check the status of INHB.

²⁾ If the host wants to apply other actions, e.g. reading or writing of the control/status block, it has to wait for the INHB bit to be reset to 0. All these additional actions should be completed within the current time frame (default: within 10 msec after the

Firmware Features

"VocoderFinished" interrupt). Otherwise special situations in the interrupt sequence have to be considered by the host, see text below.

When starting the above procedure, it begins at the point marked with "Start in first frame". This is to enable the host to have control of the real start time, so the host first has to deliver compressed data to the JADE AN and generate the corresponding interrupt. After that, the IOM/Host handshake procedure is executed cyclically.

The JADE AN starts the above interrupt procedure once every frame (default: 10 msec) for G.723 compression mode, twice for G.711 compression mode and three times for the 8 KHz pass-through mode.

In the G.711 and 8 KHz pass-through mode the mailbox cannot transfer the full data for 10 msec at once. Thus, sub-packets are build and the above interrupt handshake procedure is repeated for each sub-packet. See the following table for the number of sub-packets per 10 msec frame and the size of the packets:

Compression	Control	Number of Packets per 10 msec frame	Packet size (bytes)
8 KHz pass-through	inband	3	64-64-48
8 KHz pass-through	outband	3	64-64-32
G.711	inband	2	64-32
G.711	outband	2	64-16
G.723	inband	1	24
G.723	outband	1	8

Note: Some special situations have to be considered if one uses a slow host that cannot always ensure to finish the whole interrupt handshake in one frame period (default 10 msec), i.e. before the next VocoderFinished interrupt is generated by the JADE AN. Collisions between not finished interrupts and the new VocoderFinished Interrupt may occur.

Interrupt conflicts with a slow host

In the following some special situations and the recommended handling are described to keep the host protocol stable also in situations where the host has not finished its interrupt requests before the beginning of the next time frame, as long as the interrupt service delay is less than 160 msec.

Firmware Features

The following descriptions apply for the G.723 encoder/decoder mode. In G.711 or 8 KHz pass-through mode, the host must ensure that all interrupts are finished before the next "VocoderFinished" is generated by the JADE AN. This is because of the special double-/triple-"VocoderFinished" protocol, see text above.

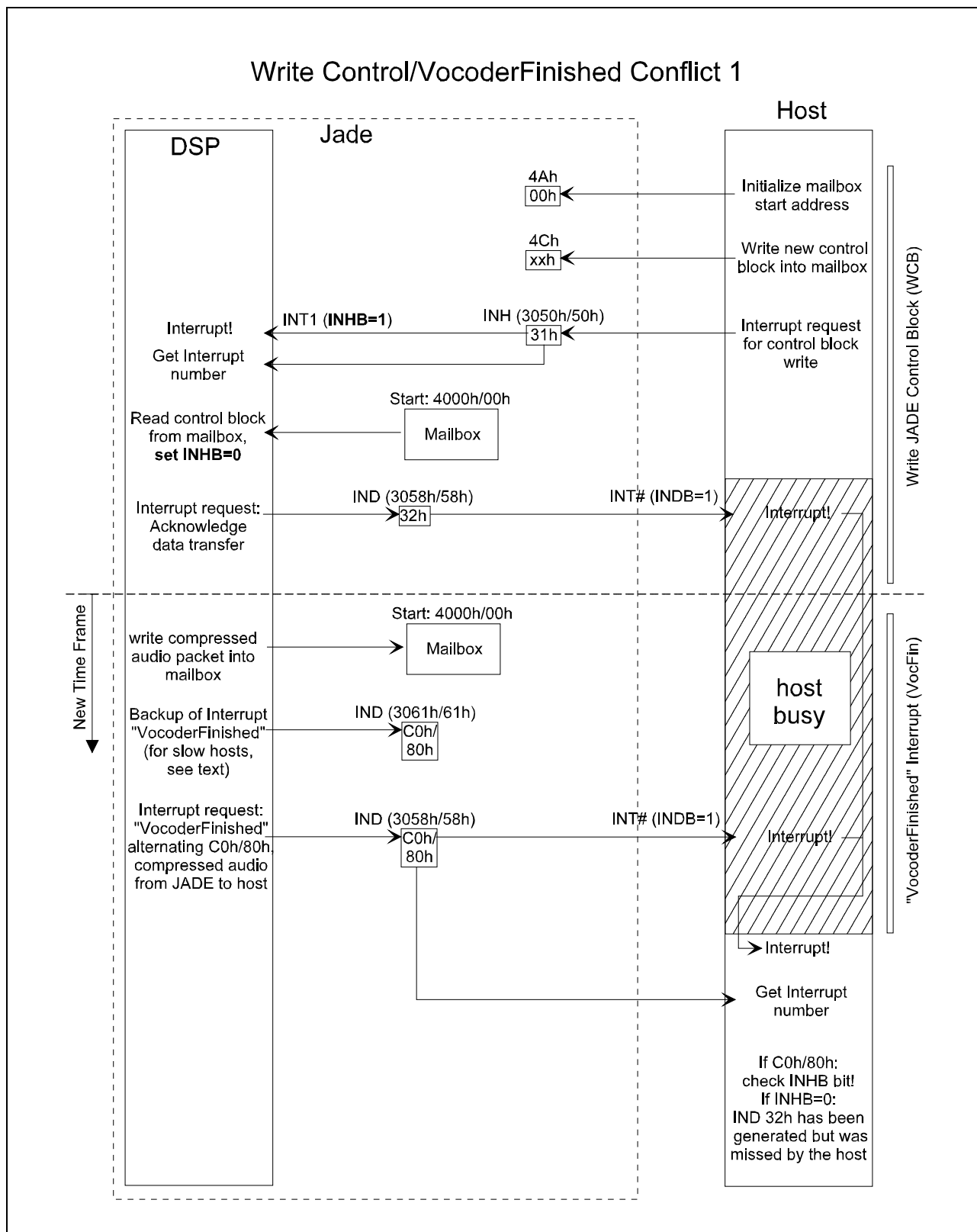
If the interrupt service from the host is delayed by up to 160 msec, none of the Interrupts during this time (usually only one "VocoderFinished" every 10 msec) is lost, but they are delayed, too, until the host is able to service them. Thus, after a gap in interrupt service a burst of interrupts has to be serviced by the host.

Note on "G.723 packet numbering P(1-0) during delayed interrupt service": During the interrupt burst to catch up for the delayed host interrupt service, the number of interrupts ensures proper synchronisation after the burst, but the data and packet numbering during the burst will be garbage. Thus, the synchronisation of encoder and decoder packets should only be done during non-delayed interrupt service.

The interrupts "Write JADE Control Block" and "Read JADE Status" are representative for all kinds of interrupts initiated by the host, so they are used in the following as an example for the corresponding type of interrupt.

1. "Write JADE Control Block" conflict with "VocoderFinished", Case 1

A critical situation for the host may occur when a "Write JADE Control Block" (WCB) interrupt handshake is done immediately before the next time frame starting with the new "VocoderFinished" (VocFin) interrupt begins. See figure below:



In this case, the WCB interrupt handshake is finished correctly, but the acknowledge interrupt IND 32h may be missed by the host if it is busy at that time, because the next

Firmware Features

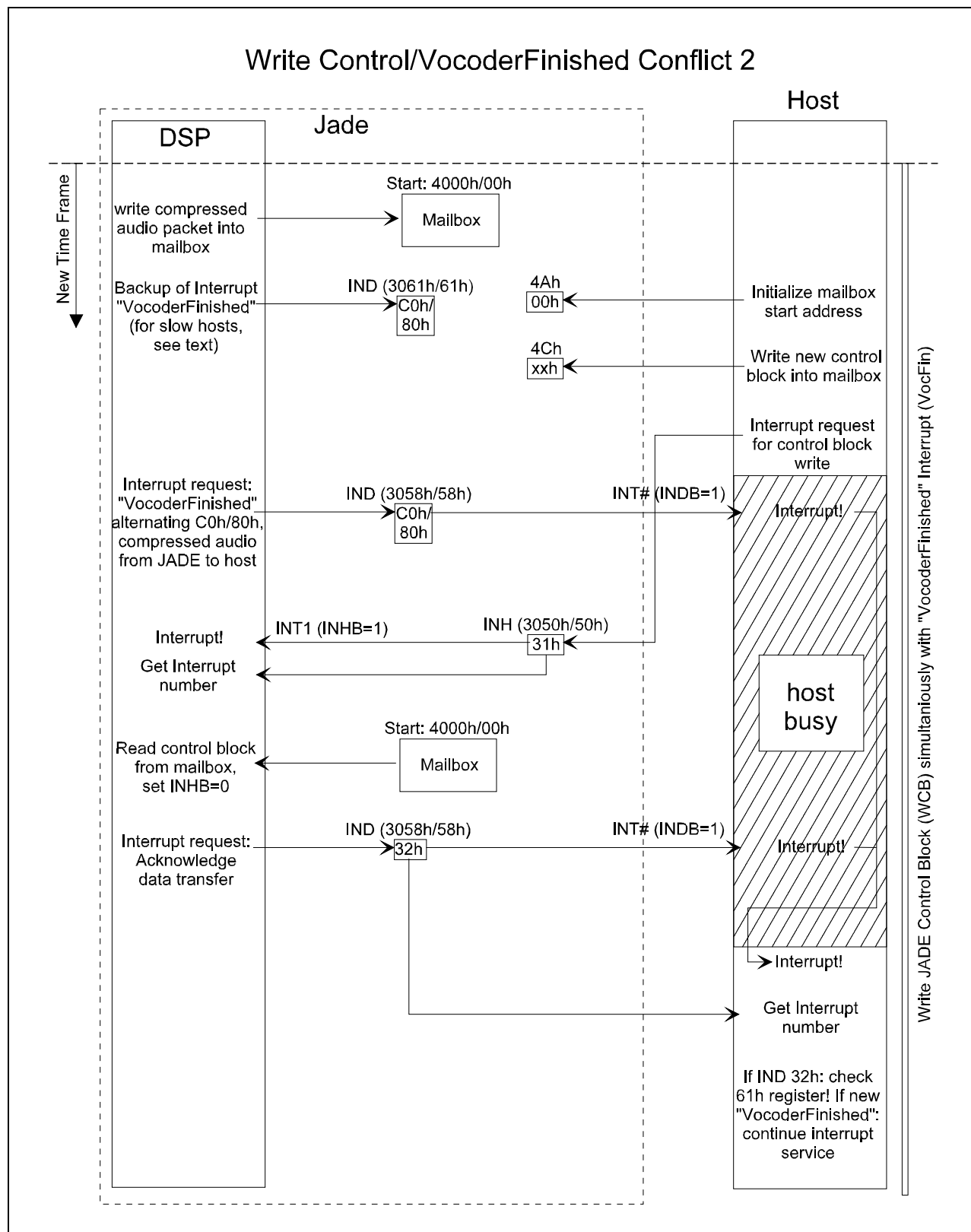
VocFin may be generated by the JADE AN before the host is able to recognize the IND 32h interrupt. The IND interrupt status register then is overwritten by the VocFin interrupt. If the host was busy during the time these two interrupts occurred, it will afterwards only detect the VocFin interrupt and miss the acknowledge of the WCB.

To handle this situation, the host should have an internal status register indicating an outstanding acknowledge interrupt. In case a VocFin is detected and an acknowledge interrupt is outstanding, the host has to check the INHB bit. As shown in the figure above, the INHB bit is reset in the WCB acknowledge procedure (see bold text). If the host detects INHB=0, the WCB interrupt has been acknowledged, but the host has missed the IND 32h interrupt. If the host detects INHB=1, the WCB interrupt has not yet been serviced and will be serviced later. For this case see also the conflict situation below.

2. "Write JADE Control Block" conflict with "VocoderFinished", Case 2

Another critical situation for the host may occur when a "Write JADE Control Block" (WCB) interrupt handshake is started in parallel with the new VocoderFinished interrupt of the new time frame.

See figure below:



In this case, the host generates the WCB interrupt before it has recognized the VocFin from the JADE AN and the JADE AN generates the VocFin before it has recognized the WCB from the host.

Immediately after the reception of WCB request the JADE AN will service that interrupt and send the corresponding acknowledge interrupt IND 32h. The VocFin interrupt status in the IND register is overwritten by that. If the host was busy between VocFin and the acknowledge of WCB, it will only receive one interrupt and recognize the later one, which is the IND 32h. To recognize, that it has missed one VocFin interrupt, the host should check the "VocoderFinished" backup register 61h. If the value of this register has toggled, it knows that there has been a VocFin before the IND 32h interrupt and must continue to service it.

Note: A parallel read/write access of the 3061/61 register is not prohibited by hardware. Thus an invalid value maybe read by the host when it reads the register at the same time as the JADE AN writes it. As a consequence, the host has to implement a double last look regarding this register, i.e. it has to read the contents until it has read the same value in two consecutive read-accesses, only then it is ensured that the value is valid.

3. "Read JADE Status" conflict with "VocoderFinished", Case 1

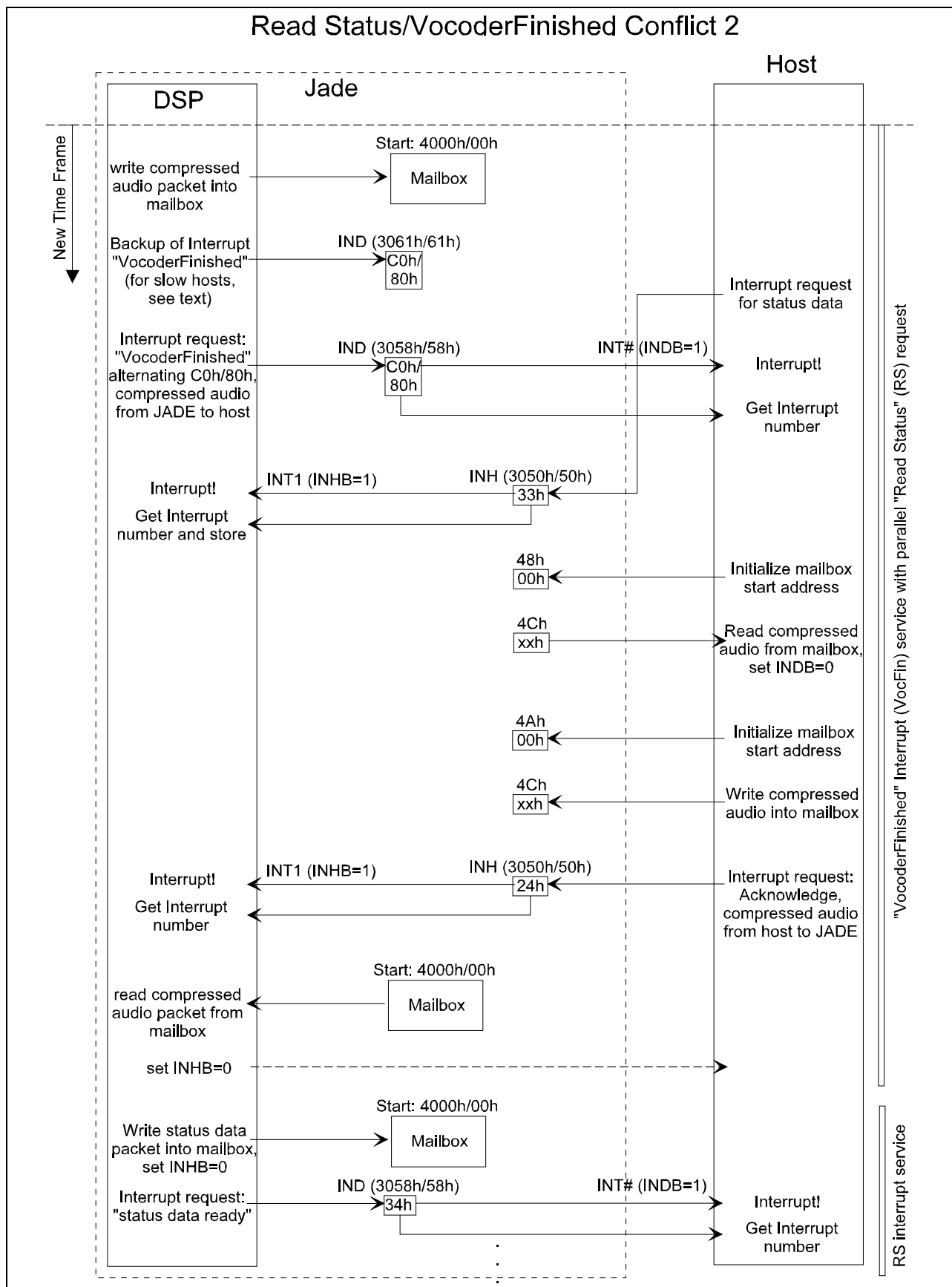
If a "Read JADE Status" (RS) interrupt handshake is initiated by the host immediately before the next time frame starts and is not completed at the time the new VocFin interrupt should occur, the VocFin is delayed until the RS is finished.

Due to audio delay reasons, the JADE AN has small internal buffers for the compressed data. This leads to an overwriting of audio data very soon after a VocFin is delayed.

It is ensured that the JADE AN is working stable in these situations (except for the G.711 and 8 KHz pass-through modes, in which two/three VocFin handshakes have to be done in each time frame, see above), nevertheless, a graceful degradation of speech quality has to be accepted by the user which is about proportional to the real delay time of the VocFin interrupt (the smaller the delay due to the busy host, the smaller the degradation of quality).

4. "Read JADE Status" conflict with "VocoderFinished", Case 2

A "Read JADE Status" (RS) request from the host coming in parallel with the VocFin of the new time frame will cause the following interrupt flow:

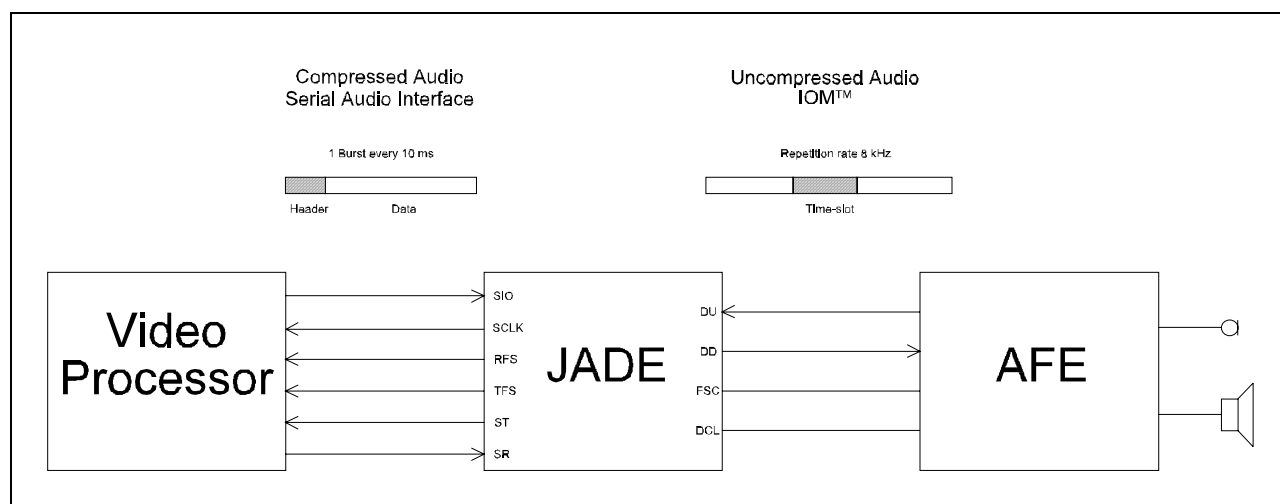


Firmware Features

The SR request will be recognized by the JADE AN, but not immediately be serviced. It is stored in an internal interrupt buffer and the VocFin is handled first as the higher priority interrupt. So, the host must not wait for the SR request to be serviced, but has to be able to recognize a VocFin interrupt from the JADE AN after an SR request. The VocFin interrupt then is serviced as usual and only after the corresponding handshake mechanism is finished, the SR request is serviced by the JADE AN.

6.2.3.3 Uncompressed Data: IOM IF Compressed Data: Serial Audio Interface (SAI)

This is the default mode of the JADE AN (ISEL(1-0)=10). The complete setup of the interfaces, timeslots and so on is done by the on-chip firmware after Reset, so that a standalone application with a video processor using the IOM-SAI interface combination can be realized without the need of an additional host.



The on-chip firmware uses the data controller for the transfer of the compressed audio data over the serial audio interface. During the initialization phase after a reset, the internal firmware programs the configuration/control registers (see section 5.3) and the data controller (see section 5.4). This results in a serial clock rate of 1.01 MHz continuously generated by the JADE AN, a 16 bit time-slot length and MSB sent/received first. The frame sync signals RFS and TFS are generated by the JADE AN non-continuously, i.e. during one frame only the exact number of frame syncs needed for the transfer of the current packet of data is generated in one burst.

The IOM Interface is in TE mode (double DCL clock) and IC1/2 channels are selected for the 16 bit linear data transfer between the JADE AN and the analog front end (AFE). The DD line is output of the JADE AN, DU is input to the JADE AN.

Firmware Features

This configuration may be changed by the host by just overwriting the corresponding registers.

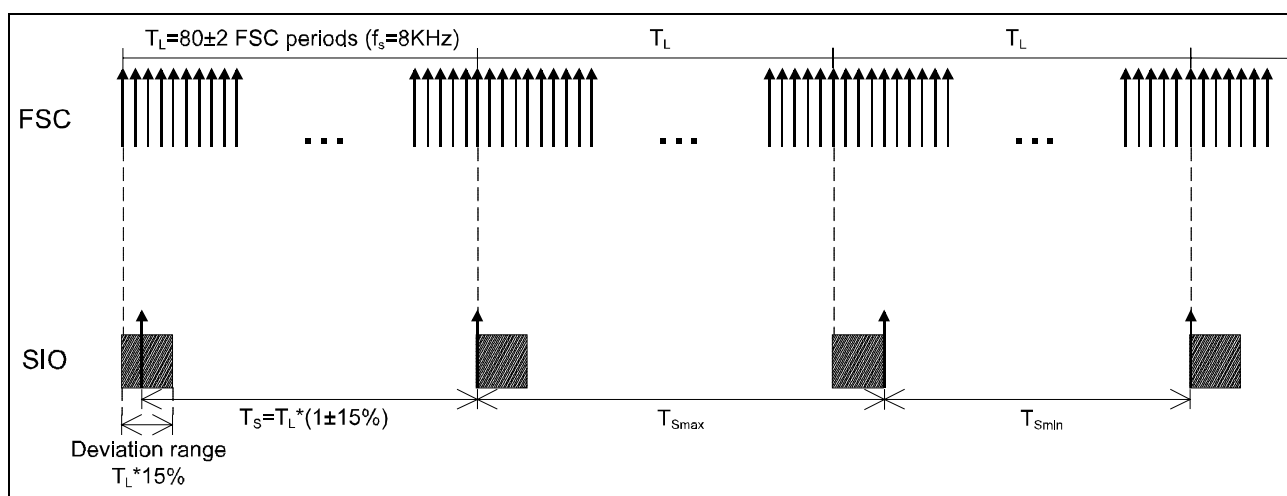
The timing of the JADE AN firmware is controlled by the video processor, which generates an interrupt every 10 msec at the SIO line. The JADE AN then starts generating a number of frame sync signals at RFS and TFS, depending on the length of the data packet that has to be exchanged. The RFS and TFS bursts are asynchronously, i.e. the RFS burst starts about 16 frame syncs before the TFS. After data packet transfer the JADE AN waits for the next SIO interrupt.

Note: During startup procedure the uncompressed interface (IOM) must be setup before the Serial Audio Interface is started, i.e. the FSC and DCL signals must be stable before the first 10 msec interrupt is generated by the video processor.

Due to small differences in the clock of the video processor and the audio output, the JADE AN is able to add or drop two uncompressed audio samples every 10 msec. That means, a skew of 2.5% ($f_s=8\text{kHz}$) between the communication board's clock and the audio codec's clock is acceptable to the JADE AN and should be aurally imperceptible. In the following this will be called the long term skew.

In addition to the long term skew, the JADE AN can correct for short term variances using an internal buffer mechanism. This allows single SIO periods to vary by $\pm 15\%$.

Please refer to the following figure:



The full definition is as follows:

Long term SIO period T_L :

$$T_L = 10ms \pm 0.25ms$$

Short term SIO period T_S :

$$T_S = T_L \cdot (1 \pm 15\%) \\ \approx 10ms \pm 1.5ms$$

Duration of n consecutive SIO periods:

The basic clock for the definition of [ms] is the frame sync signal (FSC) of the uncompressed audio interface.

Note: For maximum audio quality it is recommended to keep the skew between the IOM-2 and the SIO time base as small as possible, i.e. to adjust T_L in the above definition as close to 10 msec as possible. In an application with the VCP from 8x8 (formerly IIT) like in the Siemens/8x8 reference board design, the SIO interrupt period is locked to the IOM-2 time base after a call is setup, so no compensation on the uncompressed audio needs to be done by the JADE AN any more. This ensures the maximum possible audio quality.

Electrical Specification

7 Electrical Specification

7.1 Absolute Maximum Ratings

Parameter	Symbol	Limit values	Unit
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	−65 to 125	°C
Supply Voltage	V_{DD}	−0.5 to 4.2	V
Supply Voltage	V_{DDA}	−0.5 to 4.2	V
Supply Voltage	V_{DDP}	−0.5 to 6.0	V
Voltage of pin with respect to ground: XTAL1, XTAL2	V_S	−0.4 to $V_{DD}+0.5$	V
Voltage of any other pin with respect to ground	V_S	If $V_{DDP}<3V$: −0.4 to $V_{DD}+0.5$ If $V_{DDP}>3V$: −0.4 to $V_{DDP}+0.5$	V V

ESD-integrity is 1000V.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Operating Conditions

$V_{DD} = 3.0$ to 3.6 V, $V_{DDP} = 4.5$ to 5.5 V, $V_{SS} = 0$ V
 $V_{DDA} = 3.0$ to 3.6 V, $V_{SSA} = 0$ V;

7.3 DC Characteristics

Conditions: $V_{DD} = 3.0$ to 3.6 V, $V_{DDP} = 4.5$ to 5.5 V, $V_{SS} = 0$ V, $T_A = 0$ to $+70$ °C.
All pins except XTAL1, XTAL2:

Electrical Specification

Parameter	Symbol	Limit values		Unit	Test condition
		Min	Max		
High-Level Input Voltage	V_{IH}	2.0		V	
Low-Level Input Voltage	V_{IL}		0.8	V	
High-Level Output Voltage	V_{OH}	2.4		V	$I_{OH} = -400 \mu A$
Low-Level Output Voltage	V_{OL}		0.45	V	$I_{OL} = 7 \text{ mA}$ pins FSC, DCL, DU, DD (50 pF) $I_{OL} = 5 \text{ mA}$ all others (30 pF)
Input leakage current	I_{LI}	-1	1	μA	$0 \text{ V} < V_{IN} < V_{DD}$ for AD(0:7), ALE, \overline{WR} , \overline{CS} , \overline{RD} $0 \text{ V} < V_{IN} < V_{DDP}$ for all others
Output leakage current	I_{LO}	-1	1	μA	$0 \text{ V} < V_{OUT} < V_{DD}$ for AD(0:7) $0 \text{ V} < V_{OUT} < V_{DDP}$ for all others
$V_{DD} + V_{DDA}$ supply current	I_{DDS}		tbd	mA	
V_{DDP} supply current	I_{DDPS}		tbd	mA	

The power supply on voltage on $V_{DD} - V_{SS}$ and $V_{DDA} - V_{SSA}$ can be applied before or after the power supply on V_{DDP} / V_{SSP} without any damage to the circuit. Applying voltages to signal pins when power supply is not active (circuit not under bias) may cause damage – refer to paragraph "Absolute Maximum Ratings".

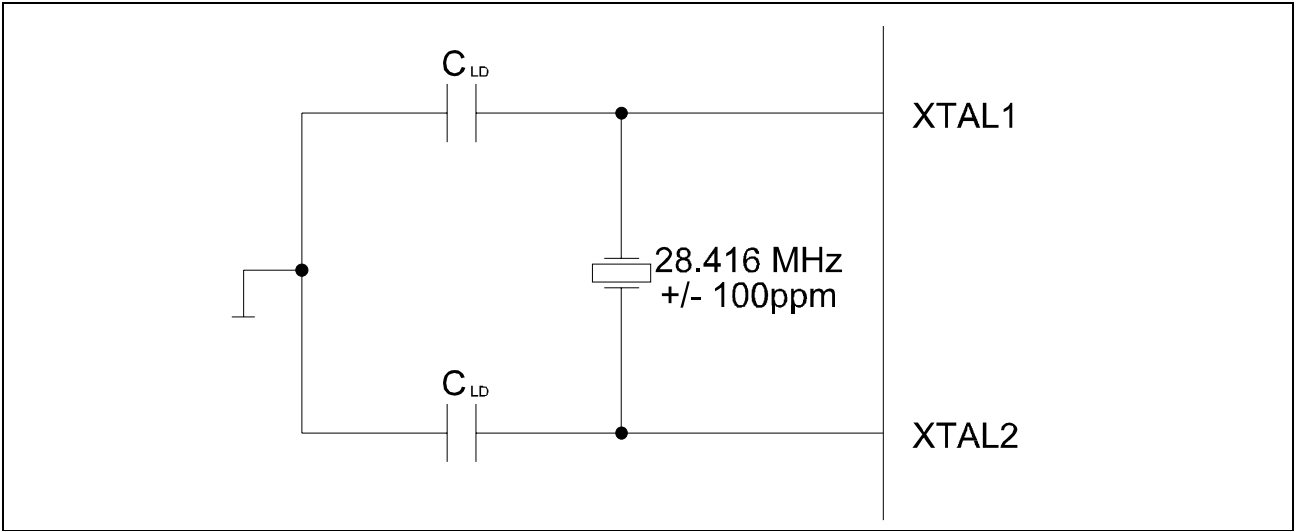
When power supply is switched on, the pads do not reach their stable bias until after 2 μs (maximum).

Electrical Specification

7.4 Capacitances

Parameter	Symbol	Limit values		Unit	Test condition
		Min	Max		
Input capacitance	C_{IN}		7	pF	
I/O capacitance	$C_{I/O}$		7	pF	
Load capacitance	C_{LD}		33	pF	XTAL1,2

7.5 Oscillator Circuit



7.6 XTAL 1,2 Recommended typical crystal parameters

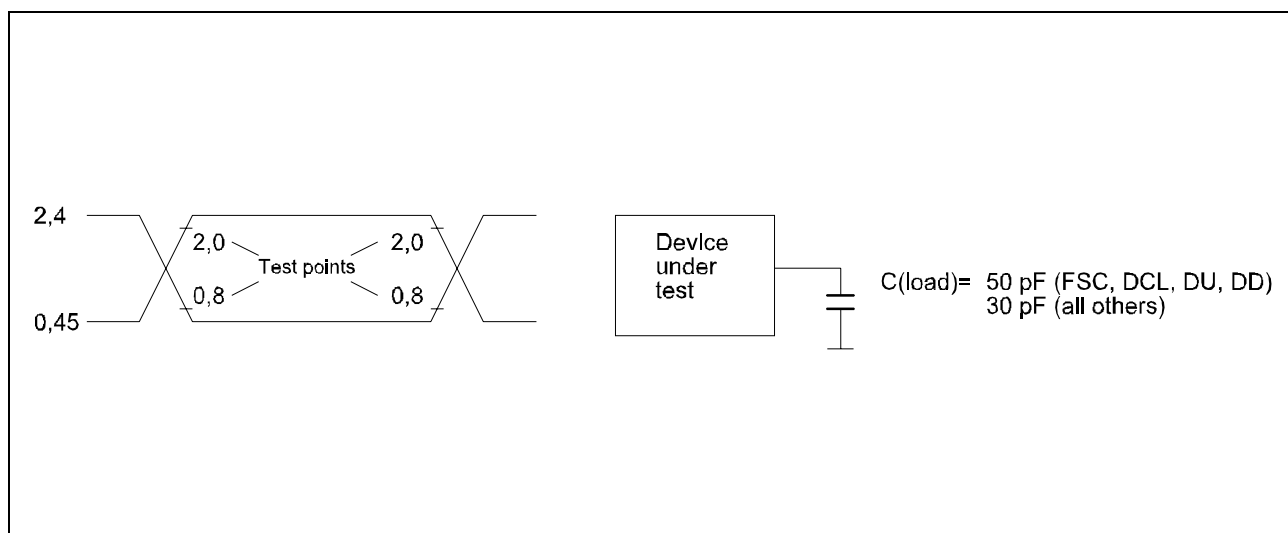
Parameter	Symbol	Limit Values	Unit
Motional capacitance	C_1	17	fF
Shunt	C_0	5	pF
Load	C_L	≤ 20	pF
Resonance resistance	R_r	≤ 50	Ω

7.7 AC Characteristics

7.7.1 Testing Waveform

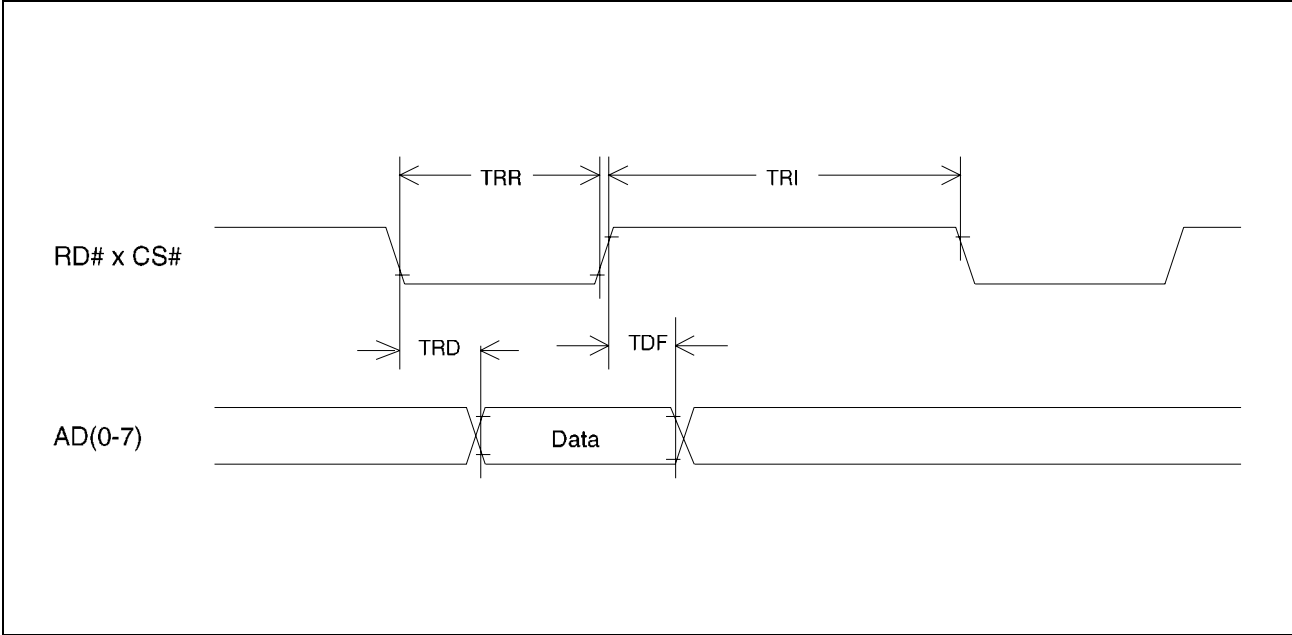
Conditions as above (Recommended Operating Conditions) at $T_A = 0$ to $70\text{ }^{\circ}\text{C}$.

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC testing input/output waveforms are shown in the **figure below**.

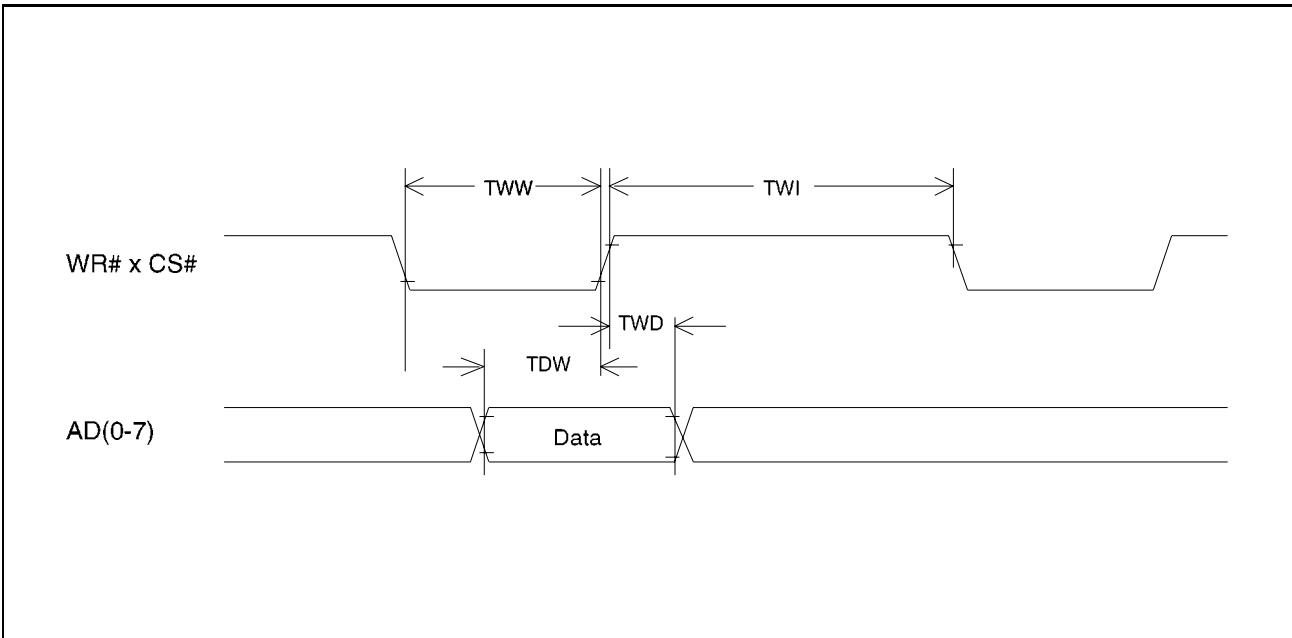


7.7.2 Parallel Host Interface Timing

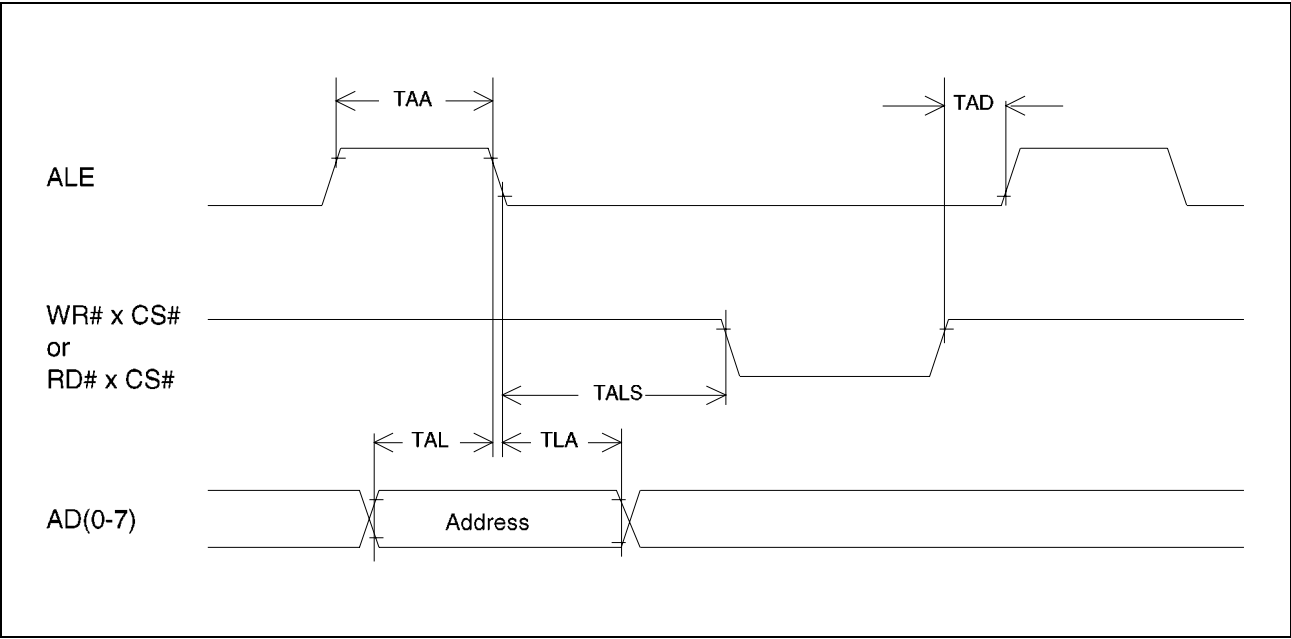
Host Interface Read Cycle



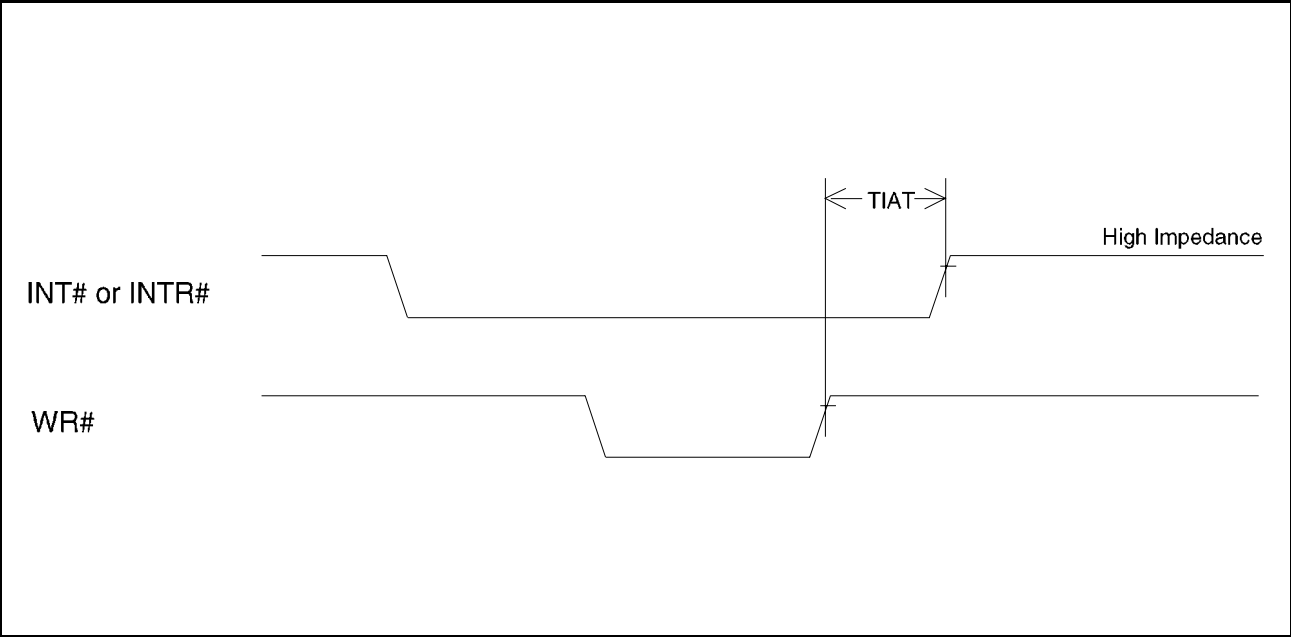
Host Interface Write Cycle



Address Timing



Interrupt Release Timing

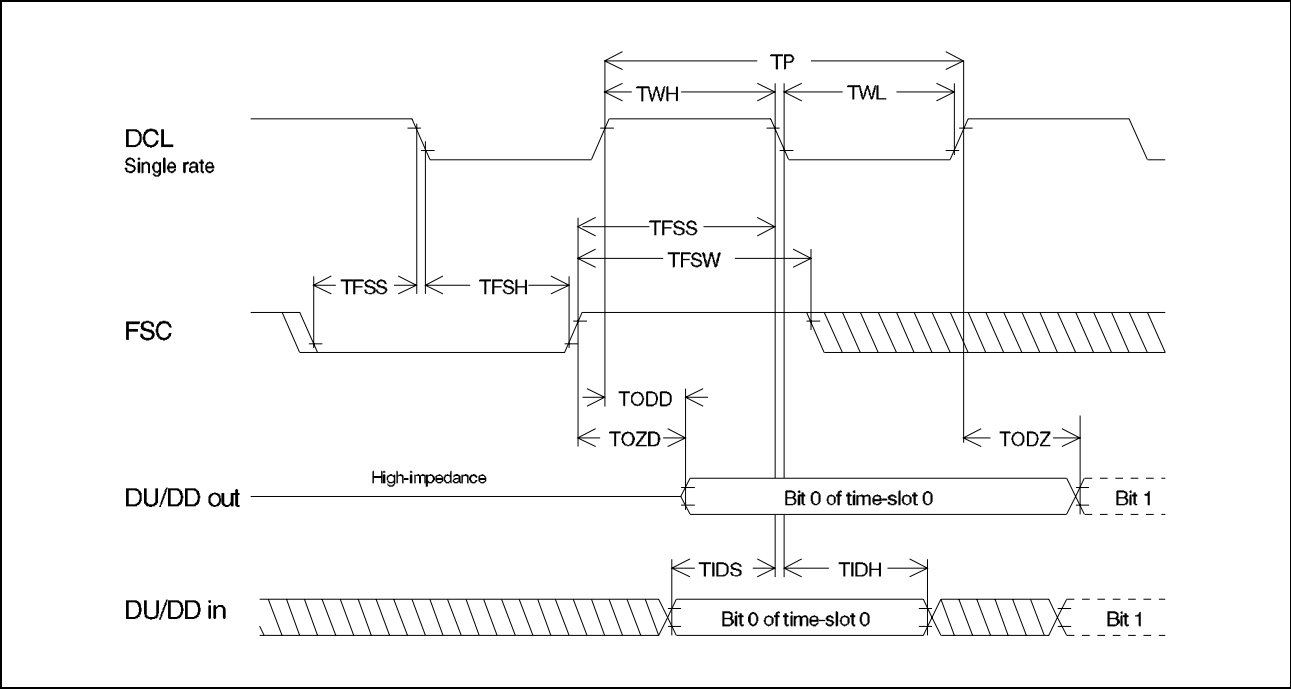


Electrical Specification

Parameter	Symbol	Limit values		Unit
		Min	Max	
ALE pulse width	t_{AA}	50		ns
Address setup time from ALE	t_{AL}	15		ns
Address hold time from ALE	t_{LA}	10		ns
Address latch setup time to \overline{WR} , \overline{RD}	t_{ALS}	0		ns
ALE guard time	t_{AD}	15		ns
\overline{RD} pulse width	t_{RR}	110		ns
Data output delay from \overline{RD}	t_{RD}		110	ns
Data float from \overline{RD}	t_{DF}		25	ns
\overline{RD} control interval	t_{RI}	70		ns
\overline{WR} pulse width	t_{WW}	60		ns
Data setup time to $\overline{WR} \times \overline{CS}$	t_{DW}	35		ns
Data hold time from $\overline{WR} \times \overline{CS}$	t_{WD}	10		ns
\overline{WR} control interval	t_{WI}	70		ns
Interrupt acknowledge to high-impedance	t_{IAT}		100	ns

7.7.3 IOM-2 Interface Timing

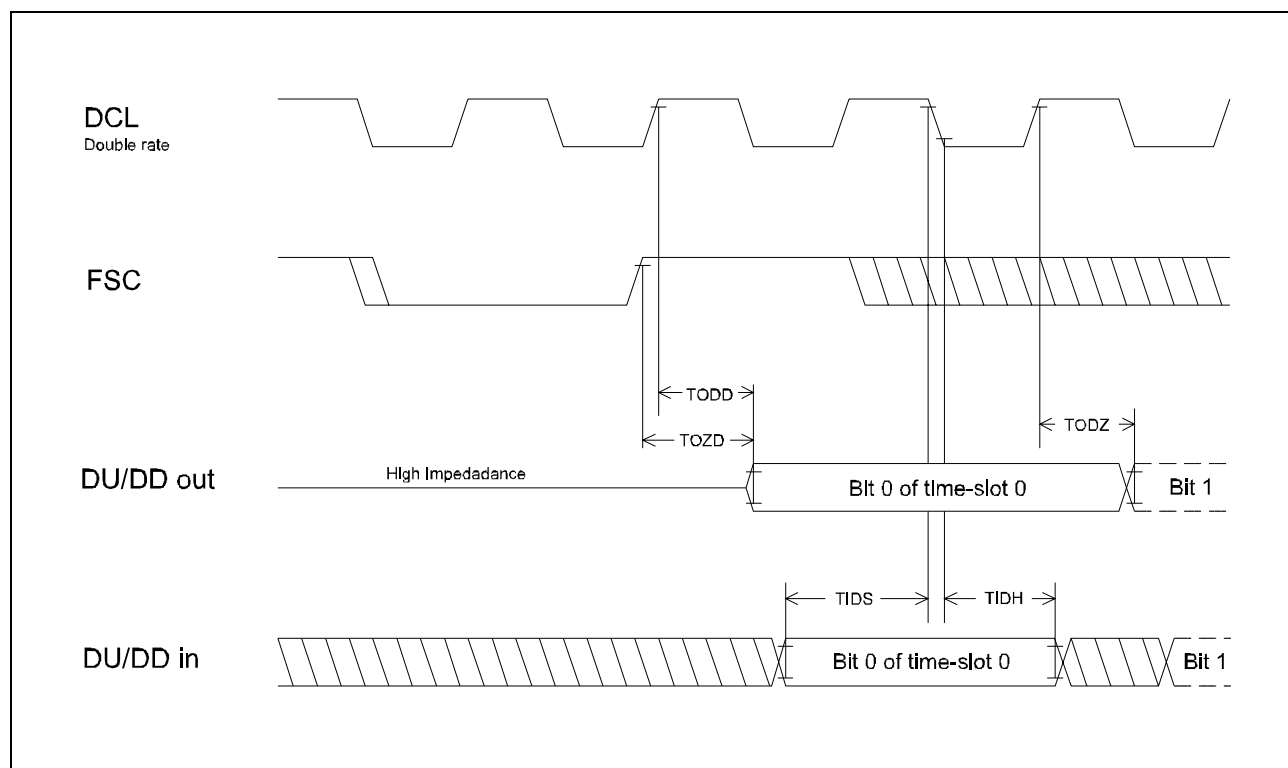
IOM-2 (PCM) Timing with Single Rate DCL



Parameter	Symbol	Limit values		Unit
		Min	Max	
DCL period	t_P	244		ns
DCL high	t_{WH}	100		ns
DCL low	t_{WL}	100		ns
Frame sync setup	t_{FSS}	120		ns
Frame sync hold	t_{FSH}	40		ns
Frame sync width	t_{FSW}	40		ns
Output data delay from FSC (if $t_{OZD} < t_{ODD}$)	t_{OZD}		100	ns
Output data delay from DCL (if $t_{ODD} < t_{OZD}$)	t_{ODD}		100	ns
Output data from active to high impedance	t_{ODZ}		80	ns
Input data setup	t_{IDS}	20		ns
Input data hold	t_{IDH}	40		ns

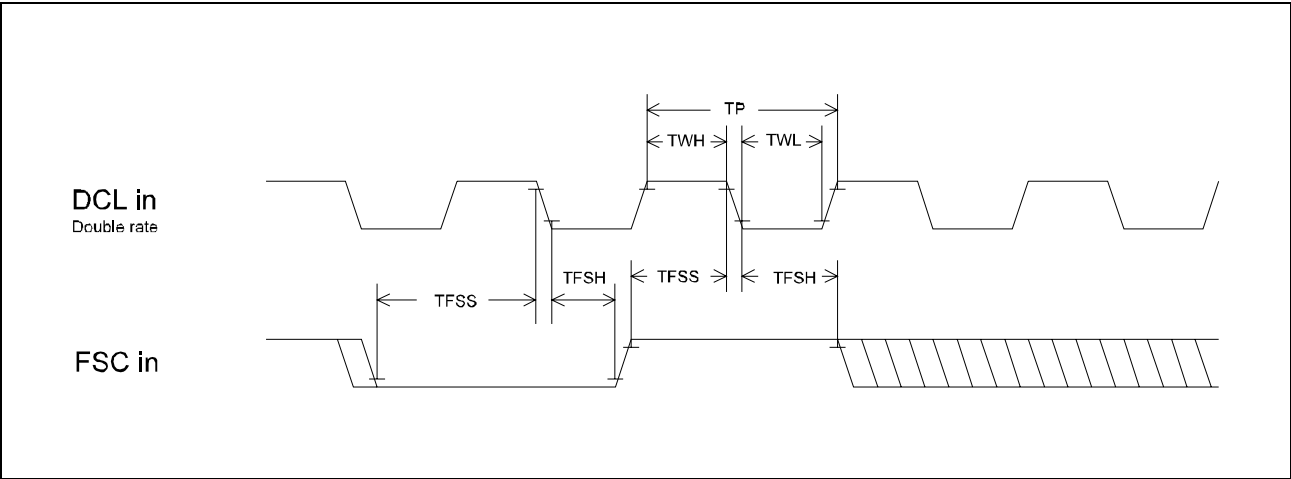
Electrical Specification

IOM-2 Timing with Double Rate DCL



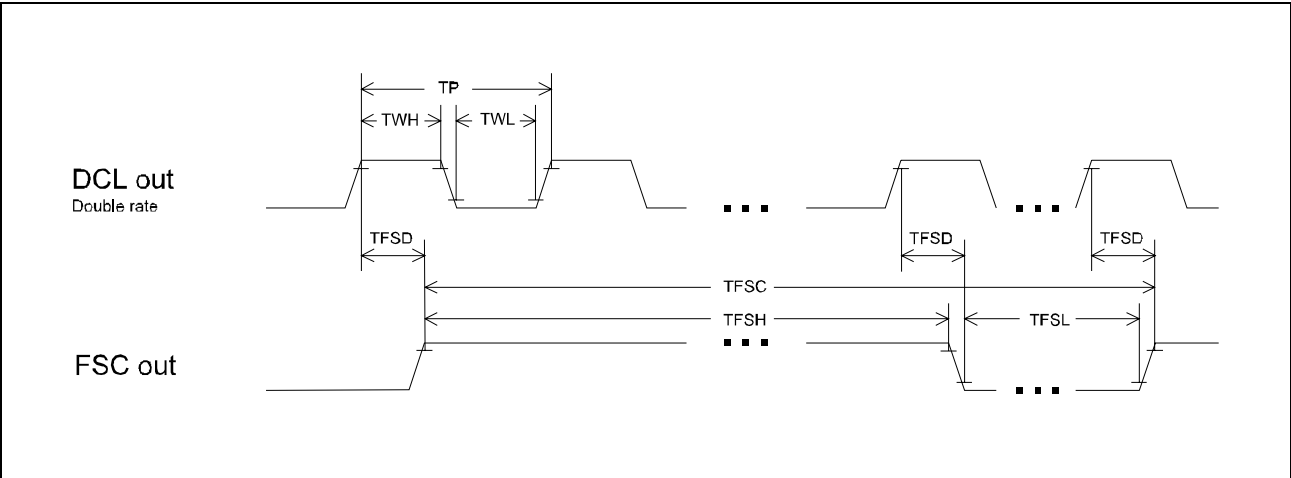
Parameter	Symbol	Limit values		Unit
		Min	Max	
Output data from high impedance to active	t_{OZD}		100	ns
Output data delay from clock	t_{ODD}		100	ns
Output data from active to high impedance	t_{ODZ}		80	ns
Input data setup	t_{IDS}	20		ns
Input data hold	t_{IDH}	40		ns

IOM-2 Input Timing with Double Rate DCL



Parameter	Symbol	Limit values		Unit
		Min	Max	
DCL period	t_p	244		ns
DCL high	t_{WH}	100		ns
DCL low	t_{WL}	100		ns
Frame sync setup	t_{FSS}	40		ns
Frame sync hold	t_{FSH}	40		ns

IOM-2 Output Timing with Double Rate DCL

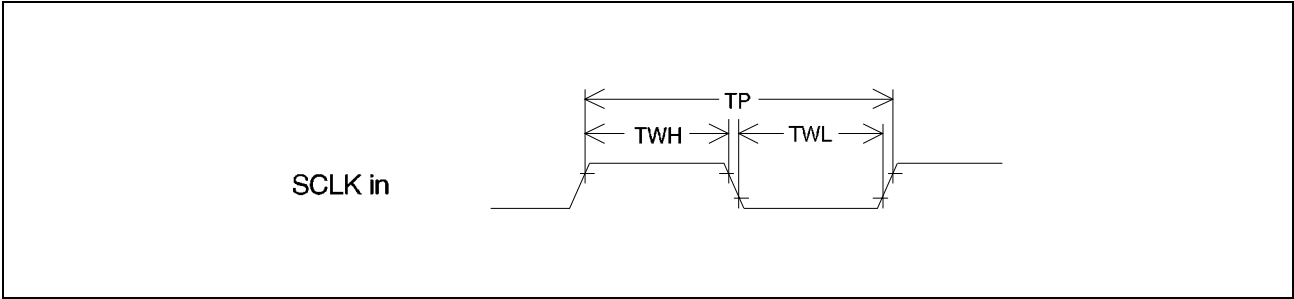


Electrical Specification

Parameter	Symbol	Limit values			Unit
		Min	Typ	Max	
DCL period	t_P	520	651	782	ns
DCL high	t_{WH}	240			ns
DCL low	t_{WL}	240			ns
Frame sync delay	t_{FSD}			100	ns
FSC period	t_{FSC}		125		μ s
FSC high period	t_{FSH}	60	62.5	65	μ s
FSC low period	t_{FSL}	60	62.5	65	μ s

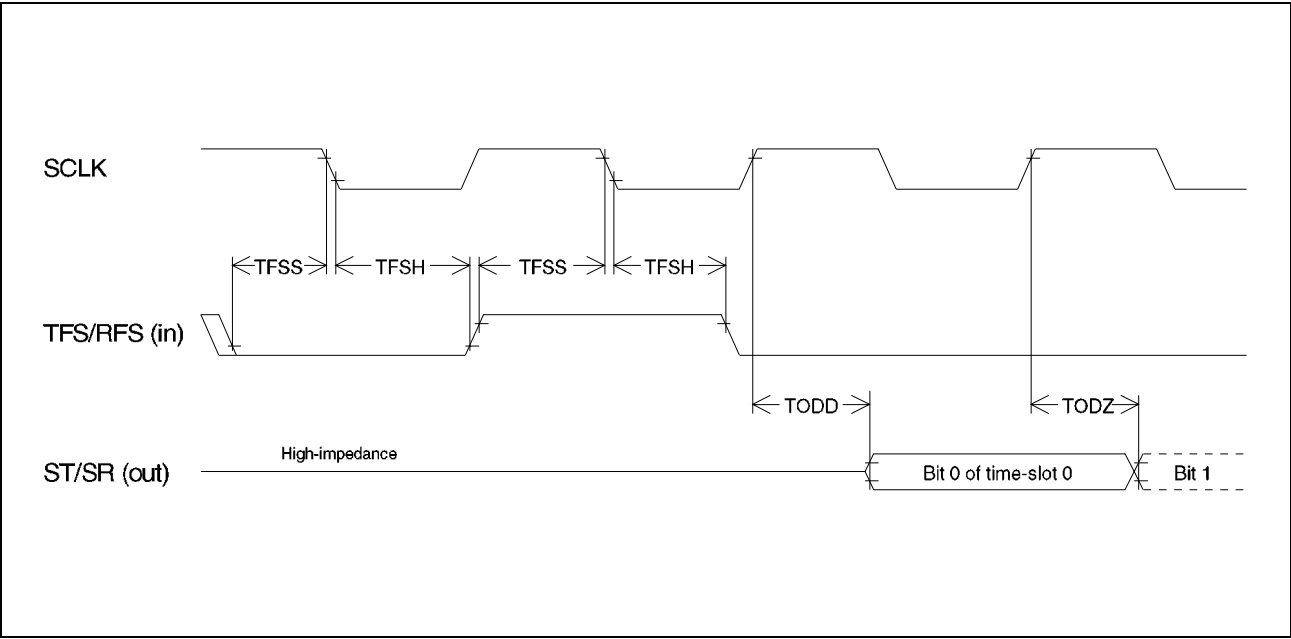
7.7.4 Serial Audio Interface Timing

Serial Clock



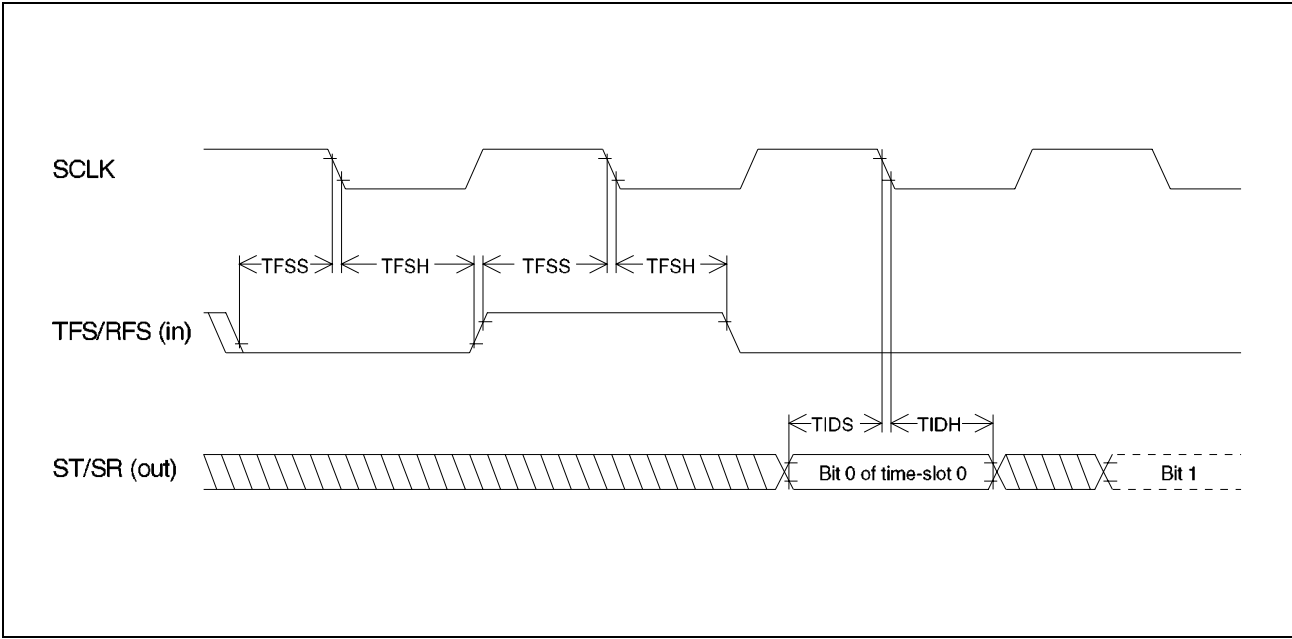
Parameter	Symbol	Limit values		Unit
		Min	Max	
SCLK period	t_P	244		ns
SCLK high	t_{WH}	100		ns
SCLK low	t_{WL}	100		ns

Serial Output Timing



Parameter	Symbol	Limit values		Unit
		Min	Max	
TFS/RFS setup	t_{FSS}	40		ns
TFS/RFS hold	t_{FSH}	40		ns
Output data delay from clock	t_{ODD}		100	ns
Output data from active to high impedance	t_{ODZ}		80	ns

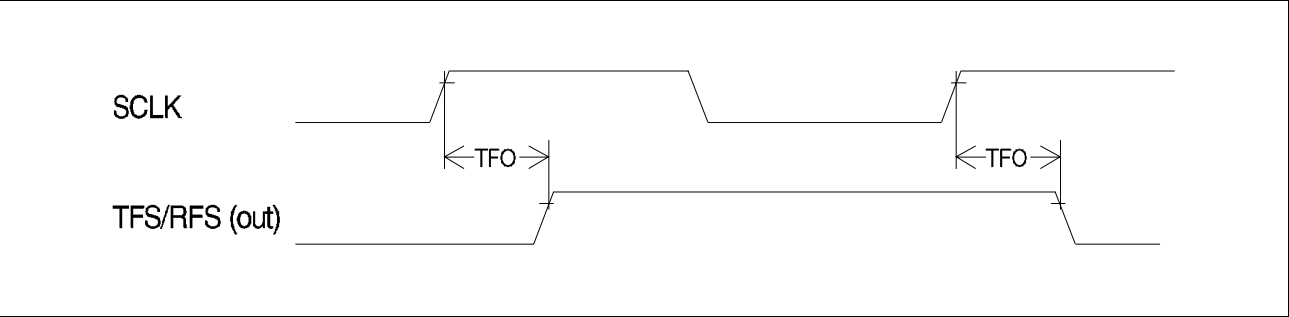
Serial Input Timing



Parameter	Symbol	Limit values		Unit
		Min	Max	
TFS/RFS setup	t_{FSS}	40		ns
TFS/RFS hold	t_{FSH}	40		ns
Input data setup	t_{IDS}	20		ns
Input data hold	t_{IDH}	40		ns

Electrical Specification

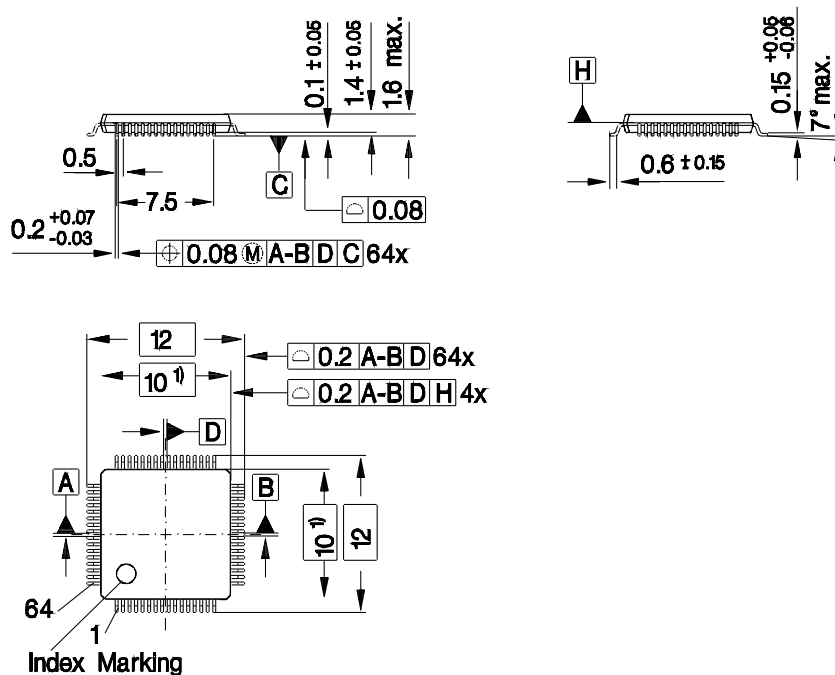
TFS/RFS Output Timing



Parameter	Symbol	Limit values		Unit
		Min	Max	
TFS/RFS out	t_{FO}		40	ns

8 Package Outline

P-TQFP-64 package with size 10x10 mm, pitch 0.5 mm, height 1.4 mm.



1) Does not include plastic or metal protrusion of 0.25 max. per slide