SIEMENS

ICs for Communications

Enhanced ISDN Data Access Controller ISAR 34

PSB 7115 Version 2.1

Product Overview 07.97

T7115-XV21-O2-7600

PSB 7115 Revision History:		Current Version: 07.97
Previous Version:		03.97
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
16-23, 25, 27, 29, 35, 37	16 - 23, 25, 27, 29, 35, 37	Pin Configuration (A3-7, V_{DDAP}, V_{SSAP})
14, 15, 25, 30	14, 15, 25, 30	FSC and DCL also output pins
30	30	DU and DD also push pull
29, 35	29, 35	Software Reset bit
29, 35	29, 35	Register Mapping

Edition 07.97

This edition was realized using the software system FrameMaker®.

Published by Siemens AG,
HL TS,
Balanstraße 73,
81541 München

Attention please!

As far as patents or other rights of third parties are concerned, liability is only assumed for components, not for applications, processes and circuits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

For questions on technology, delivery and prices please contact the Semiconductor Group Offices in Germany or the Siemens Companies and Representatives worldwide (see address list).

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Siemens Office, Semiconductor Group.

Siemens AG is an approved CECC manufacturer.

Packing

Please use the recycling operators known to you. We can also help you – get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport.

For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

Components used in life-support devices or systems must be expressly authorized for such purpose!

Critical components[1] of the Semiconductor Group of Siemens AG, may only be used in life-support devices or systems[2] with the express written approval of the Semiconductor Group of Siemens AG.

1 A critical component is a component used in a life-support device or system whose failure can reasonably be expected to cause the failure of that life-support device or system, or to affect its safety or effectiveness of that device or system.

2 Life support devices or systems are intended (a) to be implanted in the human body, or (b) to support and/or maintain and sustain human life. If they fail, it is reasonable to assume that the health of the user may be endangered.

Table of Contents **Page**

1 General Information

The ISAR 34, ISDN Data Access Controller forms an advanced solution for ISDN applications communicating with remote ISDN as well as analog terminals.
The ISAR 34 PSB 7115 follows its predecessor ISAR PSB 7110 which is capable of modem modulation up to 14400 bit/s (V.32bis). The new ISAR 34 has the similar functional architecture and additionally supports modem modulation up to 33600 bit/s (V.34bis). As well the platform is upgradeable to new modem standards (PCM modems) and is able to run algorithms for audio compression (e.g. G.728) or answering machine alternatively.

The ISAR 34 is designed for data access over ISDN or analog line. It can be used in data terminals combining ISDN and analog functionality for communication with remote subscribers. It can also be integrated in fax/modem pools and routers.
Combining with Siemens ICs for audio compression and acoustic echo cancellation, the ISAR 34 fits into H.320/H.324 video conferencing systems.

It integrates two data formatting units which support binary framing, HDLC and ASYNC, which is an asynchronous data formatting according to ITU-T V.14. The data from the formatting units is input data to a fax/modem modulation or V.110 or transparent framing towards the IOM-2 timeslots. As well dual channel DTMF generation and detection is supported in the data pump.

The ISAR 34 operates on the IOM-2 interface in terminal mode (1.536 MHz DCL) and is also designed to operate on line-card IOM-2 interfaces (4.096 MHz DCL).

A serial interface supports access of external codecs like the complete modem frontend chipset PSB 4595/4596 Analog Line Interface Solution (ALIS).

The ISAR 34 ensures firmware safety through its flexible memory interface. The DSP program is stored in external memory which can be SRAM (e.g. for DSP program download) or non-volatile memory (e.g. for stand-alone applications).

An elaborate mailbox interface with 256 byte buffers in each direction reduces the number of registers to a minimum.

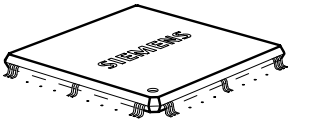
The PSB 7115 ISDN Data Access Controller is a CMOS device offered in a thin quad-flat pack package. It operates from a single 3.3 V supply with the option to drive the interface lines by a 5 V supply.

SIEMENS

Enhanced ISDN Data Access Controller PSB 7115
ISAR 34

Version 2.1 **CMOS**

1.1 Features



P-TQFP-144-2

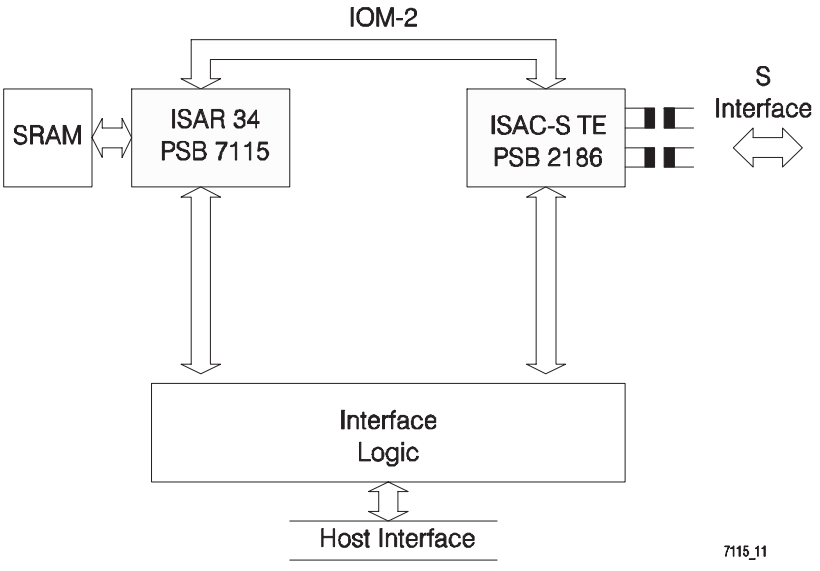
- Modem modulation up to 33600 bit/s (V.34bis) including fallback modes
- Fax modulation up to 14400 bit/s (V.17) including fallback modes
- Bit rate adaptation according to V.110 for both B-channels (except during datamodem modulation)
- Two Channel DTMF generation and detection
- Two universal formatter supporting ASYNC (ITU-T V.14), HDLC and binary framing of data for B-channel applications
- ISDN D-channel HDLC controllerwith TIC bus support
- ISDN C/I-channel and MONITOR channel handler
- IOM-2 terminal mode (1.536 MHz), line card mode (4.096 MHz)
- Serial audio interface for analog modem codecs and DAAs
- Mailbox interface for host communication
- External memory interface to connect external program and data memory
- Supports host based (program download to external SRAM) and standalone (flash memory) applications
- Upgradeable to new technologies (e.g. PCM modem)
- Hardware platform for various algorithms (e.g. audio compression G.728)
- 253 byte FIFO per direction for host interface communication of B-channel data
- 3.3 V power supply
- Thin QFP-package
- Advanced CMOS technology

Type	Ordering Code	Package
PSB 7115 F V2.1	Q67101 - H6749	P-TQFP-144-2

1.2 System Integration

1.2.1 ISDN PC/Workstation Adapter with S-Interface

The ISDN PC or Workstation Adapter is based on the ISAR 34. A PSB 2186, ISAC-S TE forms the S-transceiver and the ISAR 34 provides the HDLC controller to perform the D-channel signalling protocol. External circuitry is required for the S-interfaces which includes the transformer and protection circuitry. The host interface of the ISAR 34 is connected to the host bus.



Note: Memory configuration is described in detail in chapter 2.3.4.

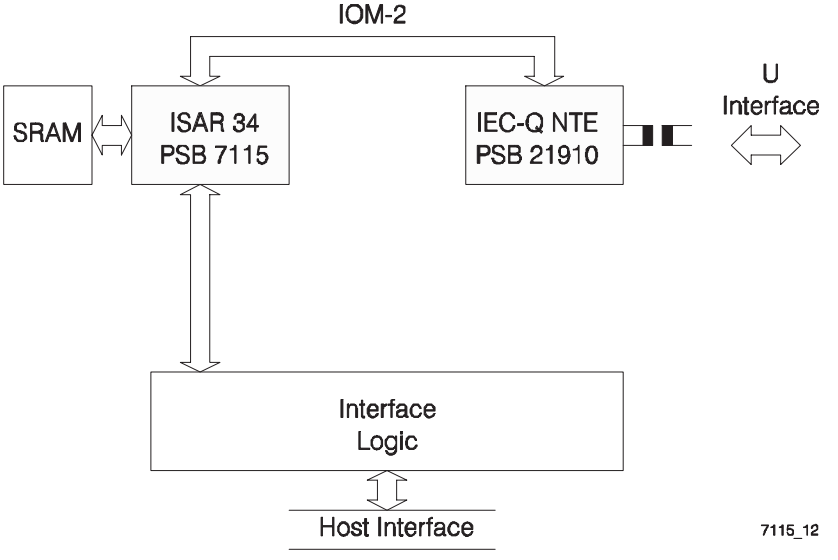
Figure 1
ISDN PC/Workstation Adapter with S-Interface

The ISAR 34 supports HDLC based applications like file transfer, access to packet switches (X.75, V.120, PPP). It also supports communication to terminal adapters which perform bit rate adaptation according to V.110.

A special feature of the ISAR 34 is its support for analog fax/modem applications. Therefore, PCM data is converted to linear data and handled by a V.34bis/V.17 data pump to support data rates up to 33600 bit/s (V.34bis) and 14400 bit/s (V.17).

1.2.2 ISDN PC / Workstation Adapter with U-Interface

Especially for the US market the U-interface formed by the PSB 21910 IEC-Q NTE, is considered as the standard basic rate interface. The ISAR 34 supports these applications in a cost effective way since it includes the D-channel HDLC controller, the command/indicate channel as well as the MONITOR channel. The IOM-2 interface supports TIC bus access.



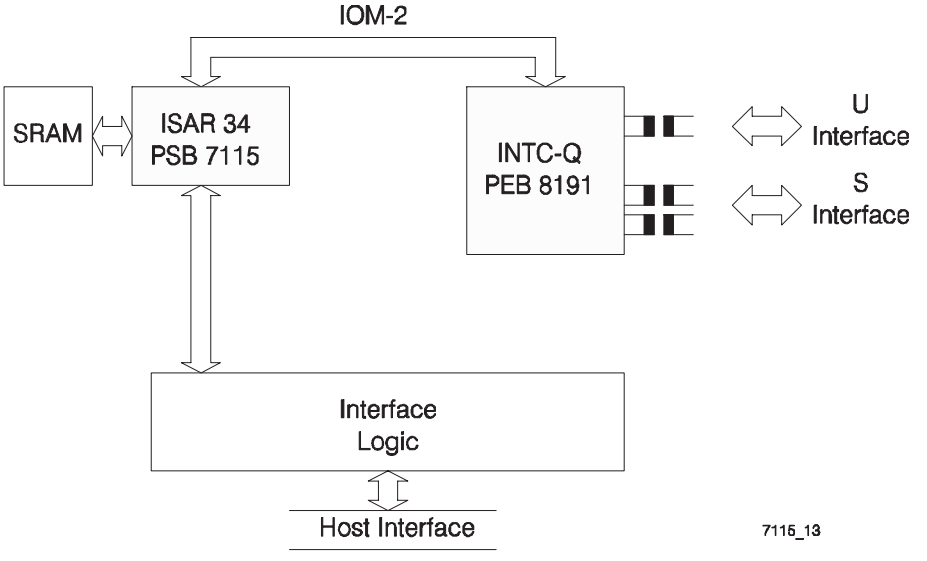
Note: Memory configuration is described in detail in chapter 2.3.4.

Figure 2
ISDN PC/Workstation Adapter with U-Interface

1.2.3 ISDN PC / Workstation Adapter as Intelligent NT

A variation of the U-interface PC card is called the intelligent NT since it provides the network termination function as part of the card.

The ISAR 34 supports the TIC bus of the IOM-2 interface which controls the D-channel data flow between the local D-channel source inside the ISAR 34 and the D-channel sources on the S-interface. The INTC-Q PEB 8191 is the integration of the S- and U-transceivers, dedicated to intelligent NT applications.

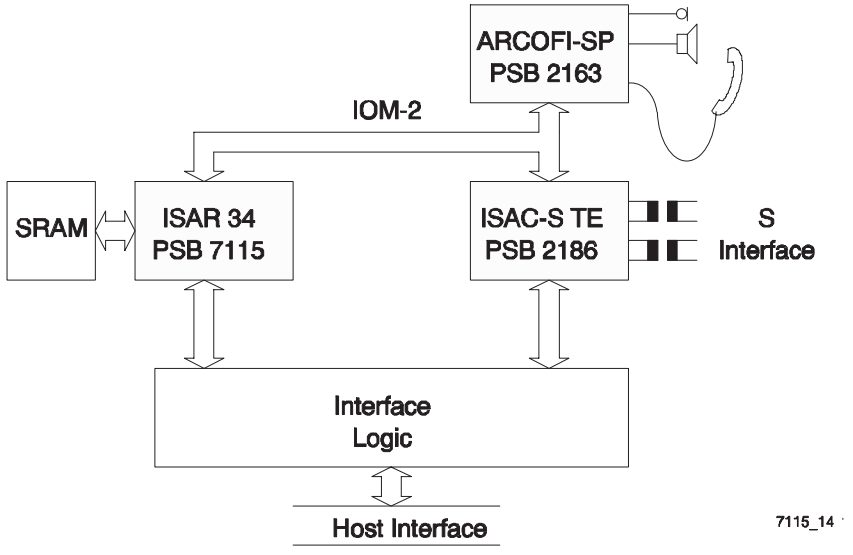


Note: Memory configuration is described in detail in chapter 2.3.4.

Figure 3
ISDN PC/Workstation Adapter as Intelligent NT

1.2.4 ISDN Voice/Data Terminal

Figure 4 shows a voice data terminal developed on a PC card, where the ISAR 34 provides its fax and modem functionality within a three chip solution. During ISDN calls the ARCOFI-SP PSB 2163 provides for speakerphone functions and includes an additional DTMF generator.



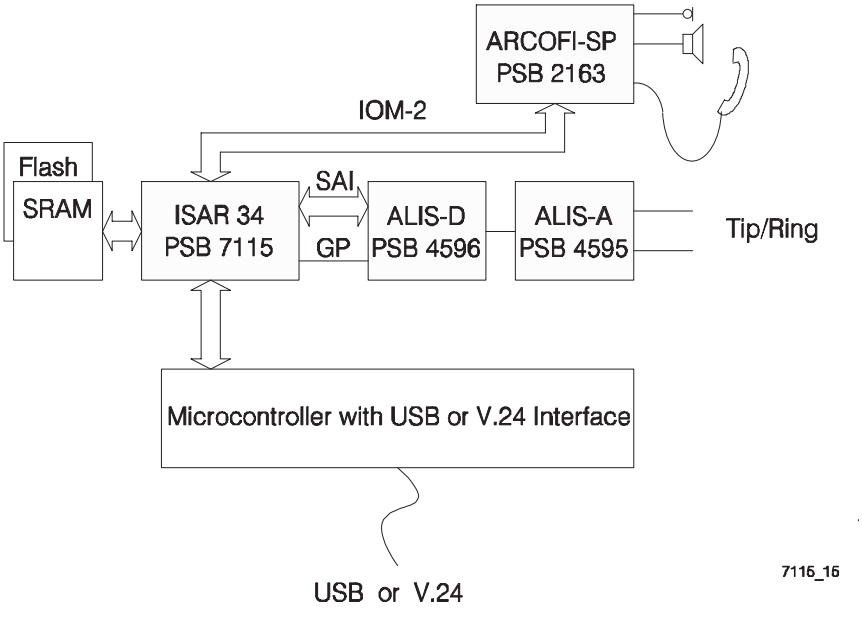
Note: Memory configuration is described in detail in chapter 2.3.4.

Figure 4
ISDN Voice/Data Terminal

1.2.5 Analog Voice/Data Modem

Figure 5 shows a microcontroller based voice/data terminal to be connected to the V.24 or USB interface of a PC. The ALIS is a two chip solution for DAA, Codec and filter and builds a transformerless connection to the tip/ring interface.

The ISAR 34 does not require host download of the DSP program as this is stored in external flash memory.

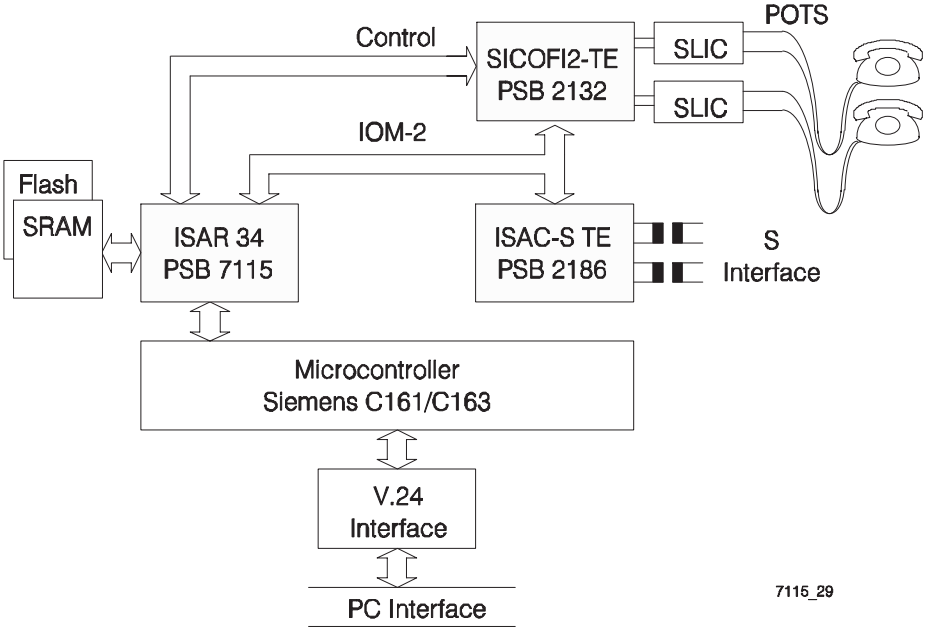


Note: Memory configuration is described in detail in chapter 2.3.4.

Figure 5
Analog Voice/Data Modem

1.2.6 ISDN Standalone Terminal with POTS Interface

Figure 6 shows a standalone terminal that may be connected to the communications interface of a PC providing the fax and modem functionality of the ISAR 34 within a microcontroller based solution. The SICOFI2-TE PSB 2132 enables connection of analog terminals, e.g. telephones, to the dual channel POTS interface.

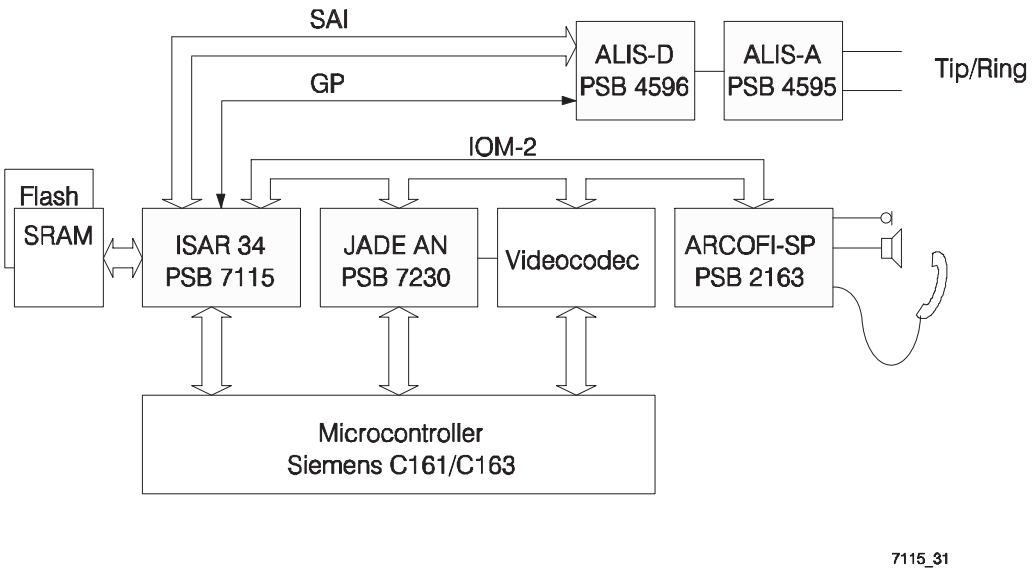


Note: Memory configuration is described in detail in chapter 2.3.4.

Figure 6
ISDN Standalone Terminal with POTS Interface

1.2.7 Analog Videophone

Figure 7 shows an analog videophone with world wide tip/ring interface through the fully programmable analog line interface solution ALIS which is connected to the serial audio interface (SAI) of the ISAR 34. The JADE AN PSB 7230 performs audio compression for the H.324 standard and the ISAR 34 realizes the modem functionality.



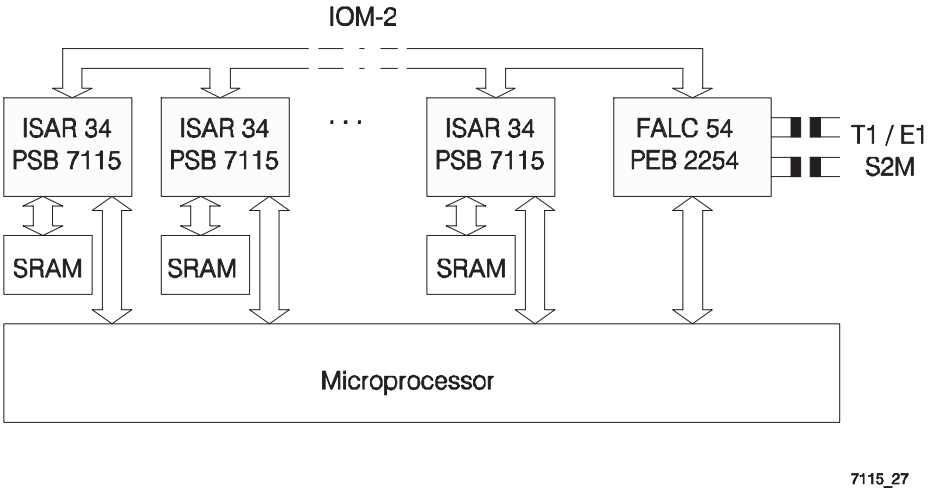
Note: Memory configuration is described in detail in chapter 2.3.4.

Figure 7
Analog Videophone

1.2.8 Fax/Modem Pool with Primary Rate Access

Figure 8 shows an application suitable for modem pools or fax servers (fax on demand). The Frame and Line Interface Controller FALC 54 PEB 2254 provides for direct access to the PCM highway, may be programmed to operate in 1.544 Mbit/s (PCM24, T1) or 2.048 Mbit/s (PCM30/E1) carrier systems and provides the complete functionality of a line interface-, framing-, clock generation- and signalling unit. The selection of timeslots on the ISAR 34 is programmable, so they are cascadable in any order.

Depending on whether or not the microprocessor performs a download to external SRAM of the ISAR 34, flash memory may be required or not.



Note: Memory configuration is described in detail in chapter 2.3.4.

Figure 8
Fax/Modem Pool with Primary Rate Access

1.3 Logic Symbol

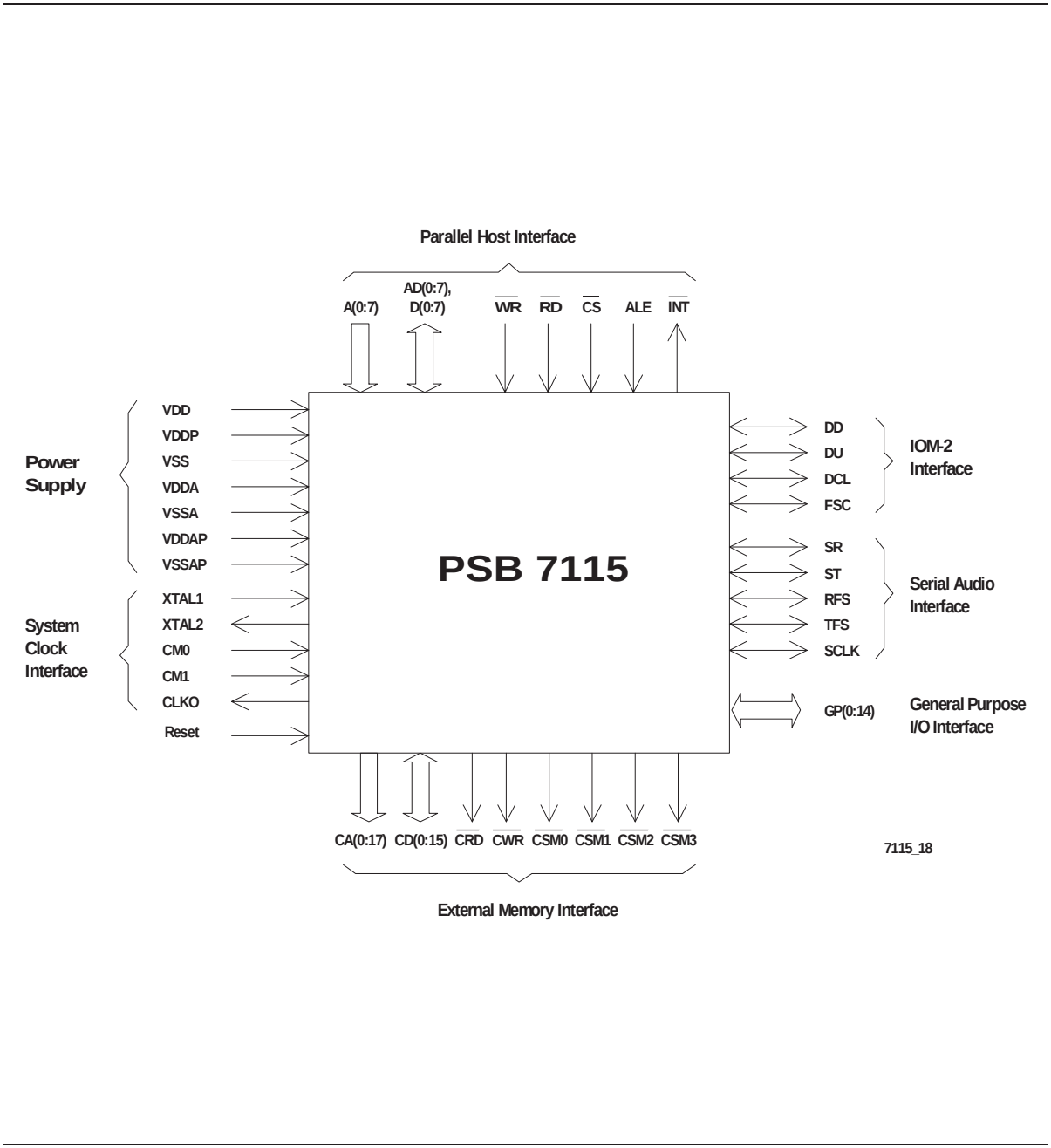


Figure 9
Logic Symbol

1.4 Device Architecture

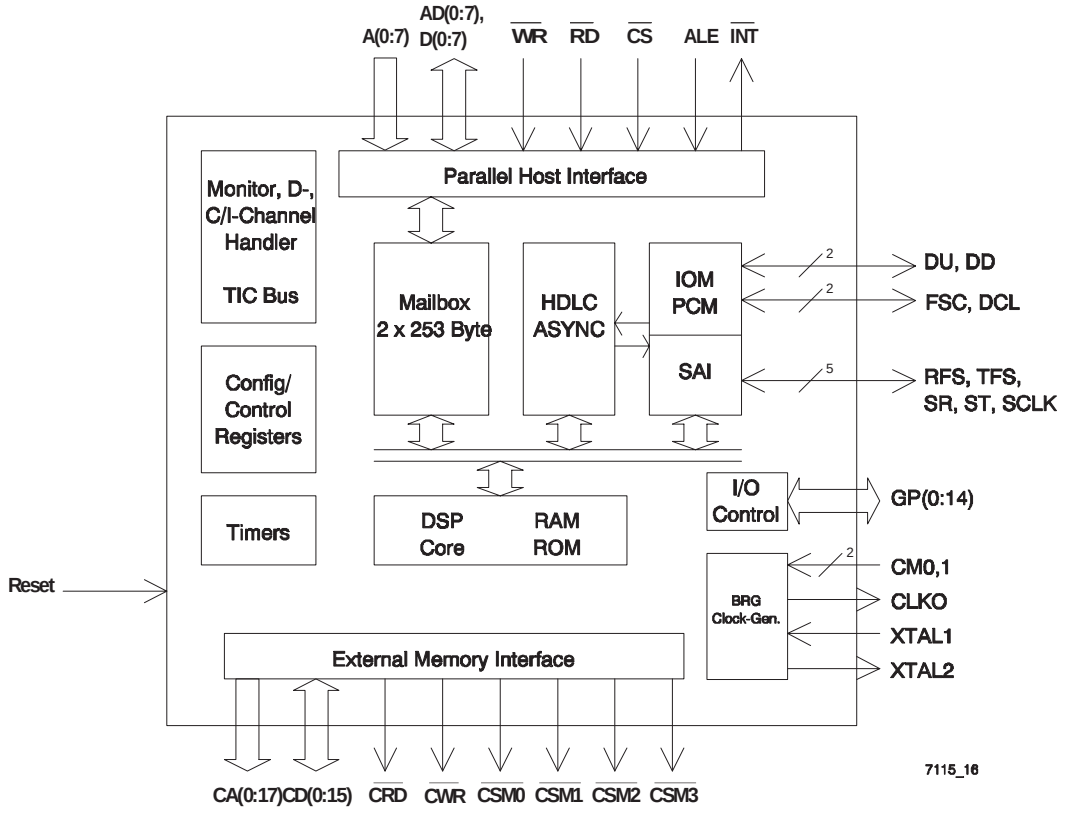


Figure 10
Device Architecture

1.5 Pin Configuration

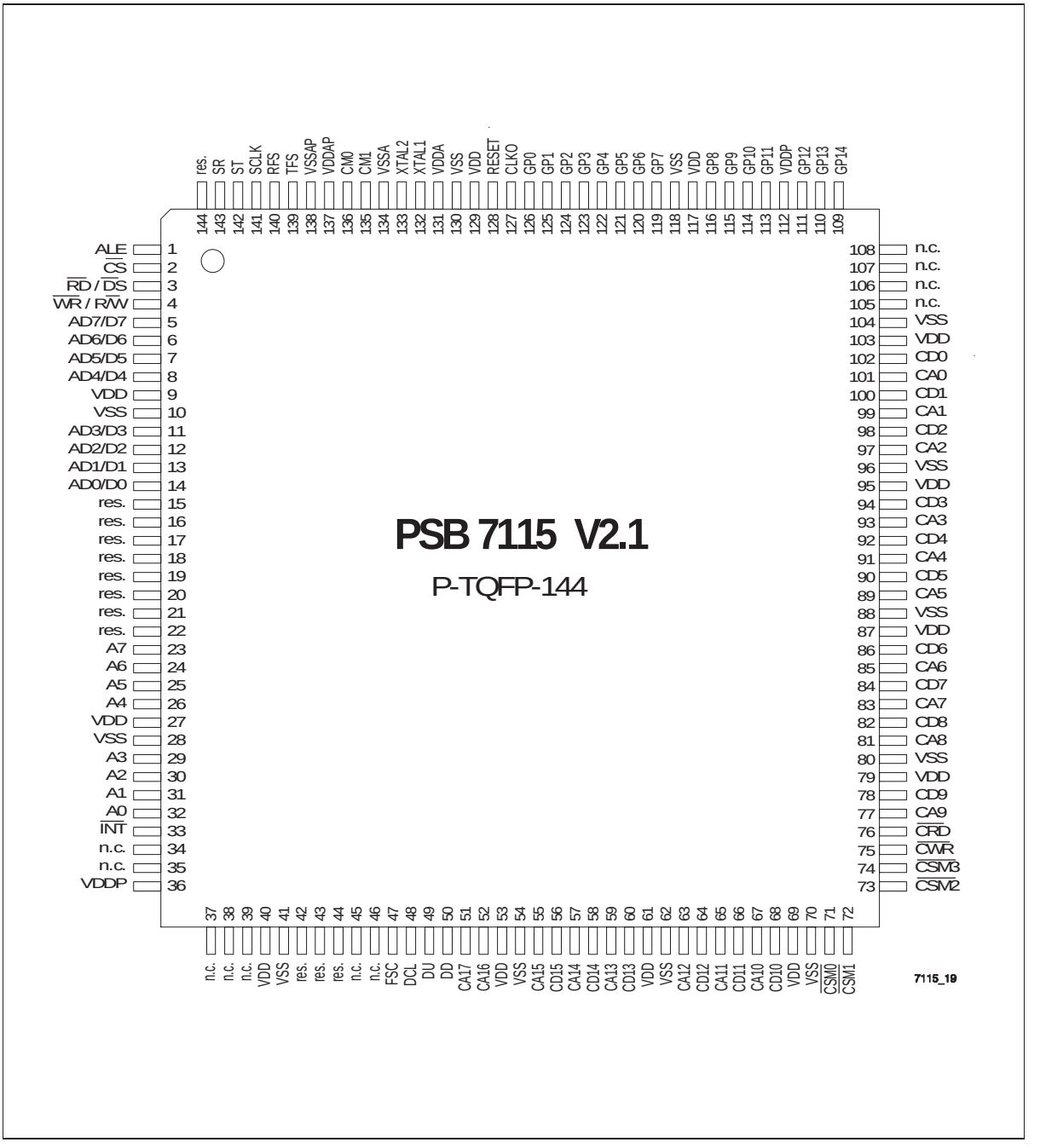


Figure 11
Pinout

1.6 Pin Description

Pin No.	Symbol	Input (I) Output (O)	Function
Parallel Host Interface			
14 13 12 11 8 7 6 5	AD0/D0 AD1/D1 AD2/D2 AD3/D3 AD4/D4 AD5/D5 AD6/D6 AD7/D7	I/O I/O I/O I/O I/O I/O I/O I/O	**Multiplexed Bus Mode: Address/Data Bus** Transfers addresses and data between the host and the ISAR 34. **Demultiplexed Bus Mode: Data Bus** Transfers data between the host and the ISAR 34.
32 31 30 29 26 25 24 23	A0 A1 A2 A3 A4 A5 A6 A7	I I I I I I I I	**Demultiplexed Bus Mode (only): Address Bus** Transfers address from the host to the ISAR 34. These pins are not used in multiplexed bus mode, therefore they should be tied to VDD in this mode.
3	$\overline{RD}$ $\overline{DS}$	I I	**Read** This signal indicates a read operation. (Siemens/Intel bus mode). **Data Strobe** The rising edge marks the end of a valid read or write operation. (Motorola bus mode).
4	$\overline{WR}$ R/$\overline{W}$	I I	**Write** This signal indicates a write operation. (Siemens/Intel bus mode). **Read/Write** A "1" identifies a valid host access as a read operation. A "0" identifies the access as a write operation. (Motorola bus mode).
2	$\overline{CS}$	I	**Chip Select** A "0" on this line selects the ISAR 34 for a read/write operation.

1.6 Pin Description (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
1	ALE	I	**Address Latch Enable** A "1" on this line indicates an address on AD (0:7), that will be latched by the ISAR 34 (multiplexed mode only). This allows the ISAR 34 to be directly connected to a host with multiplexed address/data bus. ALE also selects the interface mode (multiplexed or non-multiplexed).
33	$\overline{\text{INT}}$	O (OD)	**Interrupt Request** This signal is activated, when the ISAR 34 requests an interrupt. This pin is an open drain output.
IOM®-2 Interface			
50	DD	I/O	**Data Downstream** on IOM-2/PCM interface.
49	DU	I/O	**Data Upstream** on IOM-2/PCM interface.
48	DCL	I/O	**Data Clock** Clock frequency is twice the data rate.
47	FSC	I/O	**Frame Sync** Marks the beginning of a physical IOM-2 or PCM frame.
Serial Audio Interface			
141	SCLK	I/O	**Serial Clock** Serial clock for SR and ST.
143	SR	I/O	**Serial Data Receive**
142	ST	I/O	**Serial Data Transmit**
140	RFS	I/O	**Receive Frame Sync**
139	TFS	I/O	**Transmit Frame Sync**

1.6 Pin Description (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
System Clocks			
132	XTAL1	I	**Crystal In or Clock In** If a crystal is used, it is connected across XTAL1 and XTAL2. If a clock signal is provided (via an external oscillator), this signal is input via XTAL1. In this case the XTAL2 output is to be left non-connected.
133	XTAL2	O	**Crystal Out** Left unconnected if a crystal is not used.
136 135	CM0 CM1	I I	**Clock Mode Select** One of four different clock mode options can be selected by CM1,0 tied to VDDP or VSS.
127	CLKO	O	**Clock Out** A buffered output clock equal to the clock input at XTAL1 is provided for further devices on the system.
External Memory Interface			
101 99 97 93 91 89 85 83 81 77 67 65 63 59 57 55 52 51	CA0 CA1 CA2 CA3 CA4 CA5 CA6 CA7 CA8 CA9 CA10 CA11 CA12 CA13 CA14 CA15 CA16 CA17	O O O O O O O O O O O O O O O O O O	**C-Bus Address** Used for addressing external program and data memory.

1.6 Pin Description (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
102 100 98 94 92 90 86 84 82 78 68 66 64 60 58 56	CD0 CD1 CD2 CD3 CD4 CD5 CD6 CD7 CD8 CD9 CD10 CD11 CD12 CD13 CD14 CD15	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	**C-Bus Data** Data bus for external program and data memory.
76	$\overline{\text{CRD}}$	O	**C-Bus Read to external memory** This signal must be connected to the $\overline{\text{RD}}$ input of the external program and data memory.
75	$\overline{\text{CWR}}$	O	**C-Bus Write to external memory** This signal must be connected to the $\overline{\text{WR}}$ input of the external program and data memory.
71 72 73 74	$\overline{\text{CSM0}}$ $\overline{\text{CSM1}}$ $\overline{\text{CSM2}}$ $\overline{\text{CSM3}}$	O O O O	**C-Bus Select line for** **external memory bank #0, #1, #2, #3** This signal must be connected to the $\overline{\text{CS}}$ input of the corresponding memory bank.

1.6 Pin Description (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
General Control			
128	RESET	I	**Reset input**
126 125 124 123 122 121 120 119 116 115 114 113 111 110 109	GP0 GP1 GP2 GP3 GP4 GP5 GP6 GP7 GP8 GP9 GP10 GP11 GP12 GP13 GP14	I/O	**General Purpose Input/Output** These pins serve as general purpose input/output lines with interrupt input capability.

1.6 Pin Description (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
Power Supply			
10	V_{SS}	I	**Ground** (common to V_{DD} and V_{DDP})
28	V_{SS}	I	
41	V_{SS}	I	
54	V_{SS}	I	
62	V_{SS}	I	
70	V_{SS}	I	
80	V_{SS}	I	
88	V_{SS}	I	
96	V_{SS}	I	
104	V_{SS}	I	
118	V_{SS}	I	
130	V_{SS}	I	
9	V_{DD}	I	**Positive power supply voltage** (3.0 - 3.6 V)
27	V_{DD}	I	
40	V_{DD}	I	
53	V_{DD}	I	
61	V_{DD}	I	
69	V_{DD}	I	
79	V_{DD}	I	
87	V_{DD}	I	
95	V_{DD}	I	
103	V_{DD}	I	
117	V_{DD}	I	
129	V_{DD}	I	
36	V_{DDP}	I	**Positive power supply voltage** (4.5 - 5.5 V)
112	V_{DDP}	I	
134	V_{SSA}	I	**Separate analog ground** (0 V) for Clock Generation Unit.
131	V_{DDA}	I	**Separate analog positive power supply voltage** (3.0 - 3.6 V) for Clock Generation Unit.

1.6 Pin Description (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
138	V_{SSAP}	I	**Separate analog ground** (0 V) for PLL.
137	V_{DDAP}	I	**Separate analog positive power supply voltage** (3.0 - 3.6 V) PLL.

Reserved Pins

15 16 17 18 19 20 21 22 42 43 44 144	res.		**Reserved** These pins are reserved for further use. They must be connected to VDD.
34 35 37 38 39 45 46 105 106 107 108	n.c.		**Not Connected** These pins are not used and may be left not connected.

2 Functional Description

2.1 General Functions

Figure 12 depicts the detailed functional architecture of the ISAR 34 V2.1:

- One modem/fax engine for V.34bis (33600 bit/s), V.17 (14400 bit/s), including fallback modes
- Upgradeable to new modem standards due to flexible firmware download capability
- DTMF receiver / transmitter in two channels
- V.110 formatter in two channels (except during datamodem modulation)
- Two universal formatters SART (Synchronous Asynchronous Receiver Transmitter) supporting ASYNC (ITU-T V.14), HDLC and binary modes
- D-channel HDLC controller
- C/I and MONITOR channel handler
- IOM-2 interface for terminal or line-card applications with TIC bus support
- Serial audio interface for analog modem codecs (e.g. ALIS)
- External memory interface for program and data memory
- Communications Mailbox with 253 bytes per direction

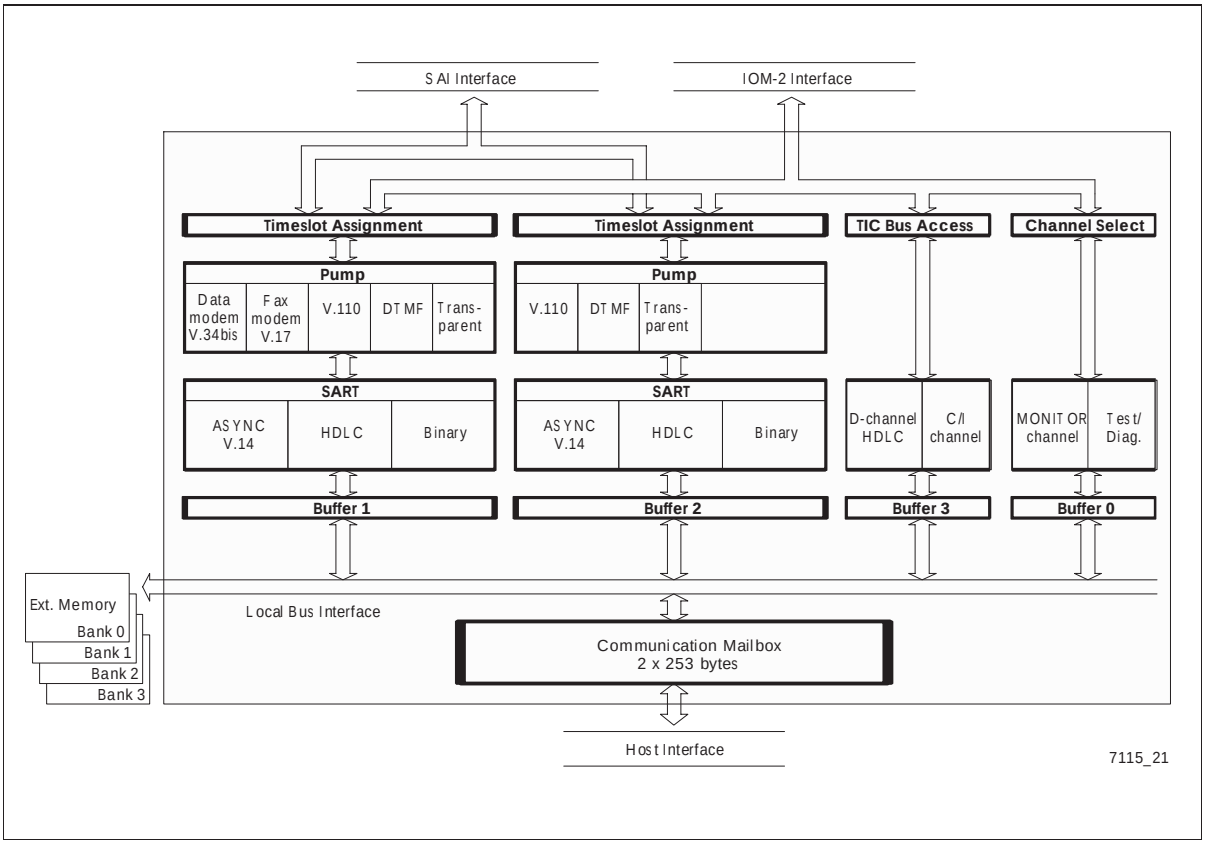


Figure 12
Functional Block Diagram of the ISDN Data Access Controller

2.2 Clock Generation

The chip internal clocks are derived from a crystal connected across XTAL1 and XTAL2 or from an external clock input via pin XTAL1.

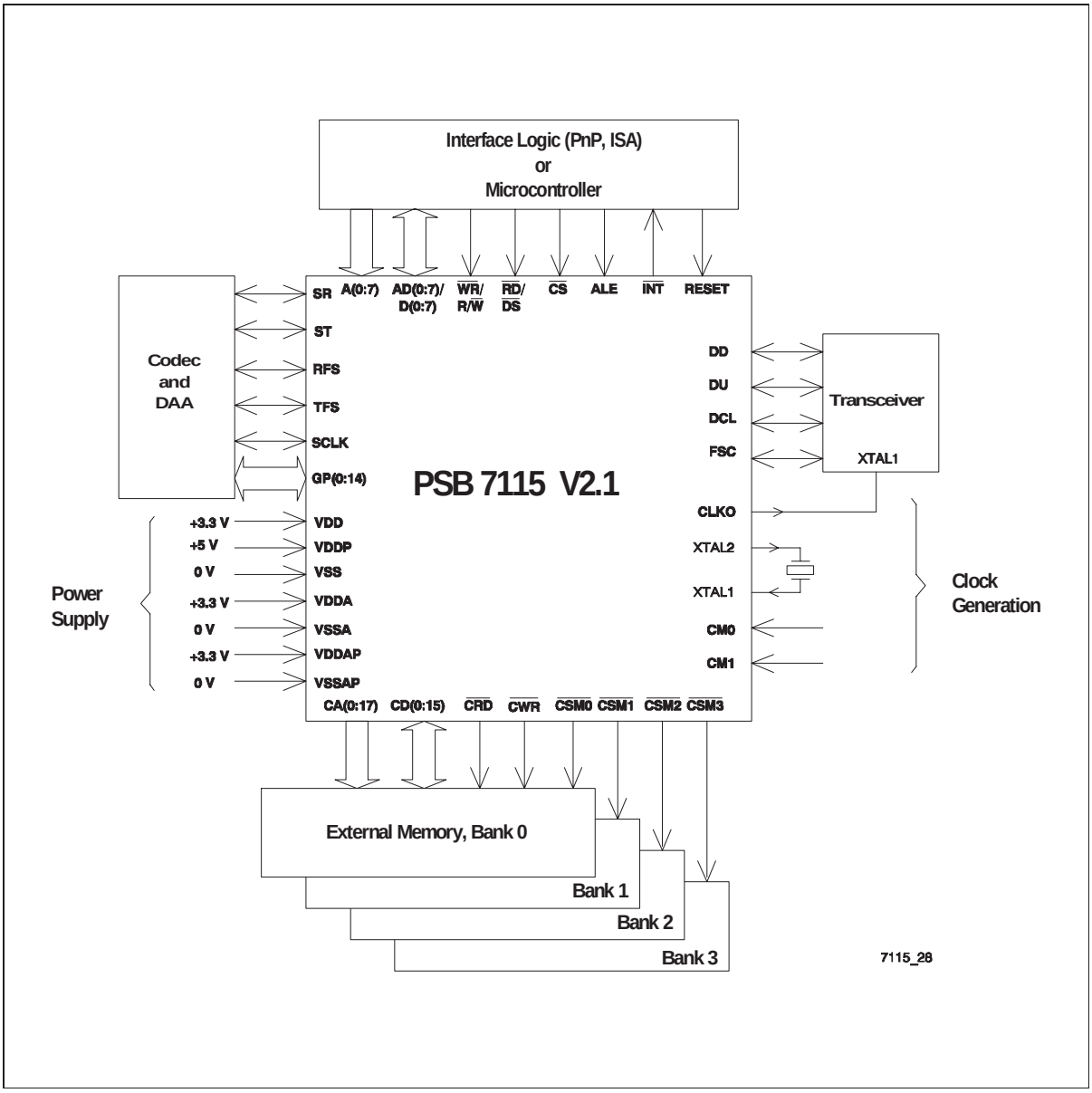


Figure 13
Clock Generation

One of four options can be used for the generation of the internal DSP master clock which is used for the fax/modem pump for example. Other functional blocks derive their clock signal directly from the IOM-2 interface.

An internal PLL derives the DSP clock from a 7.68 MHz, 15.36 MHz or 16.384 MHz source at XTAL1 (see **table 1**). In test mode the internal PLL is bypassed and the DSP clock is directly provided at XTAL1 .

Table 1
Clock Mode Settings

CM1	CM0	Clock at XTAL1	Comment
0	0	DSP clock	Test mode (PLL bypassed)
0	1	7.68 MHz	S-terminal applications
1	0	15.36 MHz	U-terminal applications
1	1	16.384 MHz	Analog modem applications (ALIS)

At CLKO a buffered output clock equal to the input clock at XTAL1 is provided. This allows for hardware designs that only require one crystal for two or more devices on the system.

The 7.68 MHz crystal is commonly used in terminal equipment with S-interface, e.g. the ISAR 34 together with the S-transceiver SBCX PEB 2081. One crystal is connected to the ISAR 34 and CLKO is connected to the XTAL1 input of the SBCX.

For U-terminals a 15.36 MHz crystal is provided at the ISAR 34 and in the same way the U-transceiver IEC-Q TE PSB 21910 derives its input clock from CLKO.

In analog modem applications with the ALIS a 16.384 MHz crystal provides the common clock for ISAR 34 and ALIS.

2.3 Physical Interfaces

The ISAR 34 provides five physical interfaces which are described in the follwing chapters:

- Host Interface
- IOM-2 Interface
- Serial Audio Interface (SAI)
- External Memory Interface
- General Purpose I/O Interface

2.3.1 Host Interface

The ISAR 34 is programmed via an 8-bit parallel host interface **(table 2**) that can be operated in multiplexed or non-multiplexed bus mode.

Table 2
Host Interface Signals

Symbol	Input (I) Output (O)	Function
AD(0:7)	I/O	**Address/Data Bus (multiplexed mode)** Transfers addresses and data between the host and the ISAR 34.
D(0:7)		**Data Bus (non-multiplexed mode)** Transfers data between the host and the ISAR 34.
A(0:7)	I	**Address Bus (non-multiplexed mode)** Input address to the ISAR 34 registers.
$\overline{RD}$	I	**Read (Siemens/Intel bus mode)** This signal indicates a read operation.
$\overline{DS}$		**Data Strobe (Motorola bus mode)** The rising edge marks the end of a valid read or write operation.
$\overline{WR}$	I	**Write (Siemens/Intel bus mode)** This signal indicates a write operation.
R/$\overline{W}$		**Read/Write (Motorola bus mode)** A "1" identifies a valid host access as a read operation and a "0" identifies it as a write operation.
$\overline{CS}$	I	**Chip Select** A "0" on this line selects the ISAR 34 for a read/write operation.

Table 2
Host Interface Signals

Symbol	Input (I) Output (O)	Function
ALE	I	**Address Latch Enable** A “1” on this line indicates an address on AD (0:7), that is latched by the ISAR 34 (multiplexed mode only). ALE also selects the interface mode (multiplexed or non-multiplexed).
$\overline{\text{INT}}$	O (OD)	**Interrupt Request** This is the interrupt output line to the host for all mailbox interrupt status requests. It is an open drain output.

The ISAR 34 provides three types of µP buses, which are selected via pin ALE:

Table 3
Bus Operation Modes

1	ALE tied to V_{DD}	**Motorola** type with control signals **$\overline{\text{CS}}$, R/$\overline{\text{W}}$, $\overline{\text{DS}}$**
2	ALE tied to V_{SS}	**Siemens/Intel non-multiplexed** bus type with control signals **$\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$**
3	Edge on ALE	**Siemens/Intel multiplexed** address/data bus type with control signals **$\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$, ALE**

The occurrence of an edge on ALE, either positive or negative, at any time during the operation immediately selects the interface type 3. A return to one of the other interface types is possible only if a hardware reset is issued.

Note: If the multiplexed address/data bus type 3 is selected, the unused address pins A0-A7 must be tied to V_{DD} or V_{SS}.

Since the mailbox structure of the ISAR 34 just requires 9 register locations, the host needs to decode only 4 address bits in non-multiplexed bus mode while the other address pins are strapped to ’0’. If the Software Reset (bit RST) is not required only 3 address bits need to be decoded (address 00H-07h).

All remaining address locations should not be accessed by the host. Test registers are located in the address range F0h-F7h and the remaining address locations (09h-EFh and F8h-FFh) are reserved for further use.

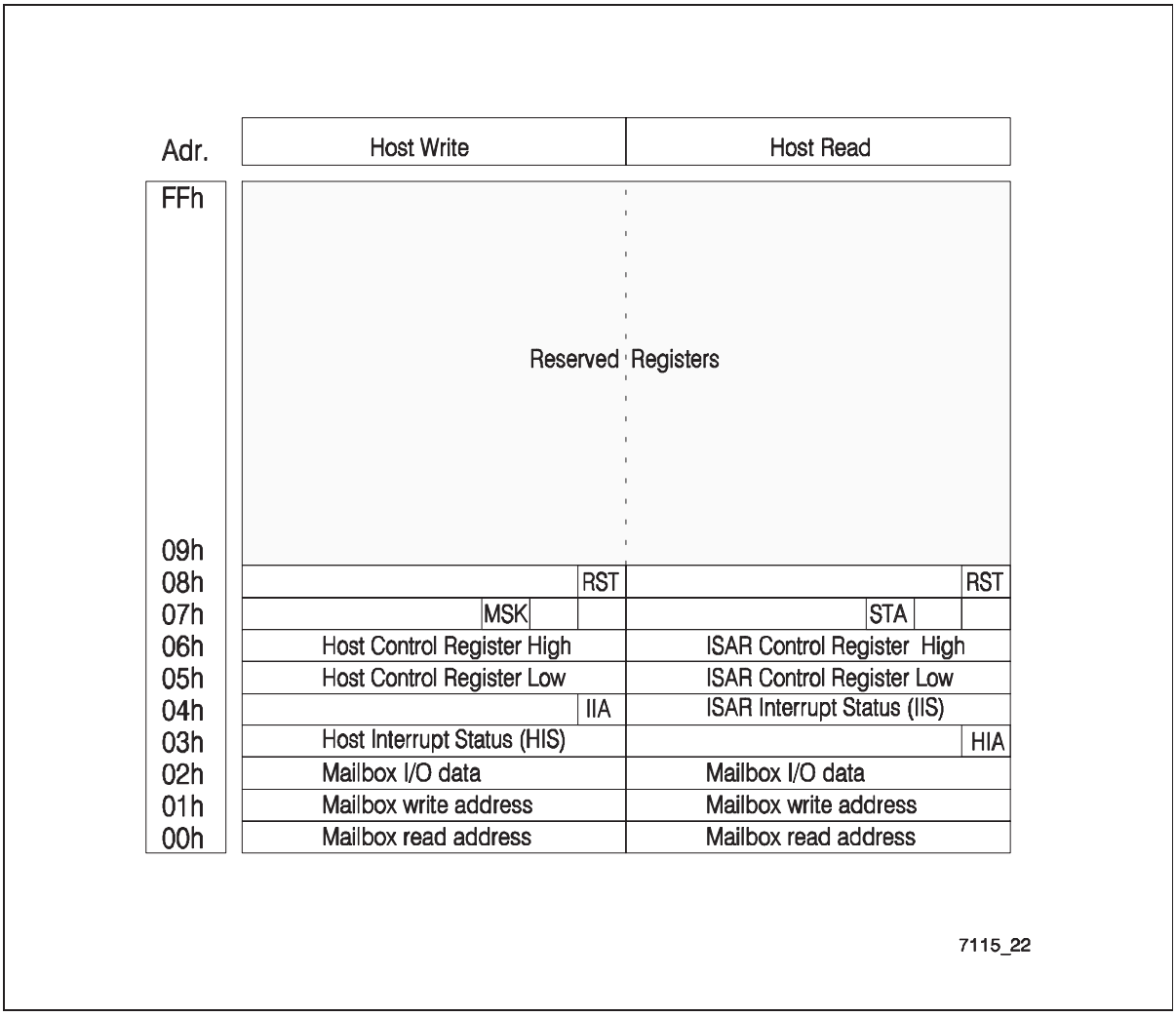


Figure 14
Register Access in Multiplexed and Non-Multiplexed Mode

Note: The address mapping is identical for multiplexed and non-multiplexed address mode.

2.3.2 IOM®-2 Interface

The IOM-2 interface is a 4-wire interface with two data lines (DU and DD), a data clock (DCL) and a frame sync signal (FSC), of which the rising edge indicates the start of an IOM-2 frame (8 kHz). For IOM-2 applications the data clock is typically set to twice the data rate.

IOM®-2 Driver

The output driver of the DD and DU pins is selectable, open drain (default) or push pull. The output drivers are active for the selected time-slot bits and remain tri-state during the rest of the frame.

The control lines FSC and DCL are input or output.

IOM®-2 Frame Structure/Timing Modes

The ISAR 34 supports the IOM-2 terminal and line-card mode.
In terminal mode, the three channel IOM-2 structure is used (see **figure 16**). In line-card mode (see **figure 15**), eight IOM-2 channels can be programmed with flexible time-slot assignment of the B-channel data.

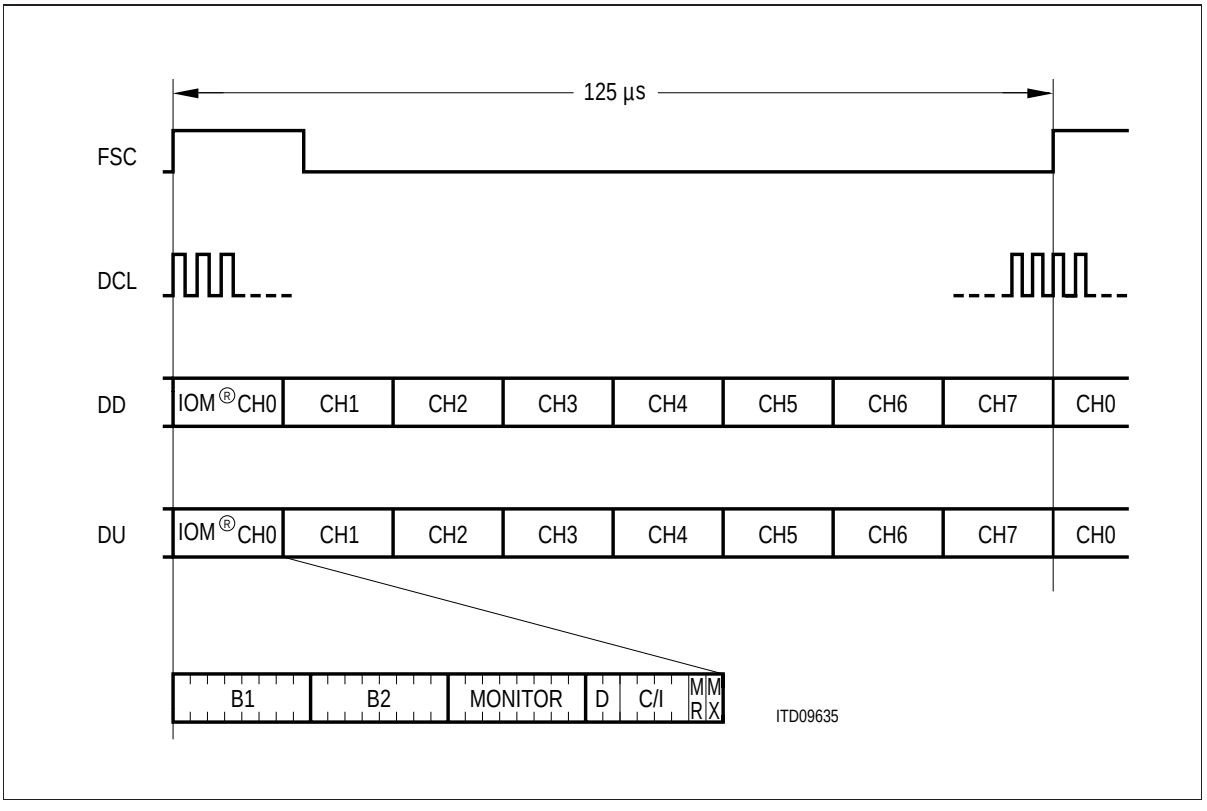


Figure 15
Linecard Mode of the IOM-2 Interface

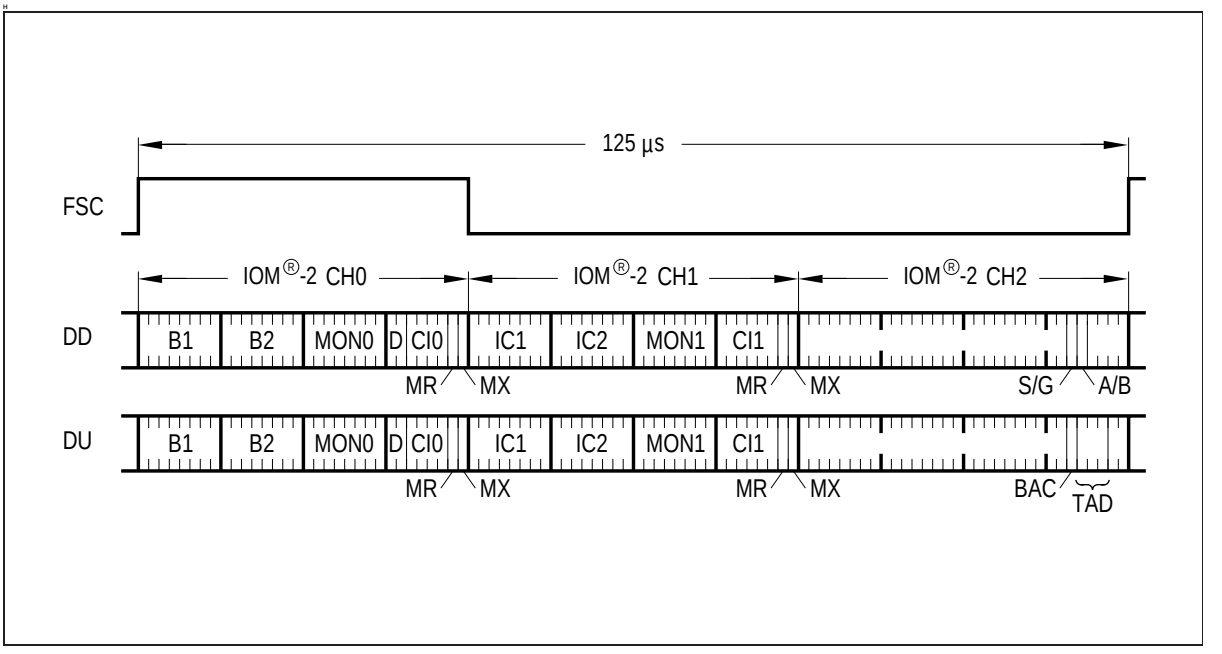


Figure 16
Terminal mode of the IOM-2 Interface

The ISAR 34 is able to make extensive use of the IOM-2 channels as it is able to access all user data timeslots by programming the timeslot number and bit shift.
The MONITOR channel is used for information exchange between the ISAR 34 and other devices connected to the IOM-2 interface. In the C/I-channel real time status information is exchanged between the devices. Both types of information transfer is supported by the ISAR 34 which provides a MONITOR and C/I-channel handler.

In TE mode the TIC bus capability is implemented in the last octett of the third IOM-2 channel (channel 2). This abritration mechanism which allows the access of up to seven D-channel sources on the IOM-2 interface, is implemented on the ISAR 34.

For detailed information refer to the “IOM-2 Interface Reference Guide”.

2.3.3 SAI Interface

The Serial Audio Interface (SAI) is a generic 5-line serial interface with the following signals:

SCLK (I/O)	Serial bit clock Bits on SR/ST are clocked out with the rising or falling edge of SCLK and clocked in with the falling or rising edge of SCLK (programmable).
SR (I/O)	Serial Data Receive By default data is received on SR, optionally SR can be programmed as output.
ST (I/O)	Serial Data Transmit By default data is transmitted on ST, optionally ST can be programmed as input.
RFS (I/O)	Receive Frame Sync Marks the beginning of a physical frame on SR.
TFS (I/O)	Transmit Frame Sync Marks the beginning of a physical frame on ST.

The SAI enables the ISAR 34 direct connection to analog modem codecs and DAAs. It is especially suitable to interface to the Siemens Analog Line Interface Solution ALIS PSB 4595/96.

Further control functions such like ring detect and hook switch are realized by the general purpose control lines.

2.3.4 External Memory Interface

The ISAR 34 provides a flexible memory interface that fulfils the requirements for different applications. External memory is required for operational data and the DSP program.

Operational data is stored in external SRAM whereas the storage of the DSP program code depends on the application. For PC based applications (e.g. plug in card) it can be downloaded into external SRAM, whereas for standalone systems (e.g. settop box) it is stored in non-volatile memory (e.g. flash), so no program download is necessary.

In total four memory banks with an address range of 256Kx16 each can be addressed, however the specific memory configuration depends on the application.

DSP Program Download

For applications where the DSP program is downloaded from the host to the external memory of the ISAR 34 (e.g. PC cards) two different memory configurations are possible, which may ease the availability of certain SRAM devices.

In the first configuration one memory bank of 128Kx16, 15 ns is connected to $\overline{\text{CSM0}}$ (memory bank 0). For the second option one SRAM of 32Kx16, 15 ns is connected to $\overline{\text{CSM0}}$ (memory bank 0) and a slower SRAM of 64Kx16, 70 ns is connected to $\overline{\text{CSM1}}$ (memory bank 1)

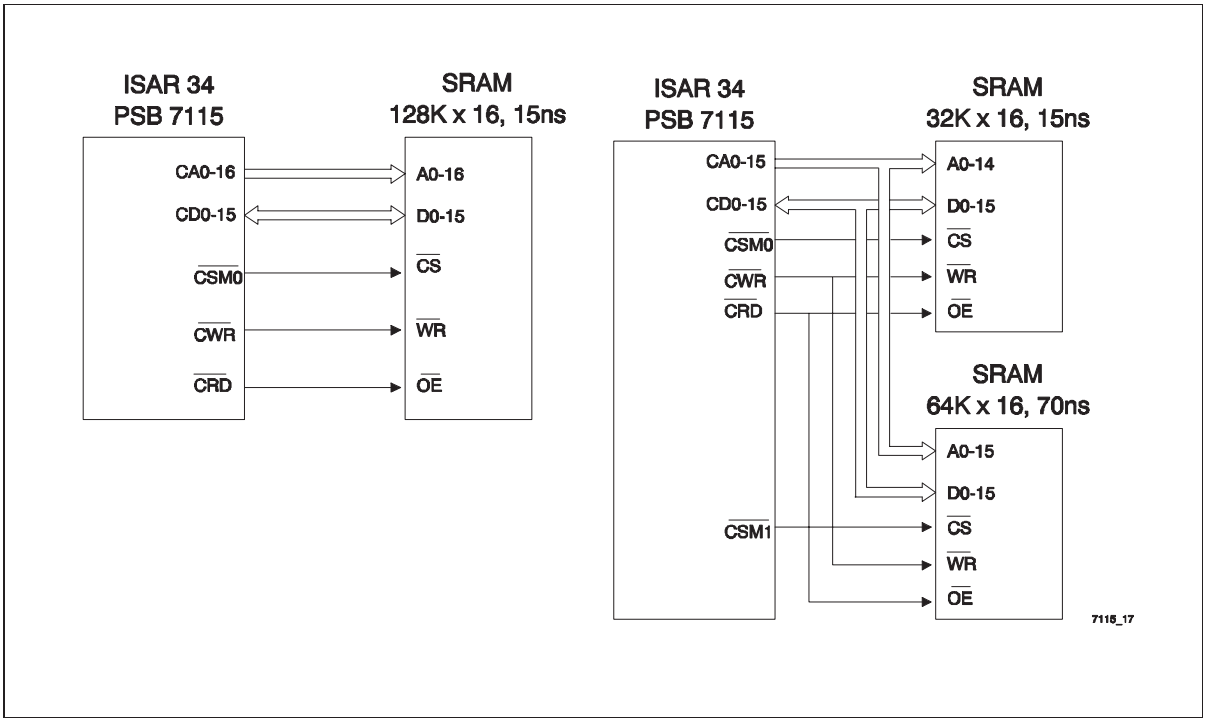


Figure 17
Memory Configuration - DSP Program Download

DSP Program in Non-volatile Memory

The DSP program can be kept in flash memory which allows for reprogramming of the DSP program through the ISAR 34.

One SRAM of 32Kx16, 15 ns is connected to $\overline{\text{CSM0}}$ (memory bank 0) and a slower flash memory of 128Kx16, 70 ns is connected to $\overline{\text{CSM1}}$ (memory bank 1).

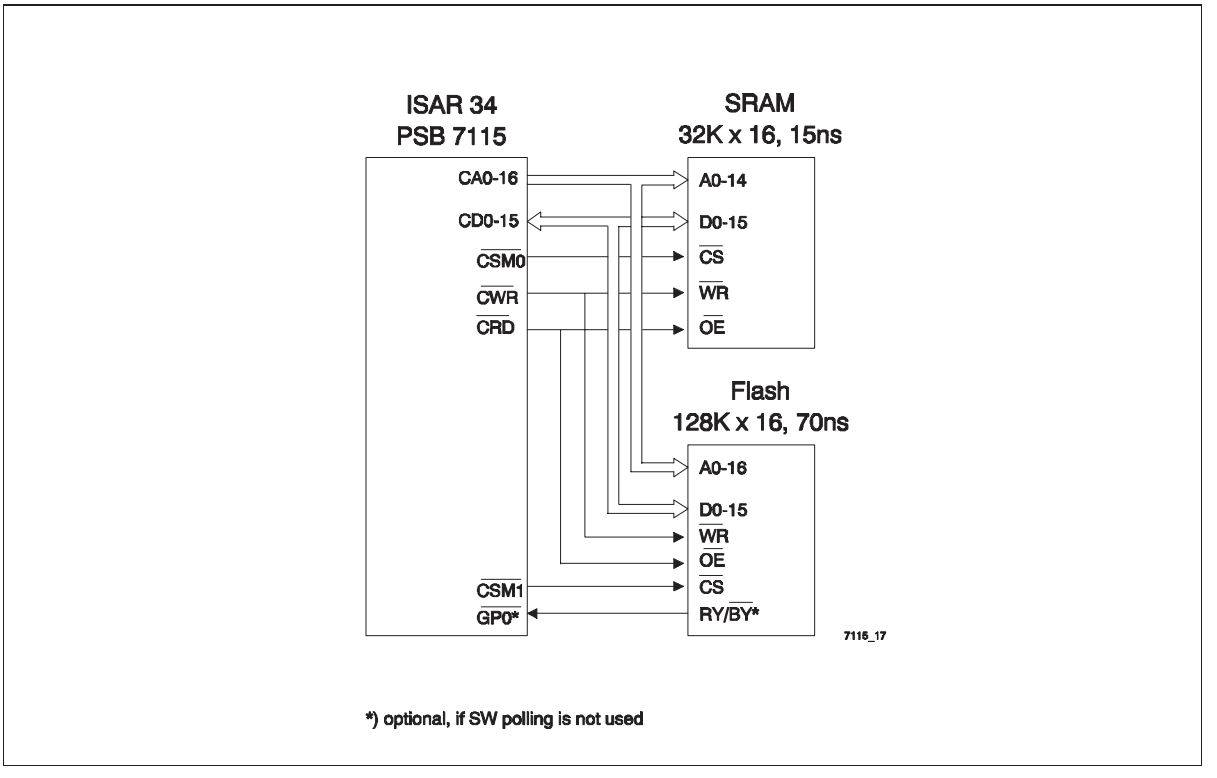


Figure 18
Memory Configuration - DSP Program in Flash

2.3.5 General Purpose I/O Interface

The ISAR 34 provides a general purpose I/O interface that fulfils the requirements for different applications. Each of the 14 pins can individually be programmed as inputs or as outputs. As inputs they can additionally generate an interrupt.

This interface can flexibly be used for general control functions or status indications from external devices. For example in modem applications hook switch and ring detect can be controlled via GP-pins.

2.4 Communications Interface

The ISAR 34 provides a communications interface in terms of a 253 byte mailbox per direction, a 16 bit control word and an 8 bit interrupt register.

Besides that, there is a reset bit (bit 0 of register 08h), an interrupt mask/status bit (bit 2 of register 07h) and two interrupt acknowledge bits (LSB of address location 04h and 03h, respectively).

The address map is shown in **figure 19**, all other address locations are not used.

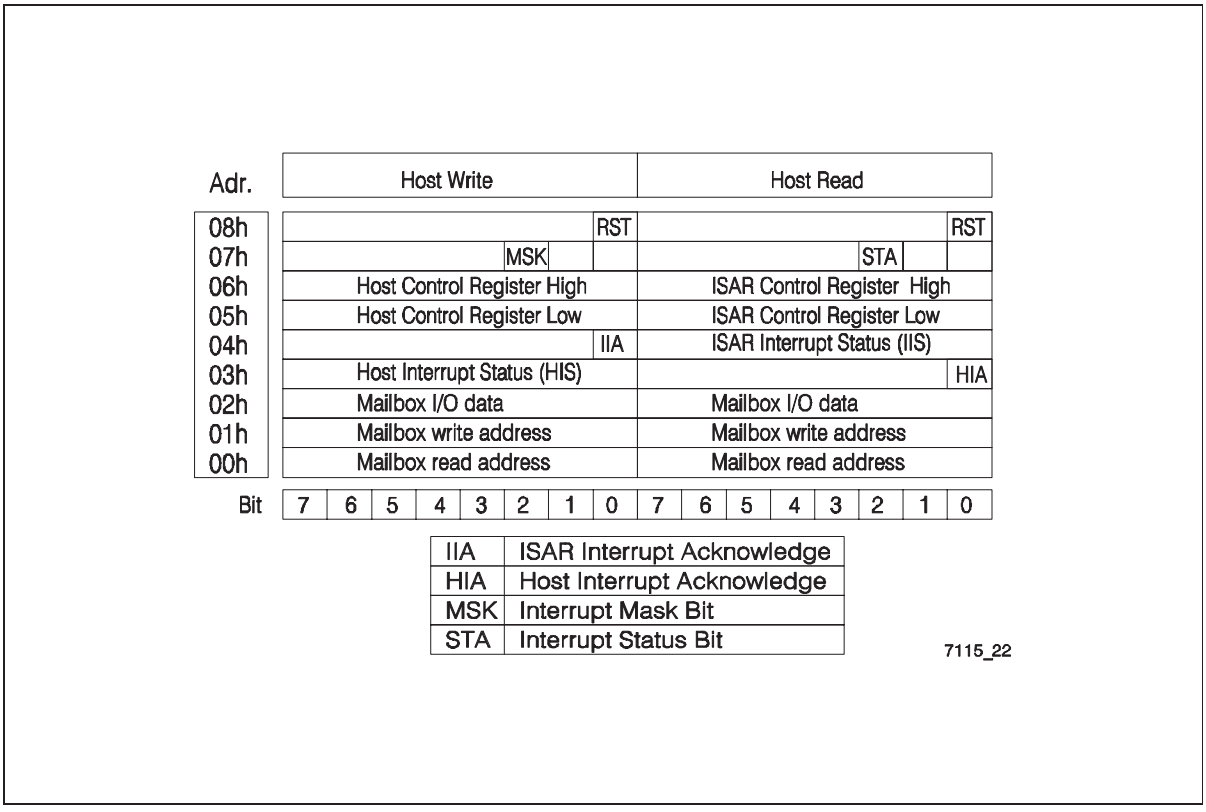


Figure 19
Host Interface Registers

Software Reset Bit (08h Write/Read)

The ISAR 34 is reset by setting and resetting this bit. It has a similar functionality as a hardware reset except this register itself is not affected and the RESET pin is not activated, i.e. the Software Reset has only effect to the internal functions of the ISAR 34.

Interrupt Mask/Status Bit (07h Write/Read)

All interrupt sources can be masked by setting the MSK-bit to ‘0’, so no interrupt is indicated to the host. The status STA-bit indicates whether an interrupt request is pending. If interrupt generation is disabled (MSK=0), requests from the ISAR 34 can be recognized by polling the STA-bit. After reset the interrupt is masked (MSK = 0), however, the mask bit affects only the generation of the interrupt, but not the interrupt status bit from being set.

Host/ISAR Control Registers

The most significant byte of the control register (CTRL MSB) contains configuration, status or control information depending on the type of message.
The least significant byte (CTRL LSB) is used to indicate the number of bytes transfered via the mailbox (Mailbox I/O Data). These mailbox data may contain additional configuration, status or control information as well as receive/transmit data.

Host/ISAR Interrupt Status Byte (HIS/IIS)

The interrupt status byte has a structure that defines the type of message, i.e. it contains information to which buffer the message is related to and to which functional block of the ISAR 34 the message is related to.

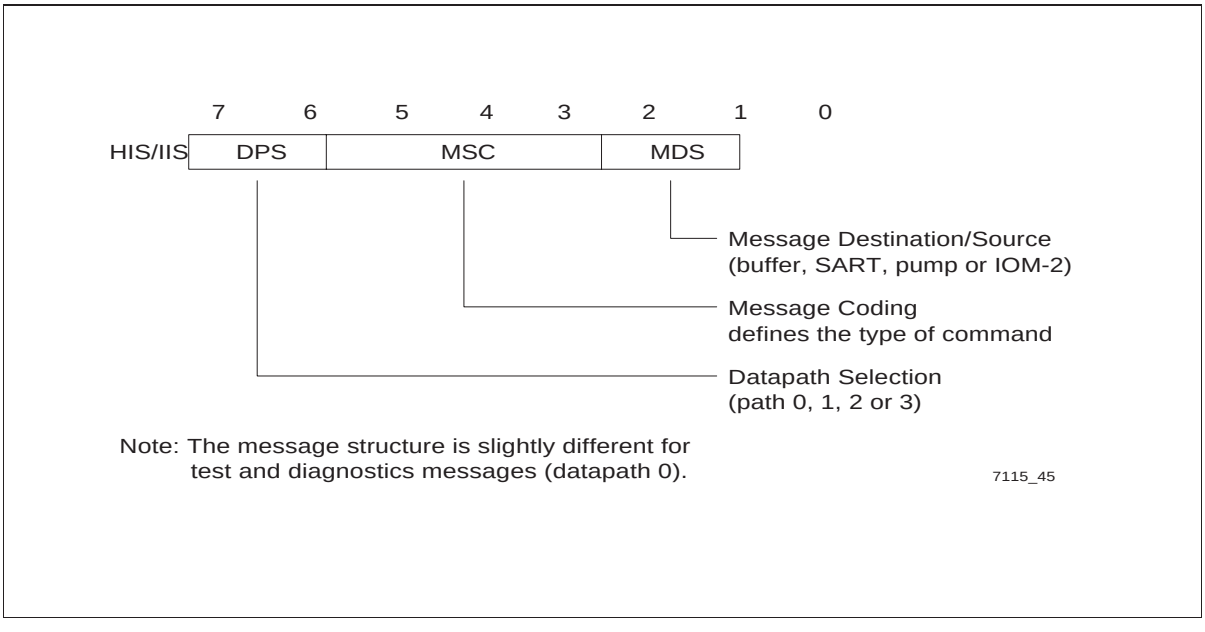


Figure 20
Structure of Interrupt Status Byte

Mailbox

The mailbox is implemented as physically two separate 253-byte memory blocks which is seen from the host as an I/O device. Thus, to read/write a byte from/to the Mailbox, the host accesses a single location (Mailbox I/O data), which is the same address but physically separate location for read and for write direction.

The address is given by an address register directly programmable by the host (Mailbox read/write address). This address is autoincremented every time an access by the host to Mailbox I/O data is performed. Thus, for sequential, fast access, the host only needs to set the start address for the first message byte and all subsequent data bytes can be read/written without reprogramming its address.

For random access to the Mailbox the Host has to reprogram the address register(s).

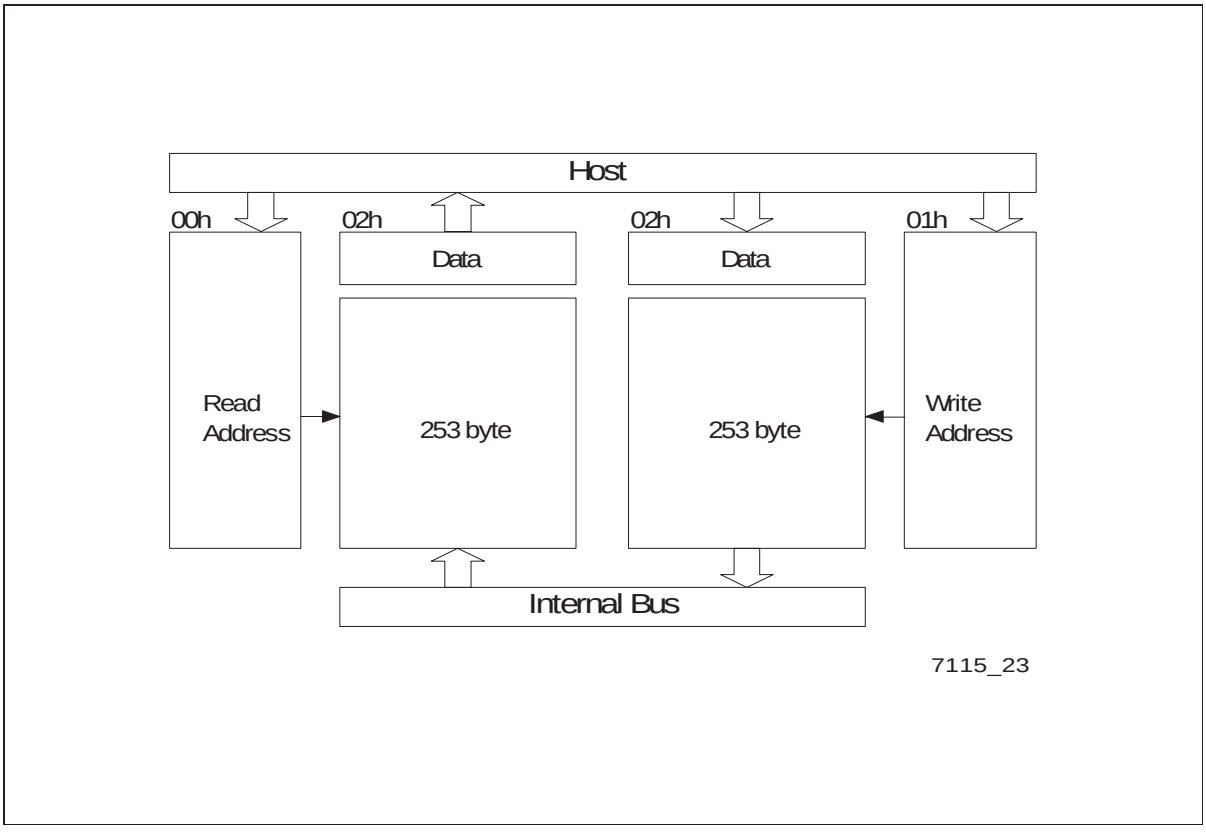


Figure 21
Mailbox Interface

2.5 Functional Blocks

The ISAR 34 host interface provides for merging/splitting of two data paths for B-channel data, one data path for D-channel data and C/I-channel access and a fourth data path for MONITOR channel data and exchange of test/diagnostics messages.

Each path is buffered both in read and write direction and the mailbox is used to access these four buffers.

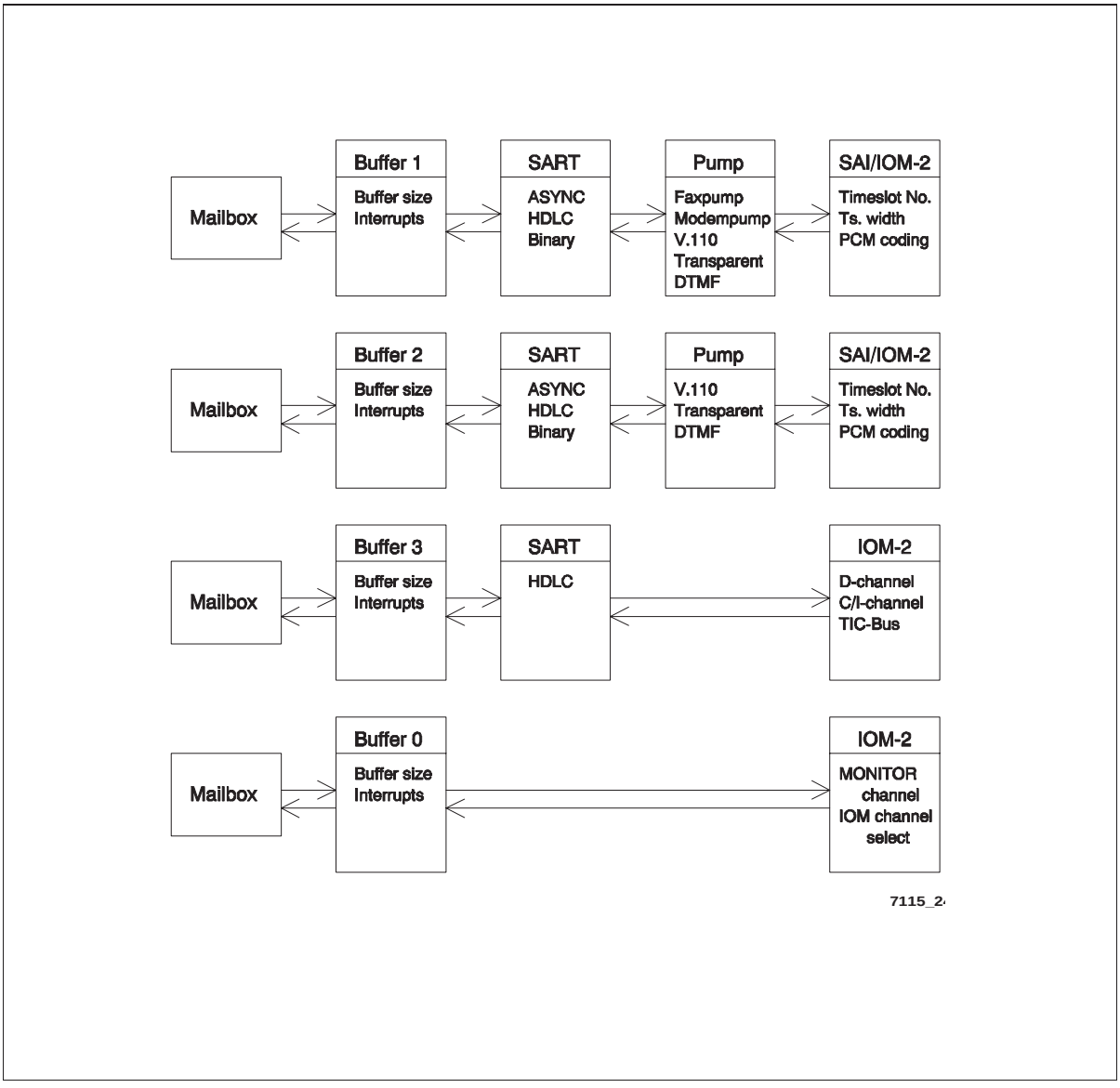


Figure 22
Communication Buffers

Path 1 is used to access the fax/modem engine, a V.110 formatter, a DTMF generator/ detector or for transparent access to the IOM-2 timeslots or the serial audio interface (SAI).

Path 2 is used to access a V.110 formatter, a DTMF generator/detector or it provides transparent access to the IOM-2 timeslots or the SAI. This datapath must not be configured to V.110 if path 1 is configured to datamodem modulations at the same time.

Path 1 and 2 integrate a SART (Synchronous Asynchronous Receiver Transmitter) which supports ASYNC, HDLC and binary mode. In ASYNC mode, the characters are formatted according to the ITU-T V.14 standard by start, parity and stop bits. In HDLC mode, the HDLC bit level functions (Flag, CRC, Zero-bit handling) are performed. Binary mode describes a synchronous, transparent mode without formatting.

Path 3 incorporates an HDLC controller for D-channel data transfer and handles the access to the C/I channel. The ISAR 34 supports the TIC bus arbitration mechanism for those applications where several controllers are connected to the IOM-2 interface.

Path 4 provides a MONITOR channel handler for information exchange with other devices. Messages for test and diagnostics purposes are also transfered via this datapath.

2.5.1 Buffer

The mailbox represents the common host interface for all data paths, which are the two B-Channel paths, the D- and C/I-channel path and the MONITOR channel and test/ diagnostics path. For each data path the read and write direction is buffered with a FIFO (see **figure 23**). These FIFO buffers reside in external memory.

The buffers size for each path is shown in **table 4**:

Table 4
Buffer size

	DPS	MPL
Datapath 0	0 0	61 byte
Datapath 1	0 1	253 byte
Datapath 2	1 0	253 byte
Datapath 3	1 1	253 byte

MPL denotes the maximum possible message length.

The complete buffer size for one data path is 2x256 or 2x64 bytes, respectively. Since the interrupt status byte and the control word is also transfered to the buffer by the ISAR 34, the maximum available message length is reduced by 3 bytes, i.e. MPL is 2x253 or 2x61 bytes.

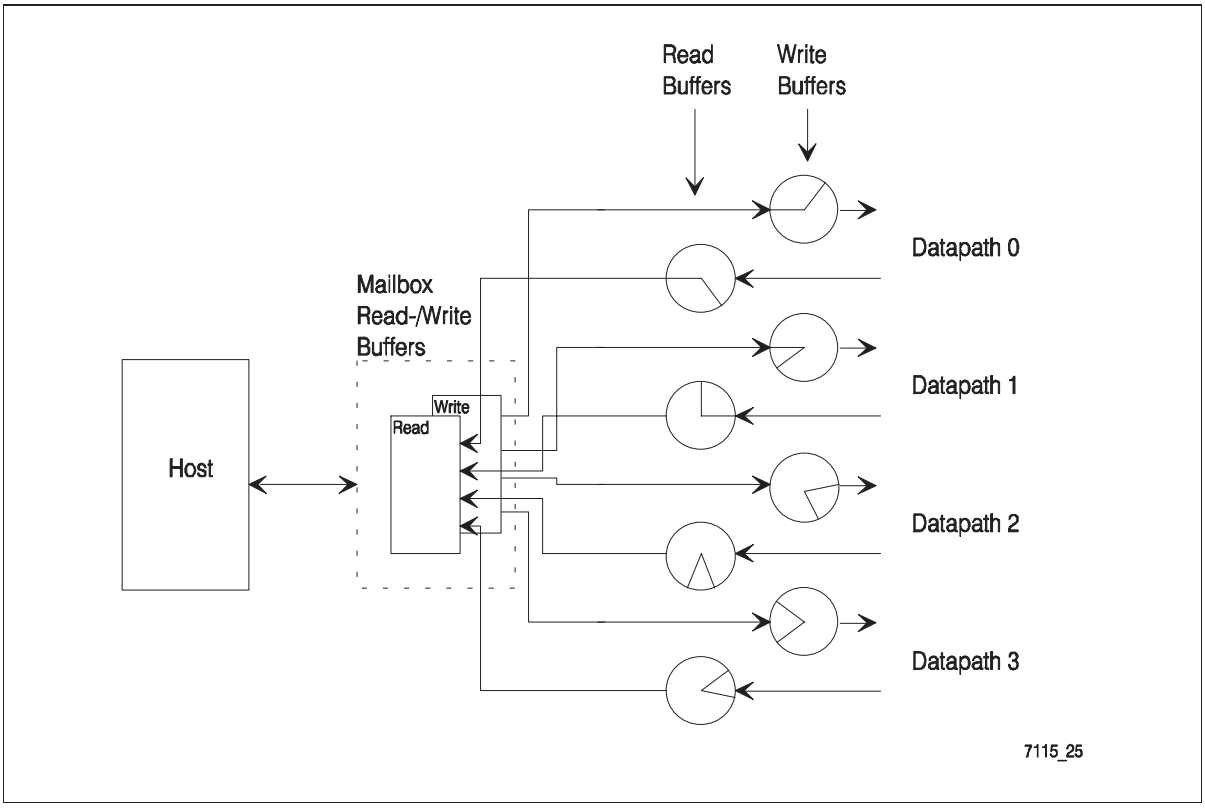


Figure 23
Structure of Datapath Buffers

Buffer Control

After the host has written a message to the write buffer, the ISAR 34 will issue a buffer available interrupt to the host if there is still enough free buffer space for another message of the programmed length (i.e. another message may be written to the mailbox). If the host enters messages into the mailbox which exceed the configured message length, the FIFO buffer may overflow and data might be lost.

If there is no free space available, the ISAR 34 won't issue a data request message.

The buffers can be set a priority to determine the sequence of service if several read buffers request for mailbox service simultaneously.

2.5.2 SART

The SART (Synchronous Asynchronous Receiver Transmitter) can be configured for ASYNC character formatting, HDLC bit level formatting and binary mode. i.e. no bit level formatting.

2.5.2.1 ASYNC Mode

ASYNC denotes an asynchronous formatting of data according to ITU-T specification V.14. In ASYNC mode, the SART adds start, parity and stop bits to each data byte. The following options are programmable:

Character Length:	6,7,8 Bit
No. of stop bits:	1,2
Parity:	No, odd, even, stick parity
Overspeed range:	12.5 or 25 % (stop bit deletion: 1 of 8, 1 of 4)

The ASYNC formatter supports overspeed handling according to V.14. Therefore a stop bit may be deleted according to the overspeed range.

The ASYNC formatter is able to generate a break signal and to detect a break signal of a minimum length of 2M+3 bits of start bit polarity.

A special option is included to generate V.42 detection timing.

2.5.2.2 HDLC Mode

In HDLC mode, the SART generates/handles the HDLC frame formatting. This includes opening and closing flag, CRC generation/detection and zero-bit insertion.

Programmable features are:

CRC:	16 Bit
Inter frame timefill:	'1' or flags
Bit stream coding:	regular, inverse
Data underrun operation:	Abort generation/frame end (CRC+flag) generation

In transmit direction a frame is started after SART data is available in the transmit FIFO buffer. The frame is continued until a frame end mark has been set in a mailbox command. In this case, the HDLC frame is closed by the CRC value and a closing flag. In case a buffer underrun occurs, the current HDLC frame is closed either by an abort sequence or by CRC and closing flag (programmable).

In receive direction, HDLC frames exceeding the programmed message length are transferred to/from the buffer in data blocks of the configured message length. A message of reduced length may be transferred if a frame start, frame end or error condition is detected. In this case the control word contains the result of the CRC check, verification of integer number of bytes and check of frame end condition.

2.5.2.3 Binary Mode

In binary mode no character formatting is performed. Octets are transferred with the least significant bit or most significant bit transferred first.

Programmable Features are:

Idle character on data underrun
Bit swapping (LSB/MSB first)

In transmit direction, data from the transmit buffer is transmitted with the LSB or MSB first. In case of data underrun, i.e. if there's no more data in the transmit buffer, a programmable byte or the last data byte is continuously transmitted.

In receive direction, the data stream is received in octets. Their contents is transferred to the receive buffer .

2.5.3 Pump

Pump in general describes the additional formatting of the SART data which is then forwarded to the IOM-2 interface.

The pump options are:

- Fax modulations
- Datamodem modulations
- Halfduplex modulations
- V.110
- DTMF
- Bypass (transparent data)

All pump modes are available in path 1, path 2 only supports V.110, DTMF and bypass mode.

V.110 operation in data path 2 is not supported to run in parallel with datamodem modulations (full duplex modulations) in data path 1.

2.5.3.1 Fax Modulations

The mode fax modulations allows modulation up to V.17 (14400 bit/s).

Programmable parameters are:

- Enabling/disabling of answer/calling tone
- Transmitter output attenuation
- Modulation scheme (V.17, V.29, V.27ter, V.21 channel 2) set by control commands

2.5.3.2 Datamodem Modulations

The mode datamodem modulations allows modulation up to V.34bis (33600 bit/s).

Programmable parameters are:

- Enabling/disabling of answer/calling tone
- Transmitter output attenuation
- Automode (EIA/TIA PN-2330) or dedicated mode
- V.8 signalling
- Modulation options according to the ITU recommendations (fallback rates, retrain, renegotiate, etc.)
- Call progress tone detection

2.5.3.3 Halfduplex Modulations

The halfduplex modulations allow modulation up to V.17 (14400 bit/s).

Programmable parameters are:

- Enabling/disabling of receive/transmit direction
- Enabling/disabling of echo protector tone
- Transmitter output attenuation
- Modulation scheme (V.17, V.29, V.27ter, V.21)

2.5.3.4 V.110

The V.110 mode allows the framing of SART data for bit rate adaptation according to the ITU-T recommendation V.110.

The programmable features are:

- Frame format/data rate
- E-, X-, S-bit control
- Transmitter flow control (X-bits)
- Remote DTE status detection
- Delay of synchronisation

In transmit direction, the V.110 frame is combined with SART data and the state of E-, X- and S-bits. Transmission of the last data byte in the mailbox is indicated to the host (buffer empty condition), which may set control bits.

Flow control by means of the X-bits is supported, which means that data transfer to the SART unit is stopped if indicated by the remote side.

In receive direction, frame synchronization is monitored while the number of frames for synchronisation (normally 1) is programmable. The D-bits are forwarded to the SART and E-, X- and S- bits are forwarded to the host as status events any time they change their state.

Status conditions of the remote DTE can be detected and indicated to the host.

2.5.3.5 DTMF

The ISAR 34 supports DTMF generation/detection in two channels.

DTMF mode allows transparent data transfer between SART unit and data pump while a DTMF detector is active, which indicates received DTMF tones to the host.

The ISAR 34 supports DTMF tone generation to the programmed SAI or IOM-2 timeslots.

2.5.3.6 Bypass Mode

The bypass mode allows the transparent transfer of a SART formatted digital data stream to the SAI or IOM-2 timeslot without additional data formatting by the pump.

In receive direction, data from the IOM-2 timeslot is directly transfered to the SART.

2.5.4 IOM®-2 Configuration

The IOM-2 configurations are separate for each datapath. Via datapath 1 and 2, any timeslot for the output of pump data can be selected.

The following programmable functions are available for path 1 and 2:

- Start of timeslot
- Length of timeslot (8 or 16 bit)
- Switching of DU/DD lines
- Coding (A-law, µ-law or 16-bit linear)

Datapath 3 is dedicated to the D-channel and the C/I channel timeslot, respectively. The TIC bus access handler which is used in terminal timing mode is operating on the TIC bus channel (3rd channel) on IOM-2.

For the MONITOR channel handler in datapath 0 one of 16 IOM-2 channels can be selected. The access is fixed to the third timeslot (MONITOR channel) of this channel.

2.5.5 SAI Configuration

The serial audio interface is dedicated to interface with analog codecs and DAAs. The ISAR 34 handles the transfer of data from the data pump to/from the SAI, the difference is, that only B-channel data (datapath 1 and 2) can be transfered from/to the SAI and not data from datapath 0 and 3 (D-channel, MONITOR channel, C/I-channel).

The configuration of the SAI depends on the specific application (e.g. analog modem with Siemens ALIS).