SIEMENS

ICs for Communications

Digital Answering Machine with Full Duplex Speakerphone

SAM EC

PSB 4860 Version 2.1

Target Specification 03.97

T4860-XV21-S1-7600

PSB 4860 **Revision History:** **Current Version: Version 2.1**		
Previous Version: Target Specification 08.96 (V1.0)		
Page (in previous Version)	Page (in new Version)	Subjects (major changes since last revision)
Hardware Changes		
		Specification of PSB 4851 deleted (now separate document)
		TM (Test Mode) pin removed
		Maximum frequency on SSDI interface now 10 MHz (formerly 5 MHz)
		Weak pulldown during reset on MA_0-MA_{15} added
		Configurable weak pullup on memory control signals added
		Hardware configuration registers 2 and 3 added
		Status register output on SPS_0/SPS_1 added
		Support for 8M, 16M and 32M flash memory (SAMSUNG) added
		Support for flash memory polling removed
		Operating frequency now 31.104 MHz (formerly 34.56 MHz)
		Crystal specification relaxed
		Supply voltage range now 3.0 V-3.6 V (formerly 3.15 V-3.46 V)
Software Changes		
		HQ data rate now 10.3 kbit/s (formerly 9.9 kbit/s)
		Compress file command added
		Activate command enhanced (memory corruption detection)
		Memory granularity now 8 kB (formerly 1 kB)
		User data word now 12 bit (formerly 15 bit)
		Restriction on phrase length removed (formerly 32 audio units)
		Equalizer module added
		Line echo canceller module added
		Second universal attenuator module removed
		AGC module separated from coder and decoder module
		DTMF/CNG detection module separated into independent modules
		Alert tone detection module separated from DTMF detection module
		Restrictions on module interconnect removed
		Status register format changed (DTC field moved to separate register)
		Status register bit SD redefined (formerly NSD)
		Status register bit ATV added
		Addresses for read/write registers added
		Exact formulas for parameters given (formerly tabular data)

Edition 03.97

This edition was realized using the software system FrameMaker®.

Published by Siemens AG,
HL TS

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1 Overview

Combined with an analog frontend (PSB 4851) the PSB 4860 provides a solution for embedded or stand alone answering machine applications. Together with a standard microcontroller for analog telephones these two chips form the core of a featurephone with full duplex speakerphone and answering machine capabilities.

The chip features two compression modes (high quality and long play), message playback at variable rates, full duplex speakerphone operation, a caller ID decoder, DTMF recognition and generation and call progress tone detection.

Messages and user data can be stored in ARAM/DRAM or flash memory which can be directly connected to the PSB 4860. The PSB 4860 also supports a voice prompt EPROM for fixed announcements.

The PSB 4860 provides an IOM®-2 compatible interface with two channels for speech data.

Alternatively to the IOM®-2 compatible interface the PSB 4860 supports a simple serial data interface with separate strobe signals for each direction (linear PCM data, one channel).

A separate interface is used for a glueless connection to the PSB 4851.

The chip is programmed by a simple four wire serial control interface and caninform the microcontroller of new events by an interrupt signal. For data retention the PSB 4860 supports a power down mode where only the real time clock and the memory refresh (in case of ARAM/DRAM) are operational.

The PSB 4860 supports interface pins to +5 V levels.

SIEMENS

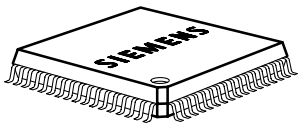
Digital Answering Machine with Full Duplex Speakerphone SAM EC

PSB 4860

Version 2.1

CMOS

1.1 Features



P-MQFP-80

Digital Functions

- Selectable compression rate (3.3 kbit/s, 10.3 kbit/s)
- Variable playback speed
- Support for ARAM or Flash Memory
- Optional voice prompt EPROM
- Full duplex speakerphone
- DTMF generation and detection
- Call progress tone detection
- Caller ID recognition
- Direct memory access
- Real time clock
- Equalizer
- Automatic timestamp
- Auxiliary parallel port
- Ultra low power refresh mode

General Features

- SSDI/IOM®-2 compatible interface
- Serial control interface for programming

Type	Ordering Code	Package
PSB 4860		P-MQFP-80

1.2 Pin Configuration
(top view)

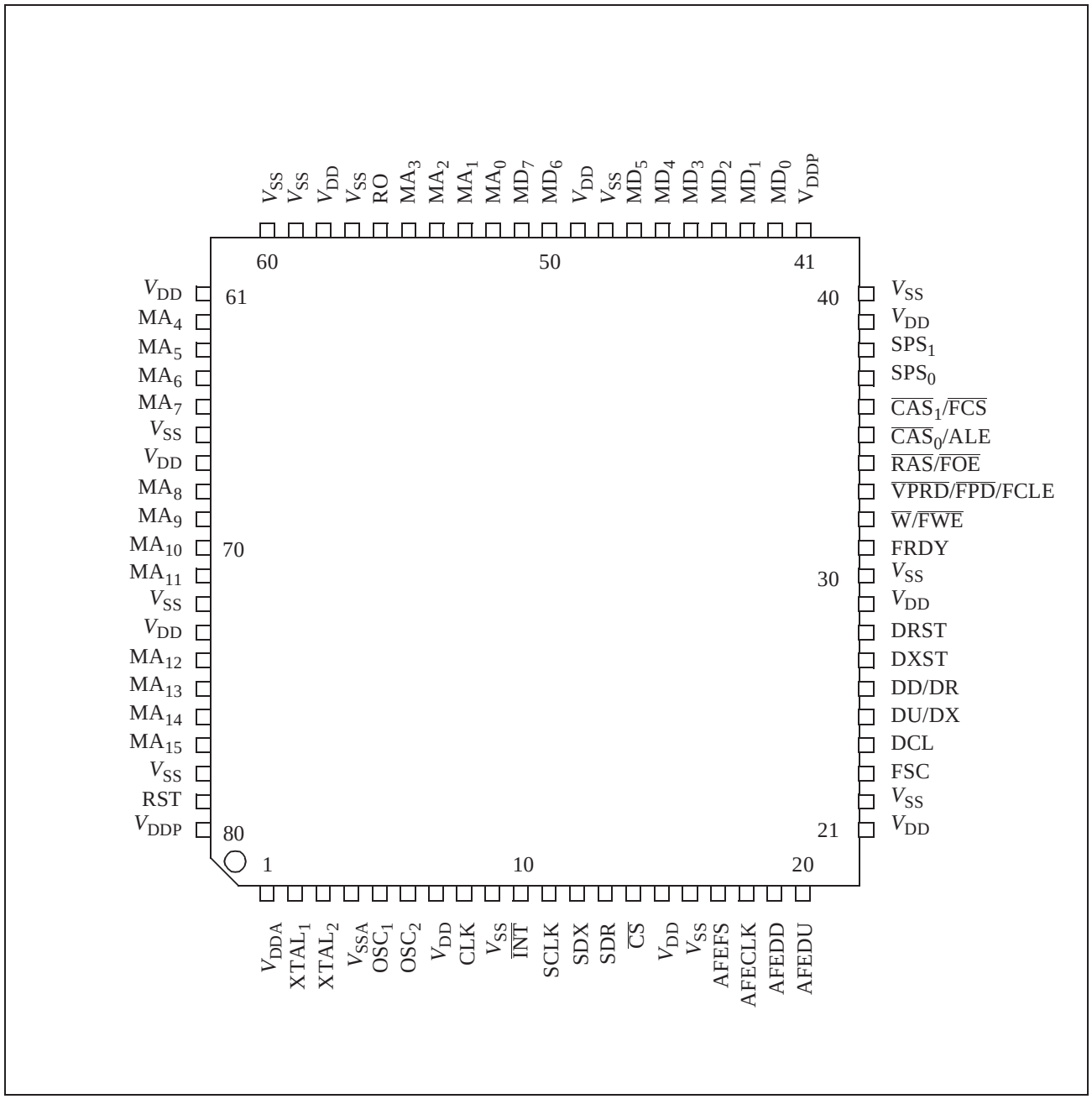


Figure 1
Pin Configuration of PSB 4860

1.3 Pin Definitions and Functions

Pin No. P-MQFP-80	Symbol	Dir.	Reset	Function
41, 80	V_{DDP}	-	-	**Power supply (5V ±10 %)** Power supply for the interface.
7, 15, 21, 29, 39, 49, 58, 61, 67, 73	V_{DD}	-	-	**Power supply (3.0 V - 3.6 V**) Power supply for logic.
1	V_{DDA}	-	-	**Power supply (3.0 V - 3.6 V)** Power supply for clock generator.
4	V_{SSA}	-	-	**Power supply (0 V)** Power supply for clock generator.
9, 16, 22, 30, 40, 48, 57, 59, 60, 78, 66, 72	V_{SS}	-	-	**Power supply (0 V)** Ground for logic and interface.
17	AFEFS	O	L	**Analog Frontend Frame Sync:** 8 kHz frame synchronization signal for the analog front end.
18	AFECLK	O	L	**Analog Frontend Clock:** Clock signal for the analog front end.
19	AFEDD	O	L	**Analog Frontend Data Downstream:** Data output to the analog frontend.
20	AFEDU	I	-	**Analog Frontend Data Upstream:** Data input from the analog frontend.
79	RST	I	-	**Reset:** Active high reset signal.
23	FSC	I	-	**Data Frame Synchronization:** 8 kHz frame synchronization signal (IOM®-2 and SSDI mode).
24	DCL	I	-	**Data Clock:** Data Clock of the serial data interface.

26	DD/DR	**I**/OD I	-	**IOM®-2 Compatible Mode:** Receive data from IOM®-2 controlling device. **SSDI Mode:** Receive data of the strobed serial data interface.
25	DU/DX	**I**/OD O/ OD	-	**IOM®-2 Compatible Mode:** Transmit data to IOM®-2 controlling device. **SSDI Mode:** Transmit data of the strobed serial data interface.
27	DXST	O	L	**DX Strobe:** Strobe for DX in SSDI interface mode.
28	DRST	I	-	**DR Strobe:** Strobe for DR in SSDI interface mode.
14	$\overline{CS}$	I	-	**Chip Select:** Select signal of the serial control interface (SCI).
11	SCLK	I	-	**Serial Clock:** Clock signal of the serial control interface (SCI).
13	SDR	I	-	**Serial Data Receive:** Data input of the serial control interface (SCI).
12	SDX	O/ **OD**	H	**Serial Data Transmit:** Data Output of the serial control interface (SCI).
10	$\overline{INT}$	O/ **OD**	H	**Interrupt** New status available.

52 53 54 55 62 63 64 65 68 69 70 71 74 75 76 77	MA_0 MA_1 MA_2 MA_3 MA_4 MA_5 MA_6 MA_7 MA_8 MA_9 MA_{10} MA_{11} MA_{12} MA_{13} MA_{14} MA_{15}	I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O**	L[1)] L L L L L L L L L L L L L L L	**Memory Address 0-15:** Multiplexed address outputs for ARAM, DRAM and Flash memory access. Non-multiplexed address outputs for voice prompt EPROM. **Auxiliary Parallel Port:** General purpose I/O.
42 43 44 45 46 47 50 51	MD_0 MD_1 MD_2 MD_3 MD_4 MD_5 MD_6 MD_7	**I**/O **I**/O **I**/O **I**/O **I**/O **I**/O **I**/O **I**/O	- - - - - - - -	**Memory Data 0-7:** Memory (ARAM, DRAM, Flash Memory, EPROM) data bus.
35 36	$\overline{CAS}_0$/ ALE $\overline{CAS}_1$/ $\overline{FCS}$	O O	H[2)]	**ARAM, DRAM:** Column address strobe for memory bank 0 or 1. **Flash Memory:** Address Latch Enable for address lines A_{16}-A_{23}. Chip select signal for Flash Memory
34	$\overline{RAS}$/ $\overline{FOE}$	O	H[2)]	**ARAM, DRAM:** Row address strobe for both memory banks. **Flash Memory:** Output enable signal for Flash Memory.
33	$\overline{VPRD}$/ $\overline{FPD}$/ FCLE	O	H[2)]	**ARAM, DRAM:** Read signal for voice prompt EPROM. **Flash Memory (except Samsung):** Power down signal to reduce operating current. **Flash Memory (Samsung only):** Command latch enable for Flash Memory.

32	$\overline{W}$/ $\overline{FWE}$	O	H[2)]	**ARAM, DRAM:** Write signal for all memory banks. **Flash Memory:** Write signal for Flash Memory.
31	FRDY	I	-	**Flash Memory Ready** Input for Ready/Busy signal of Flash Memory
5 6	OSC_1 OSC_2	I O	- Z	**Auxiliary Oscillator:** Oscillator loop for 32.768 kHz timestamp/refresh crystal.
8	CLK	I	-	**Alternative AFECLK Source** 13,824 MHz
2 3	$XTAL_1$ $XTAL_2$	I O	- Z	**Oscillator:** $XTAL_1$: External clock or input of oscillator loop. $XTAL_2$: output of oscillator loop for crystal.
37 38	SPS_0 SPS_1	O O	L L	**Multipurpose Outputs:** General purpose, speakerphone or status
8	CLK	I	-	**Alternative AFECLK Source** 13,824 MHz
56	RO	O	-	**Reserved Output** Must be left open.

1) These lines are driven low with 125 µA until the mode (address lines or auxiliary port) is defined.

2) These lines are driven high with 70 µA during reset.

1.4 Logic Symbol

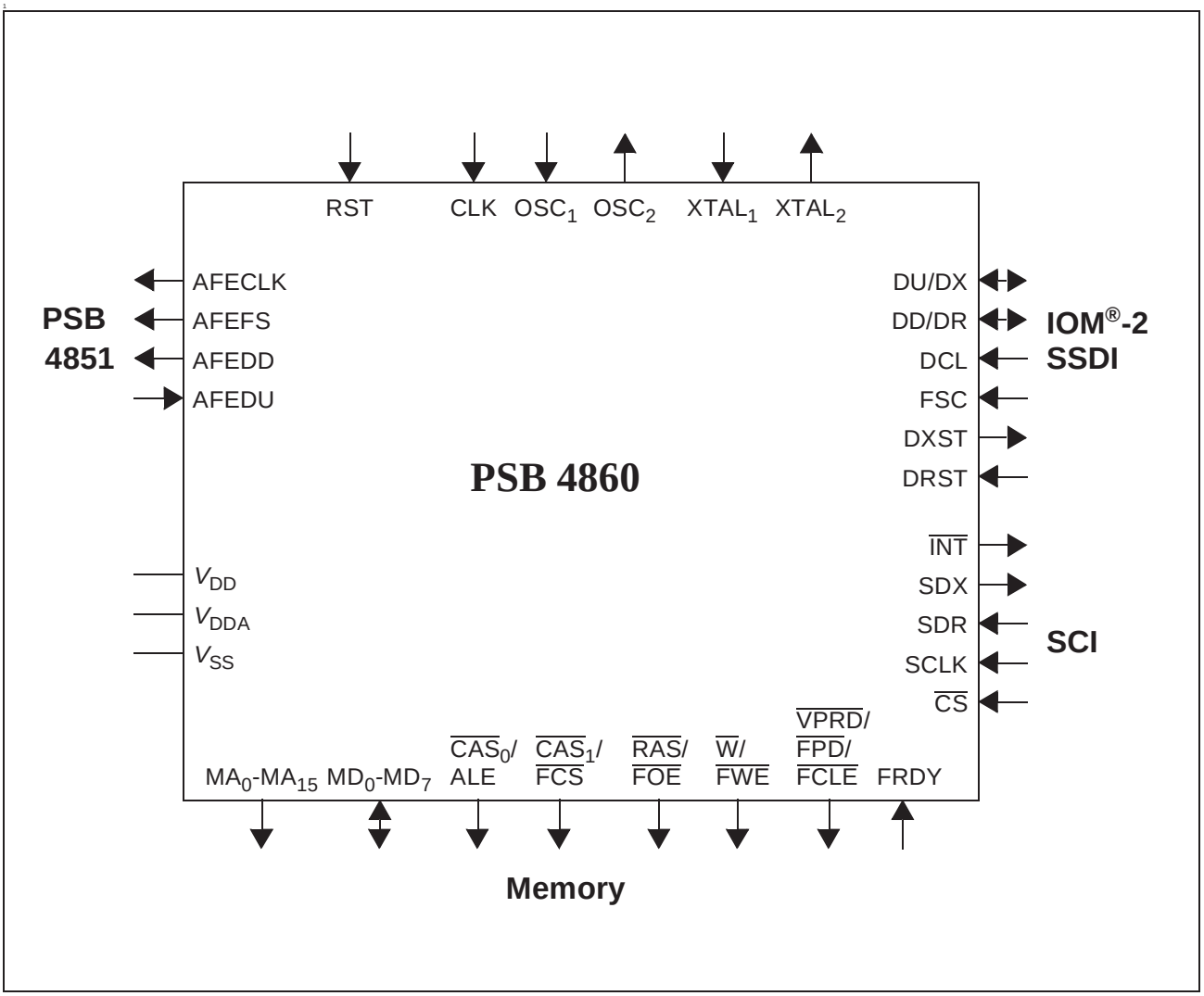


Figure 2
Logic Symbol of PSB 4860

1.5 Functional Block Diagram

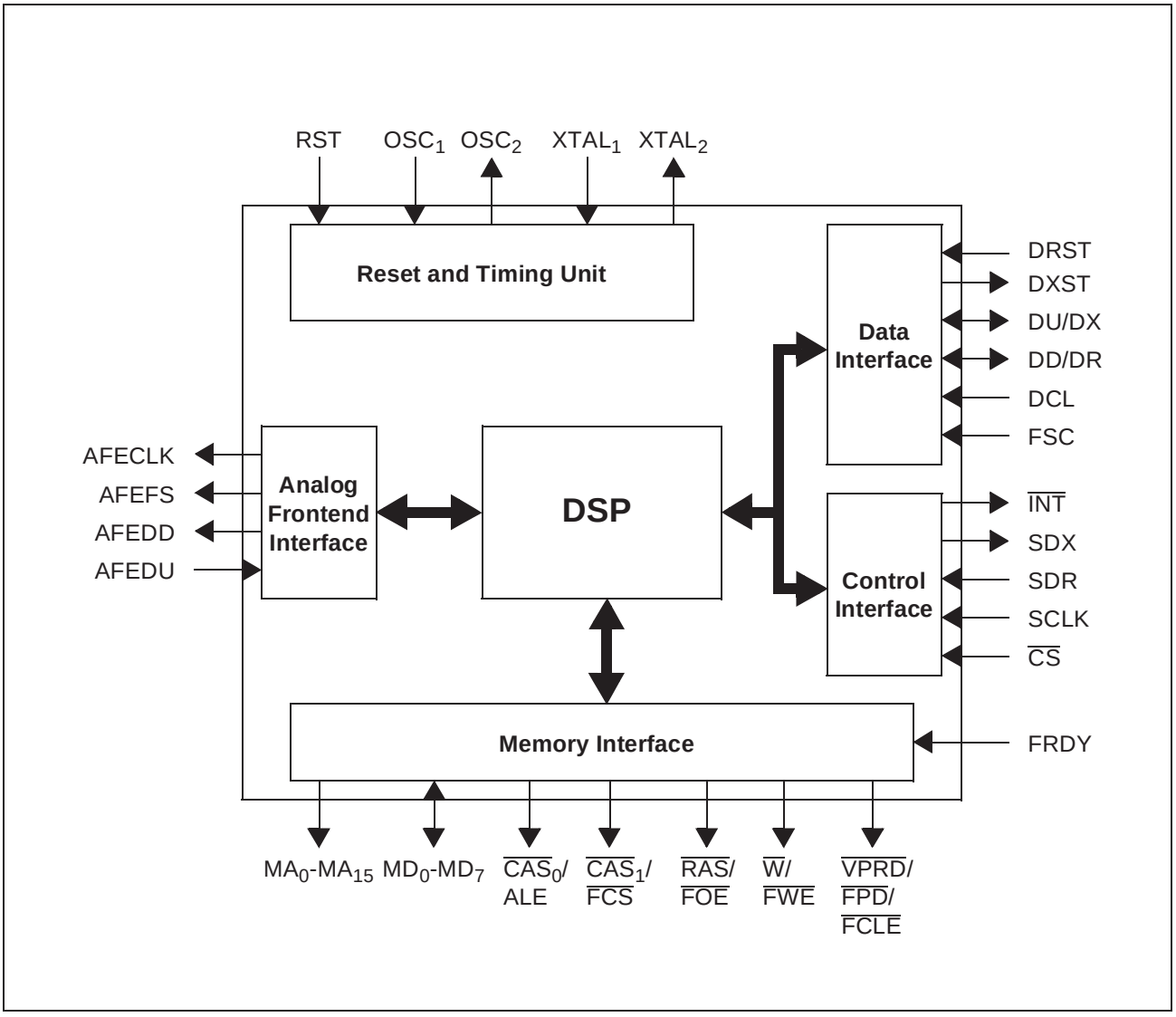


Figure 3
Block Diagram of PSB 4860

1.6 System Integration

The PSB 4860 combined with an analog frontend (PSB 4851) can be used in a variety of applications. This combination offers outstanding features like full duplex speakerphone and emergency operation. Some applications are given in the following sections.

1.6.1 Analog Featurephone with Digital Answering Machine

Figure 4 shows an example of an analog telephone system. The telephone can operate during power failure by line powering. In this case only the handset and ringer circuit are active. All other parts of the chipset are shut down leaving enough power for the external microcontroller to perform basic tasks like keyboard monitoring.

For answering machine operation the voice data is stored in ARAM or Flash Memory devices. In addition, voice prompts can be played back from an optional voice prompt EPROM. If Flash Memory is used the functionality of the voice EPROM can be realizedby the Flash Memory devices. The microcontroller can use the memory attached to the PSB 4860/PSB 4851 to store and retrieve binary data.

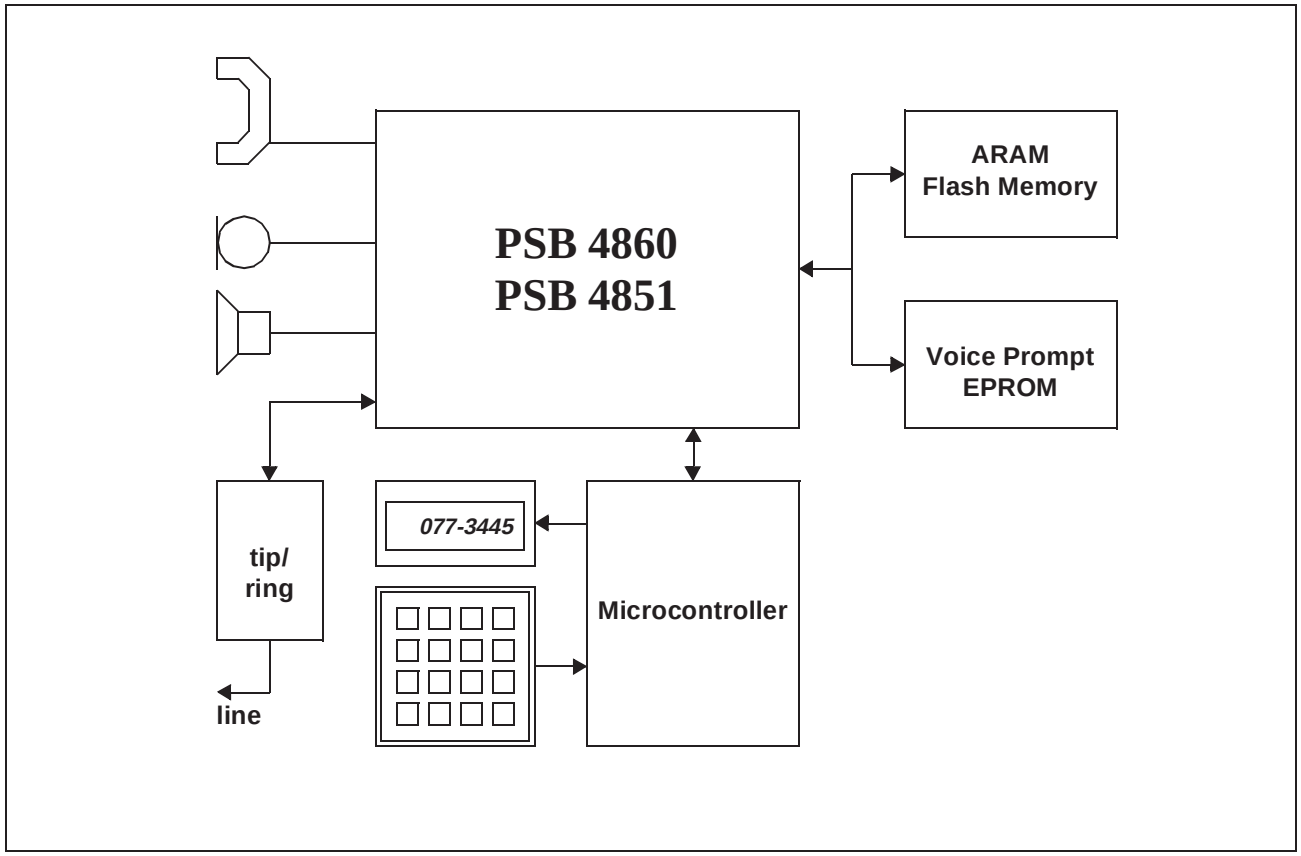


Figure 4
Analog Full Duplex Speakerphone with Digital Answering Machine

Another alternative is an implementation with a single Flash Memory connected to the microcontroller as shown in Figure 5. In this configuration the Flash Memory can be used to hold the program of the microcontroller in addition to the voice data.

For recording or playback the compressed voice data is transferred over the serial control interface of the PSB 4860/PSB 4851.

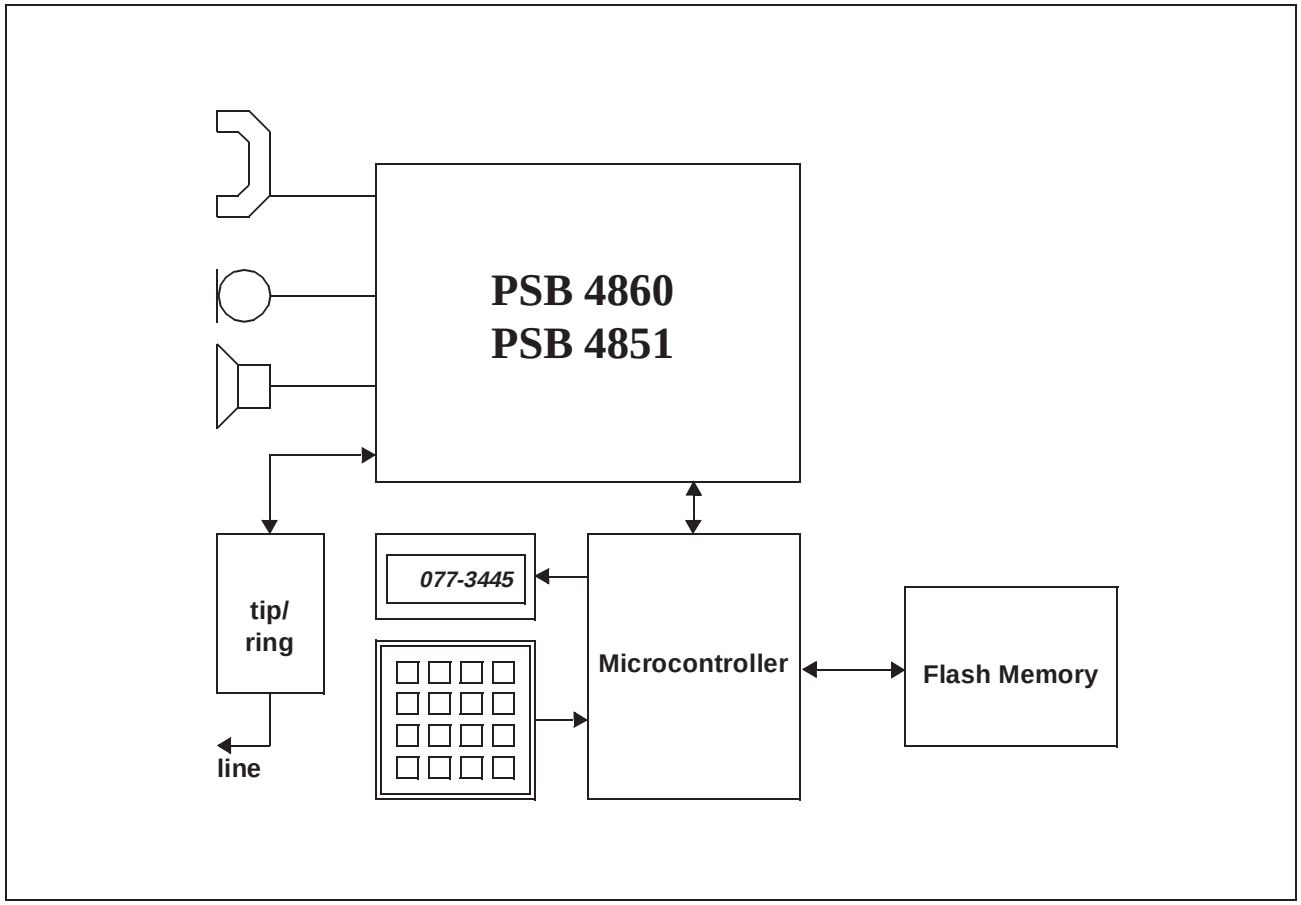


Figure 5
Full Duplex Speakerphone with Digital Answering Machine using Unified Memory

1.6.2 Featurephone with Digital Answering Machine for ISDN terminal

Figure 6 shows an ISDN featurephone that takes full advantage of two simultaneous connections. In this application one channel of the PSB 4851 interfaces to the handset and speakerphone while the other provides an interface for an external analog device (e.g. FAX machine).

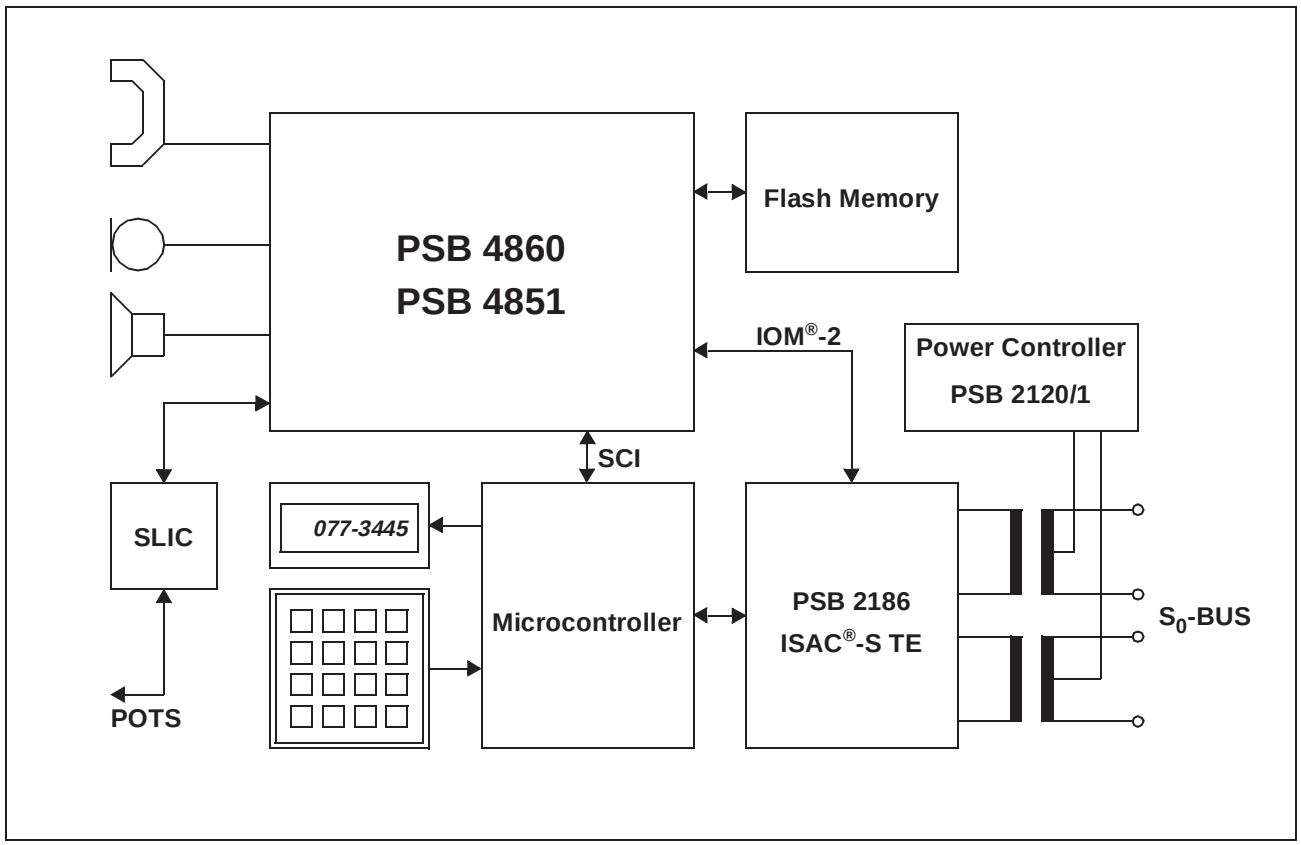


Figure 6
Featurephone with Answering Machine for ISDN Terminal

In addition, the two channels of the PSB 4851 can be used for holding two connections simultaneously. One connection can be switched to the handset and the other to the speakerphone box. Local three party conferences are also possible.

1.6.3 DECT Basestation with Integrated Digital Answering Machine

Figure 7 shows a DECT basestation based on the PSB 4860/PSB 4851 chipset. In this application it is possible to service both an external call and an internal call at the same time. For programming the serial control interface (SCI) is used while voice data is transferred via the strobed serial data interface (SSDI).

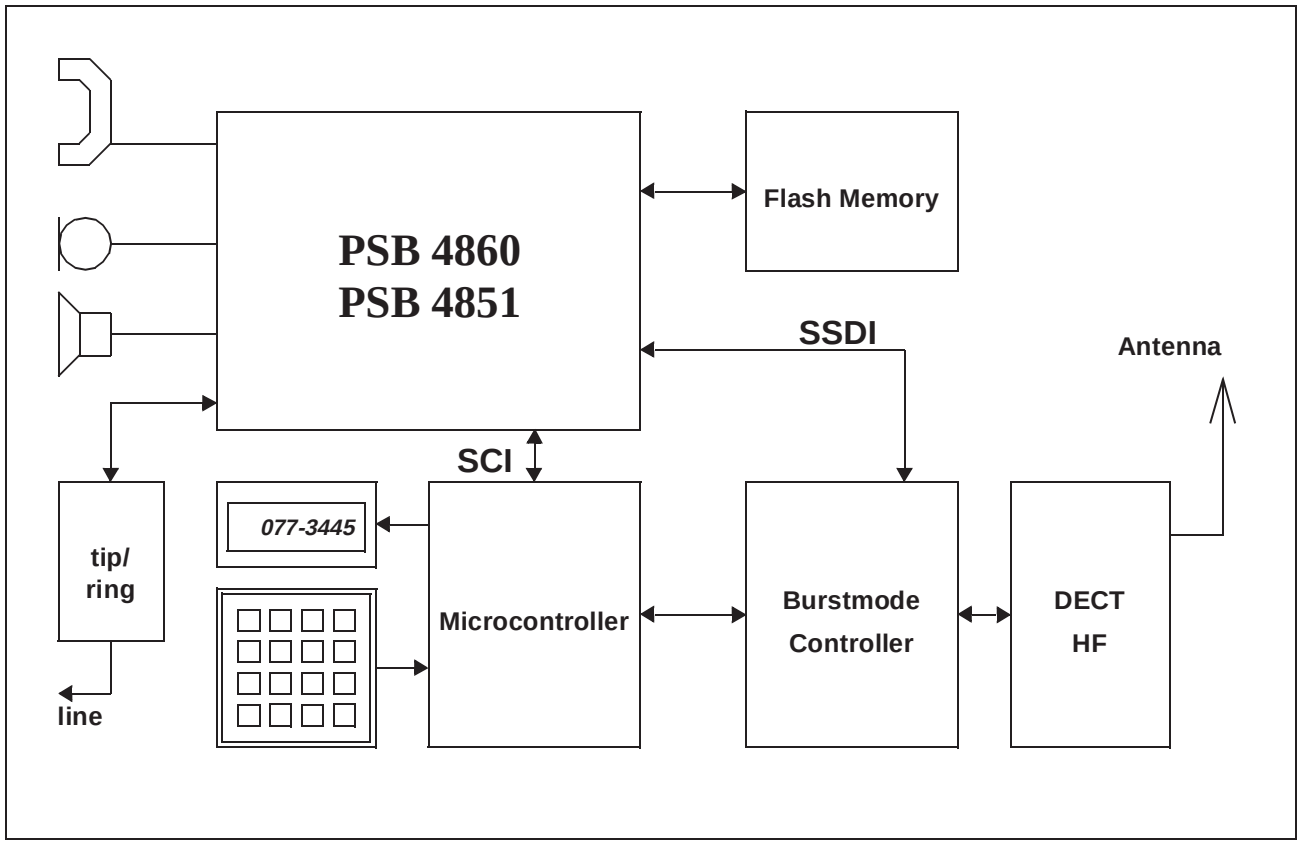


Figure 7
DECT Basestation

2 Functional Description

The PSB 4860 contains several functional units that can be combined with almost no restrictions to perform a given task. Figure 8 gives an overview of the important functional units.

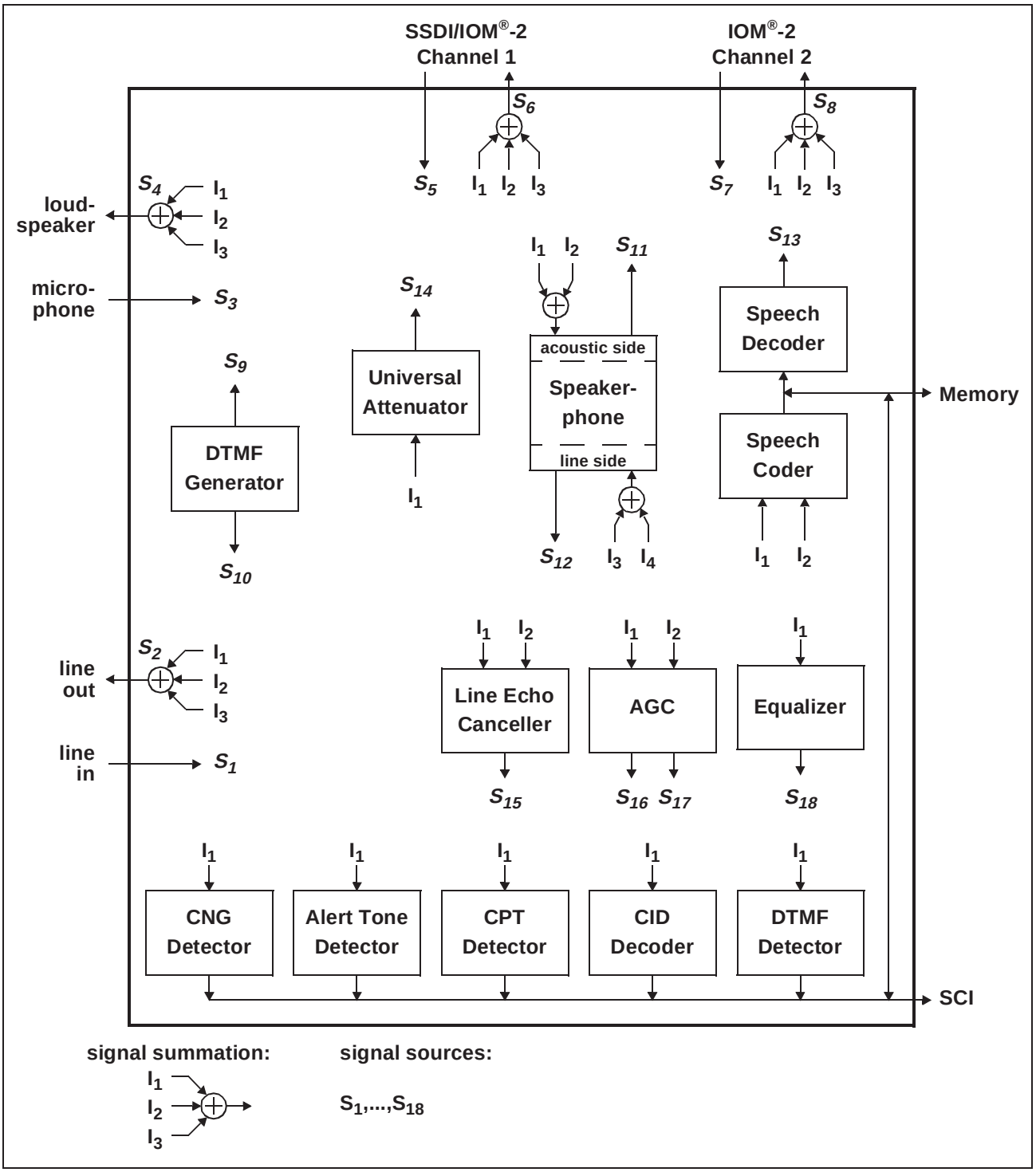


Figure 8
Functional Units - Overview

Each unit has one or more signal inputs (denoted by I). Most units have at least one signal output (denoted by S). Any input I can be connected to any signal output S. In addition to the signals shown in figure 8 there is also the signal S_0 (silence), which is useful at signal summation points. Table 1 lists the available signals within the PSB 4860 according to their reference points.

Table 1

Signal	Description
S_0	Silence
S_1	Analog line input (channel 1 of PSB 4851 interface)
S_2	Analog line output (channel 1 of PSB 4851 interface)
S_3	Microphone input (channel 2 of PSB 4851 interface)
S_4	Loudspeaker/Handset output (channel 2 of PSB 4851 interface)
S_5	Serial interface input, channel 1
S_6	Serial interface output, channel 1
S_7	Serial interface input, channel 2
S_8	Serial interface output, channel 2
S_9	DTMF generator output
S_{10}	DTMF generator auxiliary output
S_{11}	Speakerphone output (acoustic side)
S_{12}	Speakerphone output (line side)
S_{13}	Speech decoder output
S_{14}	Universal attenuator output
S_{15}	Line echo canceller output
S_{16}	Automatic gain control output (after gain stage)
S_{17}	Automatic gain control output (before gain stage)
S_{18}	Equalizer output

The following figures show the connections for two typical states during operation. Units that are not needed are not shown. Inputs that are not needed are connected to S_0 which provides silence (denoted by 0). In figure 9 a hands-free phone conversation is currently in progress. The speech coder is used to record the signals of both parties. The alert tone detector is used to detect an alerting tone of an off-hook caller id request while the CID decoder decodes the actual data transmitted in this case.

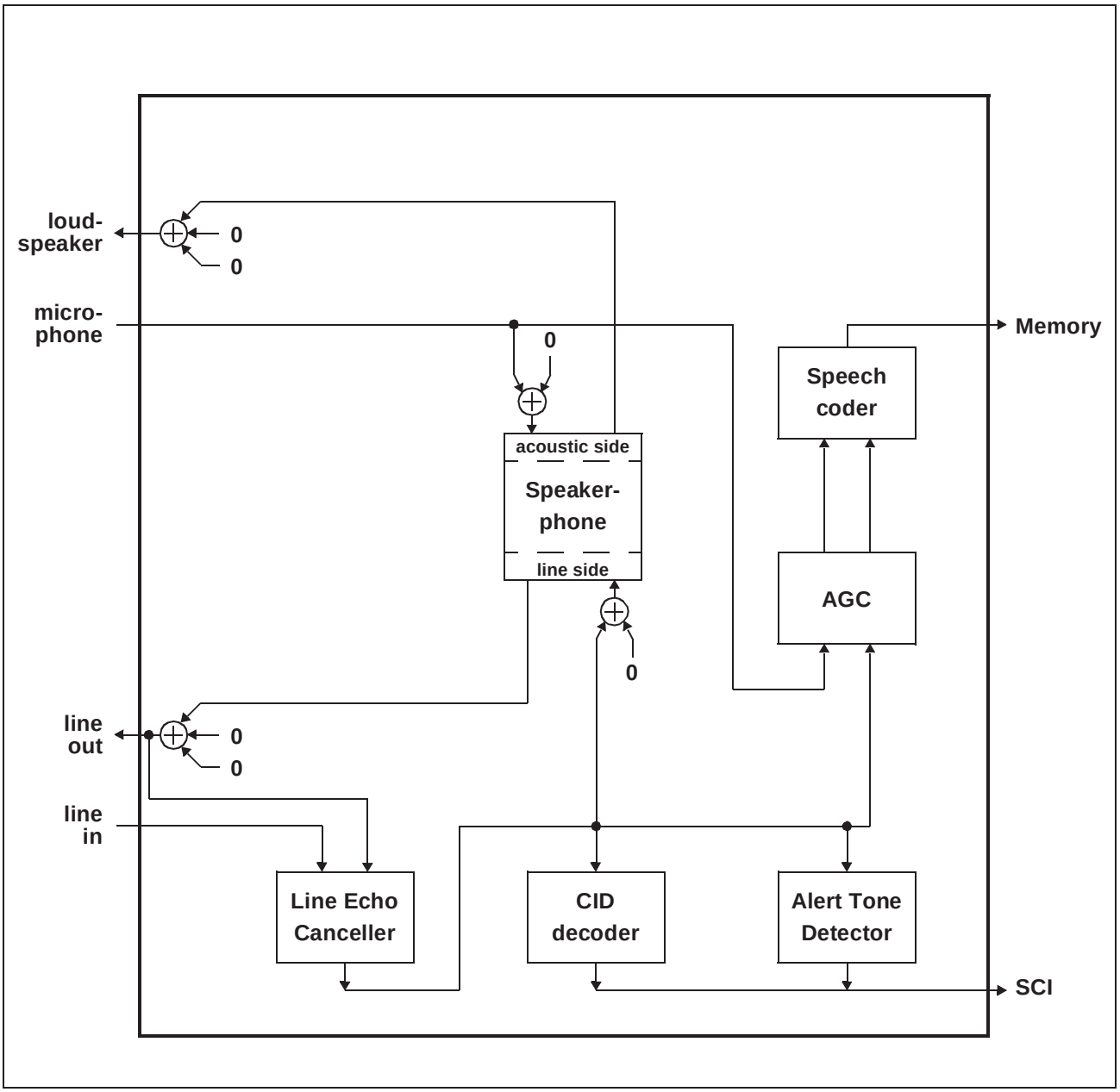


Figure 9
Functional Units - Recording a Phone Conversation

In figure 10 a phone conversation using the speakerphone is in progress. One party is using the base station of a DECT system while the other party is using a mobile handset. At the same time an external call is serviced by the answering machine. In the current state a message (recorded or outgoing) is being played back. In this case the DTMF detector is used to detect signals for remote access while the CPT detector is used to determine the end of the external call.

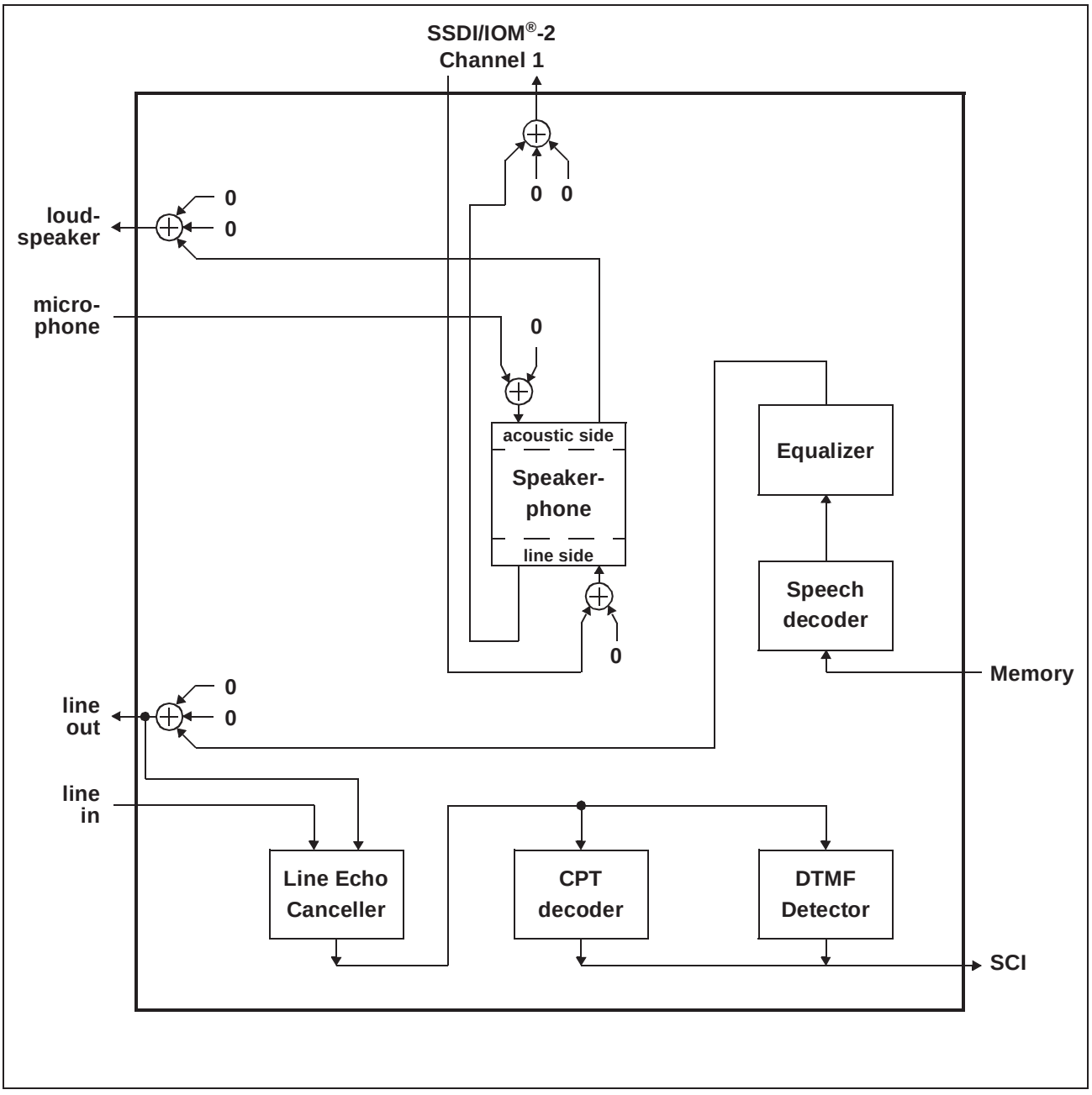


Figure 10
Functional Units - Simultaneous Internal and External Call

2.1 Functional Units

In this section the functional units of the PSB 4860 are described in detail. The functional units can be individually enabled or disabled.

2.1.1 Full Duplex Speakerphone

The speakerphone unit (figure 11) is attached to four signals (microphone, loudspeaker, line out and line in). The two input signals (microphone, line in) are preceded by a signal summation point.

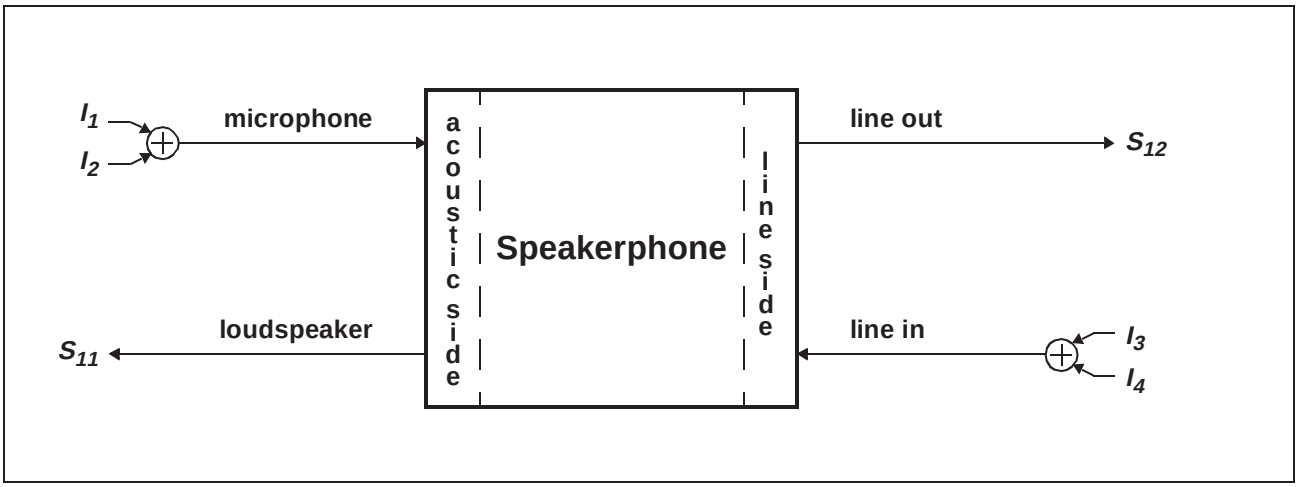


Figure 11
Speakerphone - Signal Connections

Internally, this unit can be divided into an echo cancellation unit and an echo suppression unit (figure 12). The echo cancellation unit provides the attenuation G_C while the echo suppression unit provides the attenuation G_S. The total attenuation ATT of the speakerphone is therefore $ATT=G_C+G_S$.

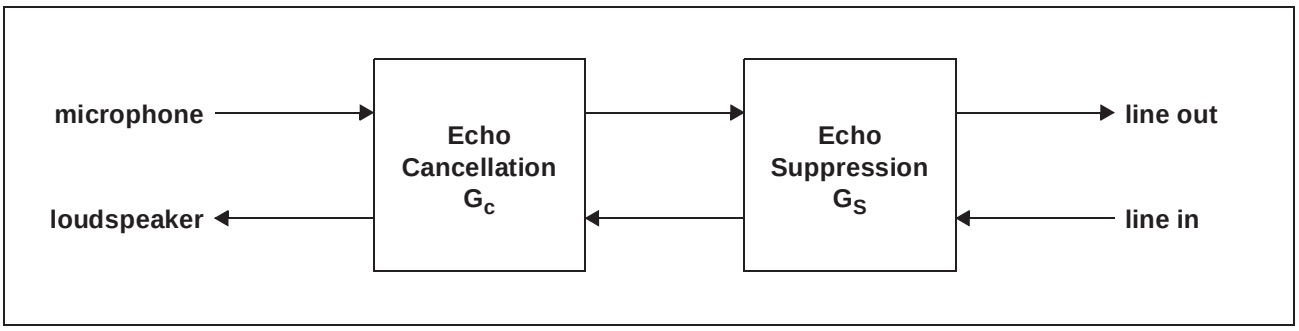


Figure 12
Speakerphone - Block Diagram

The echo suppression unit can be enabled without the echo cancellation unit. If the echo cancellation unit is disabled, the echo suppression unit still provides speakerphone

functionality, albeit only half duplex. As the echo cancellation must be disabled during recording or playback of speech data, this option allows for speakerphone operation even if recording or playback is going on. The echo suppression unit is also used to provide additional attenuation if the echo cancellation unit cannot provide all of the required attenuation itself.

2.1.2 Echo Cancellation

A simplified block diagram of the echo cancellation unit is shown in figure 13.

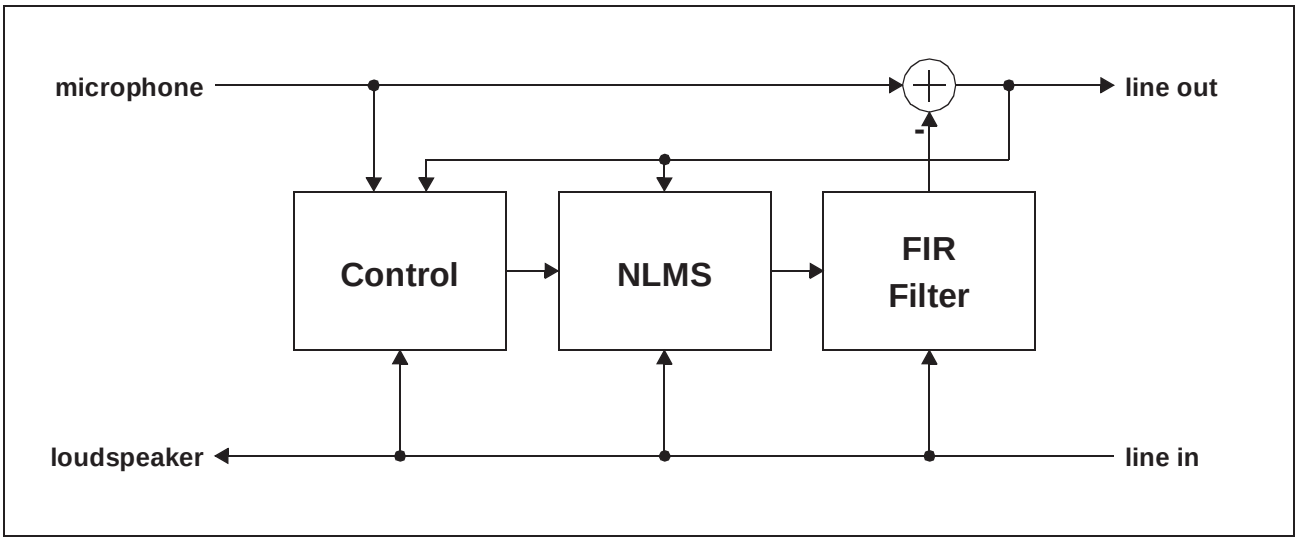


Figure 13
Echo Cancellation Unit - Block Diagram

The echo cancellation unit consists of an finite impulse response filter (FIR) that models the expected acoustic echo, an NLMS based adaption unit and a control unit. The expected echo is subtracted from the actual input signal from the microphone. If the model is exact and the echo does not exceed the length of the filter then the echo can be completely cancelled. However, even if this ideal state can be achieved for one given moment the acoustic echo usually changes over time. Therefore the NLMS unit continuously adapts the coefficients of the FIR filter. This adaption process is steered by the control unit. As an example, the adaption is inhibited as long as double talk is detected by the control unit. Furthermore the control unit informs the echo suppression unit about the achieved echo return loss.

Table 2 shows the registers associated with the echo cancellation unit.

Table 2

Register	# of Bits	Name	Comment
SAELEN	9	LEN	Length of FIR filter
SAEATT	15	ATT	Attenuation reduction during double-talk

Table 2

SAEGS	3	GS	Global scale (all blocks)
SAEPS1	3	AS	Partial scale (for blocks >= SAEPS2:FB)
SAEPS2	3	FB	First block affected by partial scale

The length of the FIR filter can be varied from 127 to 511 taps (15.875ms to 63.875ms). The taps are grouped into blocks. Each block contains 64 taps.

The performance of the FIR filter can be enhanced by prescaling some or call of the coefficients of the FIR filter. A coefficient is prescaled by multiplying it by a constant. The advantage of prescaling is an enhanced precision and consequently an enhanced echo cancellation. The disadvantage is a reduced echo cancellation performance if the signal exceeds the maximal coefficient value. More precisely, if a coefficient at tap T_i is scaled by a factor C_i then the level of the echo (room impulse response) must not exceed Max/ C_i (Max: Maximum PCM value). As an example figure shows a typical room impulse response.

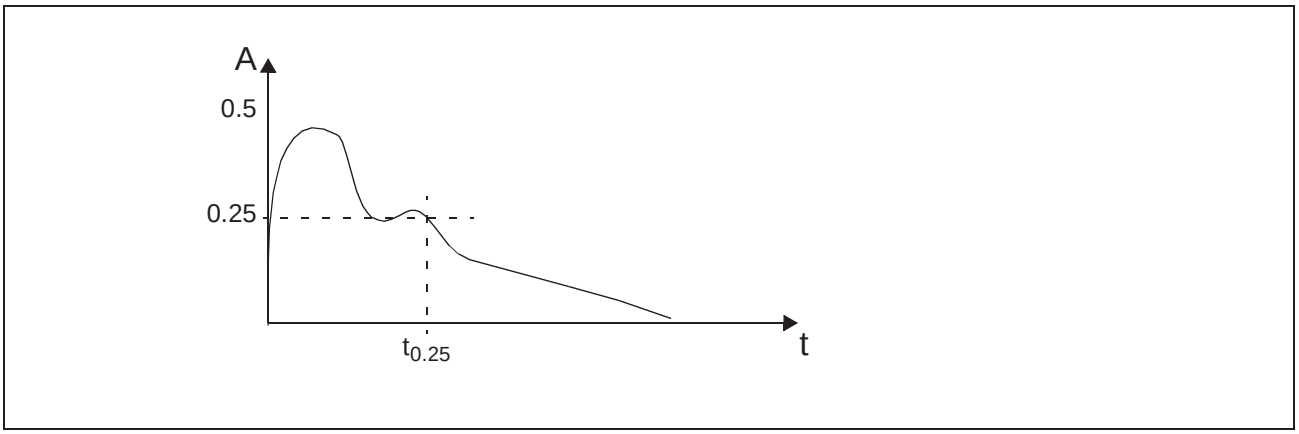


Figure 14
Echo Cancellation Unit - Typical Room Impulse Response

First of all, the echo never exceeds 0.5 of the maximum value. Furthermore the echo never exceeds 0.25 of the maximum value after time $t_{0.25}$. Therefore all coefficients can be scaled by a factor of 2 and all coefficients for taps corresponding to times after $t_{0.25}$ can be scaled a factor of 4.

The echo cancellation unit provides three parameters for scaling coefficients. The first parameter (GS) determines a scale for all coefficients. The second parameter (FB) determines the first block for which an additional scale (PS) takes effect.

This feature can be used for different default settings like large or small rooms.

2.1.3 Echo Suppression

The echo suppression unit can be in one of three states:

- transmit state
- receive state
- idle state

In transmit state the microphone signal drives the line output while the line input is attenuated. In receive state the loudspeaker signal is driven by the line input while the microphone signal is attenuated. In idle state both signal paths are active with evenly distributed attenuation.

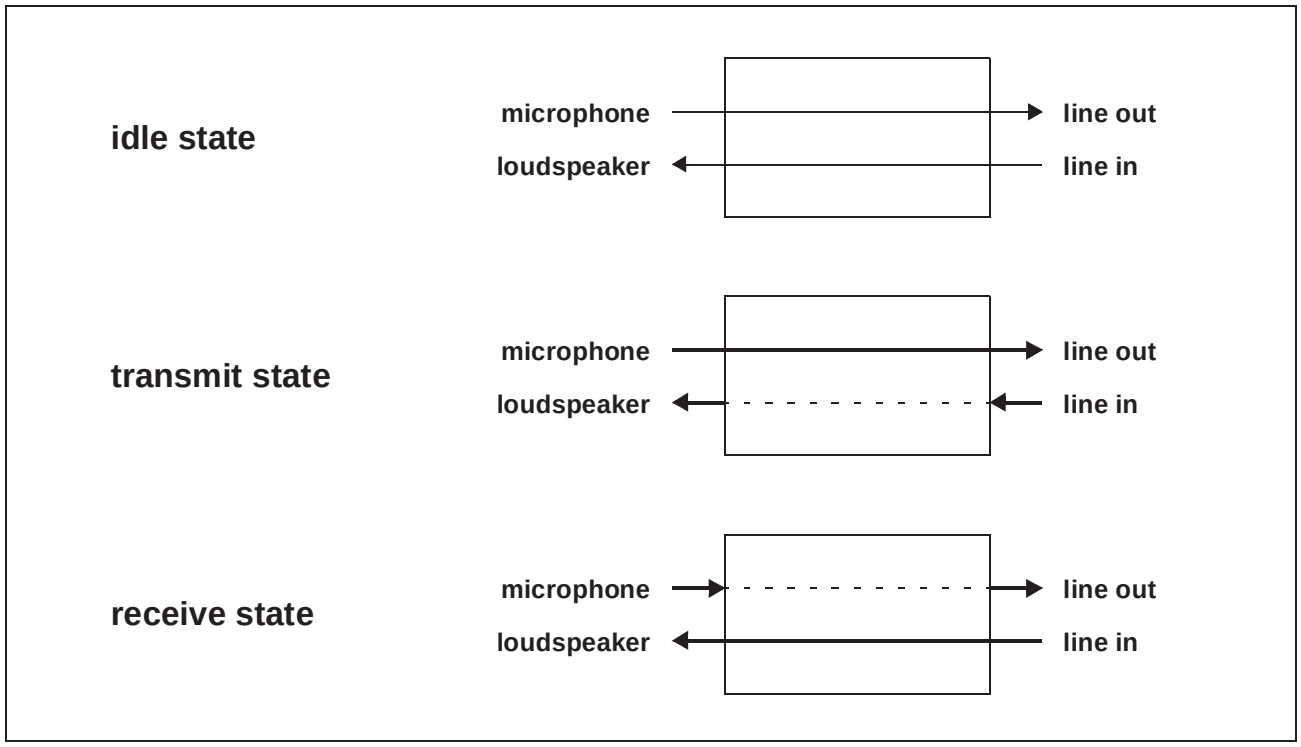


Figure 15
Echo Suppression Unit - States of Operation

Figure16 shows the signal flow graph of the echo suppression unit in more detail.

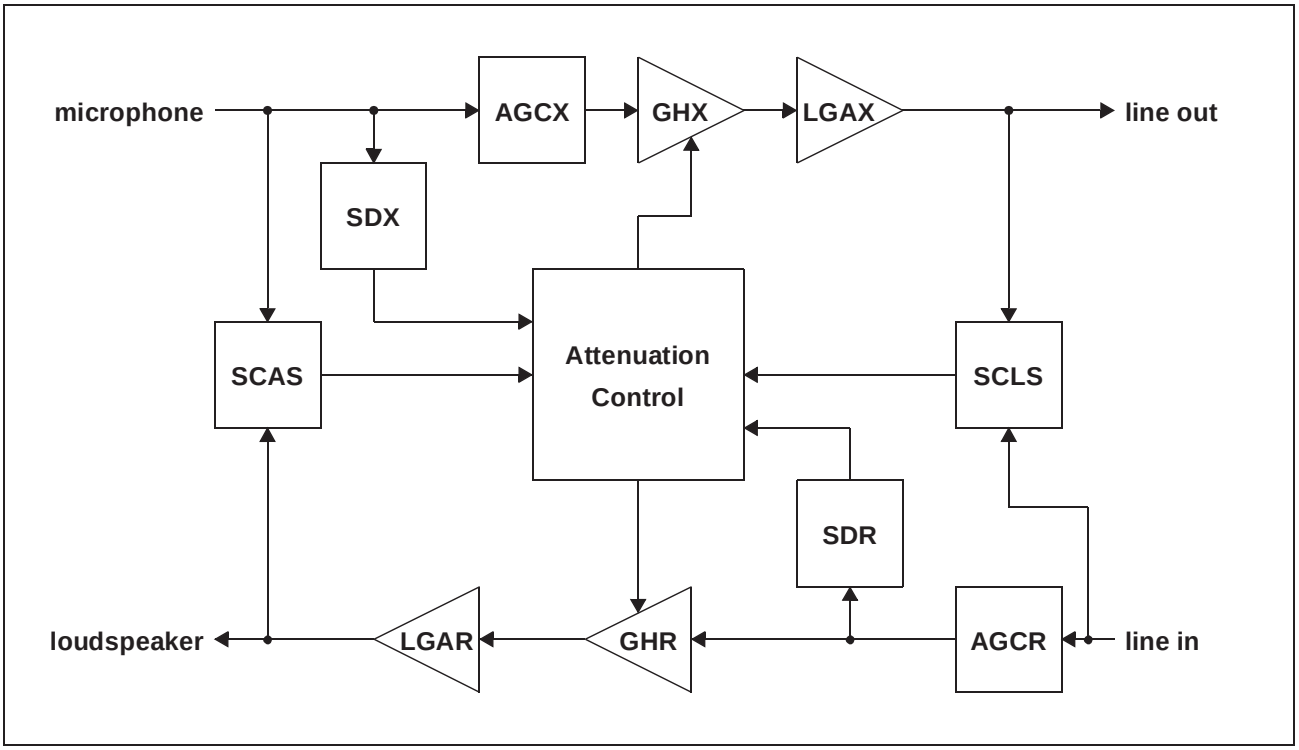


Figure 16
Echo Suppression Unit - Signal Flow Graph

State switching is controlled by the speech comparators (SCAS, SCLS) and the speech detectors (SDX, SDR). The amplifiers (AGCX, AGCR, LGAX, LGAR) are used to achieve proper signal levels for each state. All blocks are programmable. Thus the telephone set can be optimized and adjusted to the particular geometrical and acoustical environment. The following sections discuss each block of the echo suppression unit in detail.

2.1.3.1 Speech Detector

For each signal source a speech detector (SDX, SDR) is available. The speech detectors are identical but can be programmed individually. Figure 17 shows the signal flow graph of a speech detector.

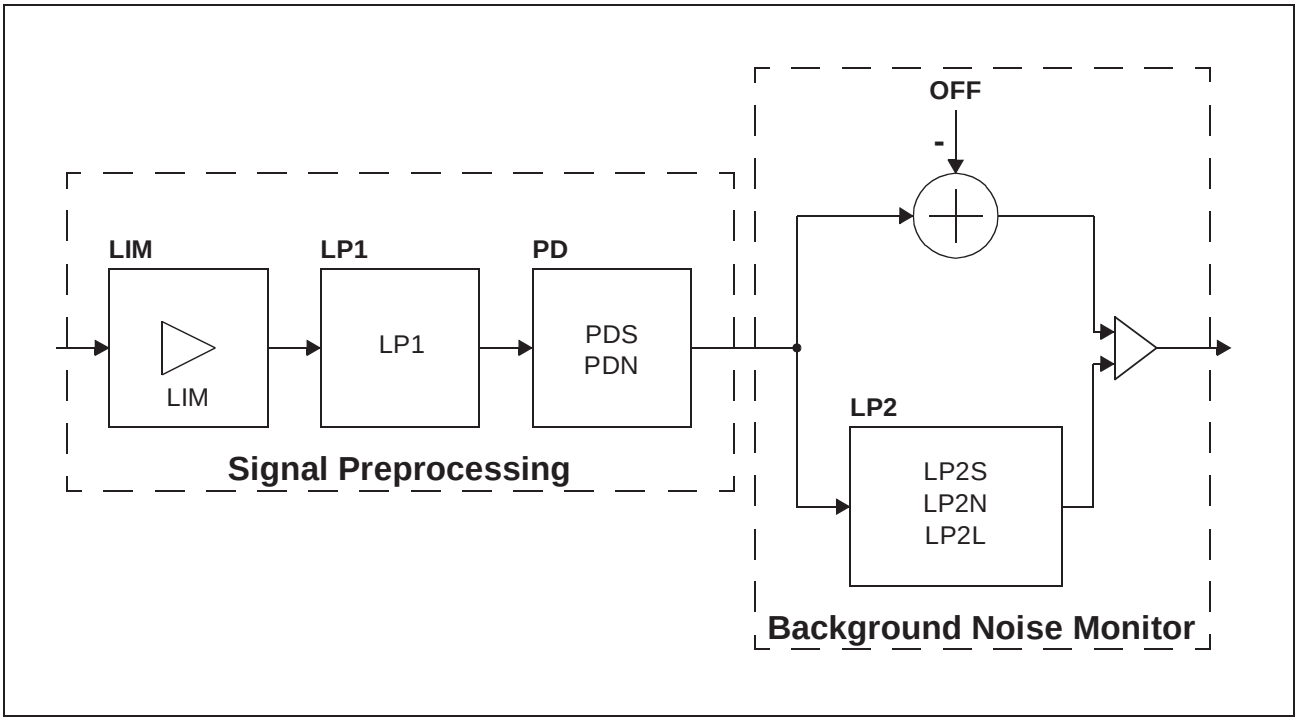


Figure 17
Speech Detector - Signal Flow Graph

The first three units (LIM, LP1, PD) are used for preprocessing the signal while the actual speech detection is performed by the background noise monitor.

Background Noise Monitor

The tasks of the noise monitor are to differentiate voice signals from background noise, even if it exceeds the voice level, and to recognize voice signals without any delay. Therefore the Background Noise Monitor consists of the Low-Pass Filter 2 (LP2) and the offset in two separate branches. Basically it works on the burst-characteristic of the speech: voice signals consist of short peaks with high power (bursts). In contrast, background noise can be regarded approximately stationary from its average power.

Low-Pass Filter 2 provides different time constants for noise (non-detected speech) and speech. It determines the average of the noise reference level. In case of background noise the level at the output of LP2 is approximately the level of the input. As in the other branch an additional offset OFF is added to the signal, the comparator signals noise. At speech bursts the digital signals arriving at the comparator via the offset branch change faster than those via the LP2-branch. If the difference exceeds the offset OFF, the

comparator signals speech. Therefore the output of the background noise monitor is a digital signal indicating speech (1) or noise (0).

A small fade constant (LP2N) enables fast settling of LP2 to the average noise level after the end of speech recognition. However, a too small time constant for LP2N can cause rapid charging to such a high level that after recognizing speech the danger of an unwanted switching back to noise exists. It is recommended to choose a large rising constant (LP2S) so that speech itself charges the LP2 very slowly. Generally, it is not recommended to choose an infinite LP2S because then approaching the noise level is disabled. During continuous speech or tones the LP2 will be charged until the limitation LP2L is reached. Then the value of LP2 is frozen until a break discharges the LP2. This limitation permits transmission of continuous tones and “music on hold”.

The offset stage represents the estimated difference between the speech signal and averaged noise.

Signal Preprocessing

As described in the preceding chapter, the background noise monitor is able to discriminate between speech and noise. In very short speech pauses e.g. between two words, however, it changes immediately to non-speech, which is equal to noise. Therefore a peak detection is required in front of the Noise Monitor.

The main task of the Peak Detector (PD) is to bridge the very short speech pauses during a monolog so that this time constant has to be long. Furthermore, the speech bursts are stored so that a sure speech detection is guaranteed. But if no speech is recognized the noise low-pass LP2 must be charged faster to the average noise level. In addition, the noise edges are to be smoothed. Therefore two time constants are necessary. As the peak detector is very sensitive to spikes, the low-pass LP1 filters the incoming signal containing noise in a way that main spikes are eliminated. Due to the programmable time constant it is possible to refuse high-energy sibilants and noise edges.

To compress the speech signals in their amplitudes and to ease the detection of speech, the signals have to be companded logarithmically. Hereby, the speech detector should not be influenced by the system noise which is always present but should discriminate between speech and background noise. The limitation of the logarithmic amplifier can be programmed via the parameter LIM. LIM is related to the maximum PCM level. A signal exceeding the limitation defined by LIM is getting amplified logarithmically, while very smooth system noise below is neglected. It should be the level of the minimum system noise which is always existing; in the transmit path the noise generated by the telephone circuitry itself and in receive direction the level of the first bit which is stable without any speech signal at the receive path. Table 5 shows the parameters for the speech detector.

Table 3

Parameter	# of bytes	Range	Comment
LIM	1	0 to 95 dB	Limitation of log. amplifier
OFF	1	0 to 95 dB	Level offset up to detected noise
PDS	1	1 to 2000 ms	Peak decrement PD1 (speech)
PDN	1	1 to 2000 ms	Peak decrement PD1 (noise)
LP1	1	1 to 2000 ms	Time constant LP1
LP2S	1	2 to 250 s	Time constant LP2 (speech)
LP2N	1	1 to 2000 ms	Time constant LP2 (noise)
LP2L	1	0 to 95 dB	Maximum value of LP2

The input signal of the speech detector can be connected to either the input signal of the echo suppression unit (as shown for SDX) or the output of the associated AGC (as shown for SDR).

2.1.3.2 Speech Comparators (SC)

The echo suppression unit has two identical speech comparators (SCAS, SCLS). Each comparator can be programmed individually to accommodate the different system characteristics of the acoustic interface and the line interface. As SCAS and SCLS are identical, the following description holds for both SCAS and SCLS.

The SC has two input signals SX and SR, which map to microphone/loudspeaker for SCAS and line in/line out for SCLS.

In principle, the SC works according to the following equation:

$$\text{if} \quad SX > SR + V \text{ then switch state}$$

Therefore, SCAS controls the switching to transmit state and SCLS controls the switching to receive state. Switching is done only if SX exceeds SR by at least the expected acoustic level enhancement V which is divided into two parts: G and GD. A block diagram of the SC is shown in figure 18.

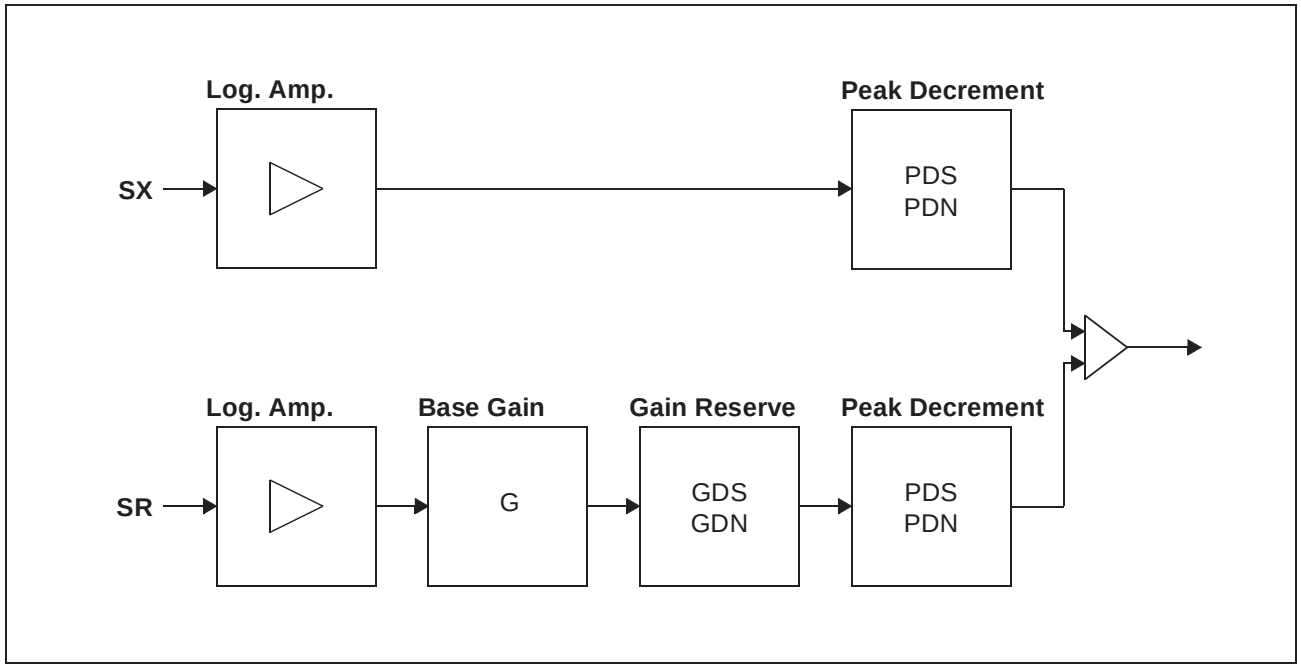


Figure 18
Speech Comparator - Block Diagram

At both inputs, logarithmic amplifiers compress the signal range. Hence after the required signal processing for controlling the acoustic echo, pure logarithmic levels on both paths are compared.

The main task of the comparator is to control the echo. The internal coupling due to the direct sound and mechanical resonances are covered by G. The external coupling, mainly caused by the acoustic feedback, is controlled by GD/PD.

The base gain (G) corresponds to the terminal couplings of the complete telephone: G is the measured or calculated level enhancement between both receive and transmit inputs of the SC.

To control the acoustic feedback two parameters are necessary: GD represents the actual reserve on the measured G. Together with the Peak Decrement (PD) it simulates the echo behavior at the acoustic side: After speech has ended there is a short time during which hard couplings through the mechanics and resonances and the direct echo are present. Till the end of that time (Δt) the level enhancement V must be at least equal to G to prevent clipping caused by these internal couplings. Then, only the acoustic feedback is present. This coupling, however, is reduced by air attenuation. For this in general the longer the delay, the smaller the echo being valid. This echo behavior is featured by the decrement PD.

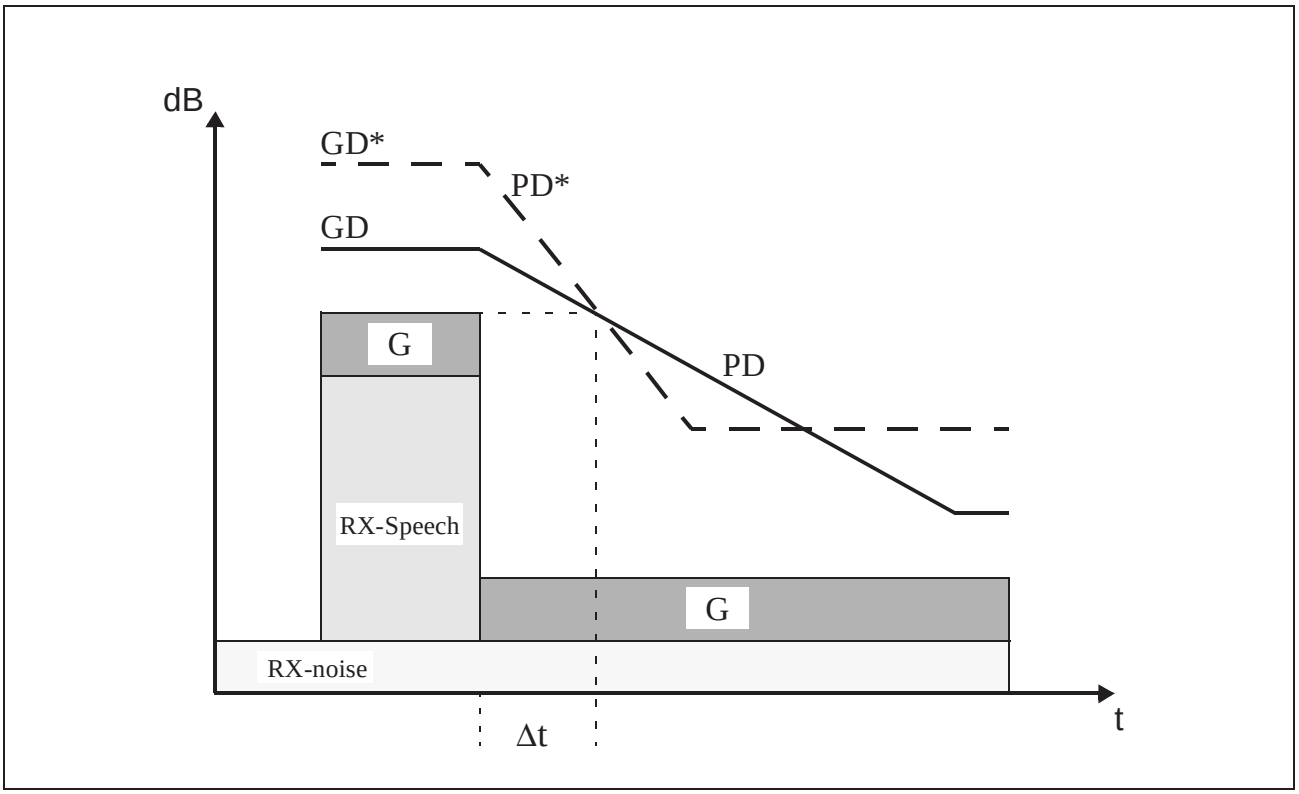


Figure 19
Speech Comparator - Interdependence of Parameters

According to figure 19, a compromise between the reserve GD and the decrement PD has to be made: a smaller reserve (GD) above the level enhancement G requires a longer time to decrease (PD). It is easy to overshout the other side but the intercommunication is harder because after the end of the speech, the level of the estimated echo has to be exceeded. In contrary, with a higher reserve (GD*) it is harder to overshout continuous speech or tones, but it enables a faster intercommunication because of a stronger decrement (PD*).

Two pairs of coefficients, GDS/PDS when speech is detected, and GDN/PDN in case of noise, offer a different echo handling for speech and non-speech.

With speech, even if very strong resonances are present, the performance will not be worsened by the high GDS needed. Only when speech is detected, a high reserve prevents clipping. A time period ET [ms] after speech end, the parameters of the comparator are switched to the “noise” values. If both sets of the parameters are equal, ET has no function.

Table 4

Parameter	# of bytes	Range	Comment
G	1	– 48 to + 48 dB	Base Gain
GDS	1	0 to 48 dB	Gain Reserve (Speech)
PDS	1	0.025 to 6 dB/ms	Peak Decrement (Speech)
GDN	1	0 to 48 dB	Gain Reserve (Noise)
PDN	1	0.025 to 6 dB/ms	Peak Decrement (Noise)
ET	1	0 to 992 ms	Time to Switch from speech to noise parameters

2.1.3.3 Attenuation Control

The attenuation control unit controls the attenuation stages GHX and GHR and performs state switching. The programmable attenuation ATT is completely switched to GHX (GHR) in receive state (transmit state). In idle state both GHX and GHR attenuate by ATT/2.

In addition, attenuation is also influenced by the automatic gain control stages (AGCX, AGCR).

State switching depends on the signals of one speech comparator and the corresponding speech detector. While each state is associated with the programmed attenuation, the time is takes to reach the steady-state attenuation after a state switch can be programmed (T_{SW}).

If the current state is either transmit or receive and no speech on either side has been detected for time T_W then idle state is entered. To smoothen the transition, the attenuation is incremented (decremented) by DS until the evenly distribution ATT/2 for both GHX and GHR is reached.

Table 5 shows the parameters for the attenuation unit. Note that T_{SW} is dependant on the current attenuation by the formula $T_{sw} = SW \times ATT$.

Table 5

Parameter	# of bytes	Range	Comment
TW	1	16 ms to 4 s	T_W to return to idle state
ATT	1	0 to 95 dB	Attenuation for GHX and GHR
DS	1	0.6 to 680 ms/dB	Decay Speed (to idle state)
SW	1	0.0052 to 10 ms/dB	Decay Rate (used for T_{SW})

Note: In addition, attenuation is also influenced by the Automatic Gain Control stages (AGCX, AGCR) in order to keep the total loop attenuation constant.

2.1.3.4 Echo Suppression Status Output

The PSB 4860 can report the current state of the echo suppression unit to ease optimization of the parameter set of the echo suppression unit. In this case the SPS_0 and SPS_1 pins are set according to table 6.

Table 6

SPS_0	SPS_1	Echo Suppression Unit State
0	0	no echo suppression operation
0	1	receive
1	0	transmit
1	1	idle

Furthermore the controller can read the current value of the SPS pins by reading register SPSCTL.

2.1.3.5 Loudhearing

The speakerphone unit can also be used for controlled loudhearing. If enabled in loudhearing mode, the loudspeaker amplifier of the PSB 4851 (ALS) is used instead of GHR (figure 16) when appropriate to avoid oscillation. In order to enable this feature, the PSB 4851 must be programmed to allow ALS override. The ALS field within the AFE control register AFECTL defines the value sent to the PSB 4851 if attenuation is necessary.

2.1.3.6 Automatic Gain Control

The echo suppression unit has two identical automatic gain control units (AGCX, AGCR).

Operation of the AGC depends on a threshold level defined by the parameter COM (value relative to the maximum PCM-value). The regulation speed is controlled by SPEEDH for signal amplitudes above the threshold and SPEEDL for amplitudes below. Usually SPEEDH will be chosen to be at least 10 times faster than SPEEDL. The bold line in Figure 20 depicts the steady-state output level of the AGC as a function of the input level.

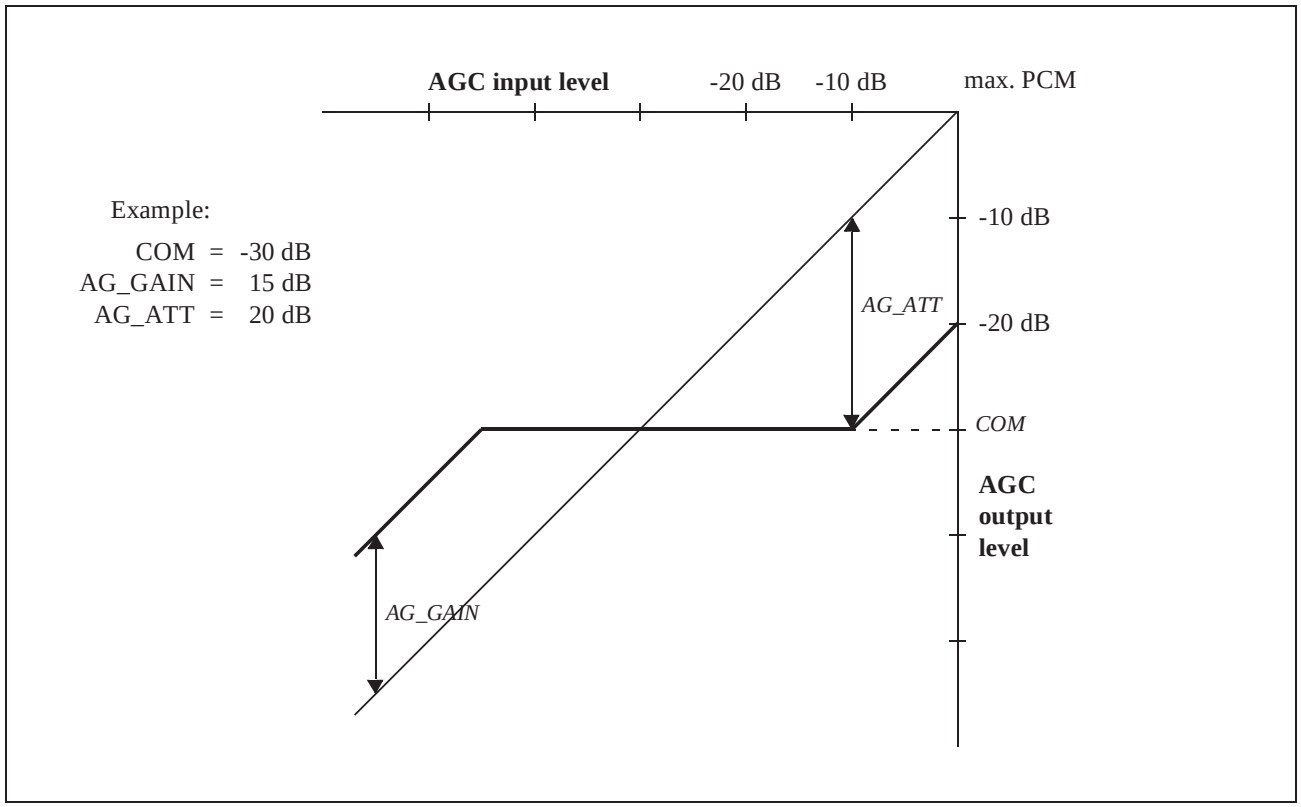


Figure 20
Echo Suppression Unit - Automatic Gain Control

For reasons of physiological acceptance the AGC gain is automatically reduced in case of continuous background noise (e.g. by ventilators). The reduction is programmed via the NOIS parameter. When the noise level exceeds the threshold determined by NOIS, the amplification will be reduced by the same amount the noise level is above the threshold. The current gain/attenuation of the AGC can be read at any time.

An additional low pass with time constant LPA is provided to avoid an immediate response of the AGC to very short signal bursts.

If SDX detects noise, AGCX is not working. In this case the last gain setting is used. Regulation starts with this value as soon as SDX detects speech.

Likewise, if SDR detects noise, AGCR is not working. In this case the last gain setting is used. Regulation starts with this value as soon as SDR detects speech. When the AGC has been disabled the initial gain used immediately after enabling the AGC can be programmed. Table 7 shows the parameters of the AGC.

Table 7

Parameter	# of Bytes	Range	Comment
AG_INIT	1	-95 dB to 95dB	Initial AGC gain/attenuation
COM	1	0 to – 95 dB	Compare level rel. to max. PCM-value
AG_ATT	1	0 to -95 dB	Attenuation range
AG_GAIN	1	0 to 95 dB	Gain range
AG_CUR	1	-95 dB to 95 dB	Current gain/attenuation
SPEEDL	1	0.25 to 62.5 dB/s	Change rate for lower levels
SPEEDH	1	0.25 to 62.5 dB/s	Change rate for higher levels
NOIS	1	0 to – 95 dB	Threshold for AGC-reduction by background noise
LPA	1	0.025 to 16 ms	AGC low pass time constant

Note: There are two sets of parameters, one for AGCX and one for AGCR.

2.1.3.7 Fixed Gain

Each signal path features an additional amplifier (LGAX, LGAR) that can be set to a fixed gain. These amplifiers should be used for the basic amplification in order to avoid saturation in the preceding stages. Table 8 shows the only parameter of this stage.

Table 8

Parameter	# of Bytes	Range	Comment
LGA	1	-12 dB to 12 dB	always active

2.1.3.8 Mode Control

Table 9 shows the registers used to determine the signal sources and the mode.

Table 9

Register	# of Bits	Name	Comment
SCTL	1	ENS	Echo suppression unit enable
SCTL	1	ENC	Echo cancellation unit enable
SCTL	1	MD	Speakerphone or loudhearing mode
SCTL	1	AGX	AGCX enable
SCTL	1	AGR	AGCR enable

Table 9

SCTL	1	SDX	SDX input tap
SCTL	1	SDR	SDR input tap
AFECTL	4	ALS	ALS value for loudhearing
SSRC1	5	I1	Input signal 1 (microphone)
SSRC1	5	I2	Input signal 2 (microphone)
SSRC2	5	I3	Input signal 3 (line in)
SSRC2	5	I4	Input signal 4 (line in)

2.1.4 Line Echo Canceller

The PSB 4860 contains an adaptive line echo cancellation unit for the cancellation of near end echoes. The unit has two modes: normal and extendend. In normal mode, the maximum echo length is 4 ms. This mode is alway available. In extendend mode, the maximum echo length is 24 ms. Extendend mode cannot be used while the speech encoder is running or while fast/slow playback.

The line echo cancellation unit is especially useful in front of the various detectors (DTMF, CPT, etc.). A block diagram is shown in figure 21.

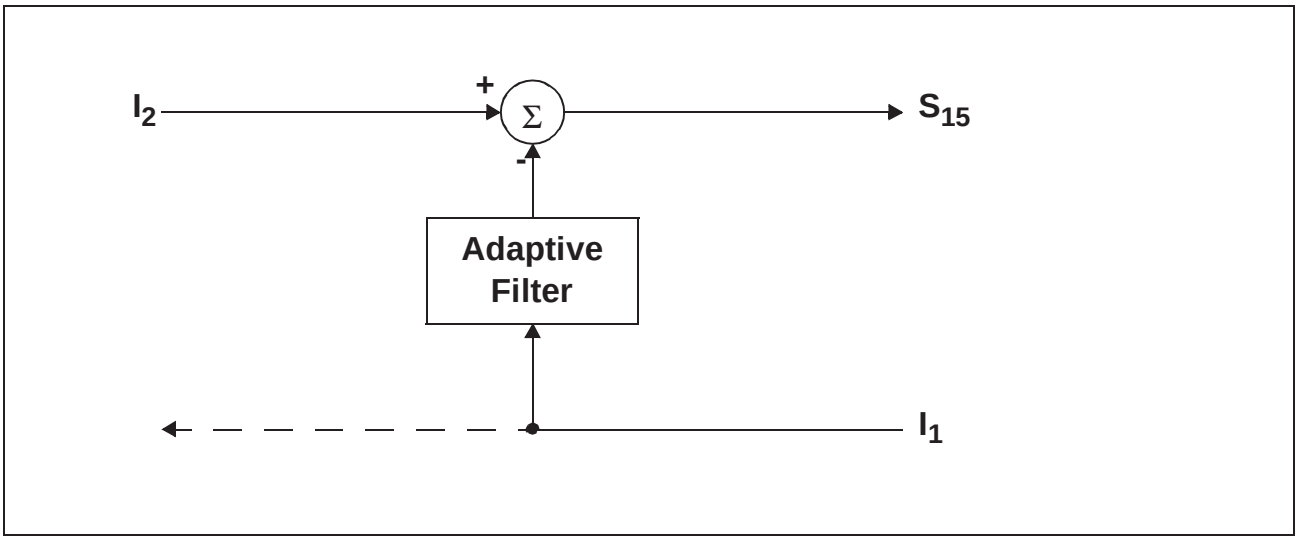


Figure 21
Line Echo Cancellation Unit - Block Diagram

The line echo canceller provides only one outgoing signal (S_{15}) as the other outgoing signal would be identical with the input signal I_1.

In normal mode the adaption process can be controlled by three parameters: MIN, ATT and MGN. Adaption takes only place if both of the following conditions hold:

1. $I1 > MIN$
2. $I1 - I2 - ATT + MGN > 0$

With the first condition adaption to small signals can be avoided. The second condition avoids adaption during double talk. The parameter ATT represents the echo loss provided by external circuitry. The adaption stops if the power of the received signal (I2) exceeds the power of the expected signal (I1-ATT) by more than the margin MGN.

Table shows the registers associated with the line echo canceller.

Table 10

Register	# of Bits	Name	Comment	Relevant Mode
LECCTL	1	EN	Line echo canceller enable	both

Table 10

LECCTL	1	MD	Line echo canceller mode	
LECCTL	5	I2	Input signal selection for I_2	both
LECCTL	5	I1	Input signal selection for I_1	both
LECLEV	15	MIN	Minimal power for signal I_1	normal
LECATT	15	ATT	Externally provided attenuation (I_1 to I_2)	normal
LECMGN	15	MGN	Margin for double talk detection	normal

2.1.5 DTMF Detector

Figure 22 shows a block diagram of the DTMF detector. The input signal can be preprocessed by a dial tone filter before it is fed to the recognition block. The dial tone filter increases the robustness of the recognition unit against call progess tones which may be coupled into the line. However, this filter also decreases the robustness of the recognition unit against speech.

The results of the detector are available in the status register and a dedicated result register that can be read via the serial control interface (SCI) by the external controller. All sixteen standard DTMF tones are recognized.

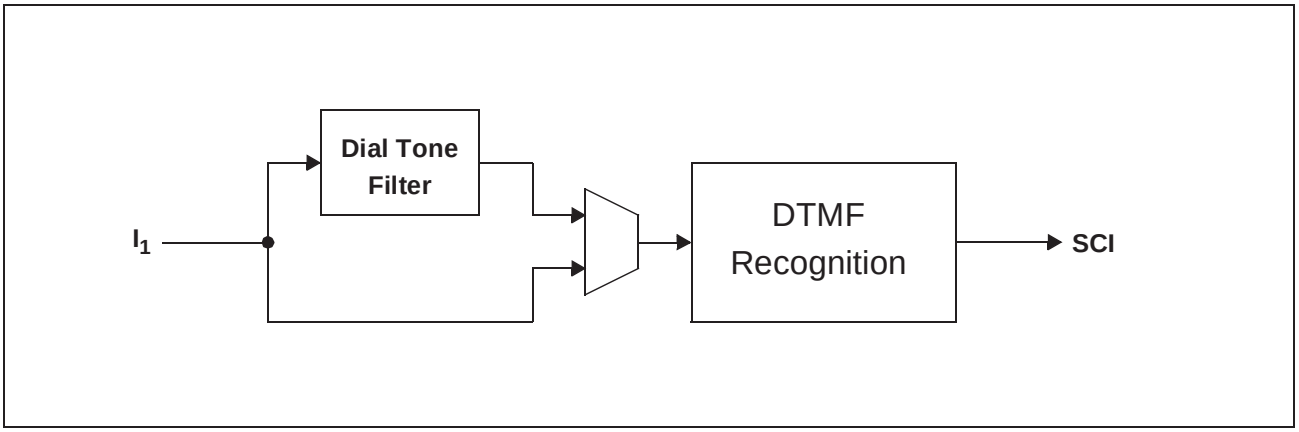


Figure 22
DTMF Detector - Block Diagram

Table 11 shows the supported modes and the input signal selection.

Table 11

Register	# of Bits	Name	Comment
DDCTL	1	END	DTMF detector enable
DDCTL	1	ENF	Dial tone filter enable
DDCTL	5	I1	Input signal selection

As soon as a valid DTMF tone is recognized, the status word and the DTMF tone code are updated (table 12).

Table 12

Register	# of Bits	Name	Comment
STATUS	1	DTV	DTMF code valid
DDCTL	5	DTC	DTMF tone code

DTV is set when a standard DTMF tone is recognized and reset when no DTMF tone is recognized or the detector is disabled. The code for the DTMF tone is placed into the register DDCTL.

The registers DDTW and DDLEV hold parameters for detection (table 13).

Table 13

Register	# of Bits	Name	Comment
DDTW	15	TWIST	Twist for DTMF recognition
DDLEV	6	MIN	Minimum signal level to detect DTMF tones

2.1.6 CNG Detector

The calling tone (CNG) detector can detect the standard calling tones of fax machines or modems. This helps to distinguish voice messages from data transfers. The result of the detector is available in the status register that can be read via the serial control interface (SCI) by the external controller. The CNG detector consists of two band-pass filters with fixed center frequency of 1100 Hz and 1300 Hz.

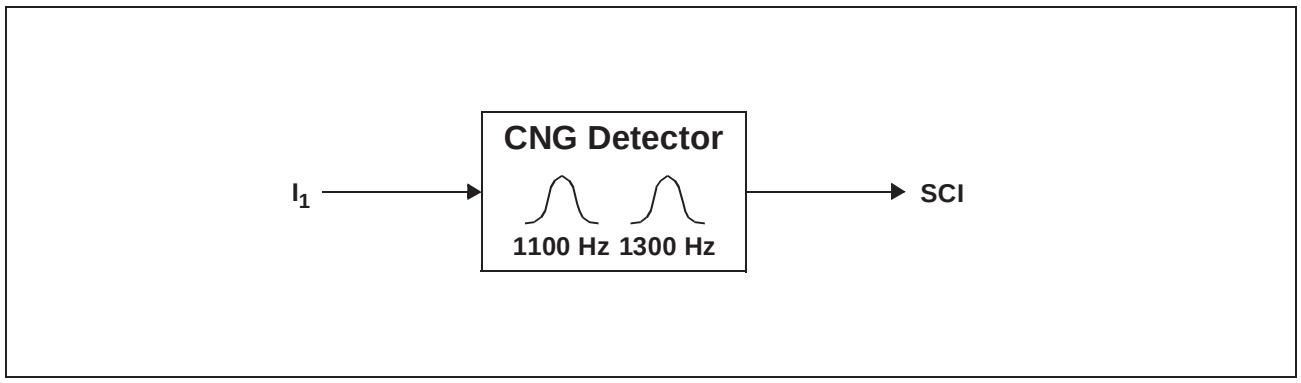


Figure 23
CNG Detector - Block Diagram

Table 14 shows the supported modes and the input signal selection.

Table 14

Register	# of Bits	Name	Comment
CNGCTL	1	EN	CNG detector enable
CNGCTL	5	I1	Input signal selection
CNGLEV	16	MIN	Minimum signal level
CNGBT	16	TIME	Minimum time of signal burst
CNGRES	16	RES	Input signal resolution

Both the programmed minimum time and the minimum signal level must be exceeded for a valid CNG tone. Furthermore the input signal resolution can be reduced by the RES parameter. This can be useful in a noisy environment at low signal levels although th accaracy of the detection decreases. As soon as a valid tone is recognized, the status word of the PSB 4860 is updated. The status bits are defined as follows:

Table 15

Register	# of Bits	Name	Comment
STATUS	1	CNG	Fax/Modem calling tone detected

2.1.7 Alert Tone Detector

The alert tone detector can detect the standard alert tones (2130 Hz and 2750 Hz) for caller id protocols. The results of the detector are available in the status register and the dedicated register ATDCTL0 that can be read via the serial control interface (SCI) by the external controller.

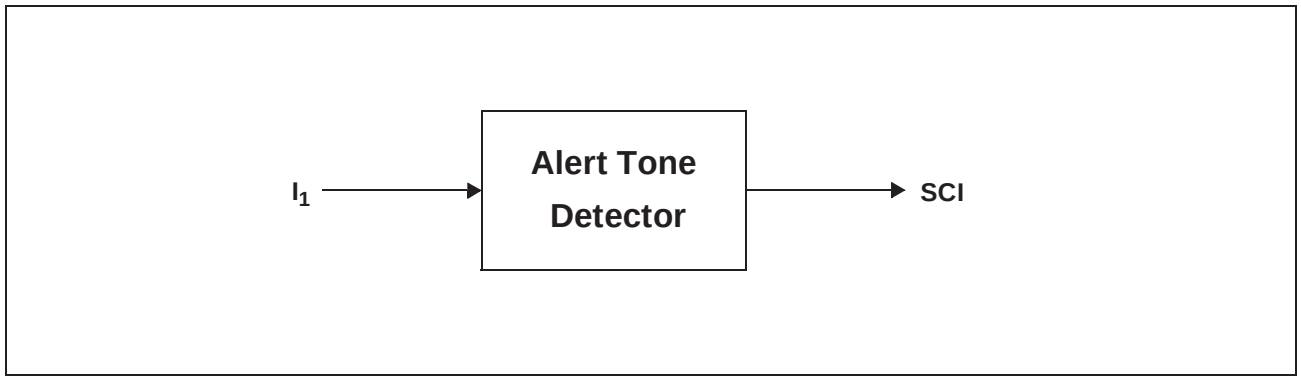


Figure 24
Alert Tone Detector - Block Diagram

Table 16

Register	# of Bits	Name	Comment
ATDCTL0	1	EN	Alert Tone Detector Enable
ATDCTL0	5	I1	Input signal selection
ATDCTL1	1	MD	Detection of dual tones or single tones
ATDCTL1	1	DEV	Maximum deviation (0.5% or 1.1%)
ATDCTL1	8	MIN	Minimum signal level to detect alert tones

As soon as a valid alert tone is recognized, the status word of the PSB 4860 and the code for the detected combination of alert tones are updated (table 17).

Table 17

Register	# of Bits	Name	Comment
STATUS	1	ATV	Alert tone detected
ATDCTL0	2	ATC	Alert tone code

2.1.8 CPT Detector

The selected signal is monitored continuously for a call progress tone. The CPT detector consists of a band-pass and an optional timing checker (figure 25).

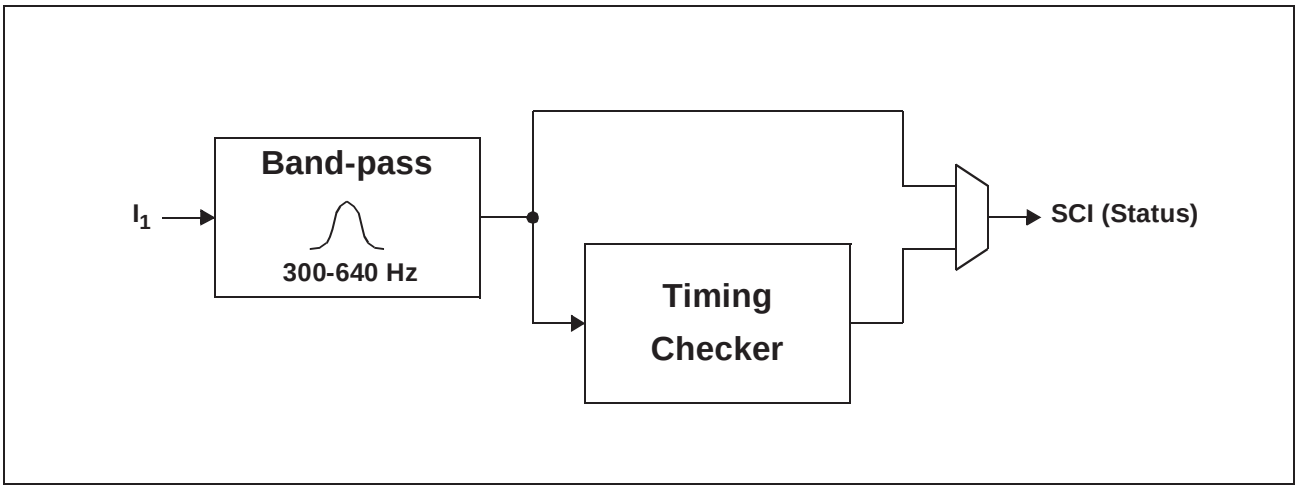


Figure 25
CPT Detector -Block Diagram

The CPT detector can be used in two modes: raw and cooked. In raw mode, the occurrence of a signal within the frequency, time and energy limits is directly reported. The timing checker is bypassed and therefore the PSB 4860 does not interpret the length or interval of the signal.

In cooked mode, the number and duration of signal bursts are interpreted by the timing checker. A signal burst followed by a gap is called a cycle. The CPT flag is set with the first burst after the programmed number of cycles has been detected. The CPT flag remains set until the unit is disabled, even if the conditions are not met anymore. In this mode the CPT is modelled as a sequence of identical bursts separated by gaps with identical length. The PSB 4860 can be programmed to accept a range for both the burst and the gap. It is also possible to specify a maximum aberration of two consecutive bursts (gaps). Figure 26 shows the parameters for a single cycle (burst and gap).

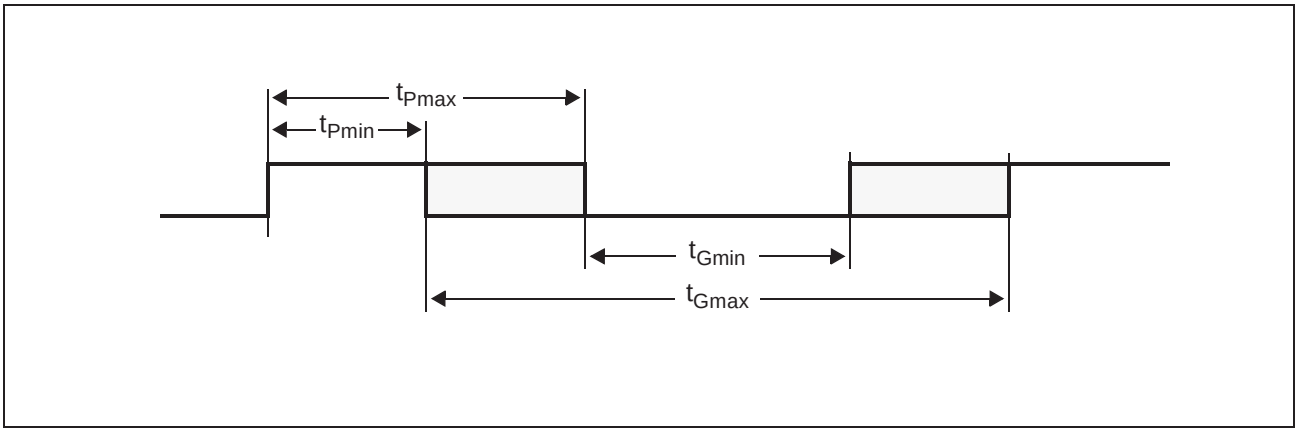


Figure 26

CPT - Cooked Mode

The status bit is defined as follows:

Table 18

Register	# of Bits	Name	Comment
STATUS	1	CPT	CP tone currently detected [340 Hz; 640 Hz]

CPT is not affected by reading the status word. It is automatically reset when the unit is disabled. Table 19 shows the control register for the CPT detector.

Table 19

Register	# of Bits	Name	Comment
CPTCTL	1	EN	Unit enable
CPTCTL	1	MD	Mode (cooked, raw)
CPTCTL	5	I1	Input signal selection
CPTMN	8	MINB	Minimum time of a signal burst (t_{Pmin})
CPTMN	8	MING	Minimum time of a signal gap (t_{Gmin})
CPTMX	8	MAXB	Maximum time of a signal burst (t_{Pmax})
CPTMX	8	MAXG	Maximum time of a signal gap (t_{Gmax})
CPTDT	8	DIFB	Maximum difference between consecutive bursts
CPTDT	8	DIFG	Maximum difference between consecutive gaps
CPTTR	3	NUM	Number of cycles (cooked mode), 0 (raw mode)
CPTTR	8	MIN	Minimum signal level to detect tones
CPTTR	4	SN	Minimal signal-to-noise ratio

If any condition is violated during a sequence of cycles the timing checker is reset and restarts with the next valid burst.

Note: In cooked mode CPT is set with the first burst after the programmed number of cycles has been detected. If CPTTR:NUM = 2, then CPT is set with the third signal burst.

Note: The number of cycles must be set to zero in raw mode.

2.1.9 Caller ID Decoder

The caller ID decoder is basically a 1200 baud modem (FSK, demodulation only). The bit stream is formatted by a subsequent UART and the data is available in a data register along with status information (figure 27).

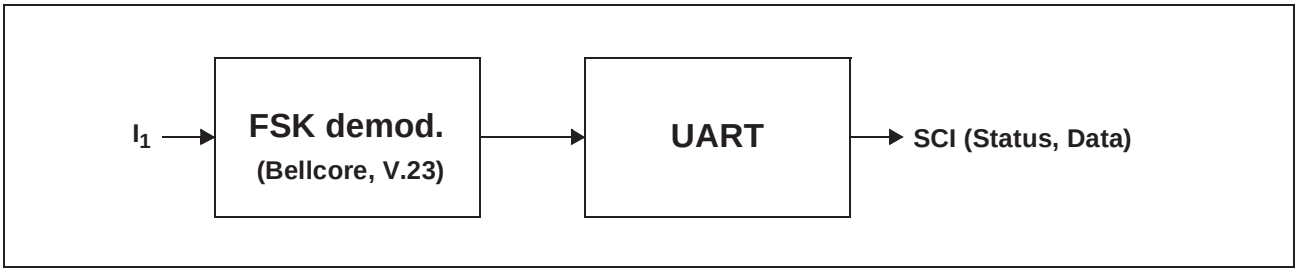


Figure 27
Caller ID Decoder - Block Diagram

The FSK demodulator supports two modes according to table 20. The appropriate mode is detected automatically.

Table 20

Mode	Mark (Hz)	Space (Hz)	Comment
1	1200	2200	Bellcore
2	1300	2100	V.23

The CID decoder does not interpret the data received. Each byte received is placed into the CIDCTL register (table 22). The status byte of the PSB 4860 is updated (table 21).

Table 21

Register	# of Bits	Name	Comment
STATUS	1	CIA	CID byte received
STATUS	1	CD	Carrier Detected

CIA and CD are cleared when the unit is disabled. In addition, CIA is cleared when CIDCTL0 is read.

Table 22

Register	# of Bits	Name	Comment
CIDCTL0	1	EN	Unit enable
CIDCTL0	5	I1	Input signal selection

Table 22

Register	# of Bits	Name	Comment
CIDCTL0	8	DATA	Last CID data byte received
CIDCTL1	5	NMSS	Number of mark/space sequences necessary for successful detection of carrier detect
CIDCTL1	6	NMB	Number of mark bits necessary before space of first byte after carrier detect
CIDCTL1	5	MIN	Minimum signal level for CID detection

When the CID unit is enabled, it first waits for a channel seizure signal consisting of a series of alternating space and mark signals. The number of spaces and marks that have to be received without errors before the PSB 4860 reports a carrier detect can be programmed.

Channel seizure must be followed by at least 16 continuous mark signals. The first space signal detected is then regarded as the start bit of the first message byte.

The interpretation of the data, including message type, length and checksum is completely left to the controller. The CID unit should be disabled as soon as the complete information has been received as it cannot detect the end of the transmission by itself.

Note: Some caller ID mechanism may require additional external components for DC coupling. These tasks must be handled by the controller.

Note: The controller is responsible for selecting and storing parts of the CID as needed.

2.1.10 DTMF Generator

The DTMF generator can generate single or dual tones with programmable frequency and gain. This unit is primarily used to generate the common DTMF tones but can also be used for signalling or other user defined tones. A block diagram is shown in figure 28.

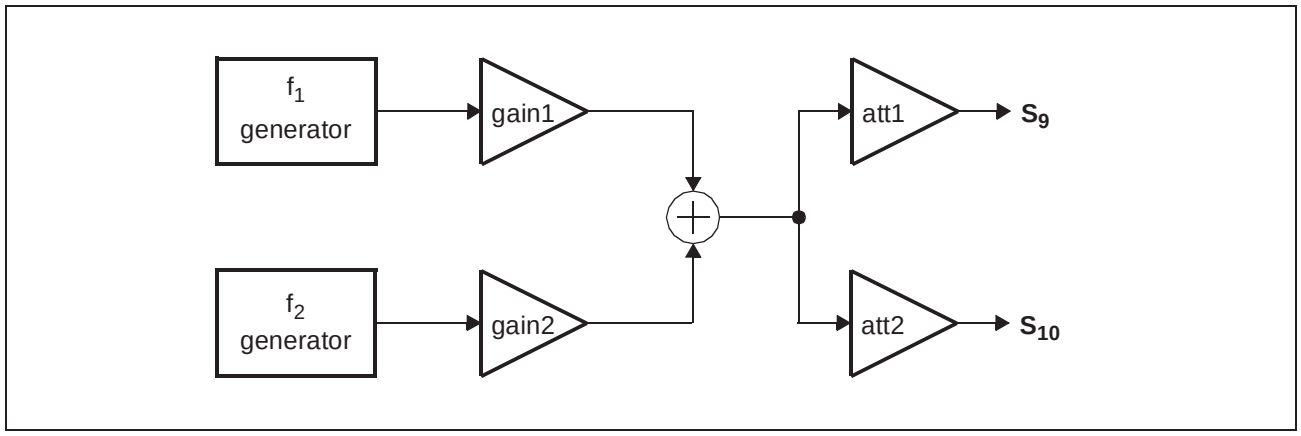


Figure 28
DTMF Generator - Block Diagram

Both generators and amplifiers are identical. There are two modes for programming the generators, cooked mode and raw mode. In cooked mode, DTMF tones are generated by programming a single 4 bit code. In raw mode, the frequency of each generator/ amplifier can be programmed individually by a separate register. The unit has two outputs which provide the same signal but with individually programmable attenuation. Table 23 shows the parameters of this unit.

Table 23

Register	# of Bits	Name	Comment
DGCTL	1	EN	Enable for generators
DGCTL	1	MD	Mode (cooked/raw)
DGCTL	4	DTC	DTMF code (cooked mode)
DGF1	15	FRQ1	Frequency of generator 1
DGF2	15	FRQ2	Frequency of generator 2
DGL	7	LEV1	Level of signal for generator 1
DGL	7	LEV2	Level of signal for generator 2
DGATT	8	ATT1	Attenuation of S_9
DGATT	8	ATT2	Attenuation of S_{10}

Note: DGF1 and DGF2 are undefined when cooked mode is used and must not be written.

2.1.11 Speech Coder

The speech coder (figure 29) has two input signals I_1 and I_2. The first signal (I_1) is fed to the coder while the second signal (I2) is used as a reference signal for voice controlled recording. The signal I_1 can be coded by either a High Quality coder or a Long Play coder.

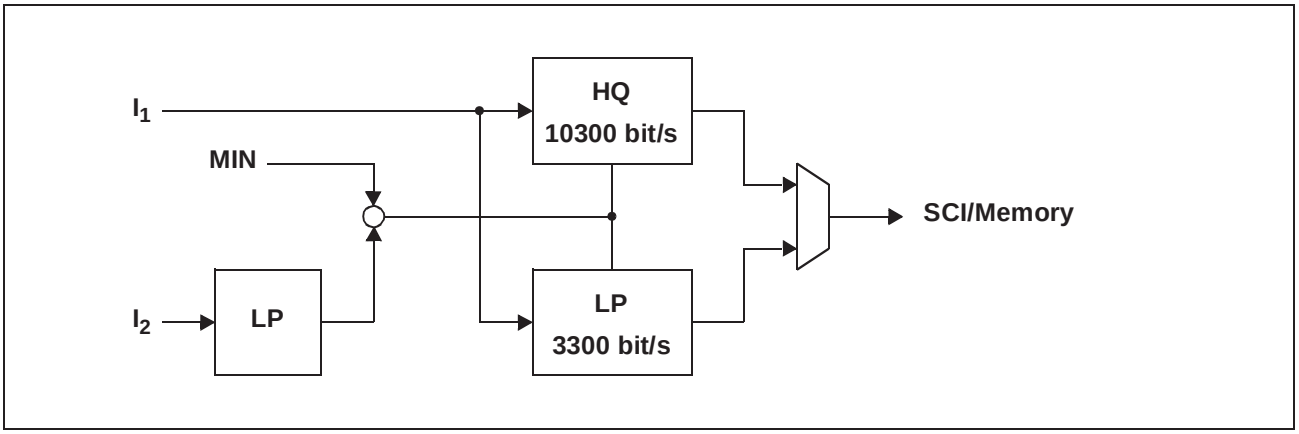


Figure 29
Speech Coder - Block Diagram

In High Quality the output data stream runs at a fixed rate of 10300 bit/s and provides excellent speech quality. In Long Play mode, the output data stream is further reduced to an average of 3300 bit/s while still maintaining good quality.

The output of the coder may be fed to the SCI interface or the memory interface. If the memory interface is selected, the data is written starting at the current file pointer and the file pointer is advanced as needed. If the SCI interface is selected, the data is written sequentially into the SCDATA register and the status word of the PSB 4860 is updated as shown in table 24 and table 25. The SDA bit is reset when SCDATA is read.

Table 24

Register	# of Bits	Name	Comment
STATUS	1	SDA	Speech data word available

Table 25

Register	# of Bits	Name	Comment
SCDATA	16		Data word

In case of any memory error (e.g. memory full) a file error is indicated and the coder is disabled. The controller must subsequently close the file.

The coder can be switched on the fly. However, it may take up to 60 ms until the switch is executed. The controller must therefore wait for at least this time until issuing another command that relies on the mode switch. No audio data is lost during switching.

The signal I_2 is first filtered by a low pass LP1 with programmable time constant and then compared to a reference level MIN. If the filtered signal exceeds MIN, then the status bit SD (table 26) is set immediately. If the filtered signal has been smaller than MIN for a programmable time TIME then the status bit SD is reset.

The coder can be enabled in permanent mode or in voice recognition mode. In permanent mode, the coder starts immediately and compresses all input data continuously. The current state of the status bit SD does not affect the coder.

In voice recognition mode, the coder is automatically started on the first transition of the status bit from 0 to 1. Once the coder has started it remains active until disabled.

Table 26

Register	# of Bits	Name	Comment
STATUS	1	SD	Speech detected

The operation of the speech coder is defined according to table 27.

Table 27

Register	# of Bits	Name	Comment
SCCTL	1	EN	Enable speech coder
SCCTL	1	HQ	High quality mode
SCCTL	1	VC	Voice controlled recording
SCCTL	1	DST	Destination selection (Memory or SCI)
SCCTL	5	I1	Input signal 1 selection
SCCTL	5	I2	Input signal 2 selection
SCCT2	8	MIN	Minimal signal level for speech detection
SCCT2	8	TIME	Minimum time for reset of SD
SCCT3	8	LP	Time constant for low-pass

Note: The peak data rate in LP mode is 4800 bit/s.

Note: Both HQ and LP mode will not produce identical bit streams after a coding/ decoding cycle.

2.1.12 Speech Decoder

The speech decoder (figure 30) decompresses the data previously coded by the speech coder unit and delivers a standard 128 kbit/s data stream.

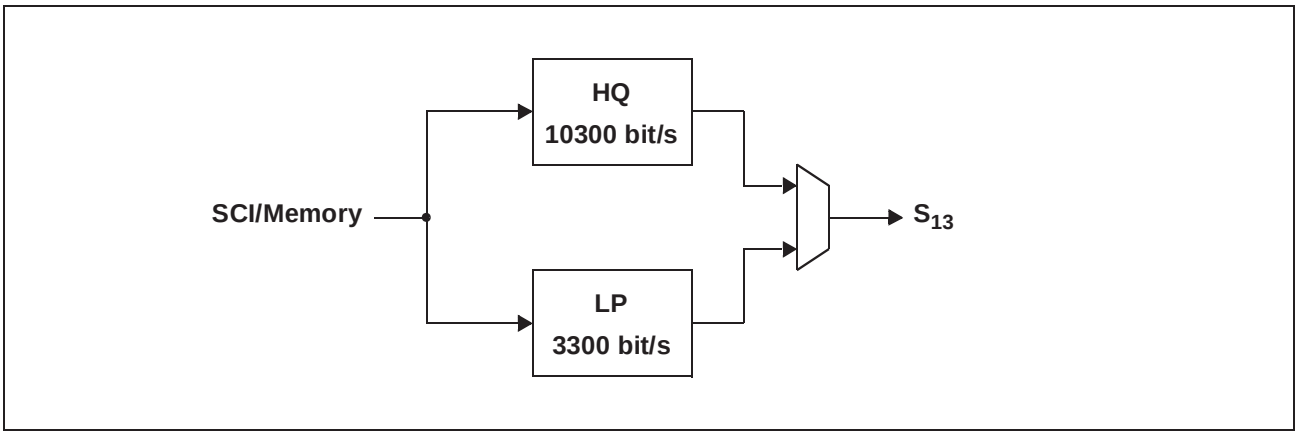


Figure 30
Speech Decoder - Block Diagram

The decoder supports fast (1.5 and 2.0 times) and slow (0.5 times) motion independent of the selected quality. The decoder requests input data as needed at a variable rate. Table 28 shows the signal and mode selection for the speech decoder.

Table 28

Register	# of Bits	Name	Comment
SDCTL	1	EN	Enable speech decoder
SDCTL	1	SRC	Selection of source (memory or SCI)
SDCTL	2	SPEED	Selection of playback speed

If the data is supplied by the external memory interface, reading starts at the location of the current file pointer. The file pointer is updated during speech decoding. If the end of the file is reached, the decoder is automatically disabled. If the data is supplied by the SCI interface, the data is taken from the SDDATA register according to table 29.

Table 29

Register	# of Bits	Name	Comment
SDDATA	16		Data word

The status register is used to indicate if new data is needed (table 30). As the decoder prefetches data, it will request data bytes prior to delivering the associated output stream.

Table 30

Register	# of Bits	Name	Comment
STATUS	1	DRQ	Request for new data

When the speech decoder is disabled it supplies silence and DRQ is reset. Speed changes can be done while the decoder is running.

2.1.13 Analog Interface

There are two identical interfaces at the analog side (to PSB 4851) as shown in figure 31.

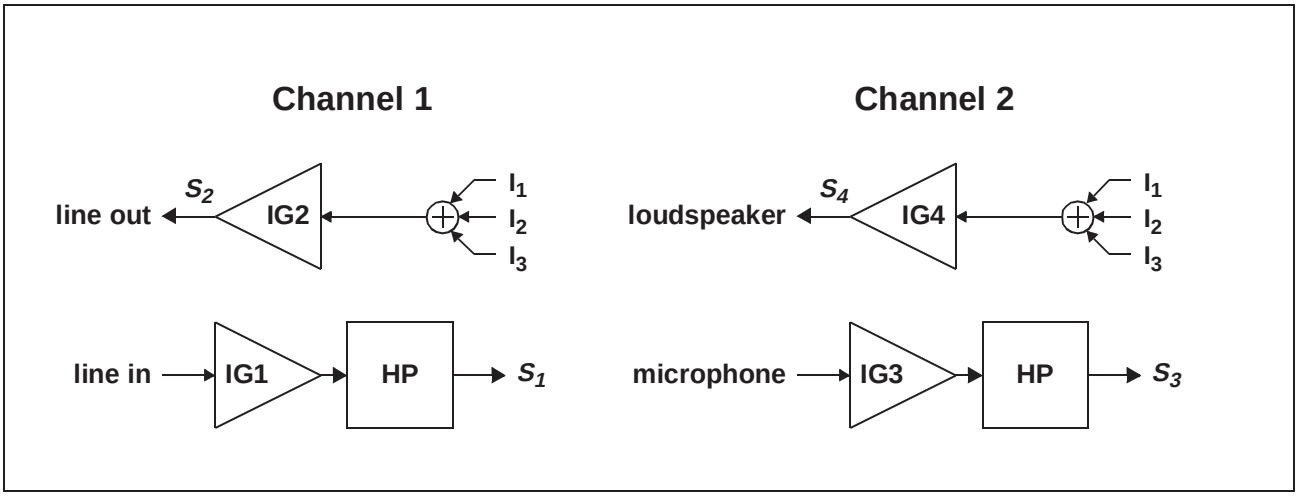


Figure 31
PSB 4851 Interface - Block Diagram

For each signal an amplifier is provided for level adjustment. The ingoing signals can be passed through an optional high-pass (HP). Furthermore, up to three signals can be mixed in order to generate the outgoing signals (S_2,S_4). Table 31 shows the associated registers.

Table 31

Register	# of Bits	Name	Comment
IFG1	16	IG1	Gain for IG1
IFG2	16	IG2	Gain for IG2
IFS1	1	HP	High-pass for S_1
IFS1	5	I1	Input signal 1 for IG2
IFS1	5	I2	Input signal 2 for IG2
IFS1	5	I3	Input signal 3 for IG2
IFG3	16	IG3	Gain for IG3
IFG4	16	IG4	Gain for IG4
IFS2	1	HP	High-pass for S_3
IFS2	5	I1	Input signal 1 for IG4
IFS2	5	I2	Input signal 2 for IG4
IFS2	5	I3	Input signal 3 for IG4

2.1.14 Digital Interface

There are two almost identical interfaces at the digital side as shown in figure 32. The only difference between these two interfaces is that only channel 1 supports the SSDI mode.

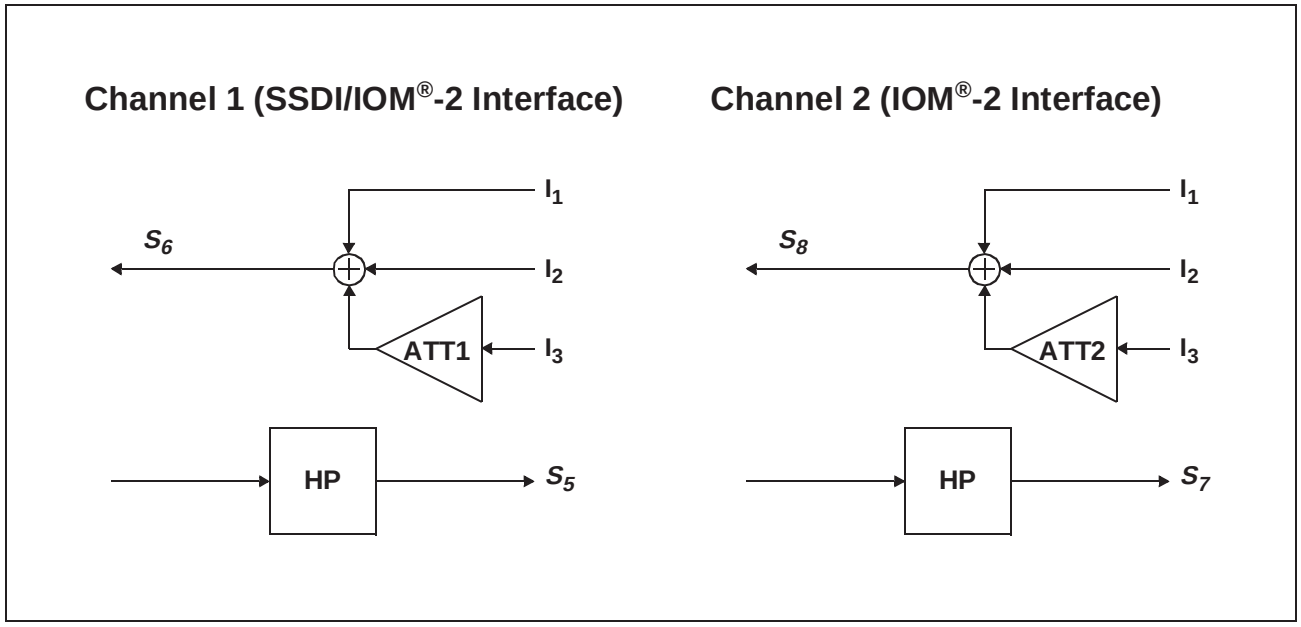


Figure 32
Digital Interface - Block Diagram

Each outgoing signal can be the sum of two signals with no attenuation and one signal with programmable attenuation (ATT). The attenuator can be used for artificial echo loss. Each input can be passed through an optional high-pass (HP). The associated registers are shown in table 32.

Table 32

Register	# of Bits	Name	Comment
IFS3	5	I1	Input signal 1 for S_6
IFS3	5	I2	Input signal 2 for S_6
IFS3	5	I3	Input signal 3 for S_6
IFS3	1	HP	High-pass for S_5
IFS4	5	I1	Input signal 1 for S_8
IFS4	5	I2	Input signal 2 for S_8
IFS4	5	I3	Input signal 3 for S_8
IFS4	1	HP	High-pass for S_7

Table 32

Register	# of Bits	Name	Comment
IFG5	8	ATT1	Attenuation for input signal I3 (Channel 1)
IFG5	8	ATT2	Attenuation for input signal I3 (Channel 2)

2.1.15 Universal Attenuator

The PSB 4860 contains an universal attenuator that can be connected to any signal (e.g. for sidetone gain).

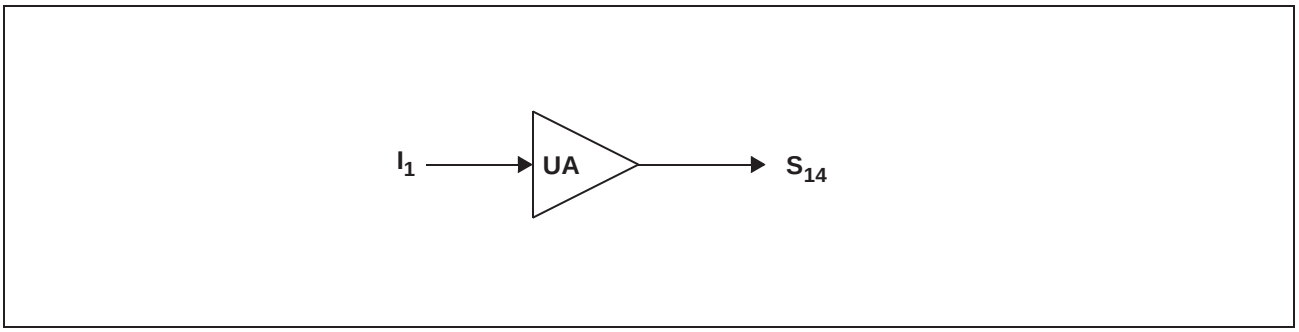


Figure 33
Universal Attenuator - Block Diagram

Table 33 shows the associated register.

Table 33

Register	# of Bits	Name	Comment
UA	8	ATT	Attenuation for UA
UA	5	I1	Input signal for UA

2.1.16 Automatic Gain Control Unit

In addition to the universal attenuator with programmable but fixed gain the PSB 4860 contains an amplifier with automatic gain control (AGC). The AGC is preceeded by a signal summation point for two input signals. One of the input signals can be attenuated.

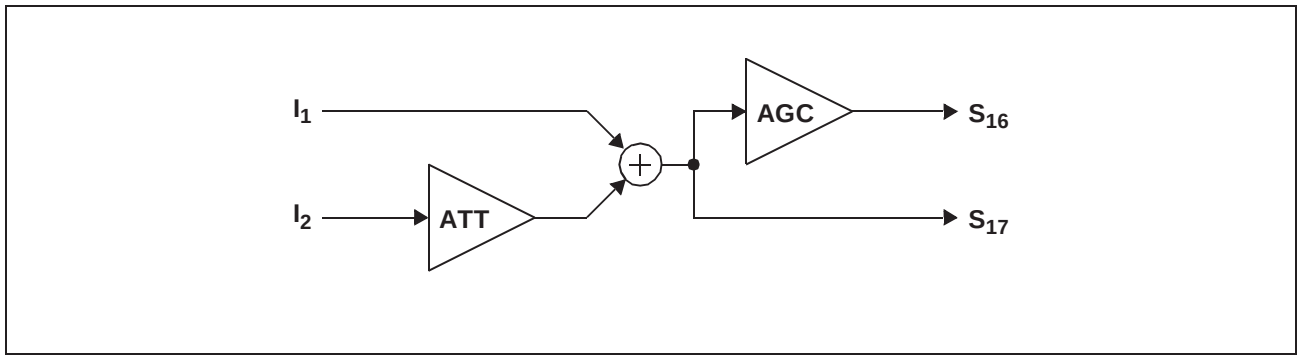


Figure 34
Automatic Gain Control Unit - Block Diagram

Furthermore the signal after the summation point is available. Besides providing a general signal summation (S_{16} not used) this signal is especially useful if the AGC unit provides the input signal for the speech coder. In this case S_{17} can be used as a reference signal for voive controlled recording.

The operation of the AGC is similar to AGCX (ACCR) of the speakerphone. The differences are as follows:

- No NOIS parameter
- Separate enable/disable control
- Slightly different coefficient format

Furthermore the AGC contains a comparator that starts and stops the gain regulation. The signal after sthe summation point (S17) is filtered by a low pass with time constant DEC an then compared to a programmable limit LIM. Regulation takes only place when the filtered signal exceed the limit.

Table 34 shows the associated registers.

Table 34

Register	# of Bits	Name	Comment
AGCCTL	1	EN	Enable
AGCCTL	5	I1	Input signal 1 for AGC
AGCCTL	5	I2	Input signal 2 for AGC
AGCATT	15	ATT	Attenuation for I_2
AGC1	8	AG_INIT	Initial AGC gain/attenuation

Table 34

Register	# of Bits	Name	Comment
AGC1	8	COM	Compare level rel. to max. PCM-value
AGC2	8	SPEEDL	Change rate for lower levels
AGC2	8	SPEEDH	Change rate for higher level
AGC3	8	AG_ATT	Attenuation range
AGC3	7	AG_GAIN	Gain range
AGC4	7	DEC	Comparator low pass time constant
AGC4	8	LIM	Comparator minimal signal level
AGC5	7	LPA	AGC low pass time constant

2.1.17 Equalizer

The PSB 4860 also provides an equalizer that can be inserted into any signal path. The main application for the equalizer is the adaption to the frequency characteristics of the microphone, transducer or loudspeaker.

The equalizer consists of an IIR filter followed by an FIR filter as shown in figure 35.

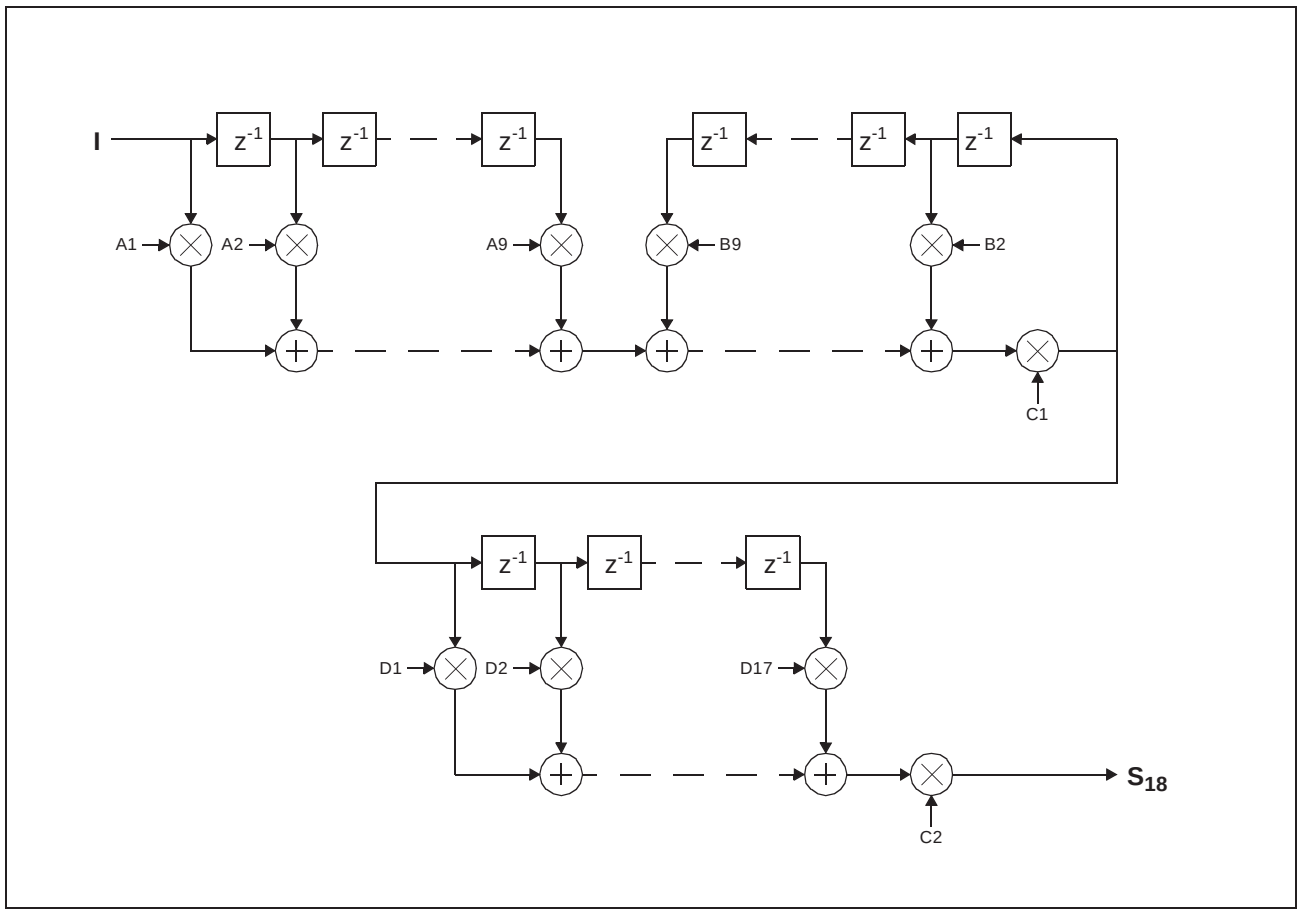


Figure 35
Equalizer - Block Diagram

The coefficients A_1-A_9, B_2-B_9 and C_1 belong to the IIR filter, the coefficients D_1-D_{17} and C_2 belong to the FIR filter. Table 35 shows the registers associated with the equalizer.

Table 35

Register	# of Bits	Name	Comment
FCFCTL	1	EN	Enable
FCFCTL	5	I	Input signal for equalizer
FCFCTL	6	ADR	Filter coefficient address
FCFCOF	16		Filter coefficient data

Due to the multitude of coefficients the uses an indirect addressing scheme for reading or writing an individual coefficient. The address of the coefficient is given by ADR and the actual value is read or written to register FCFCOF.

In order to ease programming the PSB 4860 automatically increments the address ADR after each access to FCFCOF.

Note: Any access to an out-of-range address automatically resets FCFCTL:ADR.

2.2 Memory Management

This section describes the memory management provided by the PSB 4860. As figure 36 shows, three units can access the external memory. During recording, the speech coder can write compressed speech data into the external memory. For playback, the speech decoder reads compressed speech data from external memory. In addition, the microcontroller can directly access the memory by the SCI interface.

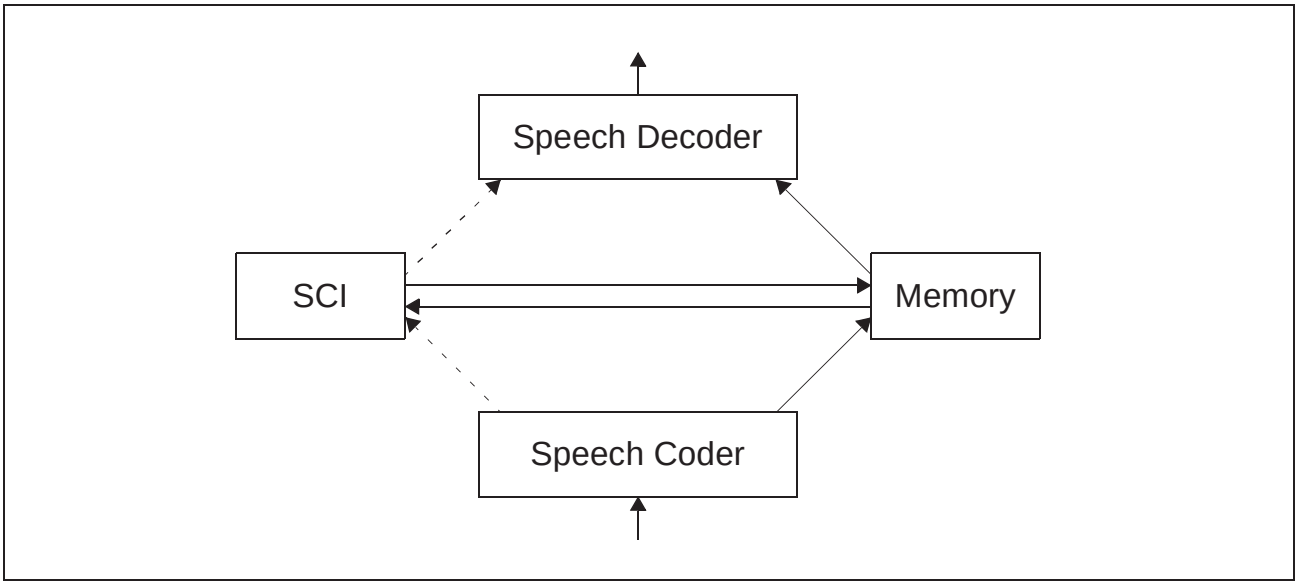


Figure 36
Memory Management - Data Flow

The memory is organized as a file system. For each memory space (R/W-memory and voice prompt memory) the PSB 4860 maintains a directory with up to 254 file descriptors (figure 37). In addition, the directory for the voice prompt memory can contain an entry for a special phrase file.

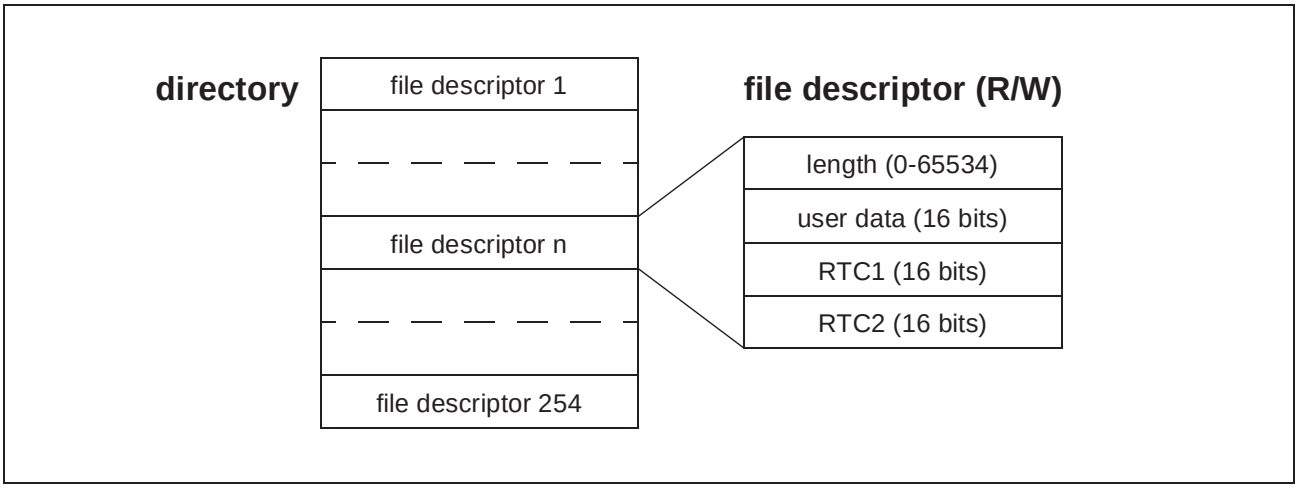


Figure 37
Memory Management - Directory Structure

The directories must be created after each power failure for volatile R/W-memory. All file descriptors are cleared (all words zero). For non-volatile memory, the directories have to be created only once. If the directories already exist, the memory has just to be activated after a reset. The file descriptors are not changed in this case.

All commands that access the other fields or involve a write access must not be used in voice prompt memory space.

2.2.1 File Definition and Access

A file is a linear sequence of units and can be accessed in two modes: binary and audio. In binary mode, a unit is a word. In audio mode, a unit is a variable number of words representing 30 ms of uncompressed speech. A file can contain at most 65534 units. Figure 38 shows an audio file containing 100 audio units. The length of the message is therefore 3 s.

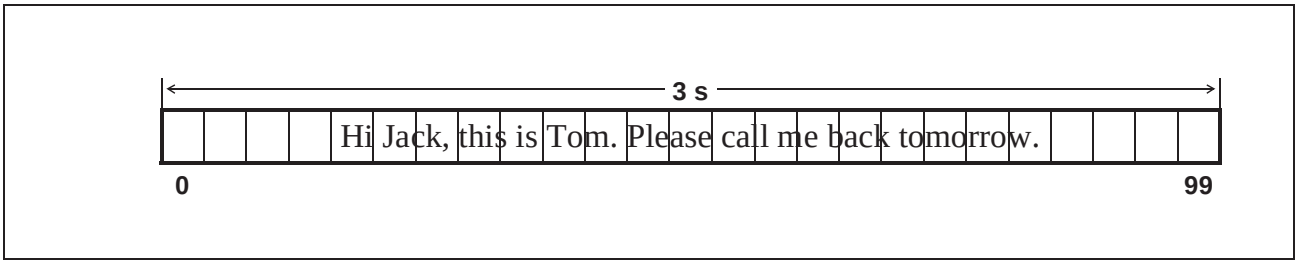


Figure 38
Audio File Organization - Example

Figure 39 shows a binary file of 11 words containing a phonebook (with only two entries).

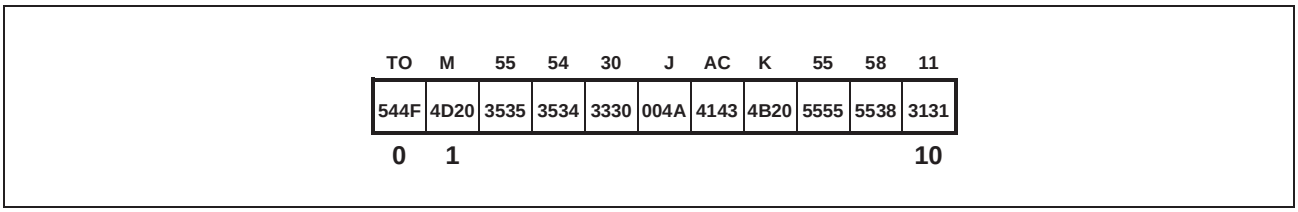


Figure 39
Binary File Organization - Example

There is one special file in the voice prompt directory (referenced by file number 255) which is intended for a large number of phrases and hence has a different organization.This file exists only in the directory for the voice prompt memory. It consists of up to 2048 phrases of arbitrary inividual length. The actual number of units within an individual phrase is determined during creation and cannot be altered afterwards. Phrases can be combined in any sequence without intermediate noise or gaps.

Figure 40 shows a phrase file containing a total of five phrases.

Figure 40
Phrase File Organization - Example

Before an access to a file can take place, the file must be opened with the following information:

1. memory space
2. file number
3. access mode

These parameters remain effective until the next open command is given or, in case of the file pointer, until a file access. All other files are closed and cannot be accessed. The file with file number 0 is not a physical file. Opening this file closes all physical files.

The PSB 4860 provides four registers for file access and two bits within the STATUS register. Table 36 shows these registers.

Table 36

Register	# of Bits	Comment
FCMD	16	Command to execute
FCTL	16	Access mode and file number
FDATA	16	Data transfer and additional parameters
FPTR	16 (11)	File pointer (phrase selector)
STATUS	16	Busy and Error indication

The status register contains two flags (table 37) to indicate if currently a file command is running and if the last file command terminated without error. A new command should only be written to FCMD if no command is running.

Table 37

Register	# of Bits	Name	Comment
STATUS	1	BSY	File command still running
STATUS	1	ERR	File command completed/aborted with error

Writing to FCMD also resets the error bit in the status register.

Table 38 shows the parameters defining the access mode and the access location. All parameters can only be written when no file command is currently running. They become effective after the completion of an open command. If another unit (e.g. speech coder) accesses the file, the file pointer is updated automatically. Therefore the controller can monitor the progess of recording or playing by reading the file pointer.

Table 38

Register	# of Bits	Name	Comment
FCTL	1	MS	Memory space (R/W or voice prompt)
FCTL	1	MD	Access mode (audio or binary)
FCTL	1	TS	Write timestamp (file open only)
FCTL	8	FNO	File number (active file)
FPTR	16		File pointer or phrase selector

Commands are written to the FCMD register and start within 30 ms. The busy bit is set immediately, however. Some commands require additional parameters which are written prior to the command into the specified registers. Data transfer is done by the register FDATA (both reading and writing).

2.2.2 User Data Word

The user data word consists of 12 bits that can be read or written by the user and four read-only bits (D,M) which indicate the status of a file.

15					0
D	M	0	0	User Definable	

If D is set, the file is marked for deletion and should not be used any more. This bit is maintained by the PSB 4860 for housekeeping.

2.2.3 Initialize

This command creates a directory, sets the external memory configuration and delivers the size of usable memory in 8 kB blocks. Furthermore the voice prompt memory space is scanned for a valid directory. The PSB 4860 can either create a completely empty directory from scratch or leave the first FNO-1 files of an existing directory untouched while clearing the remaining files. The latter option is useful if due to an unexpected event like a sudden power loss during recording some data is corrupted. In that case vital system information can still be recovered provided that it has been stored in the first files (e.g. file 1).

Table 39
Initialize Memory Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Initialize or Activate command code
FCMD	1	IN	Confirmation for Initialization (must be set for Initialize)
FCTL	8	FNO	First file to be cleared (255 for Flash)
CCTL	2	MT	Type of R/W memory (DRAM, Flash)
CCTL	1	MQ	Quality of R/W memory (Audio, Normal)
CCTL	1	MV	Voice memory available

Table 40
Initialize Memory Results

Register	# of Bits	Name	Comment
FDATA	16		Number of usable 8 kB blocks in R/W memory

Possible Errors:

- no R/W memory found

2.2.4 Activate

This command activates an existing directory, sets the external memory configuration and delivers the size of usable memory in 8 kB blocks. Furthermore the voice prompt memory space is scanned for a valid directory. Upon activation the PSB 4860 checks (in case of ARAM/DROM only) the consistency of the directory in R/W memory space. It returns the first file that contains corrupted data (if any). If corrupted data is detected an initialization should be perfomed with the same file number as an input parameter.

Table 41
Acivate Memory Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Initialize or Activate command code
CCTL	2	MT	Type of R/W memory (DRAM, Flash)
CCTL	1	MQ	Quality of R/W memory (Audio, Normal)
CCTL	1	MV	Voice memory available

Table 42
Activate Memory Results

Register	# of Bits	Name	Comment
FDATA	16		Number of usable 8 kB blocks in R/W memory
FCTL	8	FNO	First corrupted file (0 if none or Flash)

2.2.5 Open File / Open Next Free File

A file is opened for subsequent accesses with the specified access mode. Opening a new file automatically closes the currently open file an clears the file pointer. Opening file number 0 can be used to close all physical files. If the TS flag is set, the current content of RTC1 and RTC2 is written to the appropriate fields of the file descriptor in order to provide a timestamp. The Open File commands opens the file specified by the file number. The Open Next Free File command searches for the next free (unused) file starting with the current file number. If a free file has been found, the file is opened and the filenumber written into FCTL:FNO. Otherwise an error is reported.

Table 43
Open File Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Open / Open Next Free File command code
FCTL	1	MS	Memory space (R/W, voice prompt)
FCTL	1	MD	Access mode (audio or binary)
FCTL	1	TS	Write timestamp
FCTL	8	FNO	File number <fno> (Open File) Starting point (Open Next Free File)

Table 44
Open Next Free File Results

Register	# of Bits	Name	Comment
FCTL	8	FNO	File number

Possible error conditions:

- <fno> invalid
- memory space invalid
- no unused file found

Note: In case of flash memory existing ones cannot be altered. Therefore TS should be set only once during the lifetime of a file.

2.2.6 Seek

The file pointer of the currently opened file is set to the specified position. If the current file is the phrase file the PSB 4860 starts the speech decoder immediately after the seek is finished. This is done by simply enabling the decoder. All other settings of the decoder remain unaffected.

Table 45
Seek Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Seek command code
FPTR	16 (11)		File pointer (phrase selector)

Possible error conditions:

- <fno> invalid
- File pointer out of range

2.2.7 Cut File

All units after the unit addressed by the filepointer are removed from the file. The removed units are available for allocation after garbage collection again. If all units are deleted the file is marked for deletion (see user data word). However, the associated file descriptor and memory space are released only after a subsequent garbage collection. Binary files can be only deleted completely.

Table 46
Cut File Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Cut command code
FPTR	16		Position of first unit to delete (0 for binary files)

Possible error conditions:

- <fno> invalid
- File pointer out of range
- Phrase file selected

2.2.8 Compress File

An audio file that has been recorded in HQ mode can be recoded using LP mode. This reduces the file size to approximately one third of the original size. The speech quality, however, is somewhat lower compared to a signal that has been recorded in LP mode in the first place. This command can be aborted at any time an resumed later without loss of information. Table 47 shows the parameters for this command.

Table 47
Compress File Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Compress command code
FCTL	8	FNO	File number <fno>

Possible error conditions:

- <fno> invalid

2.2.9 Access File Descriptor

By this command the length, user data word and RTC1/RTC2 of a file descriptor can be read. The user data word can also be written. The file or the other entries of the file descriptor are not affected by this command.

Table 48
Access File Descriptor Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Read Access or Write Access command code
FDATA	16		User data (write access only)

Table 49
Access File Descriptor Results

Register	# of Bits	Name	Comment
FDATA	16		Content of selected entry (read access only)

Possible error conditions:

- <fno> invalid

Note: In case of flash memory existing ones cannot be altered.

2.2.10 Memory Status

This command returns the number of available 8 kB blocks in R/W memory space. This command should be preceded by a garbage collection.

Table 50
Memory Status Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Memory status code

Table 51
Memory Status Results

Register	# of Bits	Name	Comment
FDATA	16	FREE	Number of free blocks

2.2.11 Read/Write Data

These commands can be used in binary access mode only. For a read access, a single word is read at the position given by the file pointer. For a write access, a single word is written at the position of the file pointer. The file pointer is advanced by one word automatically. Note, that for FLASH memory only zeroes can be overwritten by ones. This restriction occurs only if an already used value within an existing file is to be overwritten.

Table 52
Read/Write Data Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Access Mode Command Code (including mode)
FDATA	16		Data word (write access only)

Table 53
Read/Write Data Results

Register	# of Bits	Name	Comment
FDATA	16		Data word (read access only)

Possible error conditions:

- <fno> invalid
- File pointer out of range
- Phrase file selected

2.2.12 Garbage Collection

This command initiates a garbage collection of. Until a garbage collection files that are marked for deletion still occupy the associated file descriptor and memory space. After the garbage collection these file descriptors and the associated memory space are available again. This command can optionally remap the directory. In this mode the remaining file descriptors are remapped to form a contiguous block starting with file number 1. The original order is preserved. This command requires that all files are closed, i.e. file 0 is opened. Independently of the selected directory only the read/write directory is used.

Table 54
Garbage Collection Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Garbage Collection Command Code
FCMD	1	RD	Remap Directory

Possible error conditions:

- file open

2.3 Miscellaneous

2.3.1 Real Time Clock

The PSB 4860 supplies a real time clock which maintains time with a resolution of a second and a range of up to a year. There are two registers which contain the current time and date (table 55).

Table 55

Register	# of Bits	Name	Comment
RTC1	6	SEC	Seconds elapsed
RTC1	6	MIN	Minutes elapsed
RTC2	5	HR	Hours elapsed
RTC2	11	DAY	Days elapsed

Both registers can be set to an arbitrary value. The real time clock maintains time during normal mode and power down mode only if the auxiliary oscillator OSC is running and the RTC is enabled.

Note: Writing out-of-range values to RTC1 and RTC2 results in undefined operation of the RTC

2.3.2 SPS Control Register

The two SPS outputs (SPS_0, SPS_1) can be used as either general purpose outputs, speakerphone status outputs or as status register outputs. Table 56 shows the associated register.

Table 56

Register	# of Bits	Name	Comment
SPSCTL	1	SP0	Output Value of SPS_0
SPSCTL	1	SP1	Output Value of SPS_1
SPSCTL	3	MODE	Mode of Operation
SPSCTL	4	POS	Position for status register window

When used as status register outputs, the status register bit at position POS appears at SPS_0 and the bit at position POS+1 appears at SPS_1.

2.3.3 Reset and Power Down Mode

The PSB 4860 can be in either reset mode, power down mode or active mode. During reset the PSB 4860 clears the hardware configuration registers and stops both internal and external activity. The address lines MA_0-MA_{15} provide a weak low until they are actually used as address lines (strong outputs) or auxiliary port pins (I/O). In reset mode the hardware configuration registers can be read and written. With the first access to a read/write register the PSB 4860 enters active mode. In this mode the main oscillator is running and normal operation takes place. By setting the power down bit (PD) the PSB 4860 can be brought to power down mode.

Table 57

Register	# of Bits	Name	Comment
CCTL	1	PD	power down mode

In power down mode the main oscillator is stopped. Depending on the configuration (ARAM/DRAM, APP) the PSB 4860 may still generate external activity (e.g. refresh). The PSB 4860 enters active mode again upon an access to a read/write register. Figure 41 shows a state chart of the modes of the PSB 4860.

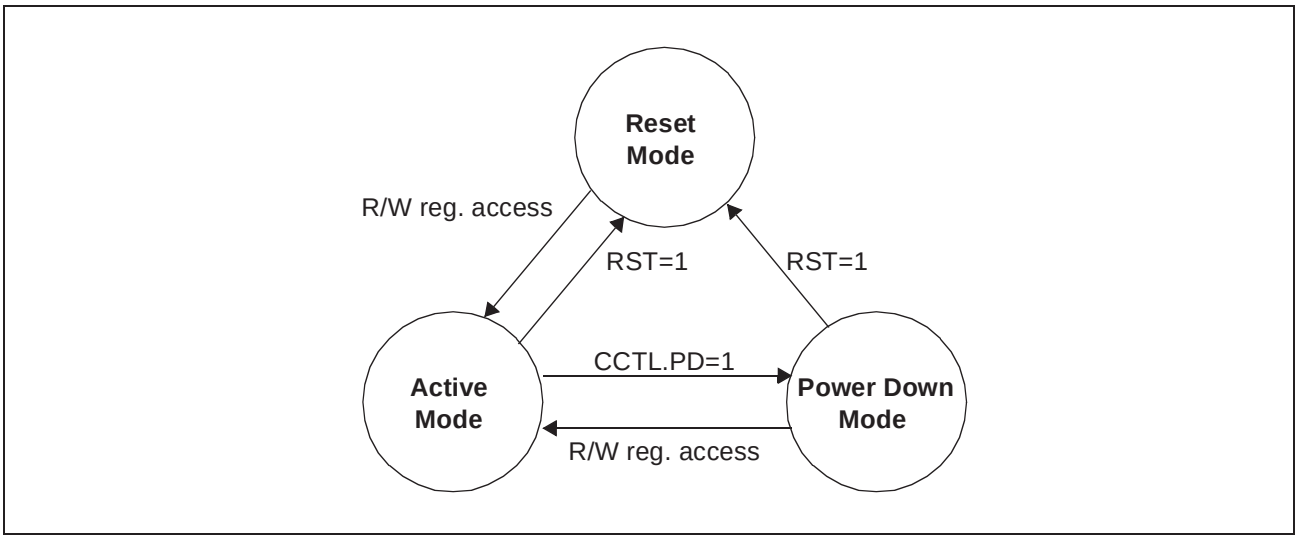


Figure 41
Operation Modes - State Chart

2.3.4 Interrupt

The PSB 4860 can generate an interrupt to inform the host of an update of the STATUS register according to table 58. An interrupt mask register (INTM) can be used to disable or enable the interrupting capability of each bit of the STATUS register except ABT individually.

Table 58

STATUS (old)	STATUS (new)	Set by	Reset by
RDY=0	RDY=1	Command completed	Command issued
DRQ=0	DRQ=1	Speech decoder requests data	SCDATA written
SDA=0	SDA=1	Speech coder delivers data	SDDATA read
CIA=0	CIA=1	New Caller ID byte available	CIDCTL0 read
CD=0	CD=1	Carrier detected	Carrier lost
CD=1	CD=0	Carrier lost	Carrier detected
CPT=0	CPT=1	Call progress tone detected	CPT lost
CPT=1	CPT=0	Call progress tone lost	CPT detected
CNG=0	CNG=1	Fax calling tone detected	CNG lost
DTV=0	DTV=1	DTMF tone detected	DTMF tone lost
DTV=1	DTV=0	DTMF tone lost	DTMF tone detected
ATV=0	ATV=1	Alert tone detected	Alert tone lost
ATV=1	ATV=0	Alert tone lost	Alert tone detected
BSY=1	BSY=0	File command completed	New command issued
SD=0	SD=1	Speech activity detected	Speech activity lost
SD=1	SD=0	Speech activity lost	Speech activity detected

An interrupt is internally generated if any combination of these events occurs an. The interrupt is cleared when the host reads the STATUS register. If a new event occurs while the host reads the status register, the status register is updated *after* the current access is terminated and a new interrupt is generated immediately after the access has ended.

2.3.5 Abort

If the PSB 4860 detects a corrupted configuration (e.g. due to a transient loss of power) it stops operation and initializes all read/write registers to their reset state. If a file was open it is closed and the file descriptor remains unmodified. For a new file that was just written this results in a file descriptor with length zero and marked for deletion. After that it sets the ABT bit of the STATUS register, generates an interrupt and goes into power down mode. The PSB 4860 discards all commands with the exception of a write command to the revision register while ABT is set. Only after the write command to the revision register (with any value) the ABT bit is reset and a reinitialization can take place.

2.3.6 Revision Register

The PSB 4860 contains a revision register. This register is read only and does not influence operation in any way. A write to the revision register clears the ABT bit of the STATUS register but does not alter the content of the revision register.

2.3.7 Hardware Configuration

The PSB 4860 can be adapted to various external hardware configurations by four special registers: HWCONFIG0 to HWCONFIG3. These registers are usually only written once during initialization and must not be changed while the PSB 4860 is in active mode. It is mandatory that the programmed configuration reflects the external hardware for proper operation. Special care must be taken to avoid I/O conflicts or excess current by enabling inputs without an external driving source. Table 59 can be used as a checklist.

Table 59

Name	Value	Check
$\overline{\text{PFRDY}}$	1	FRDY must not float
OSC	1	OSC1/2 must be connected to a crystal
ACS	1	CLK must not float (tie low if no clock present)
MFS	1	FSC must not float (tie low if no clock present)
ACT	1	FSC must not float (tie low if no clock present)

2.3.8 Frame Synchronization

The PSB 4860 locks itself to either an externally supplied clock or frame sync signal or generates the frame sync signal itself. This internal reference frame sync signal is called master frame sync (MFSC). In addition, the PSB 4860 can derive the AFECLK and AFEFSC from either the main oscillator or an auxiliary clock input. Table 60 shows how AFECLK and MFSC are derived by the PSB 4860. The bits ACS and MFS are contained in the hardware configuration registers.

Table 60

ACS	MFS	AFECLK	MFSC	Application
0	0	XTAL	AFEFSC	Analog featurephone
0	1	-	FSC	ISDN stand-alone
1	0	CLK	AFEFSC	DECT
1	1	CLK	FSC	unused

2.3.9 AFECLK Tracking

The PSB 4860 can adjust AFECLK and AFEFSC dynamically to a slightly varying FSC if AFECLK and AFEFSC are derived from the main oscillator (XTAL). This mode requires that both AFEFSC and FSC are nominally running at the same frequency (8 kHz).

2.4 Interfaces

This section describes the interfaces of the PSB 4860. The PSB 4860 supports both an IOM®-2 interface with single and double clock mode and a strobed serial data interface (SSDI). However, these two interfaces cannot be used simultaneously as they share some pins. Both interfaces are for data transfer only and cannot be used for programming the PSB 4860. Table 61 lists the features of the two alternative interfaces.

Table 61

	IOM®-2	SSDI
Signals	4	6
Channels (bidirectional)	2	1
Code	linear PCM, A-law, µ-law	linear PCM
Synchronization within frame	by timeslot (programmable)	by signal (DXST, DRST)

2.4.1 IOM®-2 Interface

The data stream is partitioned into packets called frames. Each frame is divided into a fixed number of timeslots. Each timeslot is used to transfer 8 bits. Figure 42 shows a commonly used terminal mode (three channels ch_0, ch_1 and ch_2 with four timeslots each).

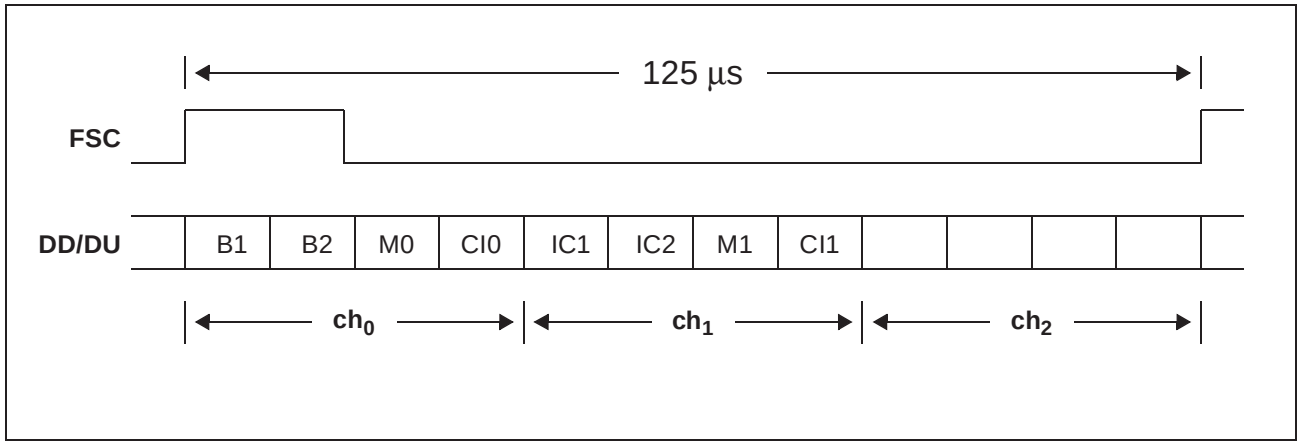


Figure 42
IOM®-2 Interface - Frame Structure

The signal FSC is used to indicate the start of a frame. Figure 43 shows as an example two valid FSC-signals (FSC, FSC*) which both indicate the same clock cycle as the first clock cycle of a new frame (T_1).

Note: Any timeslot (including M0, CI0, ...) can be used for data transfer. However, programming is not supported via the monitor channels.

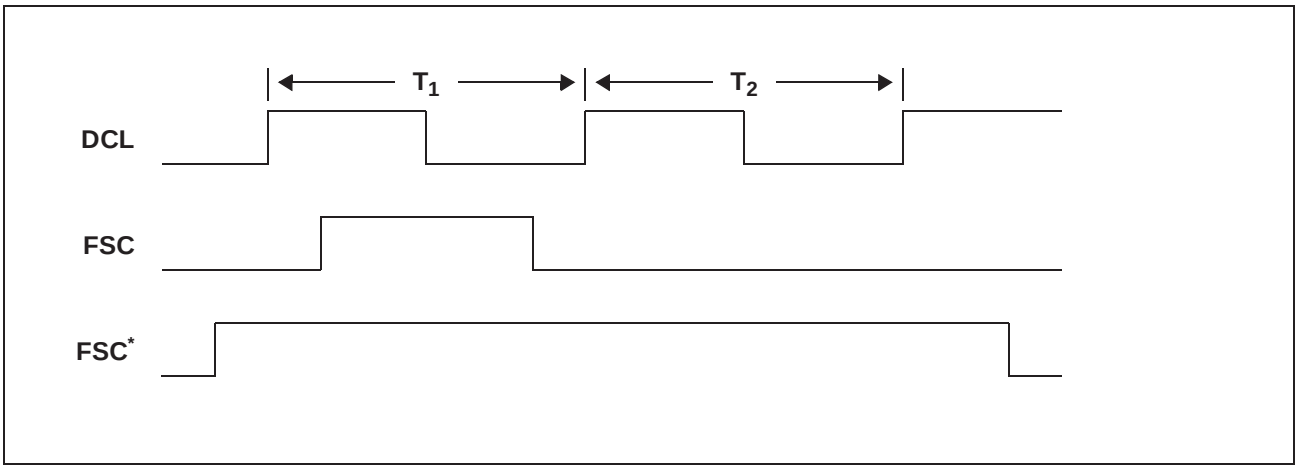


Figure 43
IOM®-2 Interface - Frame Start

The PSB 4860 supports both single clock mode and double clock mode. In single clock mode, the bit rate is equal to the clock rate. Bits are shifted out with the rising edge of DCL and sampled at the falling edge. In double clock mode, the clock runs at twice the bit rate. Therefore for each bit there are two clock cycles. Bits are shifted out with the rising edge of the first clock cycle and sampled with the falling edge of the second clock cycle. Figure 44 shows the timing for single clock mode and figure 45 shows the timing for double clock mode.

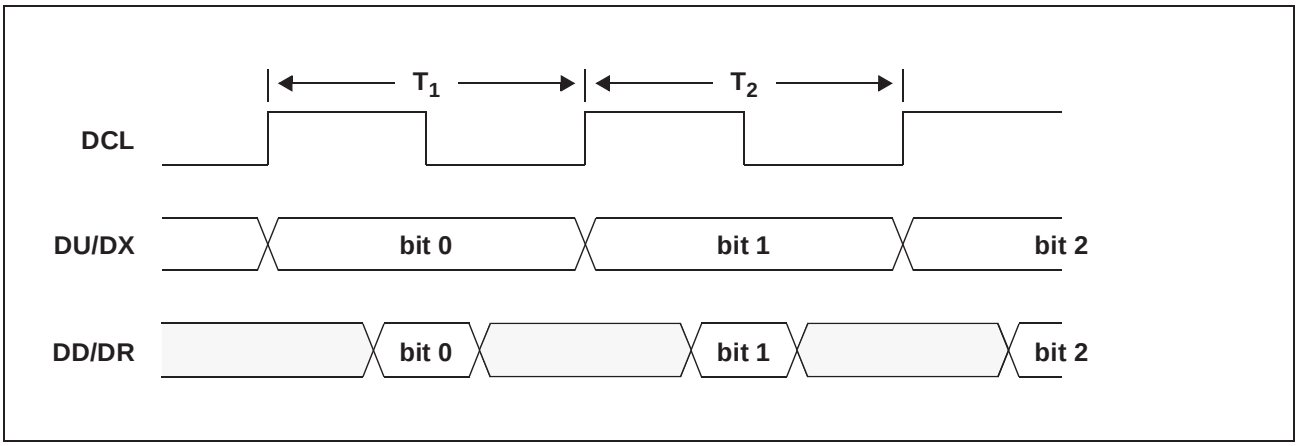


Figure 44
IOM®-2 Interface - Single Clock Mode

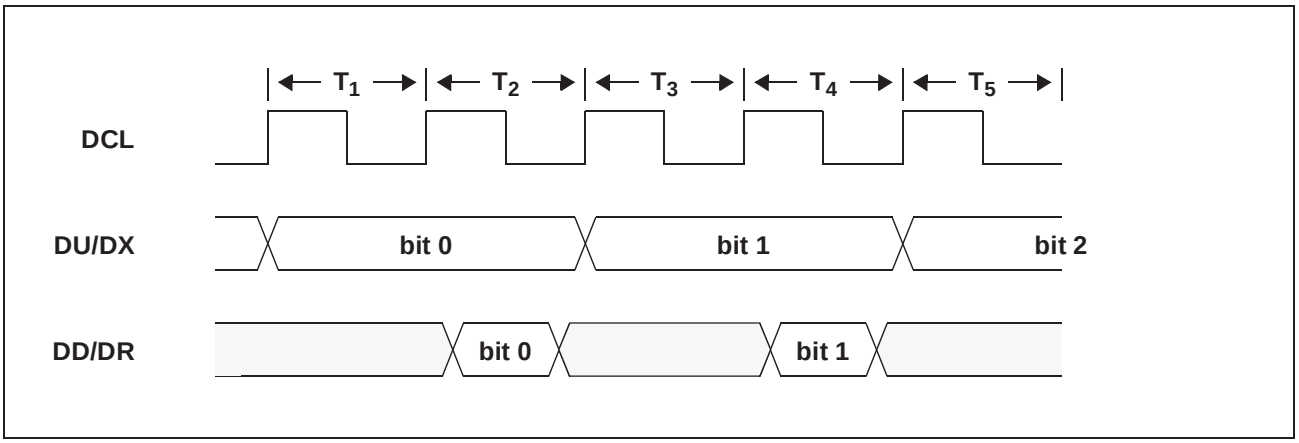


Figure 45
IOM®-2 Interface - Double Clock Mode

The PSB 4860 supports up to two channels simultaneously for data transfer. Both the coding (PCM or linear) and the data direction (DD/DU assignment for transmit/receive) can be programmed individually for each channel. Table 62 shows the registers used for configuration of the IOM®-2 interface.

Table 62

Register	# of Bits	Name	Comment
SDCONF	1	EN	Interface enable
SDCONF	1	DCL	Selection of clock mode
SDCONF	6	NTS	Number of timeslots within frame
SDCHN1	1	EN	Channel 1 enable
SDCHN1	6	TS	First timeslot (channel 1)
SDCHN1	1	DD	Data Direction (channel 1)
SDCHN1	1	PCM	8 bit code or 16 bit linear PCM (channel 1)
SDCHN1	1	PCD	8 bit code (A-law or µ-law, channel 1)
SDCHN2	1	EN	Channel 2 enable
SDCHN2	6	TS	First timeslot (channel 2)
SDCHN2	1	DD	Data Direction (channel 2)
SDCHN2	1	PCM	8 bit code or 16 bit linear PCM (channel 2)
SDCHN2	1	PCD	8 bit code (A-law or µ-law, channel 2)

In A-law or µ-law mode, only 8 bits are transferred and therefore only one timeslot is needed for a channel. In linear mode, 16 bits are needed for a single channel. In this mode, two consecutive timeslots are used for data transfer. Bits 8 to 15 are transferred

within the first timeslot and bits 0 to 7 are transferred within the next timeslot. The first timeslot must have an even number. The most significant bit is always transmitted first.

2.4.2 SSDI Interface

The SSDI interface is intended for seamless connection to low-cost burst mode controllers (e.g. PMB 27251) and supports a single channel in each direction. The data stream is partitioned into frames. Within each frame one 16 bit value can be sent and received by the PSB 4860. The start of a frame is indicated by the rising edge of FSC. Data is always latched at the falling edge of DCL and output at the rising edge of DCL.

The SSDI transmitter and receiver are operating independently of each other except that both use the same FSC and DCL signal.

2.4.2.1 SSDI Interface - Transmitter

The PSB 4860 indicates outgoing data (on signal DX) by activating DXST for 16 clocks. The signal DXST is activated with the same rising edge of DCL that is used to send the first bit (Bit 15) of the data. DXST is deactivated with the first rising edge of DCL after the last bit has been transferred. The PSB 4860 drives the signal DX only when DXST is activated. Figure 46 shows the timing for the transmitter.

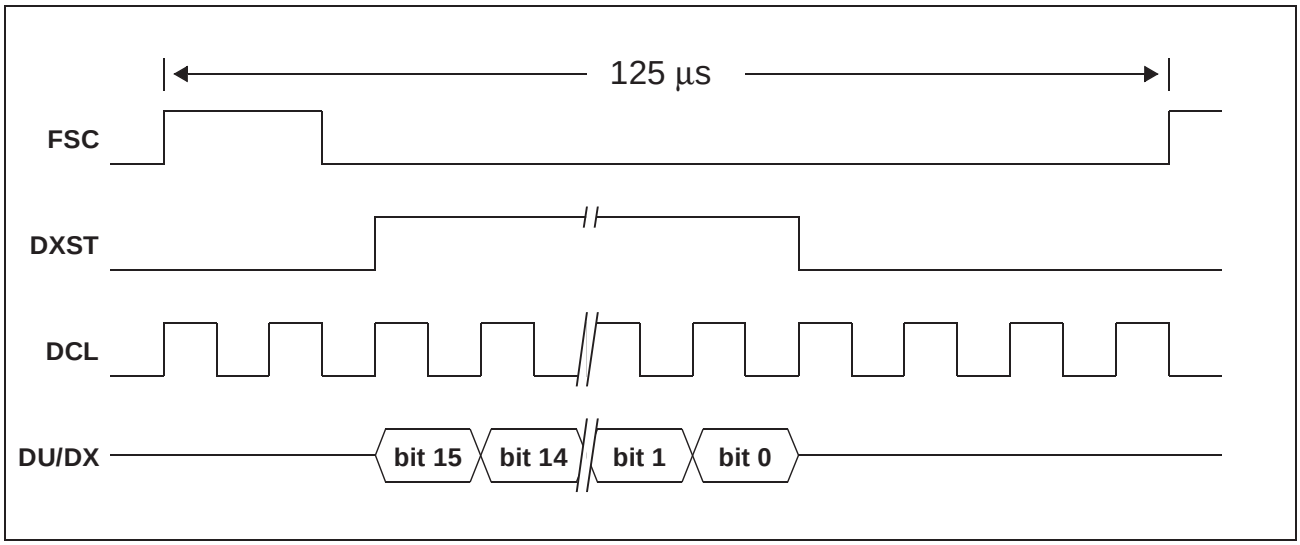


Figure 46
SSDI Interface - Transmitter Timing

2.4.2.2 SSDI Interface - Receiver

Valid data is indicated by an active DRST pulse. Each DRST pulse must last for exactly 16 DCL clocks. As there may be more than one DRST pulses within a single frame the PSB 4860 can be programmed to listen to the n-th pulse with n ranging from 1 to 16. In order to detect the first pulse properly, DRST must not be active at the rising edge of FSC. In figure 48 the PSB 4860 is listening to the third DRST pulse (n=3).

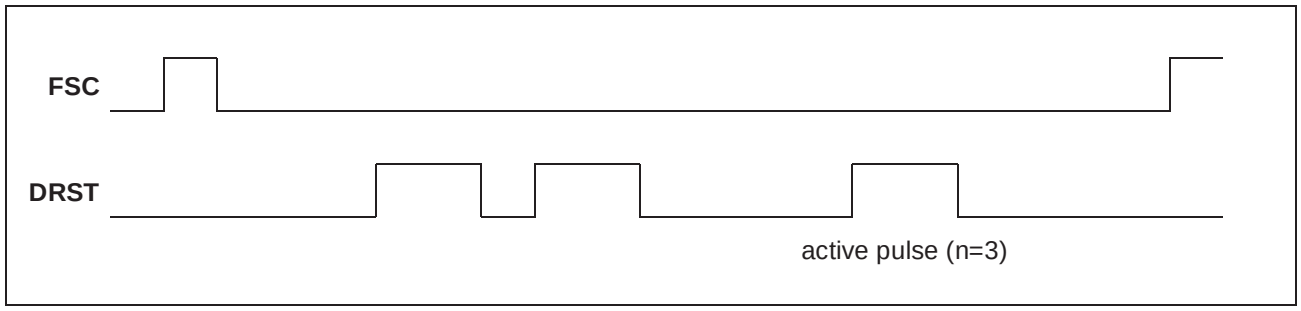


Figure 47
SSDI Interface - Active Pulse Selection

Figure 48 shows the timing for the SSDI receiver.

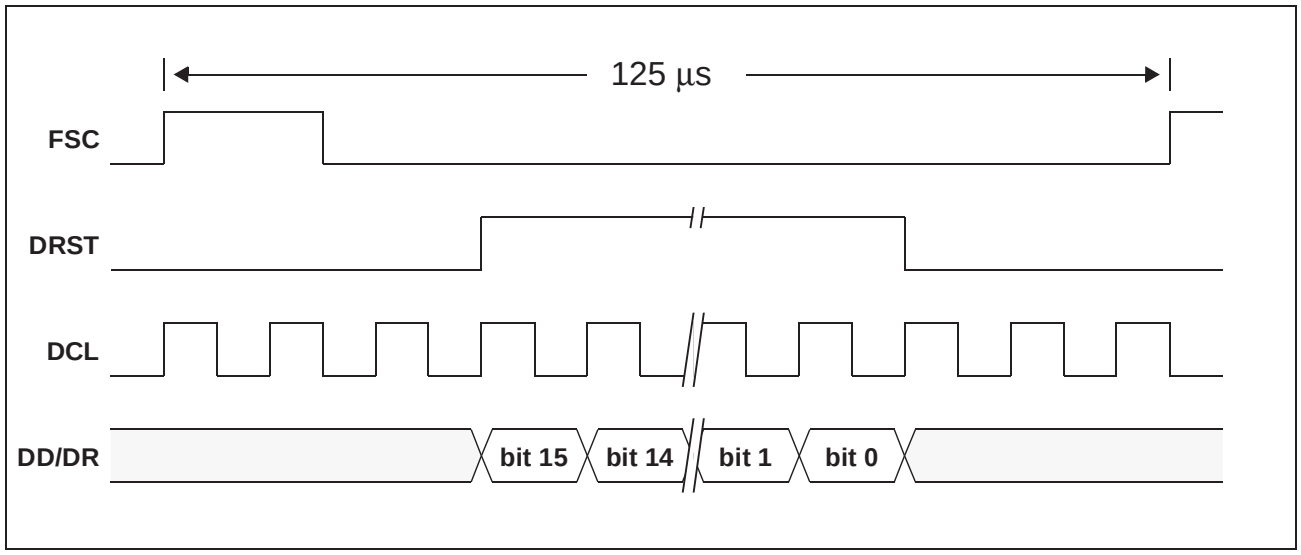


Figure 48
SSDI Interface - Receiver Timing

Table 63 shows the registers used for configuration of the SSDI interface.

Table 63

Register	# of Bits	Name	Comment
SDCHN1	4	NAS	Number of active DRST strobe

2.4.3 Analog Front End Interface

The PSB 4860 uses a four wire interface similar to the IOM®-2 interface to exchange information with the analog front end (PSB 4851). The main difference is that all timeslots and the channel assignments are fixed as shown in figure 49.

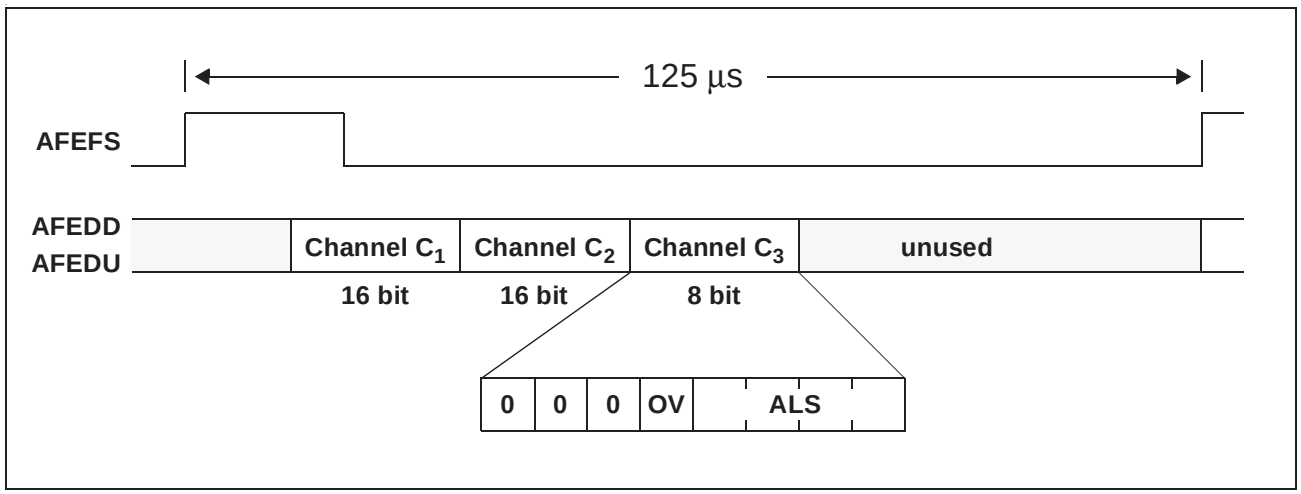


Figure 49
Analog Front End Interface - Frame Structure

Voice data is transferred in 16 bit linear coding in two bidirectional channels C_1 and C_2. An auxiliary channel C_3 is used to transfer the current setting of the loudspeaker amplifier ALS to the PSB 4860. The remaining bits are fixed to zero. In the other direction C_3 transfers an override value for ALS from the PSB 4860 to the PSB 4851. An additional override bit OV determines if the currently transmitted value should override the AOAR:LSC[1)] setting. The AOAR:LSC setting is not affected by C_3:ALS override. Table 64 shows the source control of the gain for the ALS amplifier.

Table 64

AOPR:OVRE	C_3:OV	Gain of ALS amplifier
0	-	AOAR:LSC
1	0	AOAR:LSC
1	1	C_3:ALS

Furthermore the AFE interface can be enabled or disabled according to table 65.

Table 65

Register	# of Bits	Name	Comment
AFECTL	1	EN	Interface enable

1 See specification of PSB 4851, automatically set by the PSB 4860 in loudhearing mode.

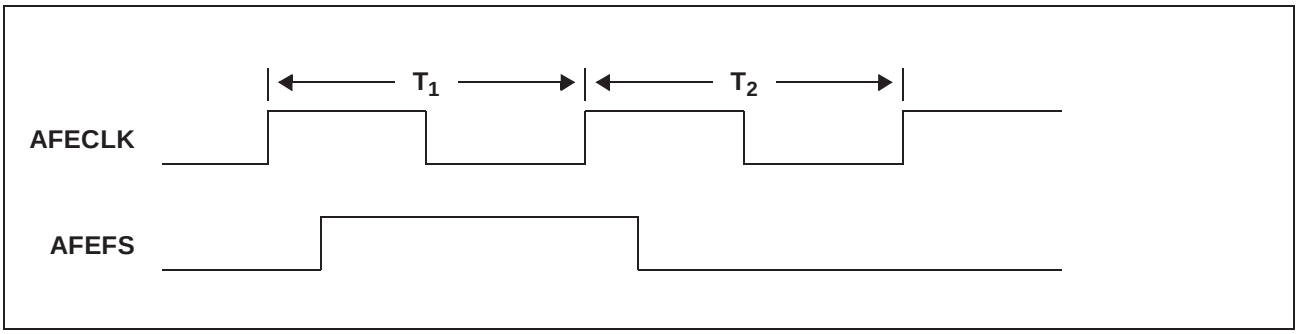


Figure 50
Analog Front End Interface - Frame Start

Figure 50 shows the synchronization of a frame by AFEFS. The first clock of a new frame (T_1) is indicated by AFEFS switching from low to high before the falling edge of T_1. AFEFS may remain high during subsequent cycles up to T_{32}.

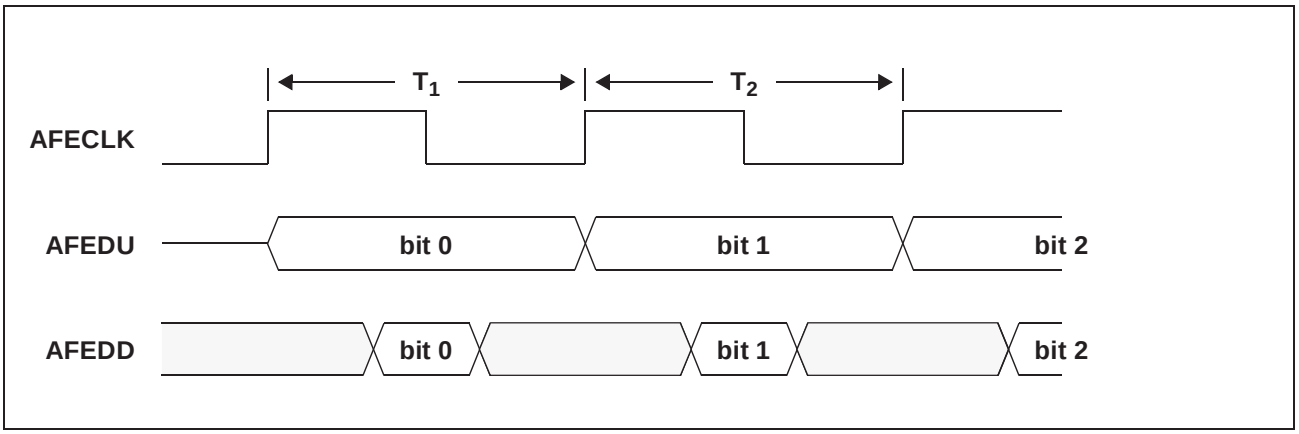


Figure 51
Analog Front End Interface - Data Transfer

The data is shifted out with the rising edge of AFECLK and sampled at the falling edge of AFECLK (figure 51). If AOPR:OVRE is not set, the channel C_3 is not used by the PSB 4851. All values (C_1, C_2, C_3:ALS) are transferred MSB first. The data clock (AFECLK) rate is fixed at 6.912 MHz. Table 66 shows the clock cycles used for the three channels.

Clock Cycles	AFEDD (driven by PSB 4860)	AFEDU (driven by PSB 4851)
T_1-T_{16}	C_1 data	C_1 data
T_{17}-T_{32}	C_2 data	C_2 data
T_{33}-T_{40}	C_3 data	C_3 data
T_{41}-T_{864}	0	tristate

2.4.4 Serial Control Interface

The serial control interface (SCI) uses four lines: SDR, SDX, SCLK and $\overline{CS}$. Data is transferred by the lines SDR and SDX at the rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of an access. Data is sampled by the PSB 4860 at the rising edge of SCLK and shifted out at the falling edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$. The accesses to the PSB 4860 can be divided into three classes:

1. Configuration Read/Write
2. Status/Data Read
3. Register Read/Write

If the PSB 4860 is in power down mode, a read access to the status register does not deliver valid data with the exception of the RDY bit. After the status has been read the access can be either terminated or extended to read data from the PSB 4860. A register read/write access can only be performed when the PSB 4860 is ready. The RDY bit in the status register provides this information.

Any access to the PSB 4860 starts with the transfer of 16 bits to the PSB 4860 over line SDR. This first word specifies the access class, access type (read or write) and, if necessary, the register accessed. If a configuration register is written, the first word also includes the data and the access is terminated. Likewise, if a register read is issued, the access is terminated after the first word. All other accesses continue by the transfer of the status register from the PSB 4860 over line SDX. If a register (excluding configuration) is to be written, the next 16 bits containing the data are transferred over line SDR and the access is terminated. Figures 52 to 55 show the timing diagrams for the different access classes and types to the PSB 4860.

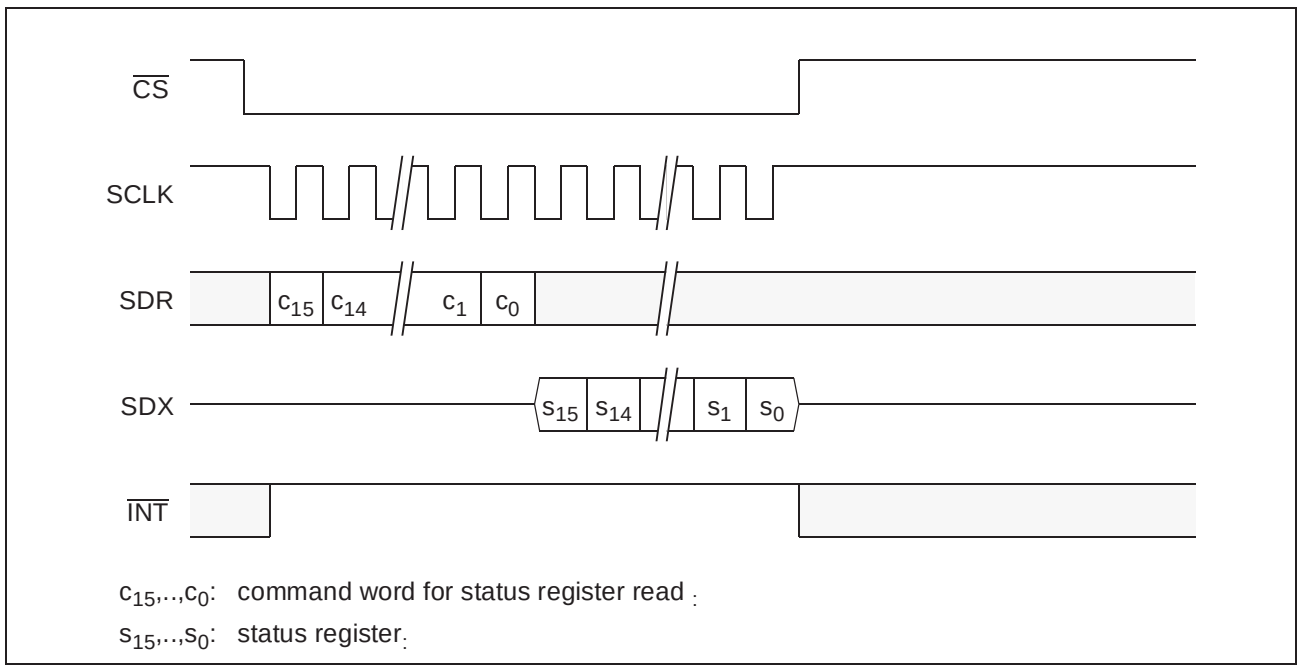
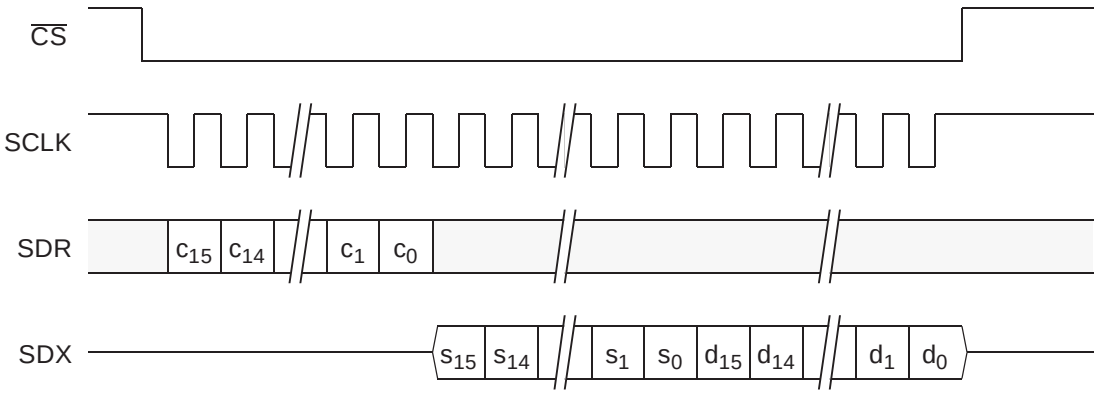
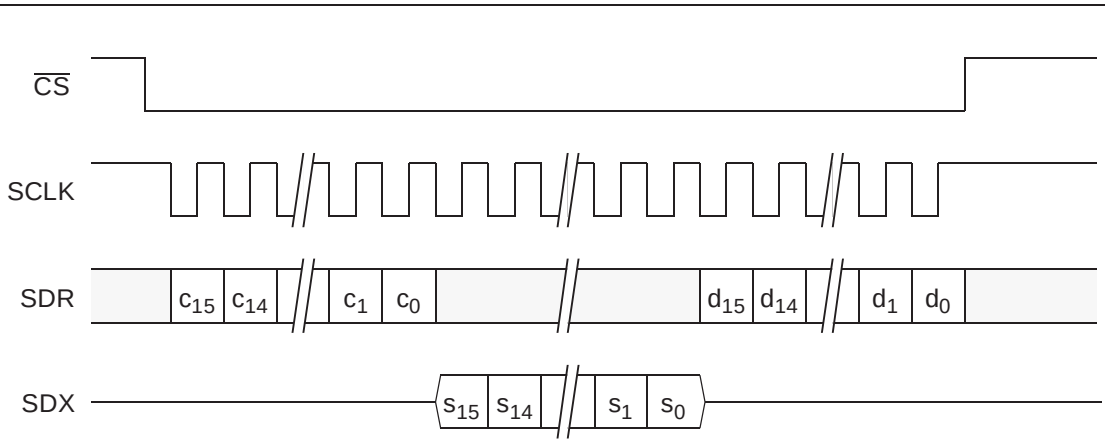


Figure 52
Status Register Read Access



$c_{15},..,c_0$: command word for data read.
$s_{15},..,s_0$: status register.
$d_{15},..,d_0$: data to be read.

Figure 53
Data Read Access



$c_{15},..,c_0$: command word for register write.
$s_{15},..,s_0$: status register.
$d_{15},..,d_0$: data to be written .

Figure 54
Register Write Access

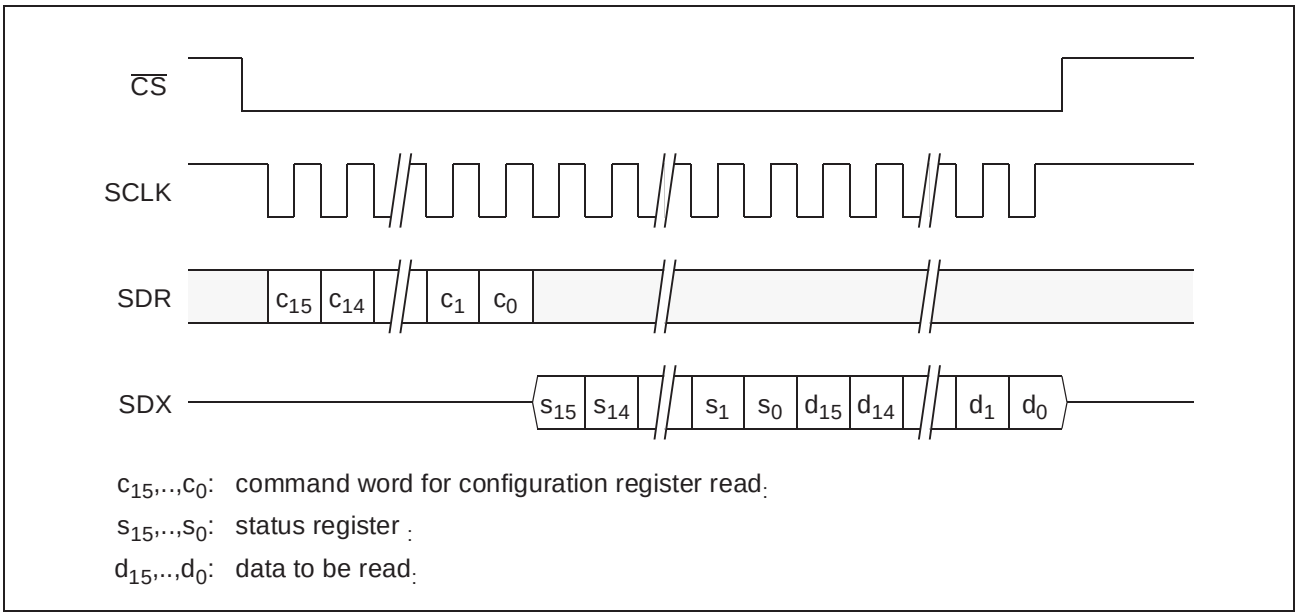


Figure 55
Configuration Register Read Access

Configuration registers at even adresses use bit positions d_7-d_0 while configuration register at odd adresses use bit positions d_{15}-d_8.

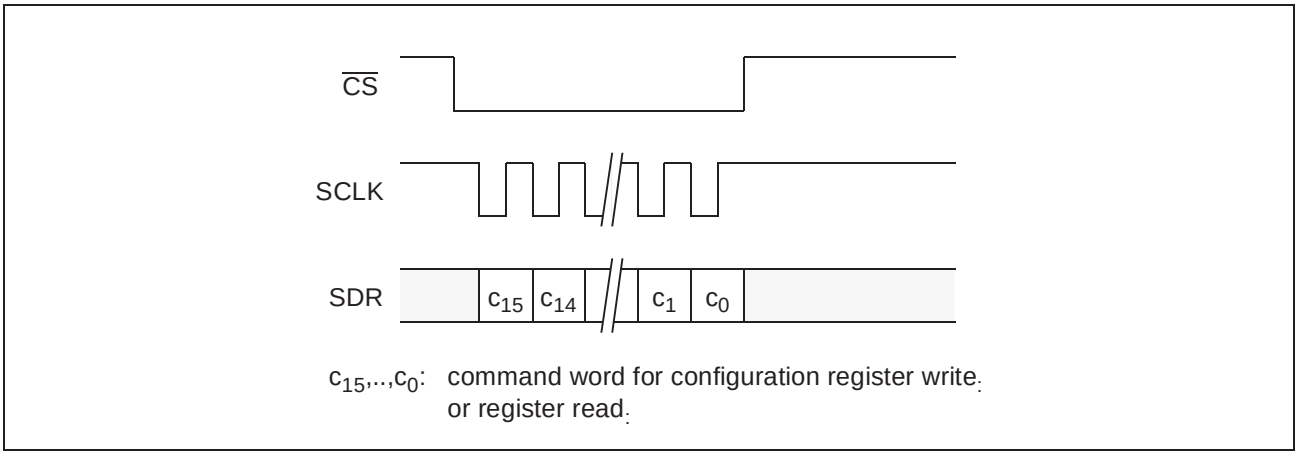


Figure 56
Configuration Register Write Access or Register Read Command

The internal interrupt signal is cleared when the first bit of the status register is put on SDX. However, externally the signal $\overline{INT}$ is deactivated as long as $\overline{CS}$ stays low. If the internal interrupt signal is not cleared or another event causing an interrupt occurs while the microcontroller is already reading the status belonging to the first event then INT goes low again immediately after $\overline{CS}$ is removed. The timing is shown in figure 52. Table 66 shows the formats of the different command words. All other command words are reserved.

Table 66
Command Words for Register Access

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Status Register	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Read Register	0	1	0	1	REG											
Write Register	0	1	0	0	REG											
Read Configuration Reg.	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	R
Write Configuration Reg.	0	1	1	0	0	0	W		DATA							

In case of a configuration register write, W determines which configuration register is to be written (table 67):

Table 67
Address Field W for Configuration Register Write

9	8	Register
0	0	HWCONFIG 0
0	1	HWCONFIG 1
1	0	HWCONFIG 2
1	1	HWCONFIG 3

In case of a configuration register read, R determines which pair of configuration registers is to be read (table 68):

Table 68
Address field R for Configuration Register Read

0	Register pair
0	HWCONFIG 0 / HWCONFIG 1
1	HWCONFIG 2 / HWCONFIG 3

2.4.5 Memory Interface

The PSB 4860 supports either Flash Memory or ARAM/DRAM as external memory for storing messages. If ARAM/DRAM is used, an EPROM can be added optionally to support read-only messages (e.g. voice prompts). Table 69 summarizes the different configurations supported.

Table 69

Mbit	Type	Bank 0 (D_0-D_3)	Bank 1 (D_4-D_7)	Comment
1	ARAM/DRAM	256kx4	-	
2	ARAM/DRAM	256kx4	256kx4	
4	ARAM/DRAM	1Mx4	-	
4	ARAM/DRAM	512kx8		
8	ARAM/DRAM	1Mx4	1Mx4	
16	ARAM/DRAM	4Mx4	-	2k or 4k refresh
16	ARAM/DRAM	2Mx8		2k refresh
32	ARAM/DRAM	4Mx4	4Mx4	2k or 4k refresh
32	ARAM/DRAM	2x2Mx8		2k refresh
64	ARAM/DRAM	16Mx4	-	4k or 8k refresh
64	ARAM/DRAM	8Mx8		4k or 8k refresh
128	ARAM/DRAM	16Mx4	16Mx4	4k or 8k refresh
4-128	FLASH	x8 devices		Intel type
4-128	FLASH	512kx8 devices		KM29N040
8-128	FLASH	1Mx8 devices		KM29W8000
16-128	FLASH	2Mx8 devices		KM29N16000
32-128	FLASH	4Mx8 devices		KM29N32000

If ARAM/DRAM is used, the total amount of memory must be a power of two and all devices must be of the same type. The pin FRDY must be tied high.

For flash devices, the PSB 4860 supports in-circuit programming of voice prompts by releasing the control lines during reset and (optionally) power down. Instead of actively driving the lines $\overline{\text{FCS}}$, $\overline{\text{FOE}}$, $\overline{\text{FWE}}$, FCLE and ALE these lines are pulled high by a weak pullup during reset and (optionally) power down.

2.4.5.1 ARAM/DRAM Interface

The PSB 4860 supports up to two banks of memory which may be 4 bit or 8 bit wide (Figure 57). If both banks are used they must be populated identically.

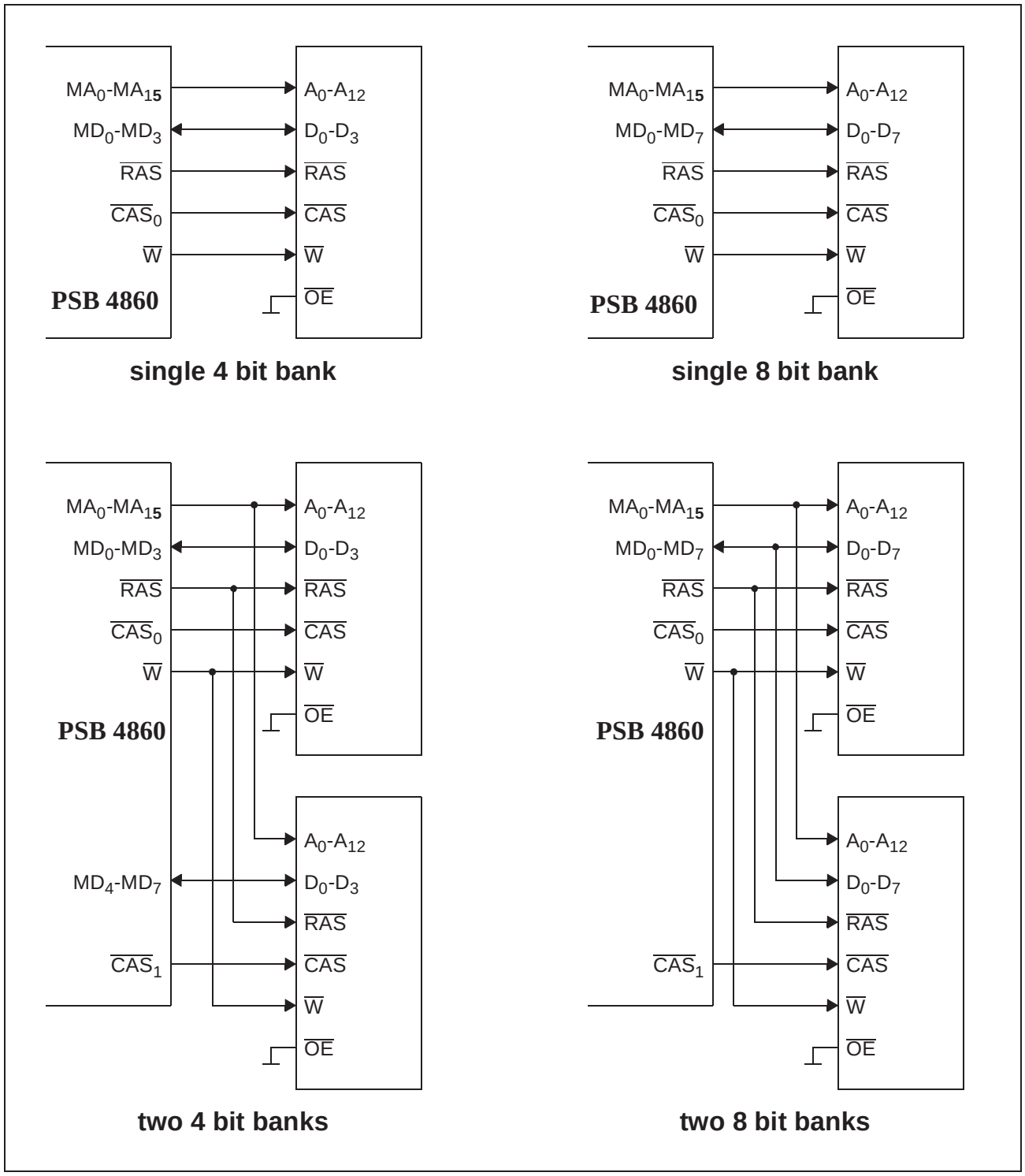


Figure 57
ARAM/DRAM Interface - Connection Diagram

The PSB 4860 also supports different internal organizations of ARAM/DRAM chips. Table 70 shows the necessary connections on the address bus.

Table 70

ARAM/DRAM	CS9	MA_0-MA_8	MA_9	MA_{10}	MA_{11}	MA_{12}	MA_{13}
256k x4	1	A_0-A_8					
512k x8	1	A_0-A_8	A_9				
1M x4	0	A_0-A_8	A_9				
4M x4 (2k refresh)	0	A_0-A_8	A_9	A_{10}			
4M x4 (4k refresh)	0	A_0-A_8	A_9	A_{10}	A_{11}		
2M x8	0	A_0-A_8	A_9	A_{10}			
16M x4 (4k refresh)	0	A_0-A_8	A_9	A_{10}		A_{11}	
16M x4 (8k refresh)	0	A_0-A_8	A_9	A_{10}		A_{11}	A_{12}
8M x8 (4k refresh)	0	A_0-A_8	A_9	A_{10}		A_{11}	
8M x8 (8k refresh)	0	A_0-A_8	A_9	A_{10}		A_{11}	A_{12}

The entry CS9 refers to the CS9 bit of the chip control register (table 71).

Table 71

Register	# of Bits	Name	Comment
CCTL	1	CS9	DRAM block size selection
CCTL	1	RFM	Refresh mode (normal, battery backup)

The timing of the ARAM/DRAM interface is shown in figures 57 to 60. The timing is derived form the internal memory clock MCLK* which runs at a quarter of the system clock. For power-down refresh, two modes are available. The normal mode ensures a refresh rate of 64 kHz while the battery backup mode uses 8 kHz for low power ARAMs/ DRAMs. The battery backup mode can only be used with the auxiliary oscillator running.

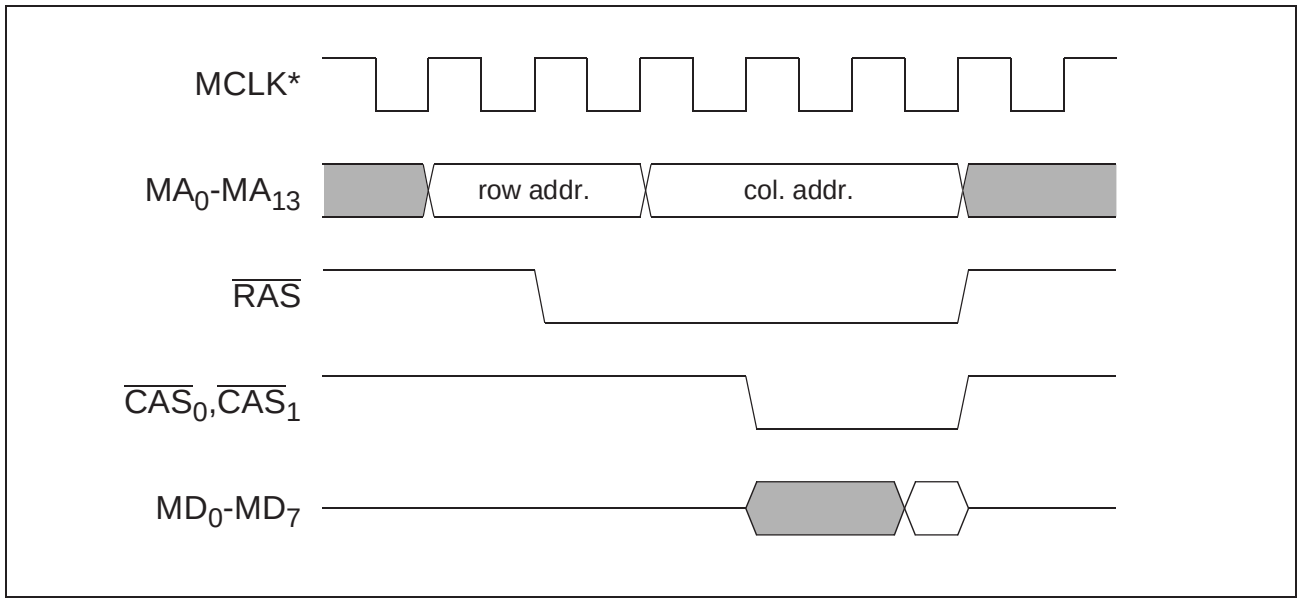


Figure 58
ARAM/DRAM Interface - Read Cycle Timing

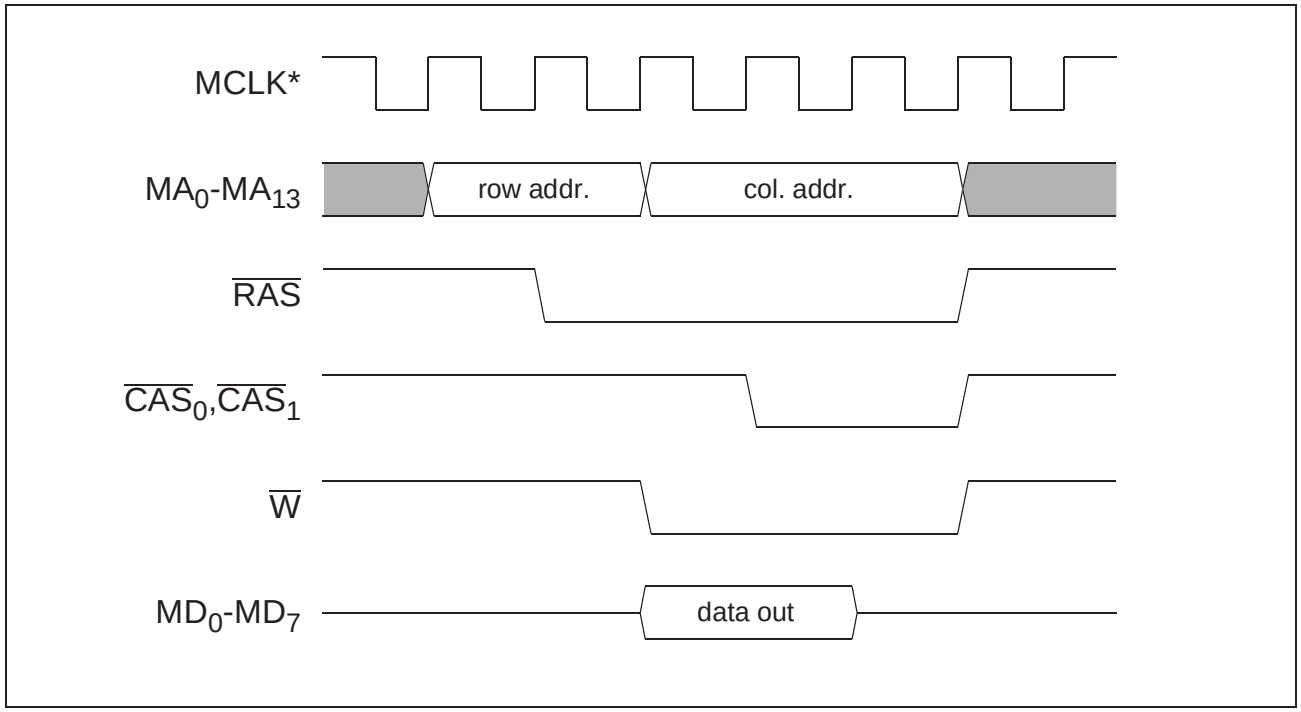


Figure 59
ARAM/DRAM Interface - Write Cycle Timing

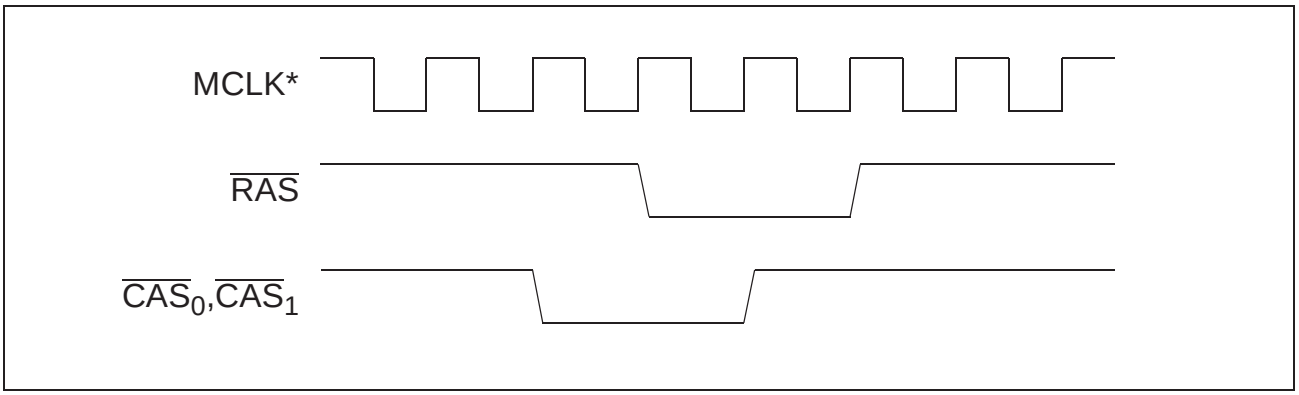


Figure 60
ARAM/DRAM Interface - Refresh Cycle Timing

The PSB 4860 ensures that $\overline{RAS}$ remains inactive for at least one MCLK*-cycle between successive accesses.

2.4.5.2 EPROM Interface

The PSB 4860 supports an EPROM in parallel with ARAM/DRAM. This interface is always 8 Bits wide and supports a maximum of 64kB. Figure 61 shows a connection diagram and figure 62 the timing. This interface supports read cycles only.

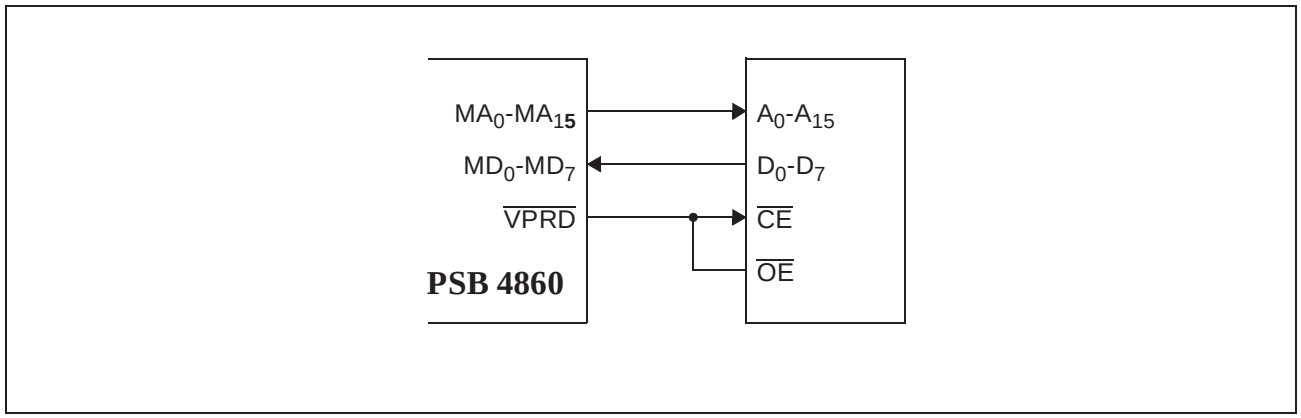


Figure 61
EPROM Interface - Connection Diagram

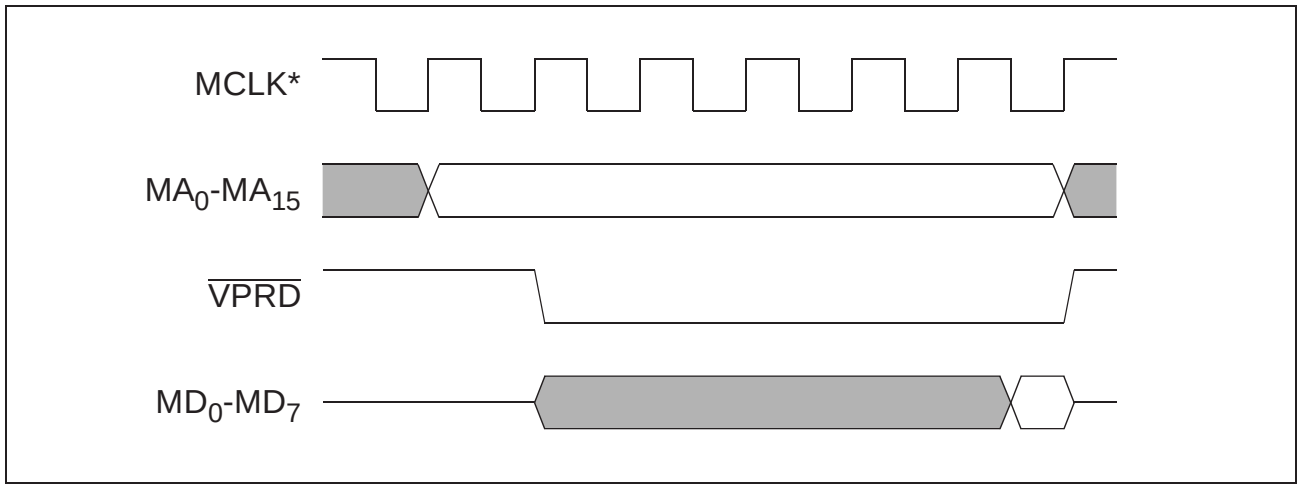


Figure 62
EPROM Interface - Read Cycle Timing

2.4.5.3 Flash Memory Interface (Samsung Mode)

The PSB 4860 has special support for the KM29N040 or equivalent devices. No external components are required for a single device. If more than one device is used, an additional external address decoder is required. Figure 63 shows the connection diagram for a single device.

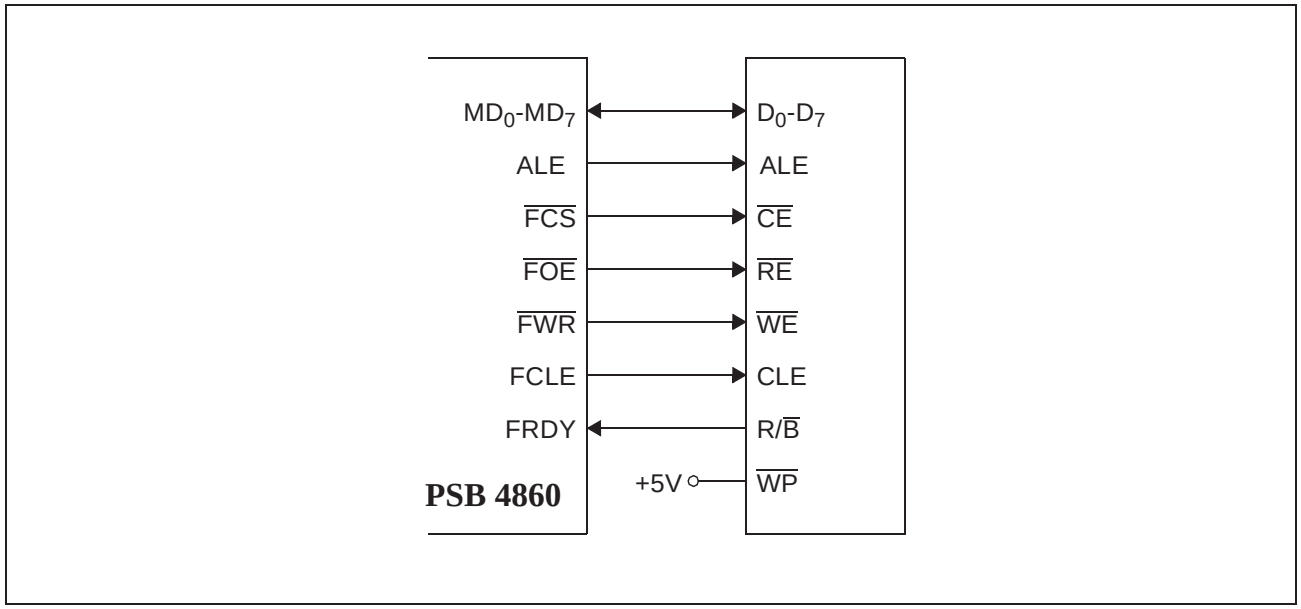


Figure 63
Flash Memory Interface (Samsung Mode) - Connection Diagram

Table 72 shows the signals output during a device access on the MA-lines. The address bits can used by an external decoder. Up to four KM29N040 are supported directly by the decoded select signals $\overline{FCS}_0$-$\overline{FCS}_3$.

Table 72

MA_{11}	MA_{10}	MA_9	MA_8	MA_7	MA_6	MA_5	MA_4	MA_3	MA_2	MA_1	MA_0
$\overline{FCS}_3$	$\overline{FCS}_2$	$\overline{FCS}_1$	$\overline{FCS}_0$	A_{23}	A_{22}	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}

Figure 64 shows an application with three KM29N040 devices.

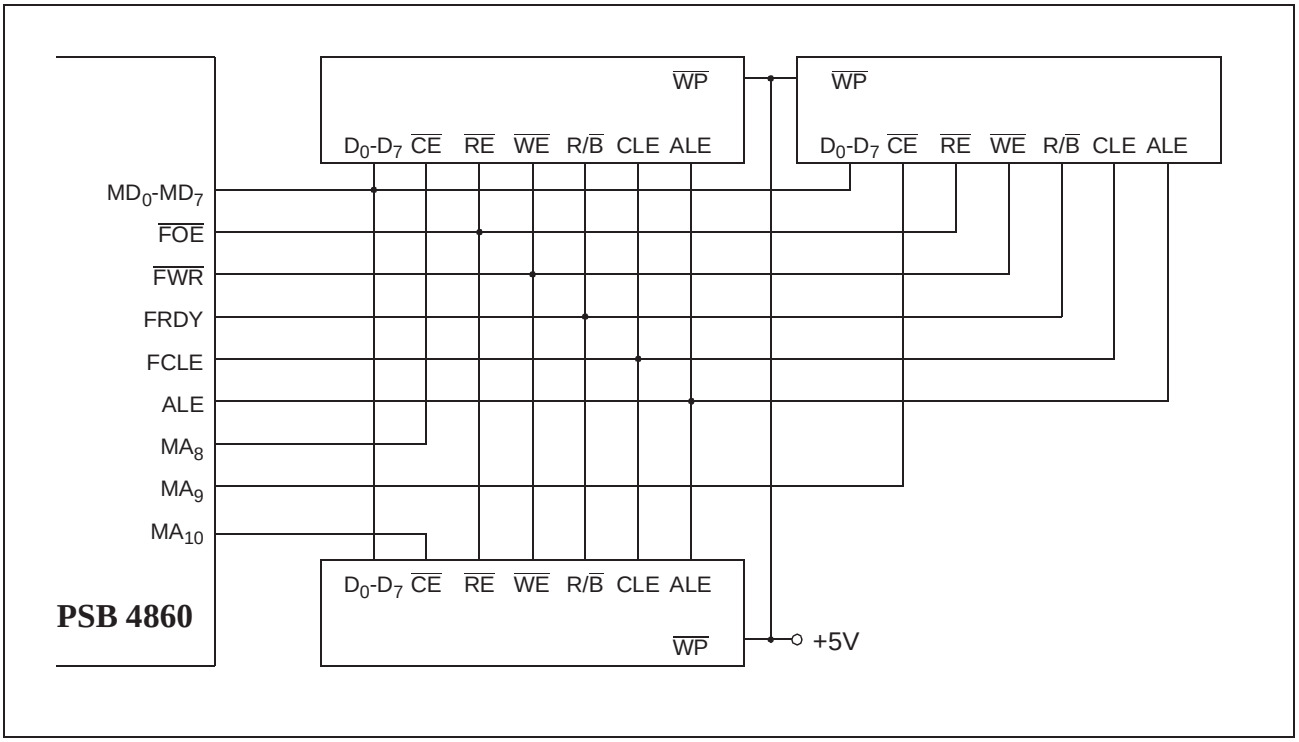


Figure 64
Flash Memory Interface (Samsung Mode) - Multiple Devices

An access to the Flash Memory can consist of several partial access cycles where only the timing of the partial access cycles is defined but not the time between two adjacent partial access cycles. The PSB 4860 performs three types of partial access cycles:

1. Command write
2. Address write
3. Data read/write

Table 73 shows the supported accesses and the corresponding partial access cycles.

Table 73

Access	Command write	Address write 1	Address write 2	Address write 3	# of Data read/write	Command write
RESET	FF	-	-	-	-	-
STATUS READ	70	-	-	-	1	-
BLOCK ERASE	60	A_8-A_{15}	A_{16}-A_{23}	-	-	D0
READ	00	A_0-A_7	A_8-A_{15}	A_{16}-A_{23}	1-32	-
WRITE	80	A_0-A7	A_8-A_{15}	A_{16}-A_{23}	1-32	10

The timing for the partial access cycles is shown in figures 65 to 66. Note that both $\overline{FCS}$ and MA_0-MA_{15} remain stable between the first and the last partial access of a device access.

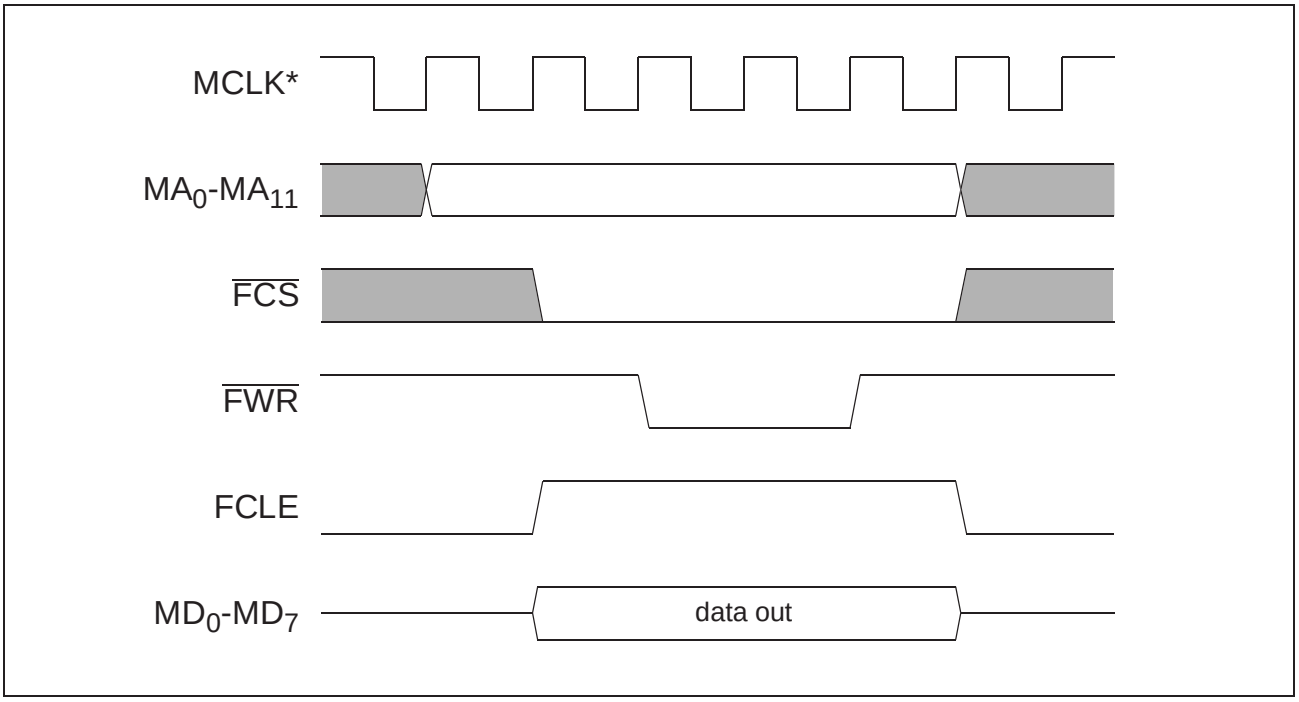


Figure 65
Flash Memory Interface (Samsung Mode) - Command Write

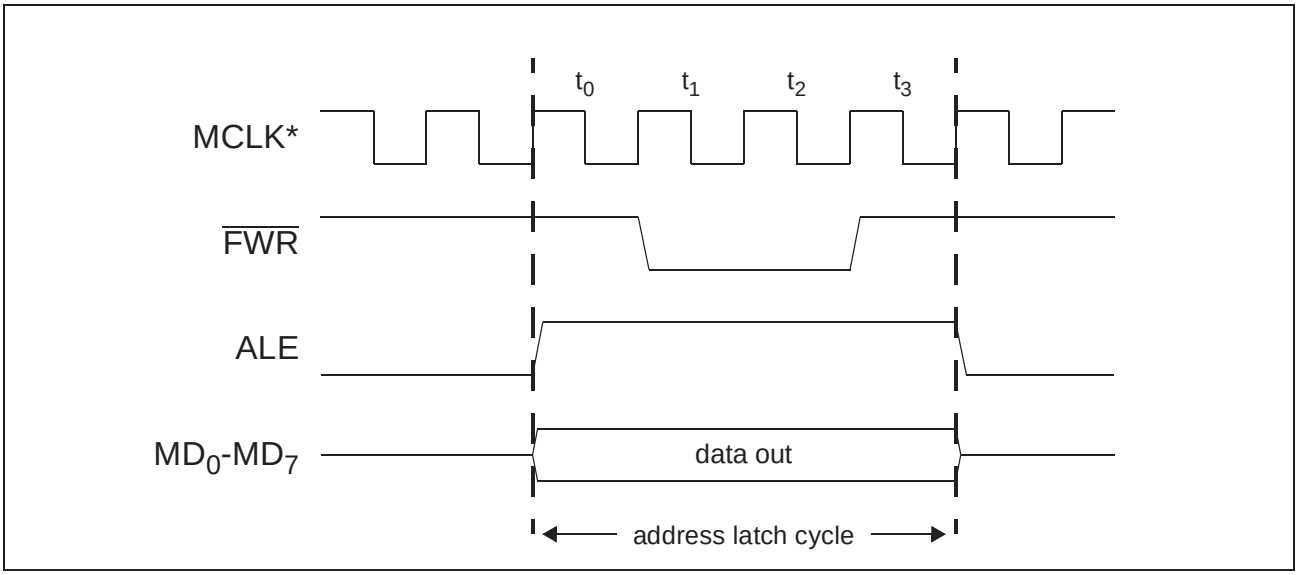


Figure 66
Flash Memory Interface (Samsung Mode) - Address Write

As there is no access that starts or stops with an address write cycle (figure 66) $\overline{FCS}$ is already low at the start of this cycle and also remains low.

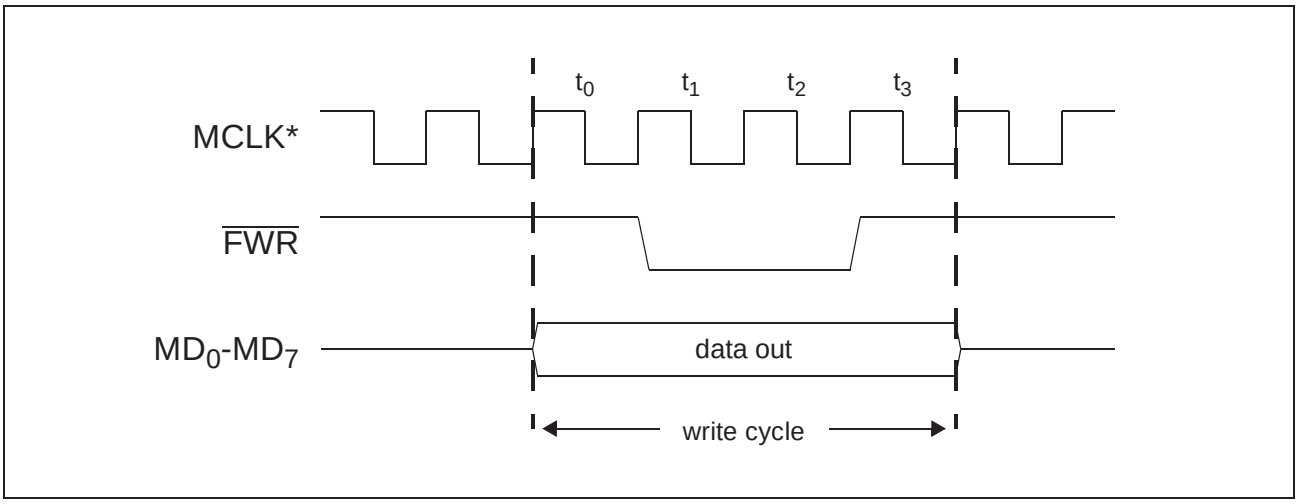


Figure 67
Flash Memory Interface (Samsung Mode) - Data Write

As there is no access that starts or stops with a data write cycle (figure 67) $\overline{FCS}$ is already low at the start of this cycle and also remains low.

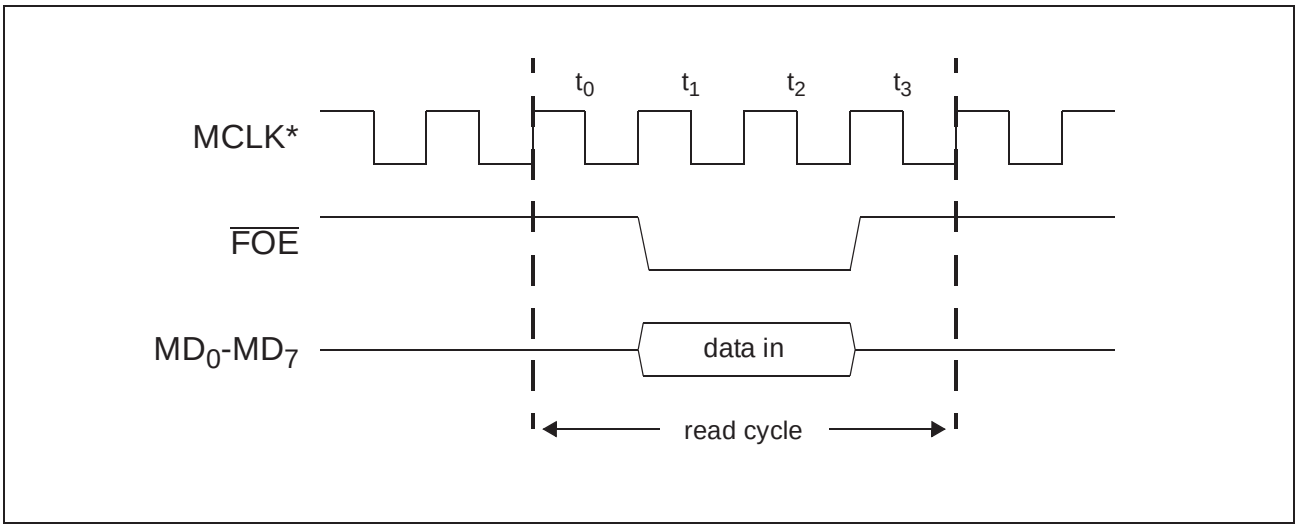


Figure 68
Flash Memory Interface (Samsung Mode) - Data Read

If the device access ends with a read cycle, the $\overline{FCS}$-signals go inactive after t_3 of the last read cycle. The data is latched at the rising edge of $\overline{FOE}$.

2.4.5.4 Flash Memory Interface (Intel Mode)

In Intel mode an additional address latch must be provided to store the address bits A_{16} to A_{23}. Figure 69 shows the connection diagram for a single device. If more than one device is used an external address latch is required.

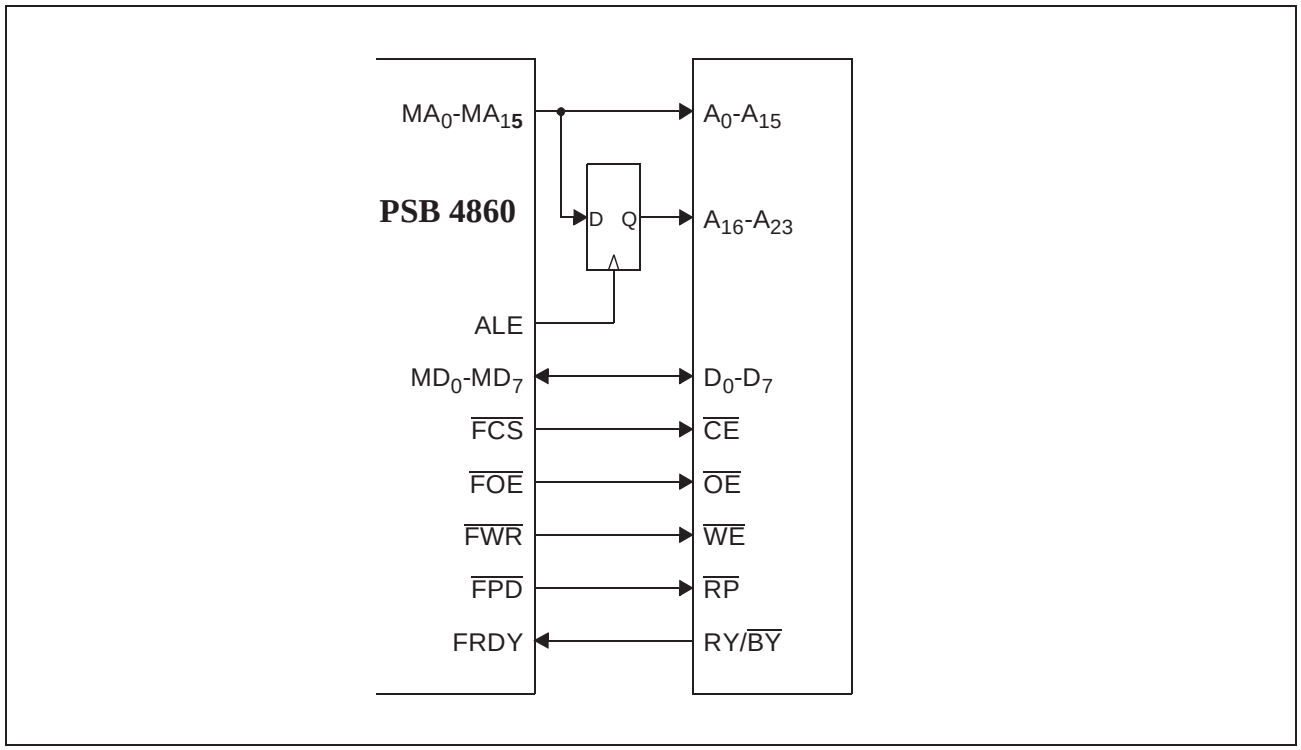


Figure 69
Flash Memory Interface (Intel Mode) - Connection Diagram

Any device access in this mode starts with an address latch cycle (figure 70). This cycle also activates $\overline{FPD}$ if it is not already active. Immediately after the address latch cycle a write cycle (figure 71) is performed to transmit the first command byte. Depending on the command (table 74), the immediately following cycle is either another write cycle or a read cycle (figure 72). The PSB 4860 terminates the device access after this cycle but does not release $\overline{FPD}$ until FRDY becomes high.

Table 74

Access	Write 1	Write 2	Read	Address
READ	FF	-	data	read address
ERASE SETUP/CONFIRM	20	D0	-	BA
ERASE SUSPEND/RESUME	B0	D0	-	undefined
BYTE WRITE	40	data	-	write address

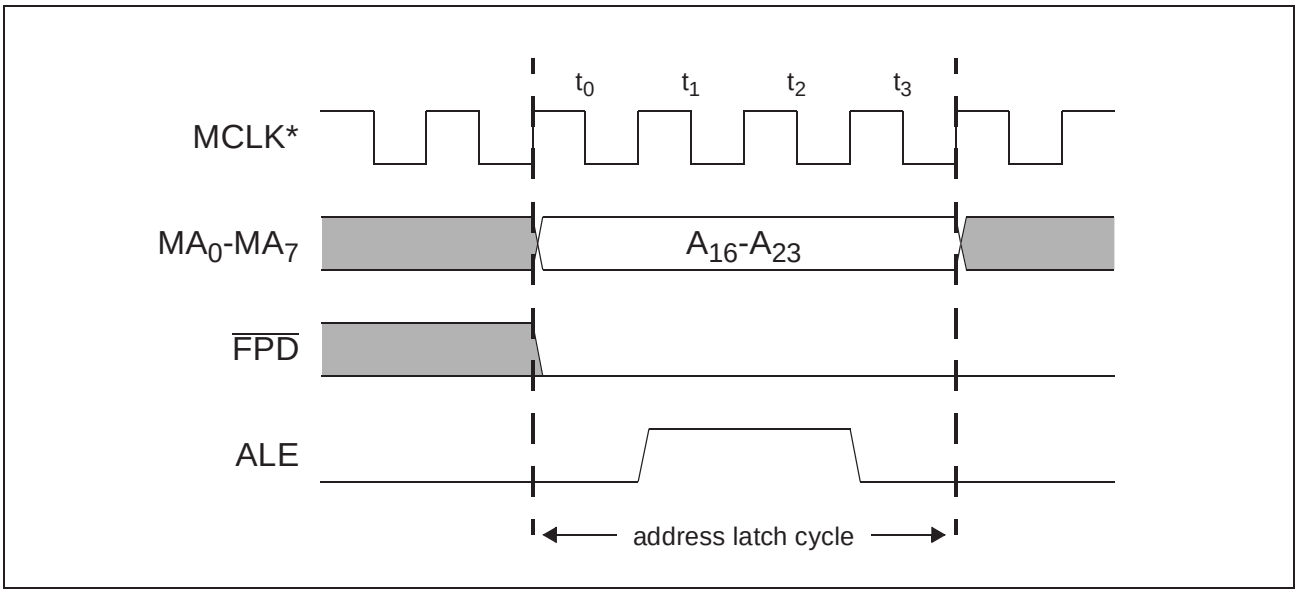


Figure 70
Flash Memory Interface (Intel Mode) - Address Latch Cycle

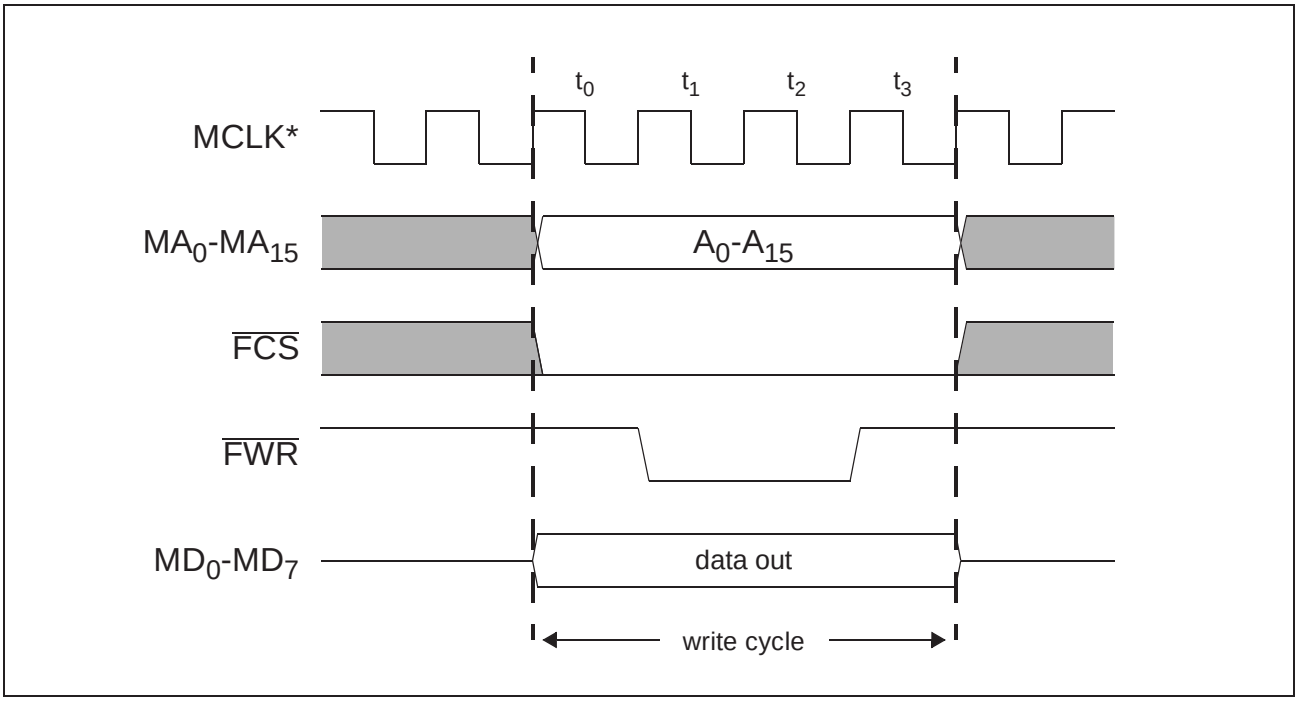


Figure 71
Flash Memory Interface (Intel Mode) - Write Cycle

Note that FCS and the MA-lines stay stable if this write cycle is immediately followed by another read or write cycle.

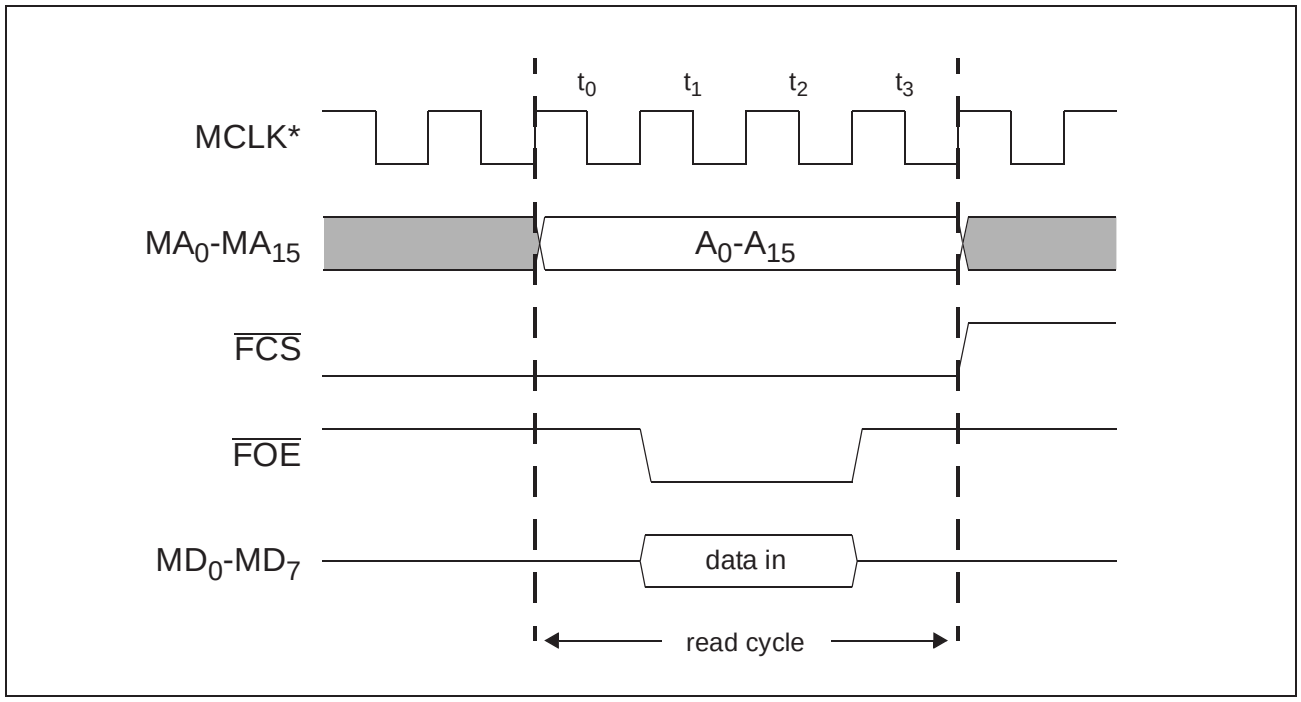


Figure 72
Flash Memory Interface (Intel mode) - Read Cycle

Note: The PSB 4860 does not support polling of the status register. Therefore the flash device must provide the ready/busy signal.

2.4.6 Auxiliary Parallel Port

The PSB 4860 provides an auxiliary parallel port if the memory interface is in Samsung mode and only one device is used. In this case the lines MA_0 to MA_{15} are not needed for the memory interface and can therefore be used for an auxiliary parallel port. This port has two modes: static mode and multiplex mode.

2.4.6.1 Static Mode

In static mode all pins of the auxiliary parallel port interface have identical functionality. Any pin can be configured as an output or an input. Pins configured as outputs provide a static signal as programmed by the controller. Pins configured as inputs are monitoring the signal continuously without latching. The controller always reads the current value. Table 75 shows the registers used for static mode.

Table 75

Register	# of bits	Comment
DOUT3	16	Output signals (for pins configured as outputs)
DIN	16	Input signals (for pins configured as inputs)
DDIR	16	Pin direction

2.4.6.2 Multiplex Mode

In multiplex mode, the PSB 4860 uses MA_{12}-MA_{15} to distinguish four timeslots. Each timeslot has a duration of approximately 2 ms. The timeslots are separated by a gap of approximately 125 µs in which none of the signals at MA_{12}-MA_{15} are active. The PSB 4860 multiplexes three more output registers to MA_0-MA_{11} in timeslots 0, 1 and 2. In timeslot 3 the direction of the pins can be programmed. For input pins, the signal is latched at the falling edge of MA_{15}. Table 76 shows the registers used for multiplex mode.

Table 76

Register	# of bits	Comment
DOUT0	12	Output signals on MA_0-MA_{11} while MA_{15}=1
DOUT1	12	Output signals on MA_0-MA_{11} while MA_{14}=1
DOUT2	12	Output signals on MA_0-MA_{11} while MA_{13}=1
DOUT3	12	Output signals (for pins configured as outputs) while MA_{12}=1
DIN	12	Input signals (for pins configured as inputs) at falling edge of MA_{12}
DDIR	12	Pin direction during MA_{12}=1

Figure 73 shows the timing diagram for multiplex mode.

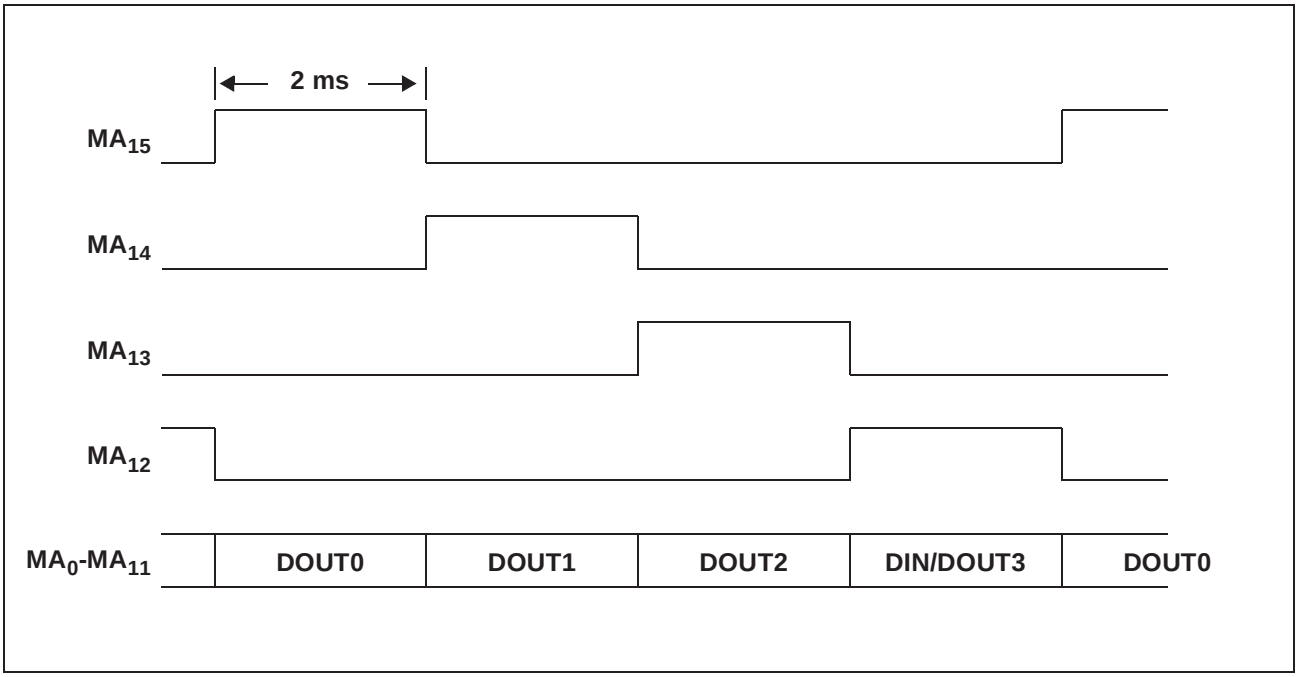


Figure 73
Auxiliary Parallel Port - Multiplex Mode

Note: In either mode the voltage on any pin (MA_0 to MA_{15}) must not exceed V_{DD}.

3 Detailed Register Description

The PSB 4860 has a single status register (read only) and an array of data registers (read/write). The purpose of the status register is to inform the external microcontroller of important status changes of the PSB 4860 and to provide a handshake mechanism for data register reading or writing. If the PSB 4860 generates an interrupt, the status register contains the reason of the interrupt.

3.1 Status Register

15															0
RDY	ABT	DRQ	SDA	CIA	CD	CPT	CNG	SD	ERR	BSY	DTV	ATV	0	0	0

RDY Ready

0: The last command (if any) is still in progress.

1: The last command has been executed.

Note: If the PSB 4860 aborts a running command due to external conditions (e.g. power drop-out, EMV) other than reset, it generates an interrupt and resets RDY. In this case the microcontroller should check the ABT bit to avoid locking the system.

ABT Abort

0: No exception during operation

1: Some exception other than reset caused the PSB 4860 to abort any operation currently in progress. The external microcontroller should reinitialize the PSB 4860 to ensure proper operation. The ABT bit is cleared by writing any value to register REV. No other command is accepted by the PSB 4860 while ABT is set.

DRQ Data Request

0: No request for data transfer

1: Request for data input (Data In)

SDA Speech Data Available

0: No request for data transfer

1: New data available (Data Out)

CIA Caller ID Available

0: No new data for caller ID

1: New caller ID byte available

CD Carrier Detect

0: No carrier detected

1: Carrier detected

CPT Call Progress Tone

0: Currently no call progress tone detected or pause detected (raw mode)

1: Currently a call progress is detected

CNG Fax Calling Tone

0: Currently no fax calling tone detected

1: Currently a fax calling tone is detected

SD Speech Detected

0: No speech detected

1: Speech signal at input of coder (output of decoder)

ERR Error (File Command)

0: No error

1: Last file command resulted in an error

BSY Busy (File Command)

0: File system idle

1: File system still busy

DTV DTMF Tone Valid

0: No new DTMF code available

1: New DTMF code available in DRDT

ATV Alert Tone Valid

0: No new alert tone code available

1: New alert tone code available in DRAT

3.2 Hardware Configuration Registers

HWCONFIG 0 - Hardware Configuration Register 0

7							0
PD	ACS	RTC	OSC	PPSDI	$\overline{\text{PFRDY}}$	PPINT	PPSDX

PPSDX Push/Pull for SDX

0: The SDX pin has open-drain characteristic

1: The SDX pin has push/pull characteristic

PPINT Push/Pull for $\overline{\text{INT}}$

0: The $\overline{\text{INT}}$ pin has open-drain characteristic

1: The $\overline{\text{INT}}$ pin has push/pull characteristic

$\overline{\text{PFRDY}}$ Pullup for FRDY

0: The internal pullup resistor of pin $\overline{\text{FRDY}}$ is enabled

1: The internal pullup resistor of $\overline{\text{FRDY}}$ is disabled

PPSDI Push/Pull for SDI interface

0: The DU and DD pins have open-drain characteristic

1: The DU and DD pins have push/pull characteristic

OSC Enable Auxiliary Oscillator

0: The auxiliary oscillator (OSC_1, OSC_2) is disabled

1: The auxiliary oscillator (OSC_1, OSC_2) is enabled

RTC Enable Real Time Clock

0: The real time clock is disabled

1: The real time clock (RTC) is enabled.

ACS AFE Clock Source

0: AFECLK is derived from the main oscillator

1: AFECLK is derived from the CLK input

PD Power Down (read only)

0: The PSB 4860 is in active mode

1: The PSB 4860 is in power down mode

HWCONFIG 1 - Hardware Configuration Register 1

7					0
APP	ACT	ADS	MFS	XTAL	SSDI

APP Auxiliary Parallel Port

7	6	Description
0	0	normal (ARAM/DRAM, Intel type flash, voice prompt EPROM)
0	1	APP static mode
1	0	APP multiplex mode
1	1	reserved

ACT AFE Clock Tracking

0: AFECLK tracking disabled

1: AFECLK tracking enabled

ADS AFE Double Speed

0: 8 kHz AFEFSC

1: 16 kHz AFEFSC

MFS Master Frame Sync Selection

0: AFEFSC

1: FSC

XTAL XTAL Frequency

2	1	Description
0	0	reserved
0	1	31.104 MHz
1	0	reserved
1	1	reserved

SSDI SSDI Interface Selection

0: IOM®-2 Interface

1: SSDI Interface

HWCONFIG 2 - Hardware Configuration Register 2

7					0
PPM	ESDX	ESDR	CSEL	CHS	RSEL

PPM Push/Pull for Memory Interface (reset, power down)

0: The signals for the memory interface have push/pull characteristic

1: The signals for the memory interface have pullup/pulldown characteristic

ESDX Edge Select for DX

0: DX is transmitted with the rising edge of DCL

1: DX is transmitted with the falling edge of DCL

ESDR Edge Select for DR

0: DR is latched with the falling edge of DCL

1: DR is latched with the rising edge of DCL

CSEL Codec Selection for AFE interface

0: Interface to PSB 4851

1: Interface to AK 4510

CHS Channel Select (AK 4510 only)

3	2	Description
0	0	left channel of AK 4510
0	1	right channel of AK4510
1	0	left and right channel
1	1	reserved

RSEL Refresh Select (low power mode)

1	0	Description
0	0	32 kHz
0	1	16 kHz
1	0	8 kHz
1	1	4 kHz

HWCONFIG 3 - Hardware Configuration Register 3

7							0
0	0	0	0	0	0	0	0

3.3 Read/Write Registers

The following sections contains all read/write registers of the PSB 4860. The register addresses are given as hexadecimal values. Registers marked with an R are affected by reset or a wake up after power down. All other registers retain their previous value. No access must be made to addresses other than those associated with a read/write register.

3.3.1 Register Table

Note: Registers CCTL, FCTL, FCMD, FDATA, FPTR and SPSCTL are only affected by reset, not by wakeup.

3.3.2 Register Naming Conventions

Several registers contain one or more fields for input signal selection. All fields labelled I_1 (I_2, I_3) are five bits wide and use the same coding as shown in table 77.

Table 77

4	3	2	1	0	Signal	Description
0	0	0	0	0	S_0	Silence
0	0	0	0	1	S_1	Analog line input (channel 1 of PSB 4851 interface)

Table 77

4	3	2	1	0	Signal	Description
0	0	0	1	0	S_2	Analog line output (channel 1 of PSB 4851 interface)
0	0	0	1	1	S_3	Microphone input (channel 2 of PSB 4851 interface)
0	0	1	0	0	S_4	Loudspeaker/Handset output (channel 2 of PSB 4851 interface)
0	0	1	0	1	S_5	Serial interface input, channel 1
0	0	1	1	0	S_6	Serial interface output, channel 1
0	0	1	1	1	S_7	Serial interface input, channel 2
0	1	0	0	0	S_8	Serial interface output, channel 2
0	1	0	0	1	S_9	DTMF generator output
0	1	0	1	0	S_{10}	DTMF generator auxiliary output
0	1	0	1	1	S_{11}	Speakerphone output (acoustic side)
0	1	1	0	0	S_{12}	Speakerphone output (line side)
0	1	1	0	1	S_{13}	Speech decoder output
0	1	1	1	0	S_{14}	Universal attenuator output
0	1	1	1	1	S_{15}	Line echo canceller output
1	0	0	0	0	S_{16}	AGC unit output (after AGC)
1	0	0	0	1	S_{17}	AGC unit output (before AGC)
1	0	0	1	0	S_{18}	Equalizer output
1	0	0	1	1		reserved
1	0	1	-	-		reserved
1	1	-	-	-		reserved

00_h REV Revision

15															0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

The revision register can only be read. For the PSB 4860, V1.0, all bits except bit 12 are zero.

Note: A write access to the revision register does not alter its content. It does, however, reset the ABT bit of the STATUS register.

01_h CCTL Chip Control

15														0
0	0	0	0	MV	RFM	0	PD	0	0	0	MQ	MT	CS9	SAS

MV Voice Prompt EPROM

0: not available

1: available

RFM Refresh Mode

0: normal

1: battery backup

PD Power Down

0: PSB 4860 is in active mode

1: enter power-down mode

MT Memory Type

3	2	Description
0	0	ARAM/DRAM
0	1	Intel flash memory
1	1	Samsung flash memory

CS9 CAS selection

0: 256kx4 or 512kx8 memory

1: other memory

SAS Split Address Space

0: other ARAM/DRAM

1: two 2Mx8 devices

02_h INTM Interrupt Mask Register

15															0
RDY	1	DRQ	SDA	CIA	CD	CPT	CNG	SD	ERR	BSY	DTV	ATV	0	0	0

If a bit of this register is reset (set to 0), the corresponding bit of the status register does not generate an interrupt.

If a bit is set (set to 1), an external interrupt can be generated by the corresponding bit of the status register.

03_h AFECTL Analog Front End Interface Control

15												0
0	0	0	0	ALS	0	0	0	0	0	0	0	EN

ALS Loudspeaker Amplification

This value is transferred on channel C3 of the AFE interface. If the PSB 4851 is used it represents the amplification of the loudspeaker amplifier.

EN Interface Enable

0: AFE interface disabled

1: AFE interface enabled

04_h IFS1 Interface Select 1

15			0
HP	I1	I2	I3

HP High-Pass for S_1

0: Disabled

1: Enabled

I1 Input signal 1 for IG2

I2 Input signal 2 for IG2

I3 Input signal 3 for IG2

Note: As all sources are always active, unused sources must be set to 0 (S_0).

05_h IFG1 Interface Gain 1

15		0
0	IG1	

IG1

In order to obtain a gain *G* the parameter IG1 can be calculated by the following formula:

$$IG1 = 32768 \times 10^{(G - 12.04\ dB)/20\ dB}$$

06_h IFG2 Interface Gain 2

15		0
0	IG2	

IG2 Gain of Amplifier IG2

In order to obtain a gain *G* the parameter IG2 can be calculated by the following formula:

$$IG2 = 32768 \times 10^{(G - 12.04\ dB)/20\ dB}$$

07_h IFS2 Interface Select 2

15			0
HP	I1	I2	I3

HP **High-Pass for S_3**

0: Disabled

1: Enabled

I1 **Input signal 1 for IG4**

I2 **Input signal 2 for IG4**

I3 **Input signal 3 for IG4**

Note: As all sources are always active, unused sources must be set to 0 (S_0).

08_h IFG3 Interface Gain 3

15		0
0	IG3	

IG3 Gain of Amplifier IG3

In order to obtain a gain *G* the parameter IG3 can be calculated by the following formula:

$$IG3 = 32768 \times 10^{(G - 12.04\ dB)/20\ dB}$$

09_h IFG4 Interface Gain 4

15		0
0	IG4	

IG4 Gain of Amplifier IG4

In order to obtain a gain *G* the parameter IG4 can be calculated by the following formula:

$$IG4 = 32768 \times 10^{(G - 12.04\ dB)/20\ dB}$$

$0A_h$ SDCONF Serial Data Interface Configuration

15										0
0	0	NTS		0	0	0	0	0	DCL	0	SDE

NTS Number of Timeslots

11	10	9	8	7	6	Description
0	0	0	0	0	0	0
0	0	0	0	0	1	1
...	...	...	...	...	...	...
1	1	1	1	1	1	63

DCL Double Clock Mode

0: Single Clock Mode

1: Double Clock Mode

EN Enable Interface

0: Interface is disabled (both channels)

1: Interface is enabled (depending on separate channel enable bits)

$0B_h$ SDCHN1 Serial Data Interface Channel 1

15							0
NAS	0	0	PCD	EN	PCM	DD	TS

NAS Number of active DRST strobe (SSDI interface mode)

15	14	13	12	Description
0	0	0	0	1
...	...	...	...	...
1	1	1	1	16

PCD PCM Code

0: A-law

1: μ-law

EN Enable Interface

0: Interface is disabled

1: Interface is enabled if SDCONF:EN=1

PCM PCM Mode

0: 16 Bit Linear Coding (two timeslots)

1: 8 Bit PCM Coding (one timeslot)

DD Data Direction

0: DD: Data Downstream, DU: Data Upstream

1: DD: Data Upstream, DU: Data Downstream

TS Timeslot for Channel 1

5	4	3	2	1	0	Description
0	0	0	0	0	0	0
...	...	...	...	...	...	...
1	1	1	1	1	1	63

Note: If PCM=0 then TS denotes the first timeslot of the two consecutive timeslots used. Only even timeslots are allowed in this case.

$0C_h$ IFS3 Interface Select 3

15			0
HP	I1	I2	I3

HP High-Pass for S_6

0: Disabled

1: Enabled

I1 Input signal 1 for S_5

I2 Input signal 2 for S_5

I3 Input signal 3 for S_5

Note: As all sources are always active, unused sources must be set to 0 (S_0).

$0D_h$ SDCHN2 Serial Data Interface Channel 2

15										0
0	0	0	0	0	0	PCD	EN	PCM	DD	TS

PCD PCM Code

0: A-law

1: µ-law

EN Enable Interface

0: Interface is disabled

1: Interface is enabled if SDCONF:EN=1

PCM PCM Mode

0: 16 Bit Linear Coding (two timeslots)

1: 8 Bit PCM Coding (one timeslot)

DD Data Direction

0: DD: Data Downstream, DU: Data Upstream

1: DD: Data Upstream, DD: Data Downstream

TS Timeslot for Channel 2

5	4	3	2	1	0	Description
0	0	0	0	0	0	0
0	0	0	0	0	1	1
...	...	...	...	...	...	...
1	1	1	1	1	1	63

Note: If PCM=0 then TS denotes the first timeslot of the two consecutive timeslots used. Only even timeslots are allowed in this case.

$0E_h$ IFS4 Interface Select 4

15			0
HP	I1	I2	I3

HP High-Pass for S_7

0: Disabled

1: Enabled

I1 Input signal 1 for S_8

I2 Input signal 2 for S_8

I3 Input signal 3 for S_8

As all sources are always active, unused sources must be set to 0 (S_0).

$0F_h$ IFG5 Interface Gain 5

15	0
ATT1	ATT2

ATT1 Attenuation for I3 (Channel 1)

In order to obtain an attenuation *A* the parameter ATT1 can be calculated by the following formula:

$$ATT1 = 256 \times 10^{A/20\ dB}$$

ATT2 Attenuation for I3 (Channel 2)

In order to obtain an attenuation *A* the parameter ATT2 can be calculated by the following formula:

$$ATT2 = 256 \times 10^{A/20\ dB}$$

10_h UA Universal Attenuator

15				0
ATT	0	0	0	I1

ATT Attenuation for UA

For a given attenuation *A* [dB] the parameter ATT can be calculated by the following formula:

$$ATT = 256 \times 10^{A/20\,dB}$$

I1 Input Selection for UA

11_h DGCTL DTMF Generator Control

15												0
EN	MD	0	0	0	0	0	0	0	0	0	0	DTC

EN Generator Enable

0: Disabled

1: Enabled

MD Mode

0: raw

1: cooked

DTC Dial Tone Code (cooked mode)

3	2	1	0	Description
0	0	0	0	697/1209
0	0	0	1	697/1336
0	0	1	0	697/1477
0	0	1	1	697/1633
0	1	0	0	770/1209
0	1	0	1	770/1336
0	1	1	0	770/1477
0	1	1	1	770/1633
1	0	0	0	852/1209
1	0	0	1	852/1336
1	0	1	0	852/1477
1	0	1	1	852/1633
1	1	0	0	941/1209
1	1	0	1	941/1336
1	1	1	0	941/1477
1	1	1	1	941/1633

12_h DGF1 DTMF Generator Frequency 1

15		0
0	FRQ	

FRQ Frequency of Generator 1

The parameter FRQ for a given frequency *f* [Hz] can be calculated by the following formula:

$$FRQ = 32768 \times \frac{f}{4000\,Hz}$$

13_h DGF2 DTMF Generator Frequency 2

15															0
0	FRQ														

FRQ Frequency of Generator 2

he parameter FRQ for a given frequency *f* [Hz] can be calculated by the following formula:

$$FRQ = 32768 \times \frac{f}{4000\text{Hz}}$$

14_h DGL DTMF Generator Level

15			0
0	LEV2	0	LEV1

LEV2 Signal Level of Generator 2

In order to obtain a signal level *L* (relative to the PCM maximum value) for generator 2 the value of LEV2 can be calculated according to the following formula:

$$\mathrm{LEV2} = 128 \times 10^{\mathrm{L}/20\ \mathrm{dB}}$$

LEV1 Signal Level of Generator 1

In order to obtain a signal level *L* (relative to the PCM maximum value) for generator 1 the value of LEV1 can be calculated according to the following formula:

$$\mathrm{LEV1} = 128 \times 10^{\mathrm{L}/20\ \mathrm{dB}}$$

15_h DGATT DTMF Generator Attenuation

15			0
0	ATT2	0	ATT1

ATT2 Attenuation of Signal S_{10}

In order to obtain attenuation *A* the parameter ATT2 can be calculated by the formula:

$$ATT2 = \begin{cases} 128 + 1024 \times 10^{A/20\ dB} & ;A > 18,1\ dB \\ 128 \times 10^{A/20\ dB} & ;A < 18,1\ dB \end{cases}$$

ATT1 Attenuation of Signal S_9

In order to obtain attenuation *A* the parameter ATT1 can be calculated by the formula:

$$ATT1 = \begin{cases} 128 + 1024 \times 10^{A/20\ dB} & ;A > 18,1\ dB \\ 128 \times 10^{A/20\ dB} & ;A < 18,1\ dB \end{cases}$$

16_h CNGCTL Calling Tone Control

15										0
EN	0	0	0	0	0	0	0	0	0	I1

EN Enable

0: CNG unit disabled

1: CNG unit enabled

I1 Input Selection for Calling Tone Detector

17_h CNGBT CNG Burst Time

15		0
0	TIME	

TIME Minimum Time for Calling Tone

In order to obtain the parameter TIME for a minimum time *t* the following formula can be used:

$$\text{TIME} = t / 0.125\ \text{ms}$$

18_h CNGLEV CNG Minimal Signal Level

15			0
0	0	MIN	

MIN Minimum Signal Level for Calling Tone

In order to obtain the parameter MIN for a minimum signal level *L* the following formula can be used:

$$\mathrm{MIN} = 16384 \times 10^{\mathrm{L}/20\ \mathrm{dB}}$$

19_h CNGRES CNG Signal Resolution

15					0
1	1	1	1	RES	

RES Signal Resolution

The parameter RES depends on the noise level *L* as follows:

$$RES = -4096 \times 10^{L/20\ dB}$$

$1A_h$ ATDCTL0 Alert Tone Detection 0

15									0
EN	0	0	I1	0	0	0	0	0	ATC

EN **Enable alert tone detection**

0: The alert tone detection is disabled

1: The alert tone detection is enabled

I1 **Input signal selection**

ATC **Alert Tone Code**

1	0	Description
0	0	no tone
0	1	2130
1	0	2750
1	1	2130/2750

$1B_h$ ATDCTL1 Alert Tone Detection 1

15								0
MD	0	0	DEV	0	0	0	0	MIN

MD **Alert tone detection mode**

0: Only a dual tone is detected

1: Either a dual or a single tone is detected

DEV **Maximum frequency deviation for alert tone**

0: 0.5%

1: 1.1%

MIN **Minimum level of alert tone signal**

For a minimum signal level *min* the parameter MIN is given by the following formula:

$$\mathrm{MIN} = 2560 \times 10^{\mathrm{min}/20\ \mathrm{dB}}$$

$1C_h$ CIDCTL0 Caller ID Control 0

15				0
EN	0	0	I1	DATA

EN **CID Enable**

0: Disabled

1: Enabled

I1 **Input signal selection**

DATA **Last received data byte**

$1D_h$ CIDCTL1 Caller ID Control 1

15		0
NMB	NMSS	MIN

NMB Minimum Number of Mark Bits

15	14	13	12	11	10	Description
0	0	0	0	0	0	0
0	0	0			1	10
...	...	...	...	...	...	...
1	1	1	1	1	1	630

NMSS Minimum Number of Mark/Space Sequences

9	8	7	6	5	Description
0	0	0	0	0	1
0	0	0	0	1	11
...	...	...	...	...	
1	1	1	1	1	311

MIN Minimum Signal Level for CID Decoder

For a minimum signal level *min* the parameter MIN is given by the following formula:

$$\mathrm{MIN} = 640 \times 10^{\mathrm{min}/20\,\mathrm{dB}}$$

20_h CPTCTL Call Progress Tone Control

15											0
EN	MD	0	0	0	0	0	0	0	0	0	I1

EN **CPT Detector Enable**

0: Disabled

1: Enabled

MD **CPT Mode**

0: raw

1: cooked

I1 **Input signal selection**

21_h CPTTR Call Progress Tone Thresholds

15			0
NUM	0	SN	MIN

NUM Number of Cycles

15	14	13	cooked mode	raw mode
0	0	0	1	0
0	0	1	2	reserved
...	...	...	...	reserved
1	1	1	8	reserved

SN Minimal Signal-to-Noise Ratio

11	10	9	8	Description
1	1	1	1	9 dB
1	0	0	0	12 dB
0	1	0	0	15 dB
0	0	1	0	18 dB
0	0	0	0	22 dB

MIN Minimum Signal Level for CPT Detector

Value	Description
89_h	-40 dB
$9C_h$	-45 dB
90_h	-50 dB
$A2_h$	-55 dB

22_h CPTMN CPT Minimum Times

15	0
MINB	MING

MINB Minimum Time for CPT Burst

The parameter MINB for a minimal burst time *TBmin* can be calculated by the following formula:

$$\text{MINB} = \frac{\text{TBmin} - 32\ \text{ms}}{4}$$

MING Minimum Time for CPT Gap

The parameter MING for a minimal burst time *TGmin* can be calculated by the following formula:

$$\text{MING} = \frac{\text{TGmin} - 32\ \text{ms}}{4}$$

23_h CPTMX CPT Maximum Times

15	0
MAXB	MAXG

MAXB Maximum Time for CPT Burst

The parameter MAXB for a maximal burst time of *TBmax* can be calculated by the following formula:

$$MINB = \frac{TBmax - TBmin}{8}$$

MAXG Maximum Time for CPT Gap

The parameter MAXG for a maximal burst time of *TGmax* can be calculated by the following formula:

$$MING = \frac{TGmax - TGmin}{8}$$

24_h CPTDT CPT Delta Times

15	0
DIFB	DIFG

DIFB Maximum Time Difference between consecutive Bursts

The parameter DIFB for a maximal difference of *t* ms of two burst durations can be calculated by the following formula:

$$\mathrm{DIFB} = \frac{t}{2\ \mathrm{ms}}$$

DIFG Maximum Time Difference between consecutive Gaps

The parameter DIFG for a maximal difference of *t* ms of two gap durations can be calculated by the following formula:

$$\mathrm{DIFG} = \frac{t}{2\ \mathrm{ms}}$$

25_h LECCTL Line Echo Cancellation Control

15							0
EN	MD	0	0	0	0	I1	I2

EN Enable

0: Disabled

1: Enabled

MD Mode

0: Normal

1: Extended

I1 Input signal selection for I_1

I2 Input signal selection for I_2

26_h LECLEV Minimal Signal Level for Line Echo Cancellation

15		0
0	MIN	

MIN

The parameter MIN for a minimal signal level *L* (dB) can be calculated by the following formula:

$$\mathrm{MIN} = \frac{512 \times (96.3 + \mathrm{L})}{5 \times \log 2}$$

27_h LECATT Externally Provided Attenuation

15		0
0	ATT	

ATT

The parameter ATT for an externally provided attenuation *A* (dB) can be calculated by the following formula:

$$\mathrm{ATT} = \frac{512 \times \mathrm{A}}{5 \times \log 2}$$

28_h LECMGN Margin for Double Talk Detection

15		0
0	MGN	

MGN

The parameter MGN for a margin of *L* (dB) can be calculated by the following formula:

$$\mathrm{MGN} = \frac{512 \times \mathrm{L}}{5 \times \log 2}$$

29_h DDCTL DTMF Recognition Control

15							0
EN	DF	0	I1	0	0	0	DTC

EN Enable DTMF tone detection

0: The DTMF detection is disabled

1: The DTMF detection is enabled

DF Dial tone filter

0: The dial tone filter is disabled

1: The dial tone filter is enabled

I1 Input signal selection

DTC DTMF Tone Code

4	3	2	1	0	Description
1	0	0	0	0	941 / 1633
1	0	0	0	1	697 / 1209
1	0	0	1	0	697 / 1336
1	0	0	1	1	697 / 1477
1	0	1	0	0	770 / 1209
1	0	1	0	1	770 / 1336
1	0	1	1	0	770 / 1477
1	0	1	1	1	852 / 1209
1	1	0	0	0	852 / 1336
1	1	0	0	1	852 / 1477
1	1	0	1	0	941 / 1336
1	1	0	1	1	941 / 1209
1	1	1	0	0	941 / 1477
1	1	1	0	1	697 / 1633
1	1	1	1	0	770 / 1633
1	1	1	1	1	852 / 1633

$2A_h$ DDTW DTMF Detector Signal Twist

15		0
0	TWIST	

TWIST Signal twist for DTMF tone

In order to obtain a minimal signal twist *T* the parameter TWIST can be calculated by the following formula:

$$\mathrm{TWIST} = 32768 \times 10^{(0.5\ \mathrm{dB} - \mathrm{T})/10\ \mathrm{dB}}$$

Note: TWIST must be in the range [4096,20480]

$2B_h$ DDLEV DTMF Detector Minimum Signal Level

15										0
1	1	1	1	1	1	1	1	1	1	MIN

MIN Minimum Signal Level

5	4	3	2	1	0	Description
0	0	1	1	1	0	-50 dB
0	0	1	1	1	1	-49 dB
...	...	...	...	...	...	...
1	0	0	0	0	1	-31 dB
1	0	0	0	1	0	-30 dB

Note: Values outside the given range are reserved an must not be used.

$2E_h$ FCFCTL Equalizer Control

15						0
EN	0	ADR	0	0	0	I

EN Enable equalizer

0: The equalizer is disabled

1: The equalizer is enabled

ADR Coefficient address

13	12	11	10	9	8	Coefficient
0	0	0	0	0	0	A1
0	0	0	0	0	1	A2
0	0	0	0	1	0	A3
0	0	0	0	1	1	A4
0	0	0	1	0	0	A5
0	0	0	1	0	1	A6
0	0	0	1	1	0	A7
0	0	0	1	1	1	A8
0	0	1	0	0	0	A9
0	0	1	0	0	1	B2
0	0	1	0	1	0	B3
0	0	1	0	1	1	B4
0	0	1	1	0	0	B5
0	0	1	1	0	1	B6
0	0	1	1	1	0	B7
0	0	1	1	1	1	B8
0	1	0	0	0	0	B9
0	1	0	0	0	1	C1
0	1	0	0	1	0	D1
0	1	0	0	1	1	D2
0	1	0	1	0	0	D3
0	1	0	1	0	1	D4
0	1	0	1	1	0	D5
0	1	0	1	1	1	D6
0	1	1	0	0	0	D7

13	12	11	10	9	8	Coefficient
0	1	1	0	0	1	D8
0	1	1	0	1	0	D9
0	1	1	0	1	1	D10
0	1	1	1	0	0	D11
0	1	1	1	0	1	D12
0	1	1	1	1	0	D13
0	1	1	1	1	1	D14
1	0	0	0	0	0	D15
1	0	0	0	0	1	D16
1	0	0	0	1	0	D17
1	0	0	0	1	1	C2

I1 Input signal selection

$2F_h$ FCFCOF Equalizer Coefficient Data

15															0
V															

V Coefficient value

For the coefficient A_1-A_9, B_2-B_9 and D_1-D_{17} the following formula can be used to calculate V for a coefficient *c*:

$$V = 32768 \times c \quad ; -1 \leq c < 1$$

For the coefficients C_1 and C_2 the following formula can be used to calculate V for a coefficient *c*:

$$V = 128 \times c \quad ; 1 \leq c < 256$$

30_h SCCTL Speech Coder Control

15							0
EN	HQ	VC	DST	0	0	I1	I2

EN Enable

0: Disabled

1: Enabled

HQ High Quality Mode

0: Long Play Mode

1: High Quality Mode

VC Voice Controlled Start of Recording

0: Disabled

1: Enabled

DST Data Destination

0: Memory

1: SCI

I1 Input signal selection (first input)

I2 Input signal selection (second input)

31_h SCCT2 Speech Coder Control 2

15	0
TIME	MIN

TIME

The parameter TIME for a time *t* ([ms]) can be calculated by the following formula:

$$\mathrm{TIME} = \frac{t}{32}$$

MIN

The parameter MIN for a signal level *L* ([dB]) can be calculated by the following formula:

$$\mathrm{MIN} = 16384 \times 10^{\frac{L}{20}}$$

33_h SCCT3 Speech Coder Control 3

15									0
0	LP	0	0	0	0	0	0	0	0

LP

The parameter LP for a time constant of *t* ([ms]) can be calculated by the following formula:

$$LP = \frac{256}{t}$$

33_h SCDATA Speech Coder Data

15															0
DATA															

Coded Speech Data

34_h SDCTL Speech Decoder Control

15														0
EN	0	0	SRC	0	0	0	0	0	0	0	0	0		SPEED

EN Enable

0: Disabled

1: Enabled

SRC Data Source

0: Memory

1: SDDATA Register

SPEED Playback Speed

1	0	Description
0	0	normal speed
0	1	0.5 times normal speed
1	0	1.5 times normal speed
1	1	2.0 times normal speed

35_h SDDATA Speech Decoder Data

15	0
Data	

Data for speech decoder if SDCTL.SRC=1.

38_h AGCCTL AGC Control

15							0
EN	0	0	0	0	0	I1	I2

EN **Enable**

0: Disabled

1: Enabled

I1 **Input signal selection for I_1**

I2 **Input signal selection for I_2**

39_h AGCATT Automatic Gain Control Attenuation

15		0

ATT

The parameter ATT for an attenuation *A* ([dB]) can be calculated by the following formula:

$$ATT = 32768 \times 10^{\frac{A}{20}}$$

$3A_h$ AGC1 Automatic Gain Control 1

15		0
COM	0	AG_INIT

COM

The parameter COM for a signal level *L* ([dB]) can be calculated by the following formula:

$$COM = \begin{cases} 128 + 10^{\frac{L + 66,22}{20}} & ;L < -42{,}14\ dB \\ 10^{\frac{L + 42,14}{20}} & ;L > -42{,}14\ dB \end{cases}$$

AG_INIT

In order to obtain an initial gain *G* ([db]) the parameter AG_INIT can be calculated by the following formula:

$$AG\_INIT = \begin{cases} 128 + 10^{\frac{G + 18,06}{20}} & ;G < 6,02\ dB \\ 10^{\frac{G - 6,02}{20}} & ;G > 6,02\ dB \end{cases}$$

$3B_h$ AGC2 Automatic Gain Control 2

15	0
SPEEDL	SPEEDH

SPEEDL

The parameter SPEEDL for a multiplication factor *M* ([0; 0.007]) is given by the following formula:

$$\mathrm{SPEEDL} = \frac{\mathrm{M}}{8192}$$

SPEEDH

The parameter SPEEDH for a multiplication factor *M* ([0; 0.007]) is given by the following formula:

$$\mathrm{SPEEDH} = \frac{\mathrm{M}}{8192}$$

$3C_h$ AGC3 Automatic Gain Control 3

15		0
MIN	0	MAX

MIN

The parameter MIN for a gain *G* ([dB]) can be calculated by the following formula:

$$MIN = \begin{cases} 128 + 10^{\frac{G + 18,06}{20}} & ;G < 6,02\ dB \\ 10^{\frac{G - 6,02}{20}} & ;G > 6,02\ dB \end{cases}$$

MAX

The parameter MAX for an attenuation *A* ([dB]) can be calculated by the following formula:

$$MAX = 10^{\frac{A + 42,14}{20}}$$

$3D_h$ AGC4 Automatic Gain Control 4

15		0
0	DEC	LIM

DEC

The parameter DEC for a time constant *t* ([1/ms]) is given by the following formula:

$$DEC = \frac{256}{t}$$

LIM

The parameter LIM for a signal level *L* ([dB]) can be calculated by the following formula:

$$LIM = \begin{cases} 128 + 10^{\frac{L + 90,3}{20}} & ;L < 66{,}22\ dB \\ 10^{\frac{L + 66,22}{20}} & ;L > 66{,}22\ dB \end{cases}$$

$3E_h$ AGC5 Automatic Gain Control 5

15									0
0	0	0	0	0	0	0	0	1	LP

LP

The parameter LP for a time constant *t* ([1/ms]) is given by the following formula:

$$LP = \frac{16}{t}$$

40_h FCTL File Control

15								0
0	MD	MS	TS	0	0	0	0	FNO

MD Mode

0: Audio Mode

1: Binary Mode

MS Memory Space

0: R/W Memory

1: Voice Prompt EPROM

TS Time Stamp

0: no update of RTC1/RTC2 entry of file descriptor

1: RTC1/RTC2 entries are updated by content of RTC1/RTC2 registers.

FNO File Number

41_h FCMD File Command

15											0
0	IN	RD	0	0	0	0	0	ABT	0	0	CMD

IN Initialize

0: no

1: yes (if CMD=1111)

RD Remap Directory

0: no

1: yes

ABT Abort Command

0: no

1: abort recompress

CMD File Command

4	3	2	1	0	Description
0	0	0	0	0	Open File
0	0	0	0	1	Activate
0	0	0	1	0	Seek
0	0	0	1	1	Cut File
0	0	1	0	0	Read Data
0	0	1	0	1	Write Data
0	0	1	1	0	Memory Status
0	0	1	1	1	Recompress file
0	1	0	0	0	Read File Descriptor - User
0	1	0	0	1	Write File Descriptor - User
0	1	0	1	0	Read File Descriptor - RTC1
0	1	0	1	1	Read File Descriptor - RTC2
0	1	1	0	0	Read File Descriptor - LEN
0	1	1	0	1	Garbage Collection
0	1	1	1	0	Open Next Free File
0	1	1	1	1	Initialize
1	-	-	-	-	reserved

42_h FDATA File Data

15															0
FREE															

The FDATA register contains the following information after a memory status command:

FREE Free Blocks

Number of blocks (8 kB) currently usable for recording.

43_h FPTR File Pointer

15						0
File Pointer						
0	0	0	0	0	Phrase selector	

47h SPSCTL SPS Control

15										0
POS	0	0	0	0	0	0	0	MODE	SP1	SP0

POS Position of Status Register Window

15	14	13	12	SPS_0	SPS_1
0	0	0	0	Bit 0	Bit 1
0	0	0	1	Bit 1	Bit 2
...	...	...	...	...	...
1	1	1	0	Bit 14	Bit 15

MODE Mode of SPS Interface

4	3	2	Description
0	0	0	Disabled (SPS_0 and SPS_1 zero)
0	0	1	Output of SP1 and SP0
1	0	0	Output of speakerphone state
1	0	1	Output of STATUS register

SP1 Direct Control for SPS_1

0: SPS_1 set to 0

1: SPS_1 set to 1

SP0 Direct Control for SPS_0

0: SPS_0 set to 0

1: SPS_0 set to 1

48_h RTC1 Real Time Clock 1

15					0
0	0	0	0	MIN	SEC

MIN Minutes

Number of minutes elapsed in the current hour (0-59).

SEC Seconds

Number of seconds elapsed in the current minute (0-59).

49_h RTC2 Real Time Clock 2

15	0
DAY	HR

DAY Days

Number of days elapsed since last reset (0-2047).

HR Hours

Number of hours elapsed in the current day (0-23).

$4A_h$ DOUT0 Data Out (Timeslot 0)

15					0
0	0	0	0	DATA	

DATA Output Data

Output data for pins MA_0-MA_{11} while MA_{12}=1 (only if HWCONFIG1:APP=10).

$4B_h$ DOUT1 Data Out (Timeslot 1)

15					0
0	0	0	0	DATA	

DATA Output Data

Output data for pins MA_0-MA_{11} while MA_{13}=1 (only if HWCONFIG1:APP=10).

$4C_h$ DOUT2 Data Out (Timeslot 2)

15					0
0	0	0	0	DATA	

DATA Output Data

Output data for pins MA_0-MA_{11} while MA_{14}=1 (only if HWCONFIG1:APP=10).

$4D_h$ DOUT3 Data Out (Timeslot 3 or Static Mode)

15	0
DATA	

DATA Output Data

Output data for pins MA_0-MA_{11} while MA_{15}=1 (only if HWCONFIG1:APP=10).

Output data for pins MA_0-MA_{15} (only if HWCONFIG1:APP=01)

$4E_h$ DIN Data In (Timeslot 3 or Static Mode)

15															0
DATA															

DATA Input Data

Input data for pins MA_0-MA_{11} at falling edge of MA_{12} (only if HWCONFIG1:APP=10).
Input data for pins MA_0-MA_{15} (only if HWCONFIG1:APP=01)

$4F_h$ DDIR Data Direction (Timeslot 3 or Static Mode)

15															0
DIR															

DIR Port Direction

Port direction during MA_{12}=1 or in static mode.

0: input

1: output

60_h SCTL Speakerphone Control

15															0
ENS	ENC	0	0	0	0	0	0	MD	SDR	SDX	0	0	AGR	AGX	0

ENS Enable Echo Suppression

0: The echo suppression unit is disabled

1: The echo suppression unit is enabled

ENC Enable Echo Cancellation

0: The echo cancellation unit is disabled

1: The echo cancellation unit is enabled

MD Mode

0: Speakerphone mode

1: Loudhearing mode

SDR Signal Source of SDR

0: after AGCR

1: before AGCR

SDX Signal Source of SDX

0: after AGCX

1: before AGCX

AGR AGCR Enable

0: AGCR disabled

1: AGCR enabled

AGX AGCX Enable

0: AGCX disabled

1: AGCX enabled

62_h SSRC1 Speakerphone Source 1

15							0
0	0	0	0	0	0	I1	I2

I1 **Input Signal Selection (Acoustic Source 1)**

I2 **Input Signal Selection (Acoustic Source 2)**

63_h SSRC2 Speakerphone Source 2

15							0
0	0	0	0	0	0	I3	I4

I3 Input Signal Selection (Line Source 1)

I4 Input Signal Selection (Line Source 2)

64_h SSDX1 Speech Detector (Transmit) 1

15			0
0	LP2L	0	LIM

LP2L

The parameter LP2L for a saturation level *L* (dB) can be calculated by the following formula:

$$LP2L = \frac{2 \times L}{5 \times \log 2}$$

LIM

The parameter LIM for a minimum signal level *L* (dB, relative to PCM max. value) can be calculated by the following formula:

$$LIM = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

65_h SSDX2 Speech Detector (Transmit) 2

15		0
LP1	0	OFF

LP1

The parameter LP1 for a time *t* (ms) can be calculated by the following formula:

$$LP1 = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

OFF

The parameter OFF for a level offset of *O* (dB) can be calculated by the following formula:

$$OFF = \frac{2 \times O}{5 \times \log 2}$$

66_h SSDX3 Speech Detector (Transmit) 3

15	0
PDN	LP2N

PDN

The parameter PDN for a time *t* (ms) can be calculated by the following formula:

$$PDN = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

LP2N

The parameter LP2N for a time *t* (ms) can be calculated by the following formula:

$$LP2N = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

67_h SSDX4 Speech Detector (Transmit) 4

15		0
PDS	0	LP2S

PDS

The parameter PDS for a time *t* (ms) can be calculated by the following formula:

$$PDS = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

LP2S

The parameter LP2S for a time *t* (ms) can be calculated by the following formula:

$$LP2S = \frac{262144}{t}$$

68_h SSDR1 Speech Detector (Receive) 1

15			0
0	LP2L	0	LIM

LP2L

The parameter LP2L for a saturation level *L* (dB) can be calculated by the following formula:

$$LP2L = \frac{2 \times L}{5 \times \log 2}$$

LIM

The parameter LIM for a minimum signal level *L* (dB, relative to PCM max. value) can be calculated by the following formula:

$$LIM = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

69_h SSDR2 Speech Detector (Receive) 2

15		0
LP1	0	OFF

LP1

The parameter LP1 for a time *t* (ms) can be calculated by the following formula:

$$LP1 = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

OFF

The parameter OFF for a level offset of *O* (dB) can be calculated by the following formula:

$$OFF = \frac{2 \times O}{5 \times \log 2}$$

$6A_h$ SSDR3 Speech Detector (Receive) 3

15	0
PDN	LP2N

PDN

The parameter PDN for a time *t* (ms) can be calculated by the following formula:

$$PDN = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

LP2N

The parameter LP2N for a time *t* (ms) can be calculated by the following formula:

$$LP2N = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

$6B_h$ SSDR4 Speech Detector (Receive) 4

15		0
PDS	0	LP2S

PDS

The parameter PDS for a time *t* (ms) can be calculated by the following formula:

$$PDS = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

LP2S

The parameter LP2S for a time *t* (ms) can be calculated by the following formula:

$$LP2S = \frac{262144}{t}$$

$6C_h$ SSCAS1 Speech Comparator (Acoustic Side) 1

15															0
G								ET							

G

The parameter G for a gain *A* (dB) can be calculated by the following formula:

$$G = \frac{2 \times A}{5 \times \log 2}$$

Note: The parameter G is interpreted in two's complement.

ET

The parameter ET for a time t (ms) can be calculated by the following formula:

$$ET = \frac{t}{4}$$

$6D_h$ SSCAS2 Speech Comparator (Acoustic Side) 2

15		0
0	GDN	PDN

GDN

The parameter GDN for a gain *G* (dB) can be calculated by the following formula:

$$\mathrm{GDN} = \frac{4 \times \mathrm{G}}{5 \times \log 2}$$

PDN

The parameter PDN for a decay rate *R* (ms/dB) can be calculated by the following formula:

$$\mathrm{PDN} = \frac{64 \times \mathrm{R}}{5 \times \log 2}$$

$6E_h$ SSCAS3 Speech Comparator (Acoustic Side) 3

15		0
0	GDS	PDS

GDS

The parameter GDS for a gain *G* (dB) can be calculated by the following formula:

$$\mathrm{GDS} = \frac{4 \times \mathrm{G}}{5 \times \log 2}$$

PDS

The parameter PDS for a decay rate *R* (ms/dB) can be calculated by the following formula:

$$\mathrm{PDS} = \frac{64 \times \mathrm{R}}{5 \times \log 2}$$

$6F_h$ SSCLS1 Speech Comparator (Line Side) 1

15															0
G								ET							

G

The parameter G for a gain *A* (dB) can be calculated by the following formula:

$$G = \frac{2 \times A}{5 \times \log 2}$$

Note: The parameter G is interpreted in two's complement.

ET

The parameter ET for a time t (ms) can be calculated by the following formula:

$$ET = \frac{t}{4}$$

70_h SSCLS2 Speech Comparator (Line Side) 2

15		0
0	GDN	PDN

GDN

The parameter GDN for a gain *G* (dB) can be calculated by the following formula:

$$GDN = \frac{4 \times G}{5 \times \log 2}$$

PDN

The parameter PDN for a decay rate *R* (ms/dB) can be calculated by the following formula:

$$PDN = \frac{64 \times R}{5 \times \log 2}$$

71_h SSCLS3 Speech Comparator (Line Side) 3

15		0
0	GDS	PDS

GDS

The parameter GDS for a gain *G* (dB) can be calculated by the following formula:

$$GDS = \frac{4 \times G}{5 \times \log 2}$$

PDS

The parameter PDS for a decay rate *R* (ms/dB) can be calculated by the following formula:

$$PDS = \frac{64 \times R}{5 \times \log 2}$$

72_h SATT1 Attenuation Unit 1

15		0
0	ATT	SW

ATT

The parameter ATT for an attenuation *A* (dB) can be calculated by the following formula:

$$\mathrm{ATT} = \frac{2 \times \mathrm{A}}{5 \times \log 2}$$

SW

The parameter SW for a switching rate *R* (ms/dB) can be calculated by the following formula:

$$\mathrm{SW} = \begin{cases} 128 + \dfrac{1}{5 \times \log 2 \times \mathrm{SW}} & ;0.0053 < \mathrm{SW} < 0.66 \\ \dfrac{16}{5 \times \log 2 \times \mathrm{SW}} & ;0.66 < \mathrm{SW} < 0.63 \end{cases}$$

73_h SATT2 Attenuation Unit 2

15	0
TW	DS

TW

The parameter TW for a time *t* (ms) can be calculated by the following formula:

$$TW = \frac{t}{16}$$

DS

The parameter DS for a decay rate *R* (ms/dB) can be calculated by the following formula:

$$DS = \frac{5 \times \log 2 \times R - 1}{4}$$

74_h SAGX1 Automatic Gain Control (Transmit) 1

15		0
AG_INIT	0	COM

AG_INIT

The parameter AG_INIT for a gain *G* (dB) can be calculated by the following formula:

$$\text{AG\_INIT} = \frac{-2 \times G}{5 \times \log 2}$$

This parameter is interpreted in two's complement.

COM

The threshold COM for a level *L* (dB) can be calculated by the following formula:

$$\text{COM} = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

75_h SAGX2 Automatic Gain Control (Transmit) 2

15		0
0	AG_ATT	SPEEDH

AG_ATT

The parameter AG_ATT for a gain *G* (dB) can be calculated by the following formula:

$$\mathrm{AG\_ATT} = \frac{-2 \times \mathrm{G}}{5 \times \log 2}$$

SPEEDH

The parameter SPEEDH for the regulation speed *R* (ms/dB) can be calculated by the following formula:

$$\mathrm{SPEEDH} = \frac{4096}{\mathrm{D} \times \mathrm{R}}$$

The variable D denotes the aberration (dB).

76_h SAGX3 Automatic Gain Control (Transmit) 3

15	0
AG_GAIN	SPEEDL

AG_GAIN

The parameter AG_GAIN for a gain *G* (dB) can be calculated by the following formula:

$$\text{AG\_GAIN} = \frac{-2 \times G}{5 \times \log 2}$$

SPEEDL

The parameter COM for a gain *G* (dB) can be calculated by the following formula:

$$\text{COM} = \frac{2 \times (96.3 + G)}{5 \times \log 2}$$

The variable D denotes the aberration (dB).

77_h SAGX4 Automatic Gain Control (Transmit) 4

15			0
0	NOIS	0	LPA

NOIS

The parameter NOIS for a threshold level *L* (dB) can be calculated by the following formula:

$$COM = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

LPA

The parameter LPA for a low pass time constant *T* (mS) can be calculated by the following formula:

$$LPA = \frac{16}{T}$$

78_h SAGX5 Automatic Gain Control (Transmit) 5

15								0
AG_CUR	0	0	0	0	0	0	0	0

AG_CUR

The current gain *G* of the AGC can be derived from the parameter Parameter AG_CUR by the following formula:

$$G = \frac{-5 \times \log 2 \times AG\_CUR}{2}$$

AG_CUR is interpreted in two’s complement.

79_h SAGR1 Automatic Gain Control (Receive) 1

15		0
AG_INIT	0	COM

AG_INIT

The parameter AG_INIT for a gain *G* (dB) can be calculated by the following formula:

$$\text{AG\_INIT} = \frac{-2 \times G}{5 \times \log 2}$$

This parameter is interpreted in two's complement.

COM

The parameter COM for a threshold *L* (dB) can be calculated by the following formula:

$$\text{COM} = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

$7A_h$ SAGR2 Automatic Gain Control (Receive) 2

15		0
0	AG_ATT	SPEEDH

AG_ATT

The parameter AG_ATT for a gain *G* (dB) can be calculated by the following formula:

$$\mathrm{AG\_ATT} = \frac{-2 \times \mathrm{G}}{5 \times \log 2}$$

SPEEDH

The parameter SPEEDH for the regulation speed *R* (ms/dB) can be calculated by the following formula:

$$\mathrm{SPEEDH} = \frac{4096}{\mathrm{D} \times \mathrm{R}}$$

The variable D denotes the aberration (dB).

$7B_h$ SAGR3 Automatic Gain Control (Receive) 3

15	0
AG_GAIN	SPEEDL

AG_GAIN

The parameter AG_GAIN for a gain *G* (dB) can be calculated by the following formula:

$$\text{AG\_GAIN} = \frac{-2 \times G}{5 \times \log 2}$$

SPEEDL

The parameter SPEEDL for the regulation speed *R* (ms/dB) can be calculated by the following formula:

$$\text{SPEEDL} = \frac{4096}{D \times R}$$

The variable D denotes the aberration (dB).

$7C_h$ SAGR4 Automatic Gain Control (Receive) 4

15			0
0	NOIS	0	LPA

NOIS

The parameter NOIS for a threshold level *L* (dB) can be calculated by the following formula:

$$COM = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

LPA

The parameter LPA for a low pass time constant *T* (mS) can be calculated by the following formula:

$$LPA = \frac{16}{T}$$

$7D_h$ SAGR5 Automatic Gain Control (Receive) 5

15								0
AG_CUR	0	0	0	0	0	0	0	0

AG_CUR

The current gain *G* of the AGC can be derived from the parameter Parameter AG_CUR by the following formula:

$$G = \frac{-5 \times \log 2 \times AG\_CUR}{2}$$

AG_CUR is interpreted in two’s complement.

$7E_h$ SLGA Line Gain

15			0
0	LGAR	0	LGAX

LGAR

The parameter LGAR for a gain *G* (dB) is given by the following formula:

$$\mathrm{LGAR} = 128 \times 10^{(G-12)/20}$$

LGAX

The parameter LGAX for a gain *G* (dB) is given by the following formula:

$$\mathrm{LGAX} = 128 \times 10^{(G-12)/20}$$

80_h SAELEN Acoustic Echo Cancellation Length

15							0
0	0	0	0	0	0	0	LEN

LEN

LEN denotes the number of FIR-taps used.

81_h SAEATT Acoustic Echo Cancellation Double Talk Attenuation

15		0
0	ATT	

ATT

The parameter ATT for an attenuation *A* (dB) is given by the following formula:

$$\mathrm{ATT} = \frac{512 \times \mathrm{A}}{5 \times \log 2}$$

82_h SAEGS Acoustic Echo Cancellation Global Scale

15													0
0	0	0	0	0	0	0	0	0	0	0	0	0	GS

GS

All coefficients of the FIR filter are scaled by a factor C. This factor is given by the following equation:

$$C = 2^{GS}$$

83_h SAEPS Acoustic Echo Cancellation Partial Scale

15													0
0	0	0	0	0	0	0	0	0	0	0	0	0	PS

PS

The additional scaling coefficient AC is given by the following formula:

$$AC = 2^{PS}$$

84_h SAEPS Acoustic Echo Cancellation First Block

15													0
0	0	0	0	0	0	0	0	0	0	0	0	0	FB

FB

The parameter FB denotes the first block that is affected by the partial scaling coefficient. If the partial coefficient is one, FB is disregarded.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	-20 to 85	°C
Storage temperature	T_{STG}	– 65 to125	°C
Supply Voltage	V_{DD}	-0.5 to 4.2	V
Supply Voltage	V_{DDA}	-0.5 to 4.2	V
Supply Voltage	V_{DDP}	-0.5 to 6	V
Voltage of pin with respect to ground: $XTAL_1$, $XTAL_2$	V_S	0 to V_{DDA}	V
Voltage on any pin with respect to ground	V_S	If V_{DDP} < 3 V: – 0.4 to V_{DD} + 0.5 If V_{DDP} > 3 V: – 0.4 to V_{DDP} + 0.5	V

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.2 DC Characteristics

V_{DD}/V_{DDA} = 3.3 V ± 0.3 V; V_{DDP} = 5 V ± 10%; V_{SS}/V_{SSA} = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input leakage current	I_{IL}	– 1.0		1.0	µA	0 V ≤ V_{IN} ≤ V_{DD}
H-input level (except MA_0-MA_{15}, $XTAL_1$,OSC_1)	V_{IH1}	2.0		V_{DDP} + 0.3	V	
H-input level ($XTAL_1$)	V_{IH2}	2.4		V_{DD}	V	
H-input level (OSC_1)	V_{IH3}	0.7 V_{DD}		V_{DD} + 0.3	V	
H-input level (MA_0-MA_{15})	V_{IH4}	2.0		V_{DD}	V	
L-input level (except pins $XTAL_1$,OSC_1)	V_{IL1}	– 0.3		0.8	V	
L-input level ($XTAL_1$)	V_{IL2}	0		0.4	V	

V_{DD}/V_{DDA} = 3.3 V ± 0.3 V; V_{DDP} = 5 V ± 10%; V_{SS}/V_{SSA} = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
L-input level (OSC_1)	V_{IL3}	– 0.3		0.3 V_{DD}	V	
H-output level (except DU/DX, DD/DR, MA_0-MA_{15}, SPS_0, SPS_1, MD_0-MD_7)	V_{OH1}	V_{DD} – 0.45			V	I_O = 2 mA
H-output level (SPS_0, SPS_1, MD_0-MD_7, SDX)	V_{OH2}	*2.4*			V	I_O = 2 mA
H-output level (SPS_0, SPS_1, MD_0-MD_7, SDX)	V_{OH3}	V_{DD} – 0.45			V	I_O = 1 mA
H-output level (MA_0-MA_{15})	V_{OH4}	V_{DD} – 0.45			V	I_O = 5 mA
H-output level (DU/DX, DD/DR)	V_{OH5}	V_{DD} – 0.45			V	I_O = 7 mA
L-output level (except DU/DX, DD/DR, MA_0-MA_{15})	V_{OL1}			0.45	V	I_O = – 2 mA
L-output level (MA_0-MA_{15}) (address mode or APP output)	V_{OL2}			0.45	V	I_O = – 5 mA
L-output current (MA_0-MA_{15}) (after reset)	I_{LO}		125		µA	RST=1
H-output current ($\overline{W}/\overline{FWE}$, $\overline{VPRD}/\overline{FPD}$/FCLE, $\overline{RAS}/\overline{FOE}$, $\overline{CAS_0}$/ALE, $\overline{CAS_1}/\overline{FCS}$) (during reset)	I_{HO}		70		µA	RST=1
L-output level (pins DU/DX, DD/DR)	V_{OL3}			0.45	V	I_O = – 7 mA
Internal pullup current ($\overline{FRDY}$)	I_{LI}		750		µA	
Input capacitance	C_I			10	pF	
Output capacitance	C_O			15	pF	
V_{DD} supply current (power down, no refresh, no RTC)	I_{DDS1}			50	µA	V_{DD} = 3.3 V
V_{DD} supply current (power down, refresh, no RTC)	I_{DDS2}			500	µA	V_{DD} = 3.3 V
V_{DD} supply current (power down, refresh, RTC)	I_{DDS3}			700	µA	V_{DD} = 3.3 V
V_{DD} supply current operating	I_{DDO}			100	mA	V_{DD} = 3.3 V
V_{DDP} supply current	I_{DDP}			100	µA	

4.3 AC Characteristics

Digital inputs are driven to 2.4 V for a logical “1” and to 0.45 V for a logical “0”. Timing measurements are made at 2.0 V for a logical “1” and 0.8 V for a logical “0”. The AC-testing input/output waveforms are shown below.

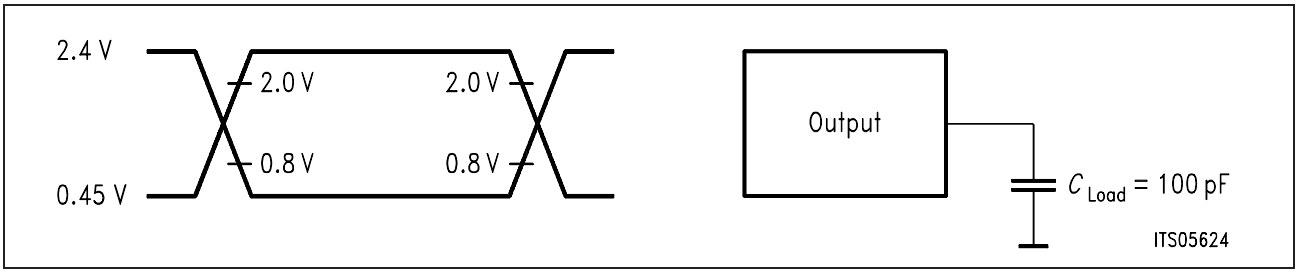


Figure 38
Input/Output Waveforms for AC-Tests

DTMF Detector

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency deviation accept		-1.5		1.5	%	
Frequency deviation reject		3.5		-3.5	%	
Acceptance level		-45		0	dB	rel. to max. PCM
Rejection level				-50	dB	rel. to max. PCM
Twist deviation accept		+/-2		+/-8	dB	programmable
Noise Tolerance				-12	dB	
Signal duration accept		40			ms	
Signal duration reject				23	ms	

CPT Detector

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency acceptance range		300		640	Hz	
Frequency rejection range		800		200	Hz	
Acceptance level		-45		0	dB	rel. to max. PCM
Rejection level				-50	dB	rel. to max. PCM
Noise Tolerance					dB	
Signal duration accept		50			ms	programmable
Signal duration reject				10	ms	

Caller ID Decoder

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency deviation accept		-2		2	%	
Acceptance level		-45		0	dB	rel. to max. PCM
Transmission rate		1188	1200	12121	baud	
Noise Tolerance				12	dB	

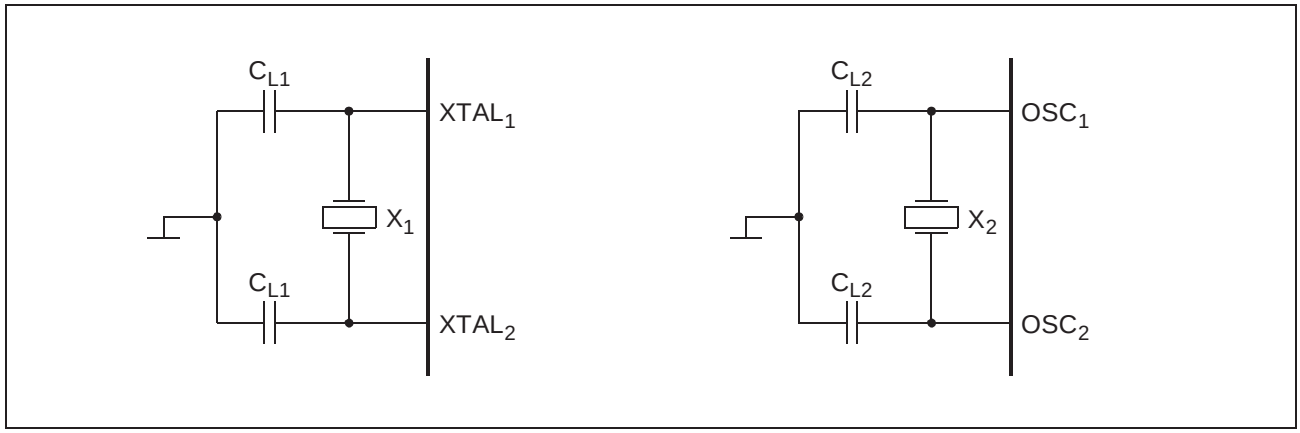


Figure 74
Oscillator Circuits

Recommended Values Oscillator Circuits	Value			Unit
	Min	Typ	Max	
Load CL_1			40	pF
Static capacitance X_1			5	pF
Motional capacitance X_1			17	fF
Resonance resistor X_1			60	Ω
Load CL_2			30	pF
Static Capacitance X_2		1.7		pF
Motional capacitance X_2		3.5		fF
Resonance resistor X_2		18	40	kΩ
Frequency deviation			100	ppm

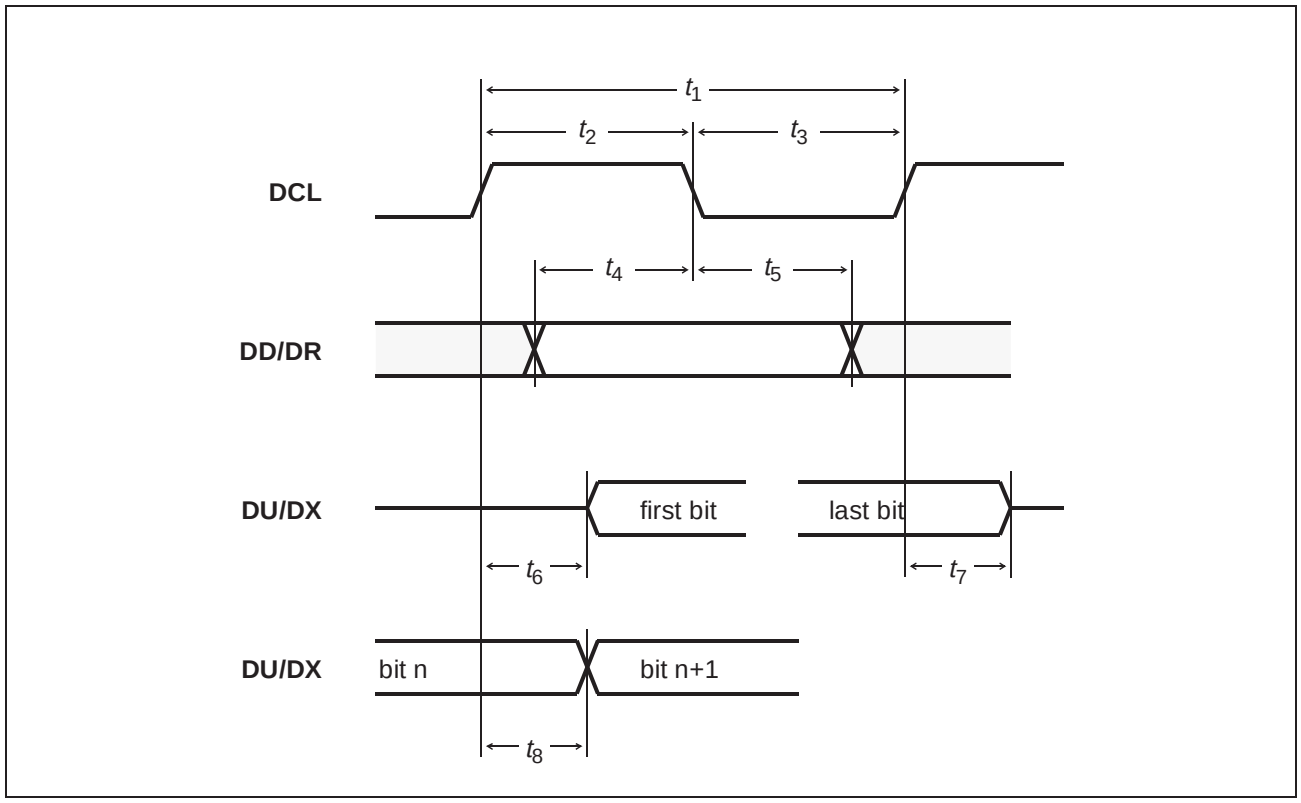


Figure 75
SSDI/IOM®-2 Interface - Bit Synchronization Timing

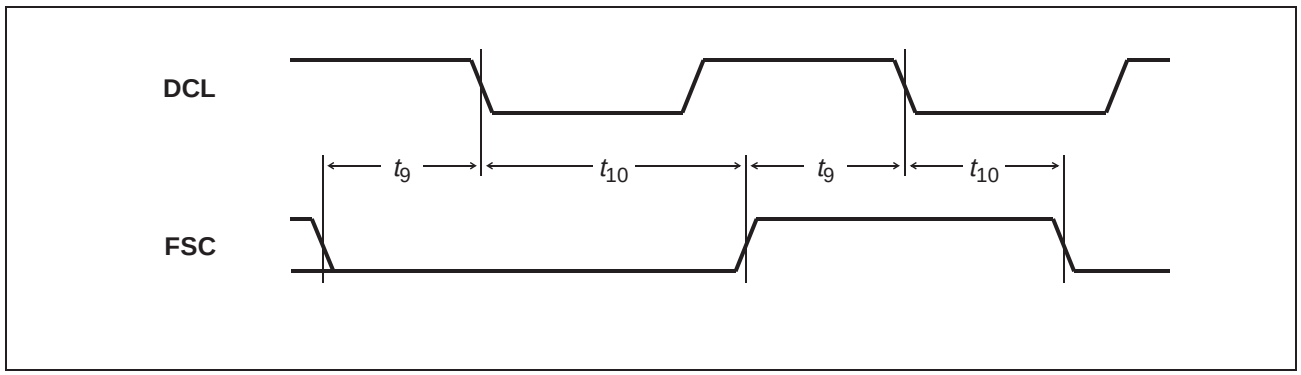


Figure 76
SSDI/IOM®-2 Interface - Frame Synchronization Timing

Parameter SSDI/IOM®-2 Interface	Symbol	Limit values		Unit
		Min	Max	
DCL period	t_1	90		ns
DCL high	t_2	35		ns
DCL low	t_3	35		ns

Parameter SSDI/IOM®-2 Interface	Symbol	Limit values		Unit
		Min	Max	
Input data setup	t_4	20		ns
Input data hold	t_5	20		ns
Output data from high impedance to active (FSC high or other than first timeslot)	t_6		30	ns
Output data from active to high impedance	t_7		30	ns
Output data delay from clock	t_8		30	ns
FSC setup	t_9	40		ns
FSC hold	t_{10}	40		ns
FSC jitter (deviation per frame)		-200	200	ns

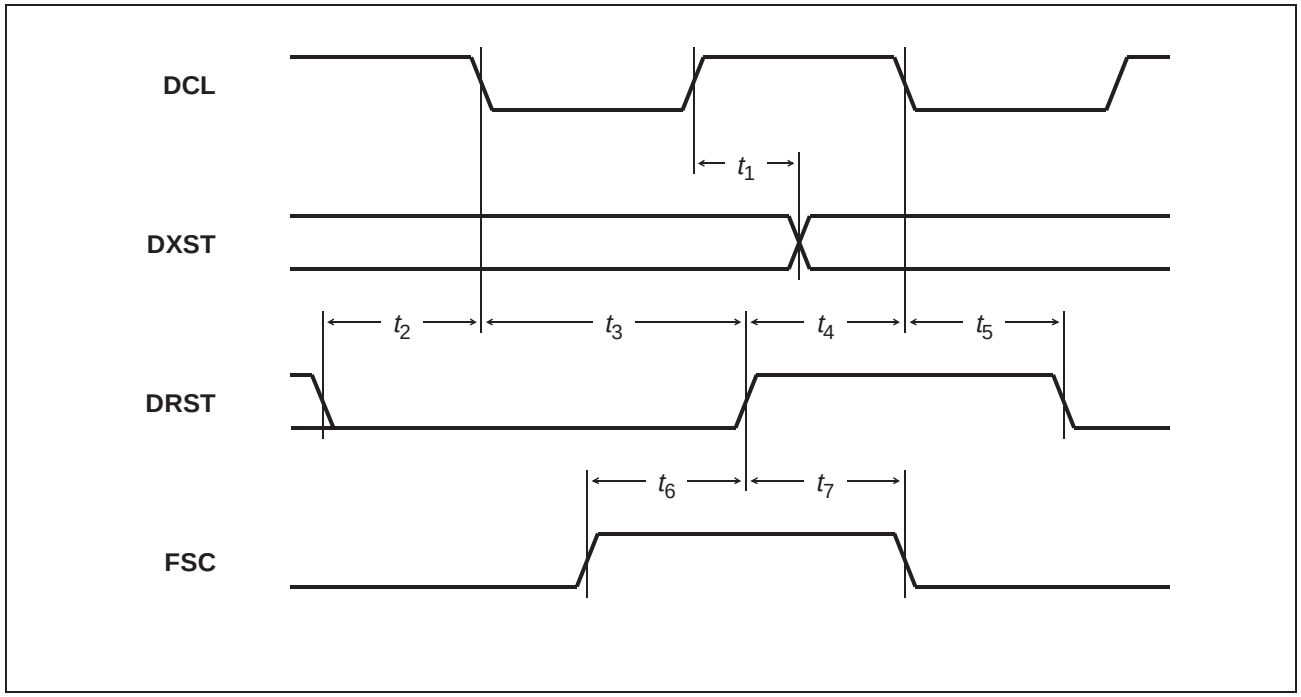


Figure 77
SSDI Interface - Strobe Timing

Parameter SSDI Interface	Symbol	Limit values		Unit
		Min	Max	
DXST delay	t_1		20	ns
DRST inactive setup	t_2	20		ns
DRST inactive hold	t_3	20		ns
DRST active setup	t_4	20		ns
DRST active hold	t_5	20		ns
FSC setup	t_6	8		DCL cycles
FSC hold	t_7	40		ns

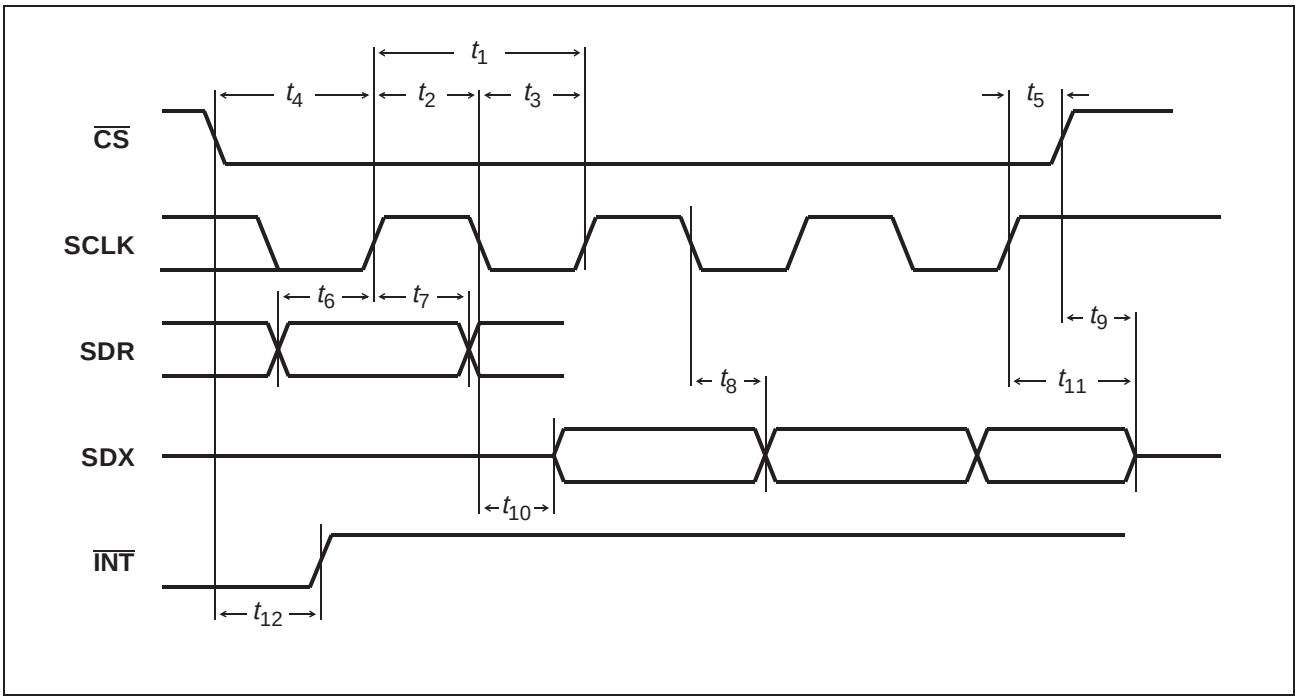


Figure 78
SCI Interface

Parameter SCI Interface	Symbol	Limit values		Unit
		Min	Max	
SCLK cycle time	t_1	500		ns
SCLK high time	t_2	100		ns
SCLK low time	t_3	100		ns
$\overline{CS}$ setup time	t_4	40		ns
$\overline{CS}$ hold time	t_5	10		ns
SDR setup time	t_6	40		ns
SDR hold time	t_7	40		ns
SDX data out delay	t_8		80	ns
$\overline{CS}$ high to SDX tristate	t_9		40	ns
SCLK to SDX active	t_{10}		80	ns
SCLK to SDX tristate	t_{11}		40	ns
$\overline{CS}$ to $\overline{INT}$ delay	t_{12}		80	ns

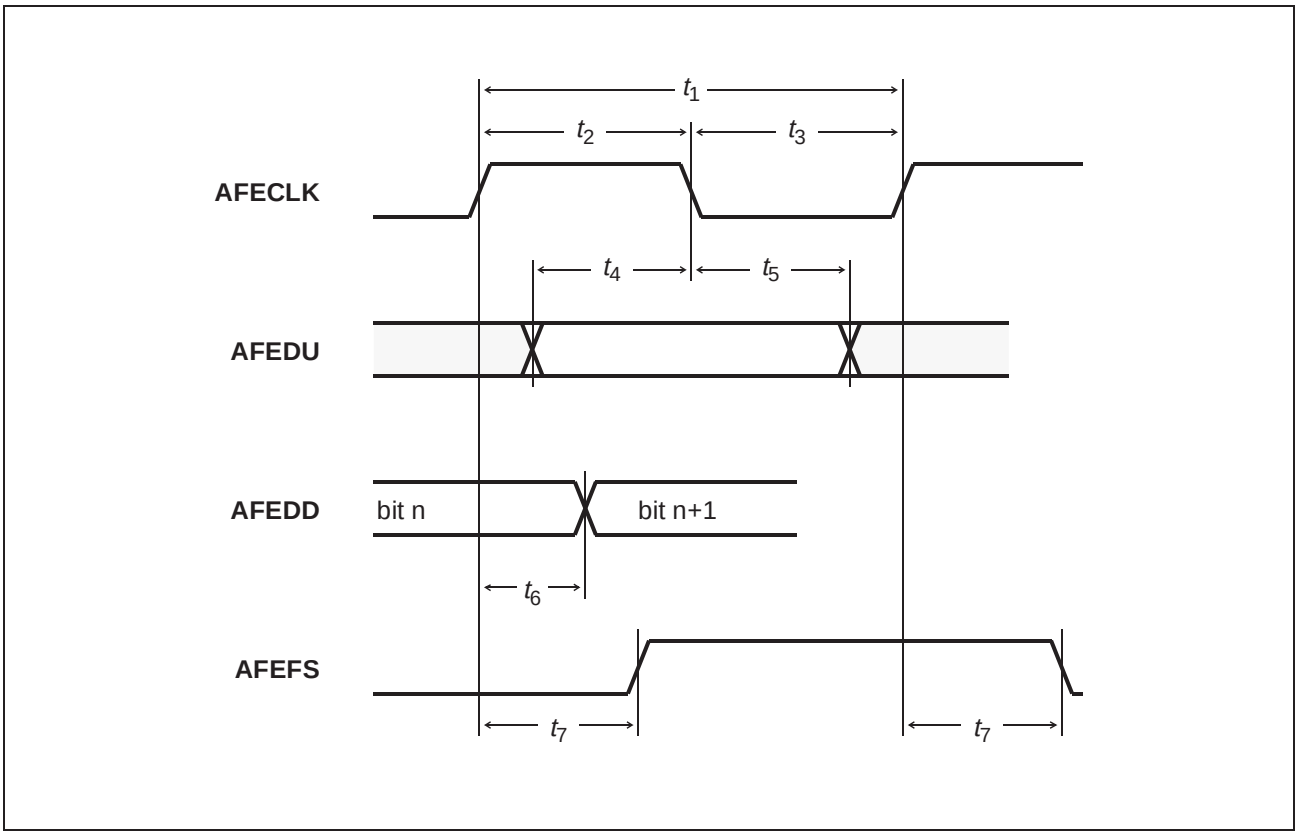


Figure 79
AFE Interface

Parameter AFE Interface	Symbol	Limit values		Unit
		Min	Max	
AFECLK period	t_1	125	165	ns
AFECLK high	t_2	2		$1/f_{XTAL}$
AFECLK low	t_3	2		$1/f_{XTAL}$
AFEDU setup	t_4	20		ns
AFEDU hold	t_5	20		ns
AFEDD output delay	t_6		30	ns
AFEFS output delay	t_7		30	ns

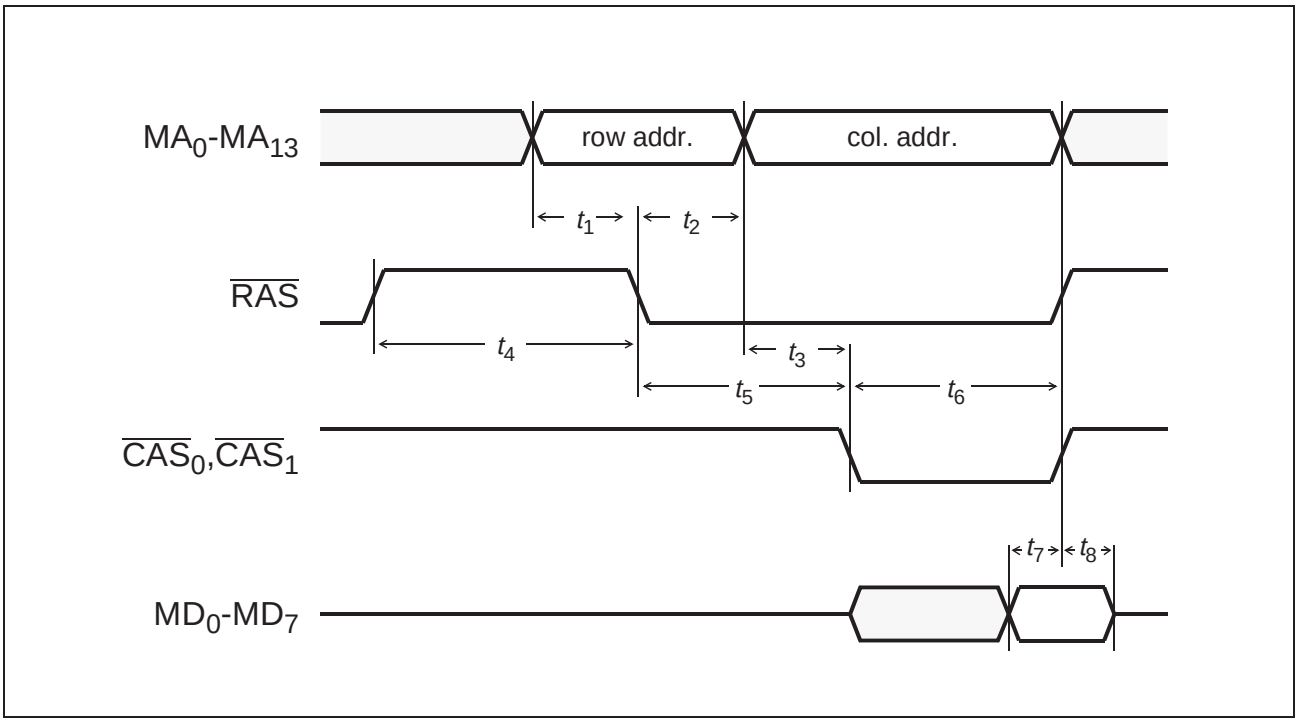


Figure 80
Memory Interface - DRAM Read Access

Parameter Memory Interface - DRAM Read Access	Symbol	Limit values		Unit
		Min	Max	
row address setup time	t_1	50		ns
row address hold time	t_2	50		ns
column address setup time	t_3	50		ns
$\overline{\text{RAS}}$ precharge time	t_4	110		ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay	t_5	110	2000	ns
$\overline{\text{CAS}}$ pulse width	t_6	110	2000	ns
Data input setup time	t_7	40		ns
Data input hold time	t_8	0		ns

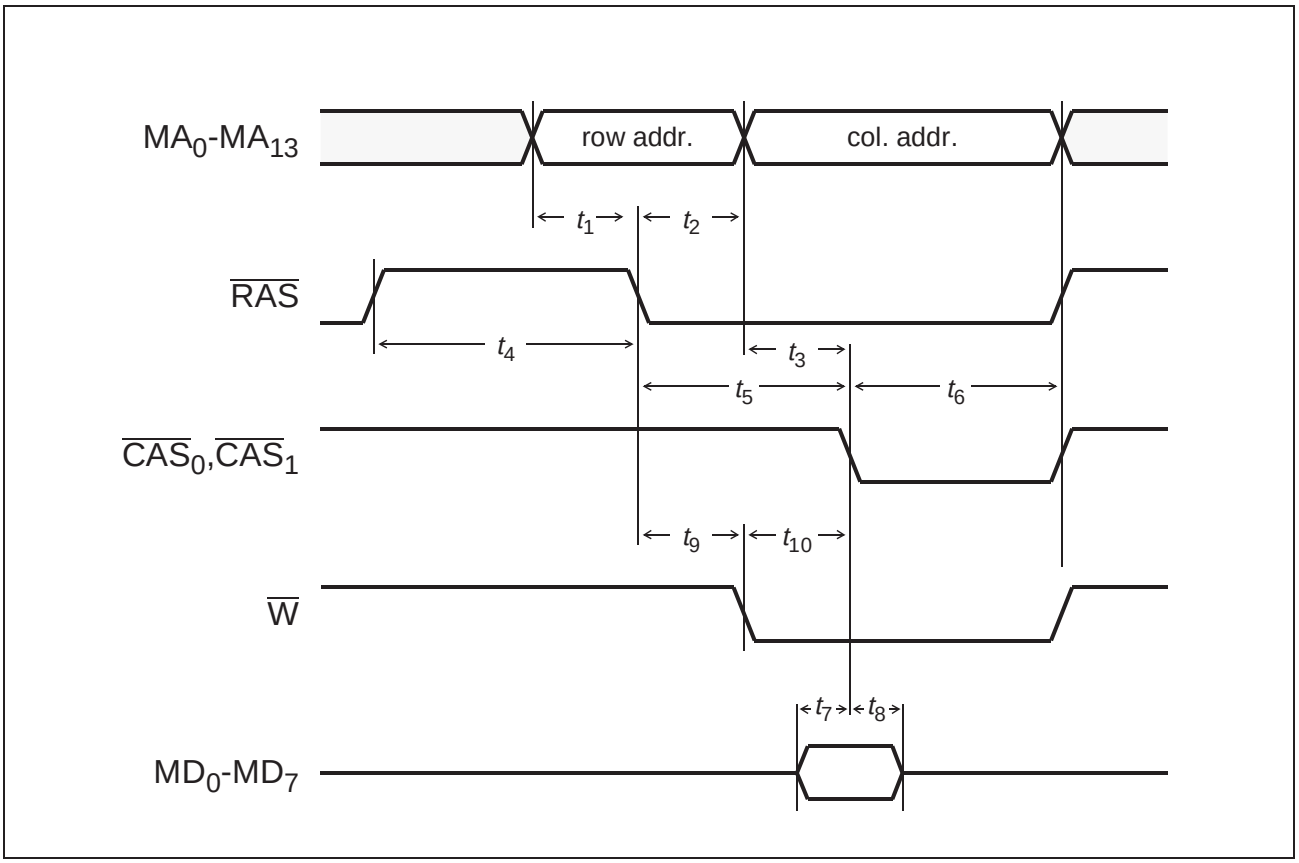


Figure 81
Memory Interface - DRAM Write Access

Parameter Memory Interface - DRAM Write Access	Symbol	Limit values		Unit
		Min	Max	
row address setup time	t_1	50		ns
row address hold time	t_2	50		ns
column address setup time	t_3	50		ns
$\overline{RAS}$ precharge time	t_4	110		ns
$\overline{RAS}$ to $\overline{CAS}$ delay	t_5	110	2000	ns
$\overline{CAS}$ pulse width	t_6	110	2000	ns
Data output setup time	t_7	100		ns
Data output hold time	t_8	50		ns
$\overline{RAS}$ to $\overline{W}$ delay	t_9	50		ns
$\overline{W}$ to $\overline{CAS}$ setup	t_{10}	50		ns

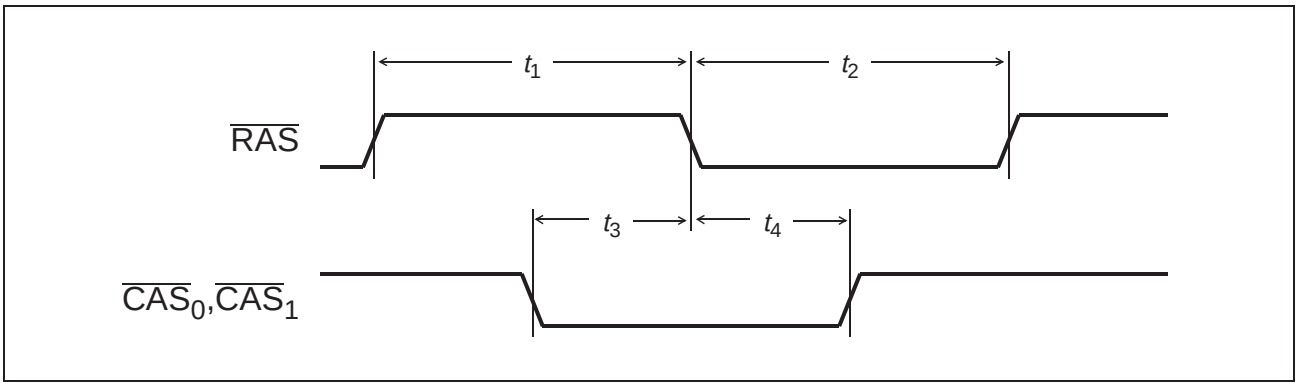


Figure 82
Memory Interface - DRAM Refresh Cycle

Parameter Memory Interface - DRAM Refresh Cycle	Symbol	Limit values		Unit
		Min	Max	
$\overline{RAS}$ precharge time	t_1	100		ns
$\overline{RAS}$ low time	t_2	200	5000	ns
$\overline{CAS}$ setup	t_3	100		ns
$\overline{CAS}$ hold	t_4	100		ns

Note: The frequency of the DRAM refresh cycle depends on the selected mode. In active mode or normal refresh mode (during power down) the minimal frequency is 64 kHz. In battery backup mode, the refresh frequency is 8 kHz.

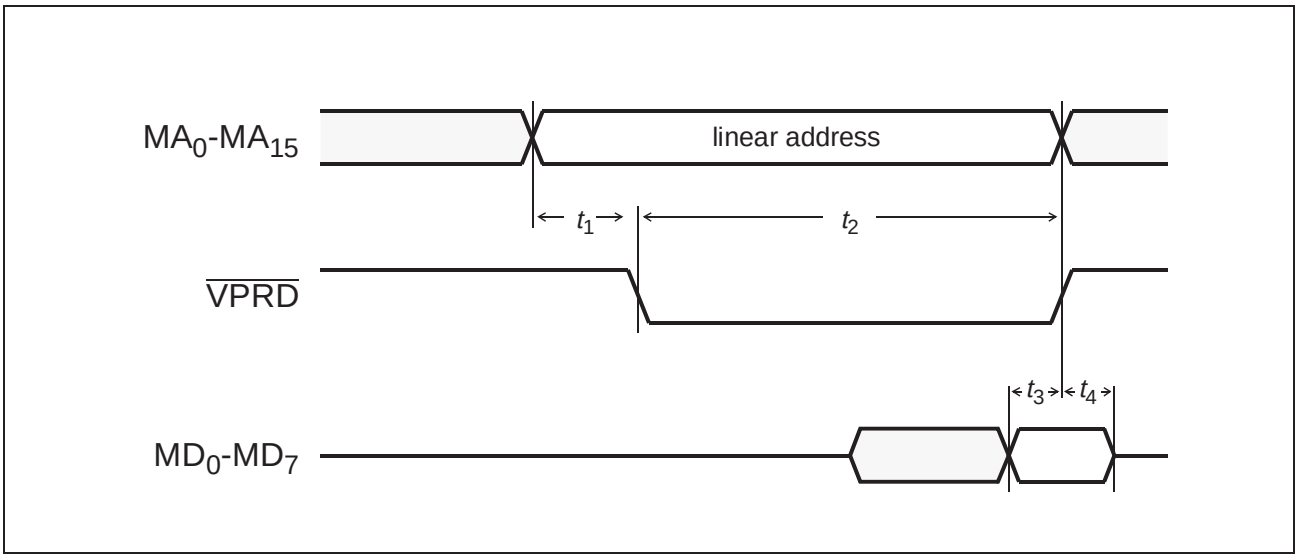


Figure 83
Memory Interface - EPROM Read

Parameter Memory Interface - EPROM Read	Symbol	Limit values		Unit
		Min	Max	
Address setup before $\overline{\text{VPRD}}$	t_1	110		ns
$\overline{\text{VPRD}}$ low time	t_2	500		ns
Data setup time	t_3	40		ns
Data hold time	t_4	0		ns

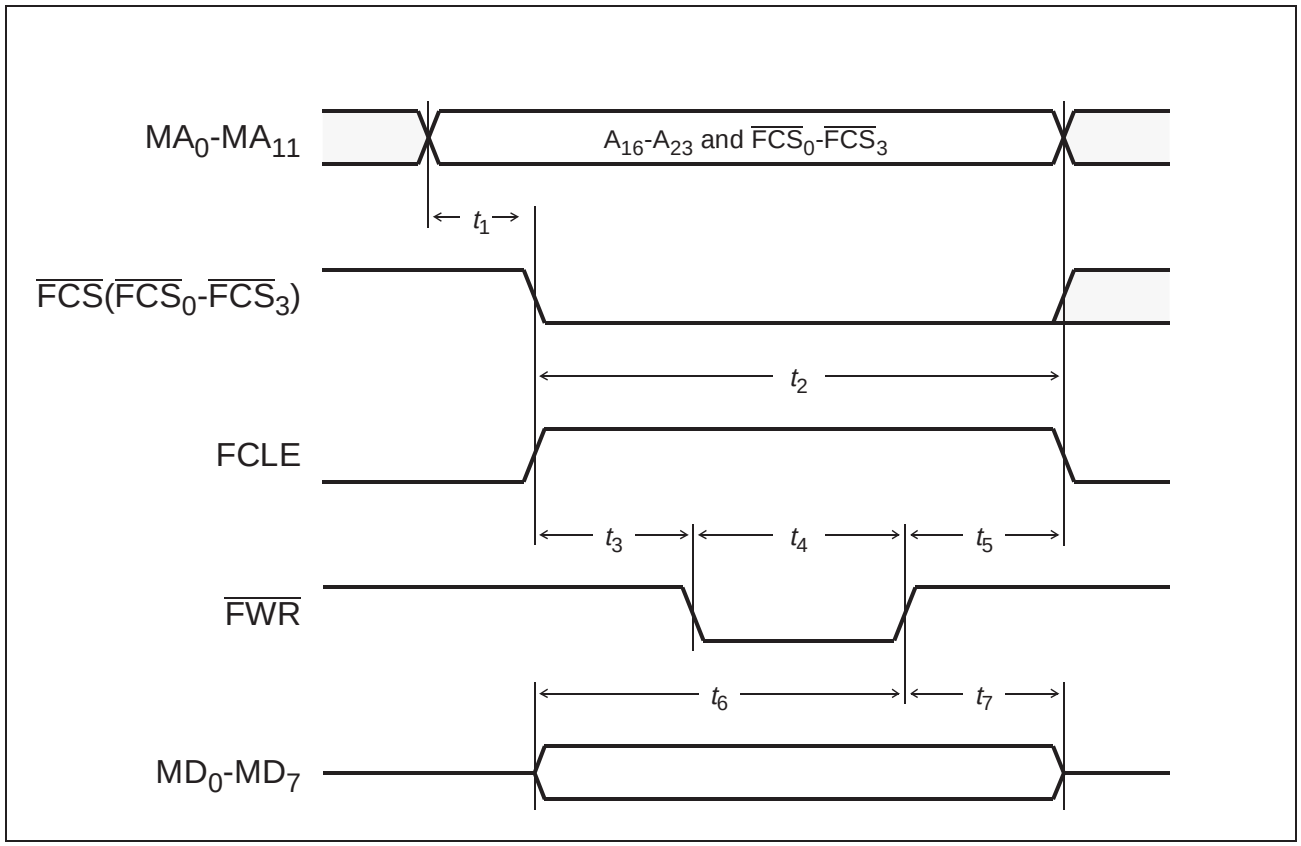


Figure 84
Memory Interface - Samsung Command Write

Parameter Memory Interface - Samsung Command Write	Symbol	Limit values		Unit
		Min	Max	
Address setup before $\overline{FCS}$, FCLE	t_1	100		ns
$\overline{FCS}$ low time, FCLE high time	t_2	400		ns
$\overline{FWR}$ hold after FCLE rising	t_3	100		ns
$\overline{FWR}$ low time	t_4	200		ns
$\overline{FWR}$ setup before FCLE falling	t_5	100		ns
Data setup time	t_6	200		ns
Data hold time	t_7	50		ns

Note: $\overline{FCS}$ stays low if other cycles follow for the same access.

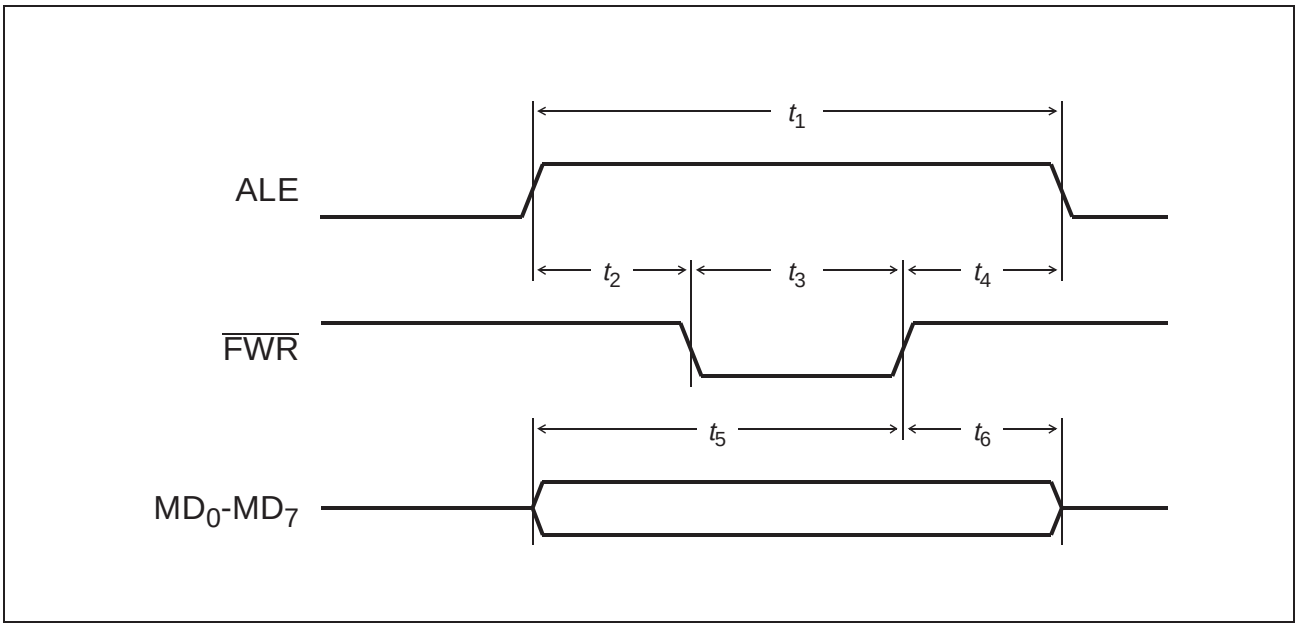


Figure 85
Memory Interface - Samsung Address Write

Parameter Memory Interface - Samsung Address Write	Symbol	Limit values		Unit
		Min	Max	
ALE high time	t_1	400		ns
$\overline{FWR}$ hold after ALE rising	t_2	100		ns
$\overline{FWR}$ low time	t_3	200		ns
$\overline{FWR}$ setup before ALE falling	t_4	100		ns
Data setup time	t_5	200		ns
Data hold time	t_6	50		ns

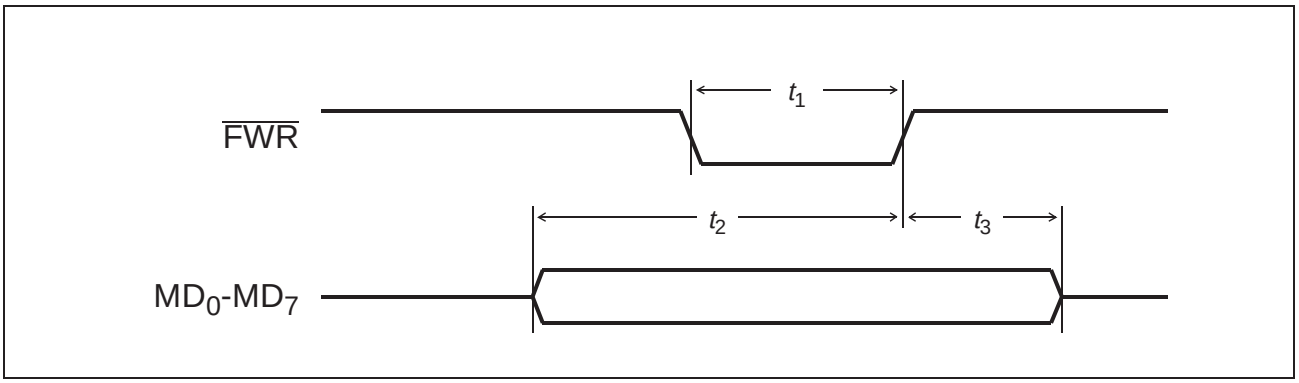


Figure 86
Memory Interface - Samsung Data Write

Parameter Memory Interface - Samsung Data Write	Symbol	Limit values		Unit
		Min	Max	
$\overline{FWR}$ low time	t_1	200		ns
Data setup time	t_2	200		ns
Data hold time	t_3	50		ns

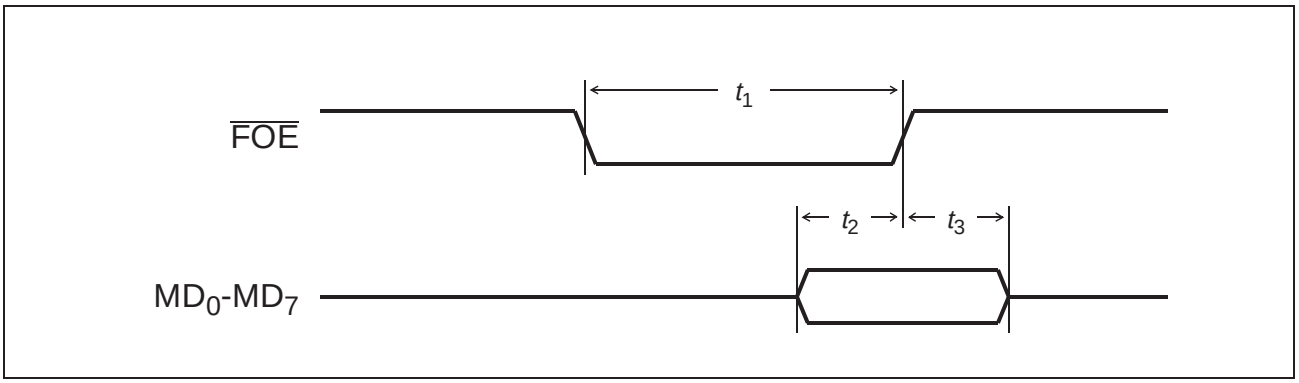


Figure 87
Memory Interface - Samsung Data Read

Parameter Memory Interface - Samsung Data Read	Symbol	Limit values		Unit
		Min	Max	
$\overline{\text{FOE}}$ low time	t_1	200		ns
Data setup time	t_2	40		ns
Data hold time	t_3	0		ns

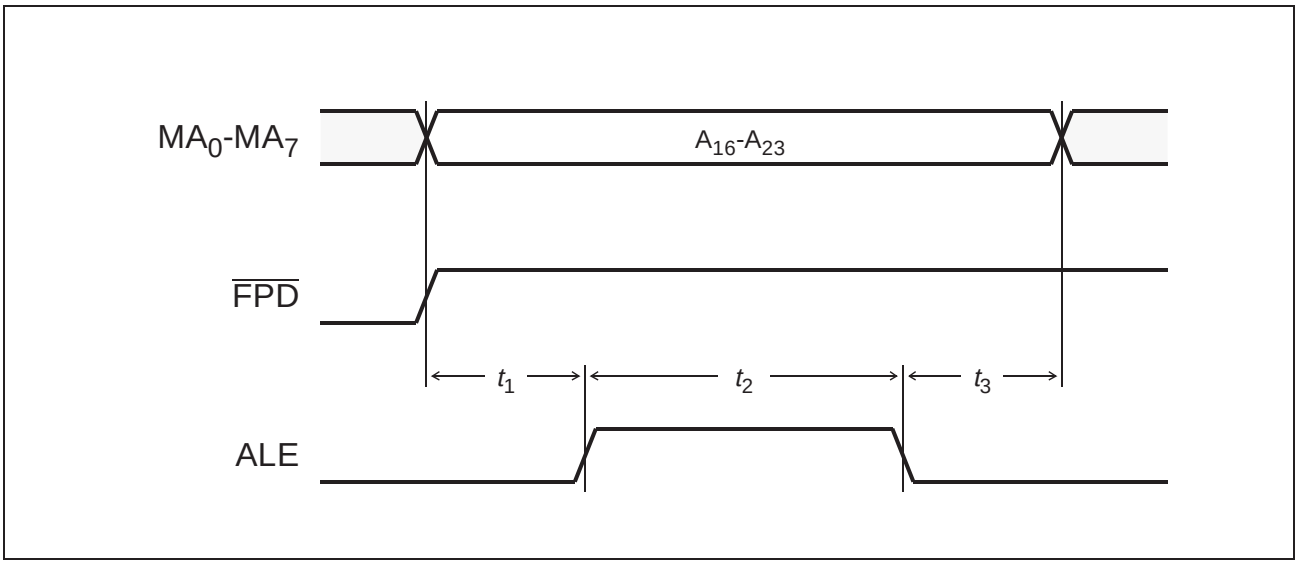


Figure 88
Memory Interface - Intel Address Latch Cycle

Parameter Memory Interface - Intel Address Latch Cycle	Symbol	Limit values		Unit
		Min	Max	
Address and $\overline{\text{FPD}}$ setup before ALE	t_1	100		ns
ALE high time	t_2	200		ns
Address hold time after ALE	t_3	100		ns

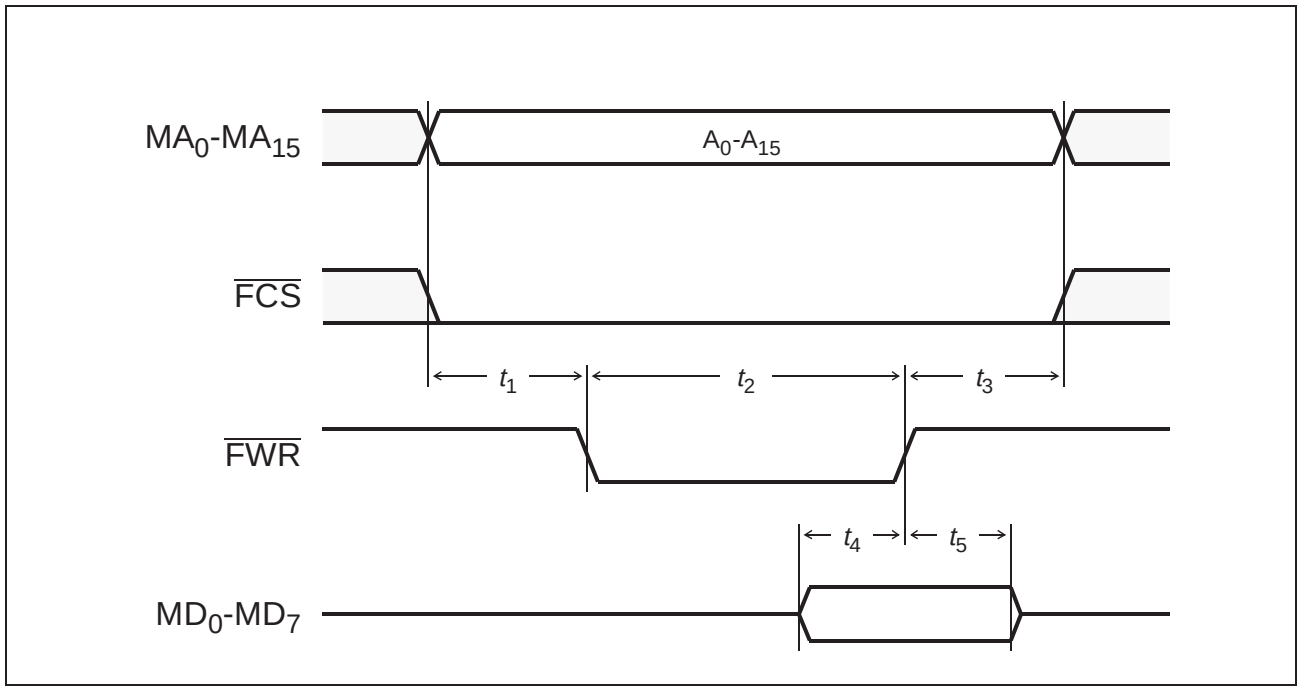


Figure 89
Memory Interface - Intel Write Cycle

Parameter Memory Interface - Intel Write Cycle	Symbol	Limit values		Unit
		Min	Max	
Address and $\overline{FCS}$ setup before $\overline{FWR}$	t_1	100		ns
$\overline{FWR}$ low time	t_2	200		ns
Address and $\overline{FCS}$ hold time after $\overline{FWR}$	t_3	100		ns
Data out setup before $\overline{FWR}$ rising	t_4	100		ns
Data out hold after $\overline{FWR}$ rising	t_5	50		ns

Note: $\overline{FCS}$ stays low if other cycles follow for the same access

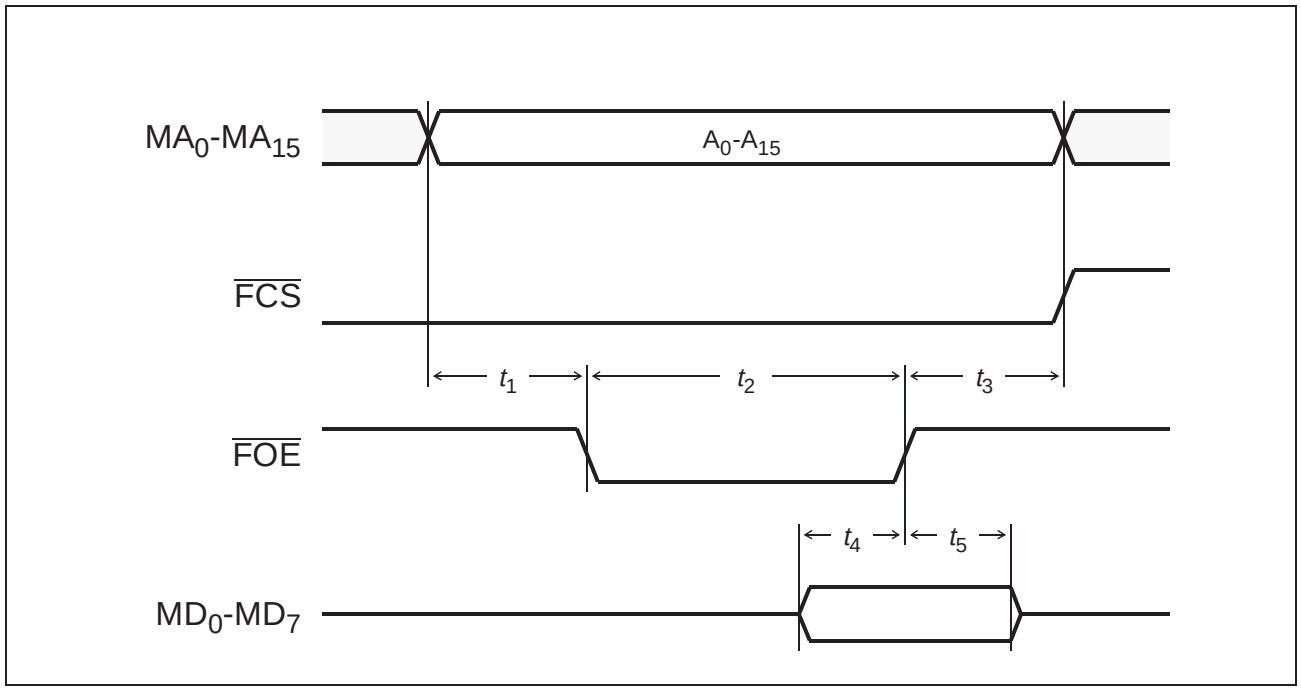


Figure 90
Memory Interface - Intel Read Cycle

Parameter Memory Interface - Intel Read Cycle	Symbol	Limit values		Unit
		Min	Max	
Address and $\overline{FCS}$ setup before $\overline{FOE}$	t_1	100		ns
$\overline{FOE}$ low time	t_2	200		ns
Address and $\overline{FCS}$ hold time after $\overline{FOE}$	t_3	100		ns
Data in setup before $\overline{FOE}$ rising	t_4	40		ns
Data in hold after $\overline{FOE}$ rising	t_5	0		ns

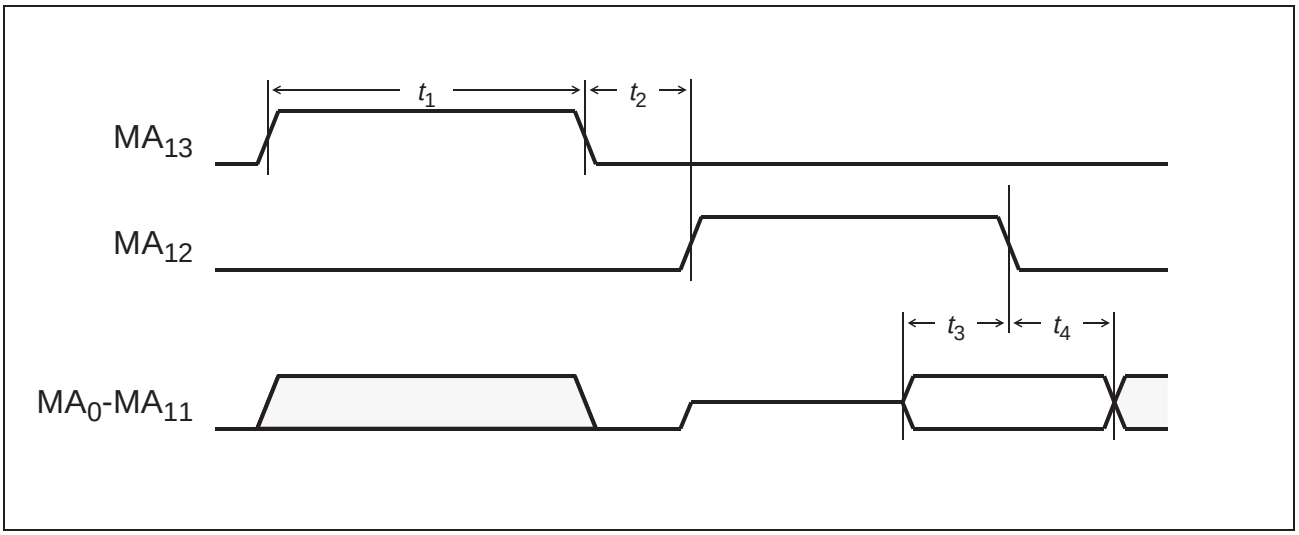


Figure 91
Auxiliary Port Interface - Dynamic Mode

Parameter Auxiliary Port Interface - Dynamic Mode	Symbol	Limit values			Unit
		Min	Typ	Max	
Active time (MA_0-MA_{15})	t_1		2		ms
Gap time (MA_0-MA_{15})	t_2		125		µs
Data setup time	t_3	50			ns
Data hold time	t_4	0			ns

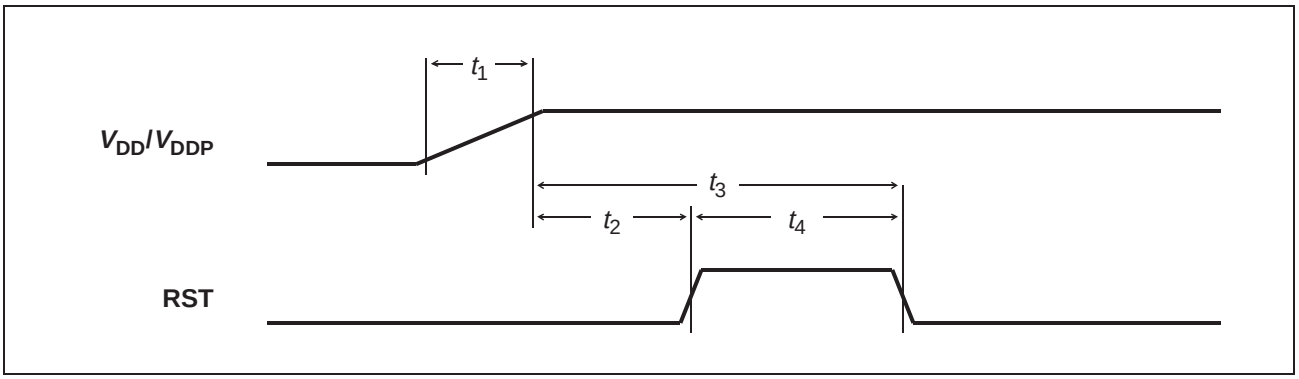
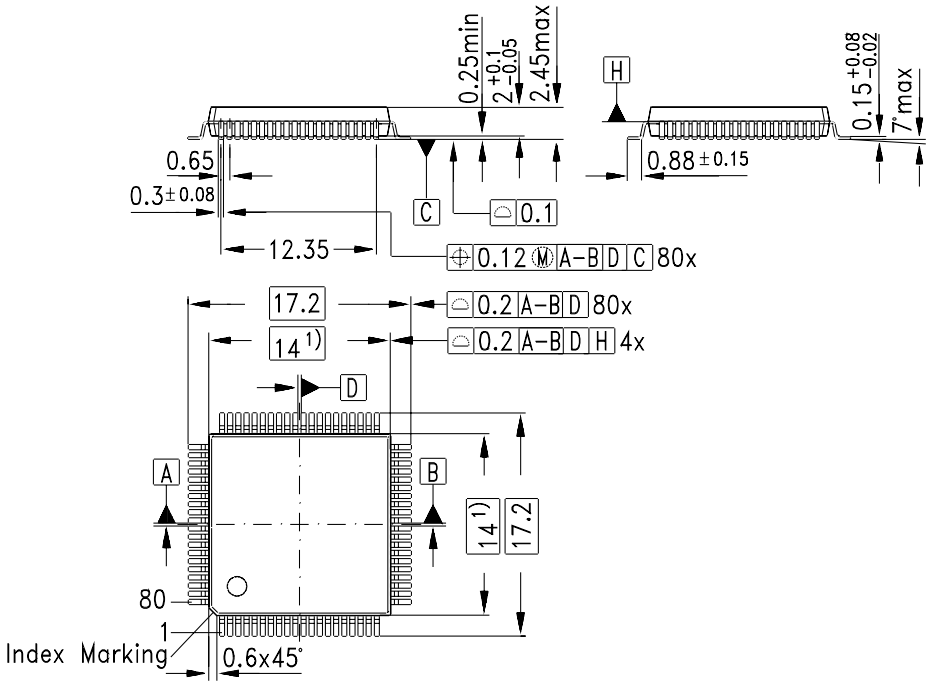


Figure 92
Reset Timing

Parameter Reset Timing	Symbol	Limit values		Unit
		Min	Max	
$V_{DD}/V_{DDP}/V_{DDA}$ rise time 5%-95%	t_1		20	ms
Supply voltages stable to RST high	t_2	0		ns
Supply voltages stable to RST low	t_3	0.1		ms
RST high time	t_4	1000		ns

5 Package Outlines

Plastic Package, P-MQFP-80 (SMD)
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusions of 0.25 max per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm