SIEMENS

ICs for Communications

Digital Answering Machine with Full Duplex Speakerphone SAM EC

PSB 4860 Version 3.1

Product Overview 09.97

DS 1

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Edition 09.97

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1 Overview

Combined with an analog frontend (PSB 4851) the PSB 4860 provides a solution for embedded or stand alone answering machine applications. Together with a standard microcontroller for analog telephones these two chips form the core of a featurephone with full duplex speakerphone and answering machine capabilities.

The chip features two compression modes (high quality and long play), message playback at variable rates, full duplex speakerphone operation, a caller ID decoder, DTMF recognition and generation and call progress tone detection.

Messages and user data can be stored in ARAM/DRAM or flash memory which can be directly connected to the PSB 4860. The PSB 4860 also supports a voice prompt EPROM for fixed announcements.

The PSB 4860 provides an IOM®-2 compatible interface with up to three channels for speech data.

Alternatively to the IOM®-2 compatible interface the PSB 4860 supports a simple serial data interface with separate strobe signals for each direction (linear PCM data, one channel).

A separate interface is used for a glueless connection to the PSB 4851.

The chip is programmed by a simple four wire serial control interface and can inform the microcontroller of new events by an interrupt signal. For data retention the PSB 4860 supports a power down mode where only the real time clock and the memory refresh (in case of ARAM/DRAM) are operational.

The PSB 4860 supports interface pins to +5 V levels.

SIEMENS

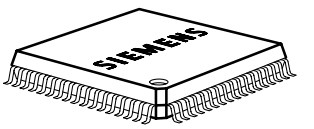
Digital Answering Machine with Full Duplex Speakerphone
SAM EC

PSB 4860

Version 3.1

CMOS

1.1 Features



P-MQFP-80

General Features

- Selectable compression rate (3.3 kbit/s, 10.3 kbit/s)
- Variable playback speed
- Support for ARAM or Flash Memory
- Optional voice prompt EPROM
- Full duplex speakerphone
- DTMF generation and detection
- Call progress tone detection
- Caller ID recognition
- Direct memory access
- Real time clock for automatic timestamp
- Equalizer
- Auxiliary parallel port
- Ultra low power refresh mode
- SSDI/IOM®-2 compatible interface
- Automatic Gain Control
- Backward compatible with PSB 4860 V2.1 (hardware and software)

New in Version 3.1[1)]

- *Third data channel (IOM®-2 compatible interface)*
- *Up to four serial flash devices supported (Toshiba, Atmel)*
- *Support for x1 ARAM/DRAM*
- *New command for easier programming*
- *Auxiliary parallel port available in all flash configurations (even multiple devices)*
- *Programmable CPT filter*
- *Enhanced memory management*

1) New or improved items are written in italics throughout this document

Type	Ordering Code	Package
PSB 4860		P-MQFP-80

1.2 Pin Configuration

(top view)

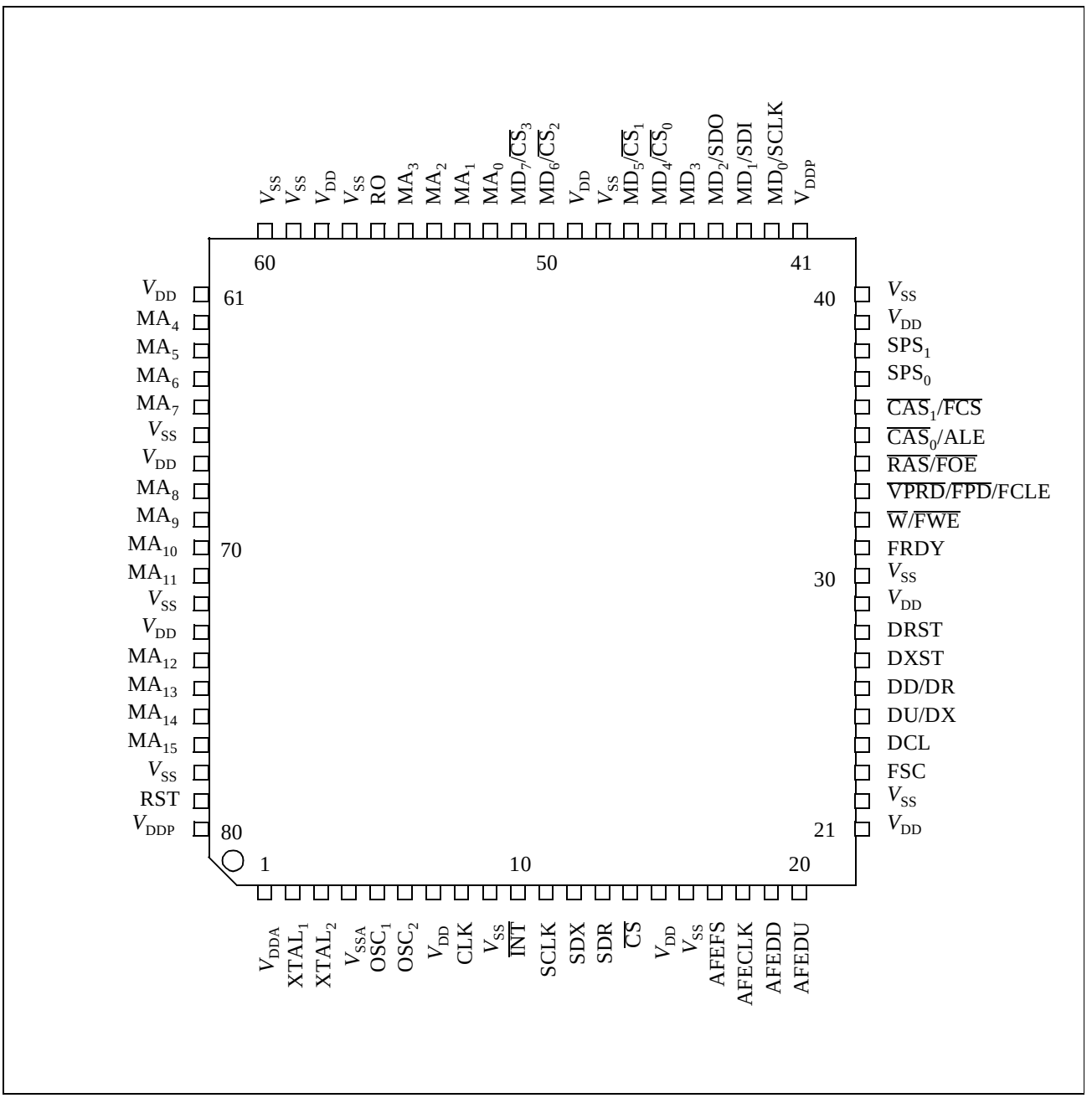


Figure 1 Pin Configuration of PSB 4860

1.3 Pin Definitions and Functions

Pin No. P-MQFP-80	Symbol	Dir.	Reset	Function
41, 80	V_{DDP}	-	-	**Power supply (5V ±10 %)** Power supply for the interface.
7, 15, 21, 29, 39, 49, 58, 61, 67, 73	V_{DD}	-	-	**Power supply (3.0 V - 3.6 V**) Power supply for logic.
1	V_{DDA}	-	-	**Power supply (3.0 V - 3.6 V)** Power supply for clock generator.
4	V_{SSA}	-	-	**Power supply (0 V)** Ground for clock generator.
9, 16, 22, 30, 40, 48, 57, 59, 60, 78, 66, 72	V_{SS}	-	-	**Power supply (0 V)** Ground for logic and interface.
17	AFEFS	O	L	**Analog Frontend Frame Sync:** 8 kHz frame synchronization signal for the analog front end.
18	AFECLK	O	L	**Analog Frontend Clock:** Clock signal for the analog front end.
19	AFEDD	O	L	**Analog Frontend Data Downstream:** Data output to the analog frontend.
20	AFEDU	I	-	**Analog Frontend Data Upstream:** Data input from the analog frontend.
23	FSC	I	-	**Data Frame Synchronization:** 8 kHz frame synchronization signal (IOM®-2 and SSDI mode).
24	DCL	I	-	**Data Clock:** Data Clock of the serial data interface.
26	DD/DR	**I**/OD I	-	**IOM®-2 Compatible Mode:** Receive data from IOM®-2 controlling device. **SSDI Mode:** Receive data.

25	DU/DX	**I**/OD O/ OD	-	**IOM®-2 Compatible Mode:** Transmit data to IOM®-2 controlling device. **SSDI Mode:** Transmit data.
27	DXST	O	L	**DX Strobe:** Strobe for DX in SSDI interface mode.
28	DRST	I	-	**DR Strobe:** Strobe for DR in SSDI interface mode.
79	RST	I	-	**Reset:** Active high reset signal.
14	$\overline{CS}$	I	-	**Chip Select:** Select signal of the serial control interface.
11	SCLK	I	-	**Serial Clock:** Clock signal of the serial control interface.
13	SDR	I	-	**Serial Data Receive:** Data input of the serial control interface.
12	SDX	O/ **OD**	H	**Serial Data Transmit:** Data Output of the serial control interface.
10	$\overline{INT}$	O/ **OD**	H	**Interrupt** New status available.
35 36	$\overline{CAS}_0$/ALE $\overline{CAS}_1$/FCS	O O	H[1)]	**ARAM, DRAM:** Column address strobes. **Samsung Flash Memory:** Address Latch Enable and chip select signal.
34	$\overline{RAS}$/$\overline{FOE}$	O	H[1)]	**ARAM, DRAM:** Row address strobe for both memory banks. **Samsung Flash Memory:** Output enable signal for Flash Memory.
33	$\overline{VPRD}$/ FCLE	O	H[1)]	**ARAM, DRAM:** Read signal for voice prompt EPROM. **Samsung Flash Memory:** Command latch enable for Flash Memory.
32	$\overline{W}$/$\overline{FWE}$	O	H[1)]	**ARAM, DRAM:** Write signal for all memory banks. **Samsung Flash Memory:** Write signal for Flash Memory.

31	FRDY	I	-	**Flash Memory Ready** Input for Ready/Busy signal of Flash Memory
5 6	OSC_1 OSC_2	I O	- Z	**Auxiliary Oscillator:** Oscillator loop for 32.768 kHz crystal.
8	CLK	I	-	**Alternative AFECLK Source** 13,824 MHz
2 3	$XTAL_1$ $XTAL_2$	I O	- Z	**Oscillator:** Oscillator loop for main crystal.
42 *43* *44* *45* *46* *47* *50* *51*	*MD_0/SCLK* *MD_1/SDI* *MD_2/SDO* *MD_3* *$MD_4/\overline{CS}_0$* *$MD_5/\overline{CS}_1$* *$MD_6/\overline{CS}_2$* *$MD_7/\overline{CS}_3$*	***I**/O* ***I**/O* ***I**/O* ***I**/O* ***I**/O* ***I**/O* ***I**/O* ***I**/O*	- - - - - - - -	***ARAM/DRAM or Samsung Flash:*** *Memory data bus.* ***Serial Flash Memory (Toshiba, Atmel):*** *Serial interface signals and predecoded chip select lines.*
37 38	SPS_0 SPS_1	O O	L L	**Multipurpose Outputs:** General purpose, speakerphone, voice prompt EPROM address lines or status
52 53 54 55 62 63 64 65 68 69 70 71 74 75 76 77	MA_0 MA_1 MA_2 MA_3 MA_4 MA_5 MA_6 MA_7 MA_8 MA_9 MA_{10} MA_{11} MA_{12} MA_{13} MA_{14} MA_{15}	I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O**	L[2)] L L L L L L L L L L L L L L L	**Memory Address 0-15:** Multiplexed address outputs for ARAM/DRAM. Non-multiplexed address outputs for voice prompt EPROM. **Auxiliary Parallel Port:** General purpose I/O.
56	RO	O	-	**Reserved Output** Must be left open.

[1)] These lines are driven high with 70 µA during reset.

[2)] These lines are driven low with 125 µA until the mode (address lines or auxiliary port) is defined.

1.4 Logic Symbol

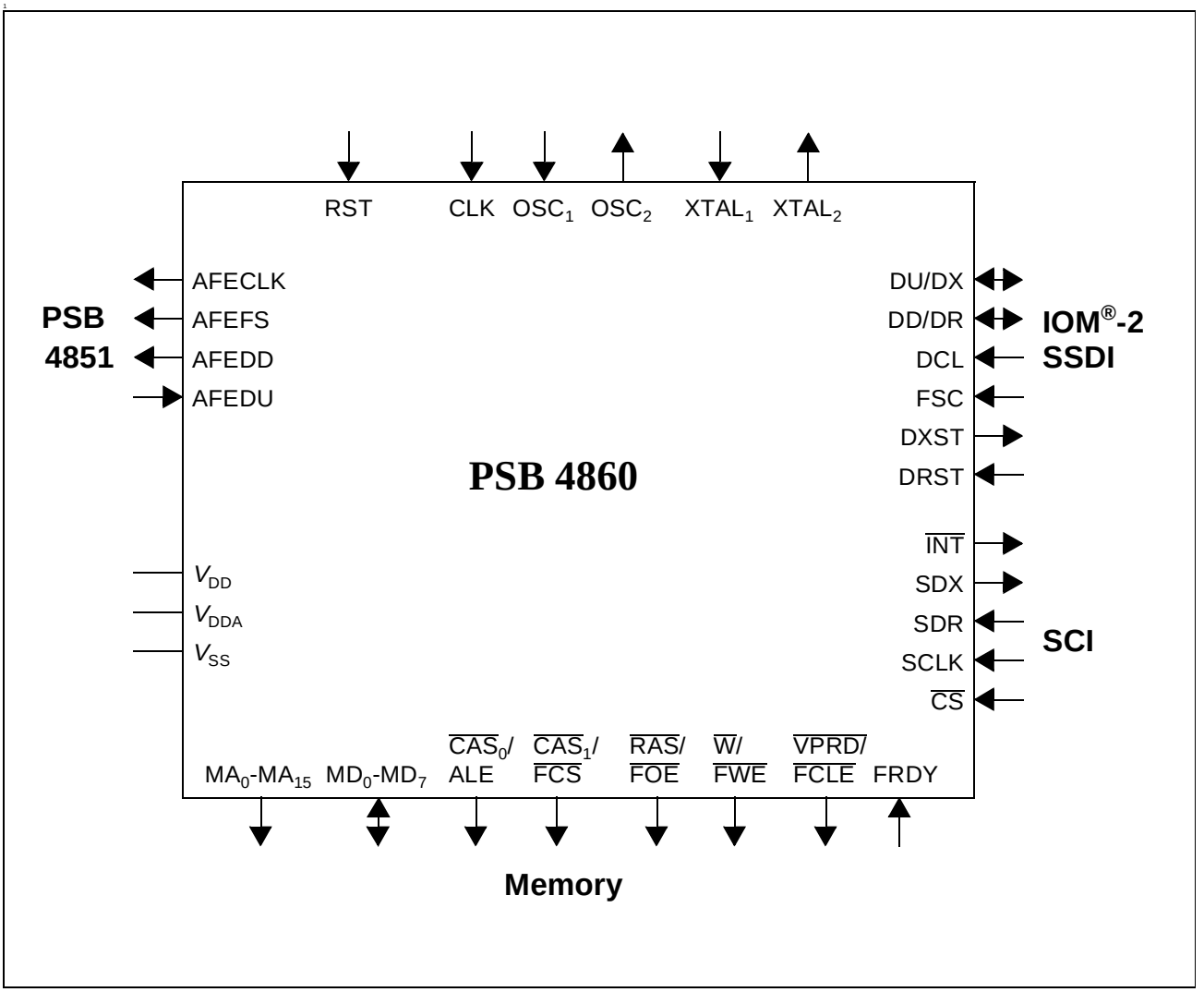


Figure 2 Logic Symbol of PSB 4860

1.5 Functional Block Diagram

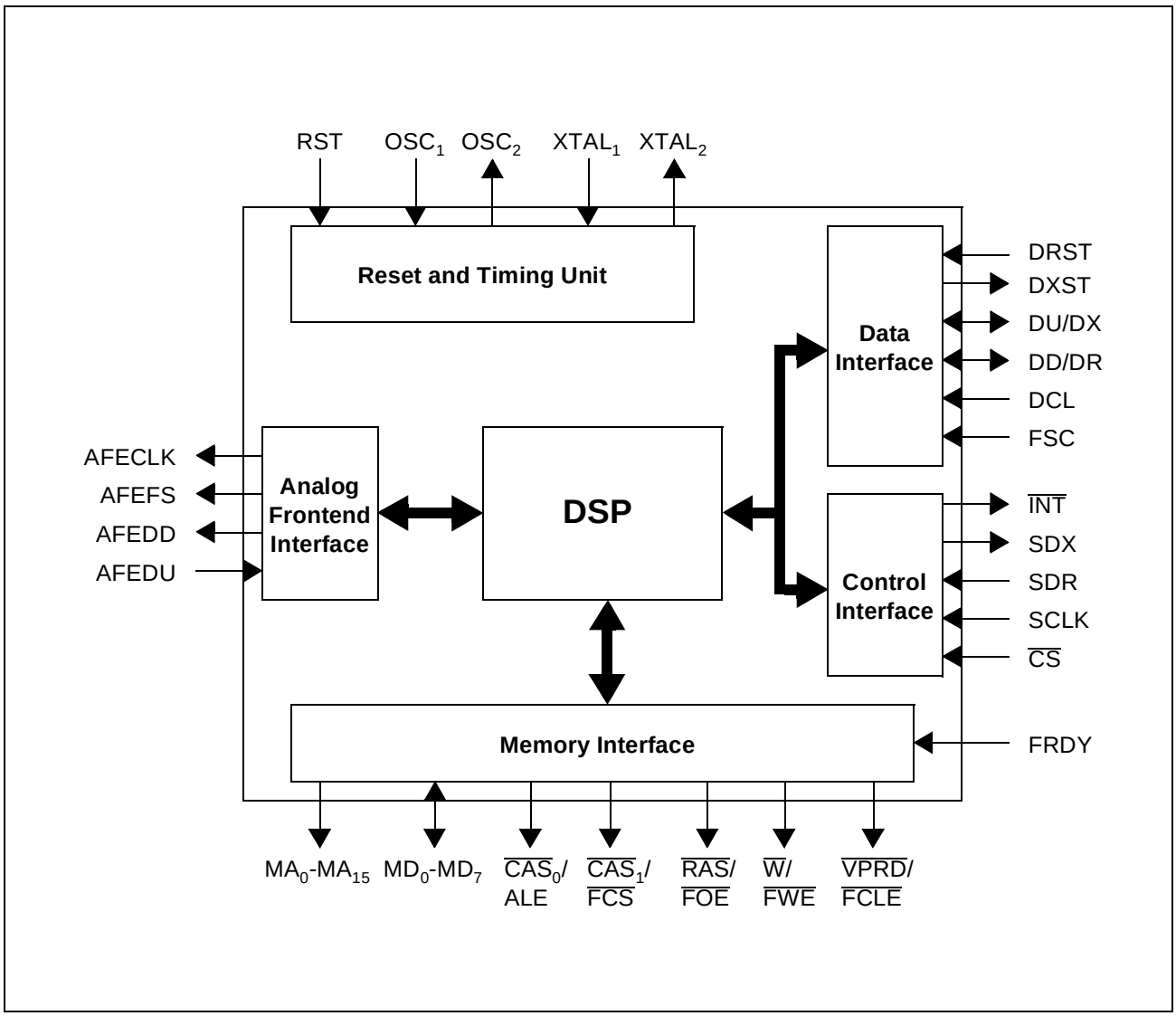


Figure 3 Block Diagram of PSB 4860

1.6 System Integration

The PSB 4860 combined with an analog frontend (PSB 4851) can be used in a variety of applications. This combination offers outstanding features like full duplex speakerphone and emergency operation. Some applications are given in the following sections.

1.6.1 Analog Featurephone with Digital Answering Machine

Figure **4** shows an example of an analog telephone system. The telephone can operate during power failure by line powering. In this case only the handset and ringer circuit are active. All other parts of the chipset are shut down leaving enough power for the external microcontroller to perform basic tasks like keyboard monitoring.

For answering machine operation the voice data is stored in ARAM or flash memory devices. In addition, voice prompts can be played back from an optional voice prompt EPROM. If flash memory is used the functionality of the voice prompt EPROM can be realized by the flash memory devices. The microcontroller can use the memory attached to the PSB 4860/PSB 4851 to store and retrieve binary data.

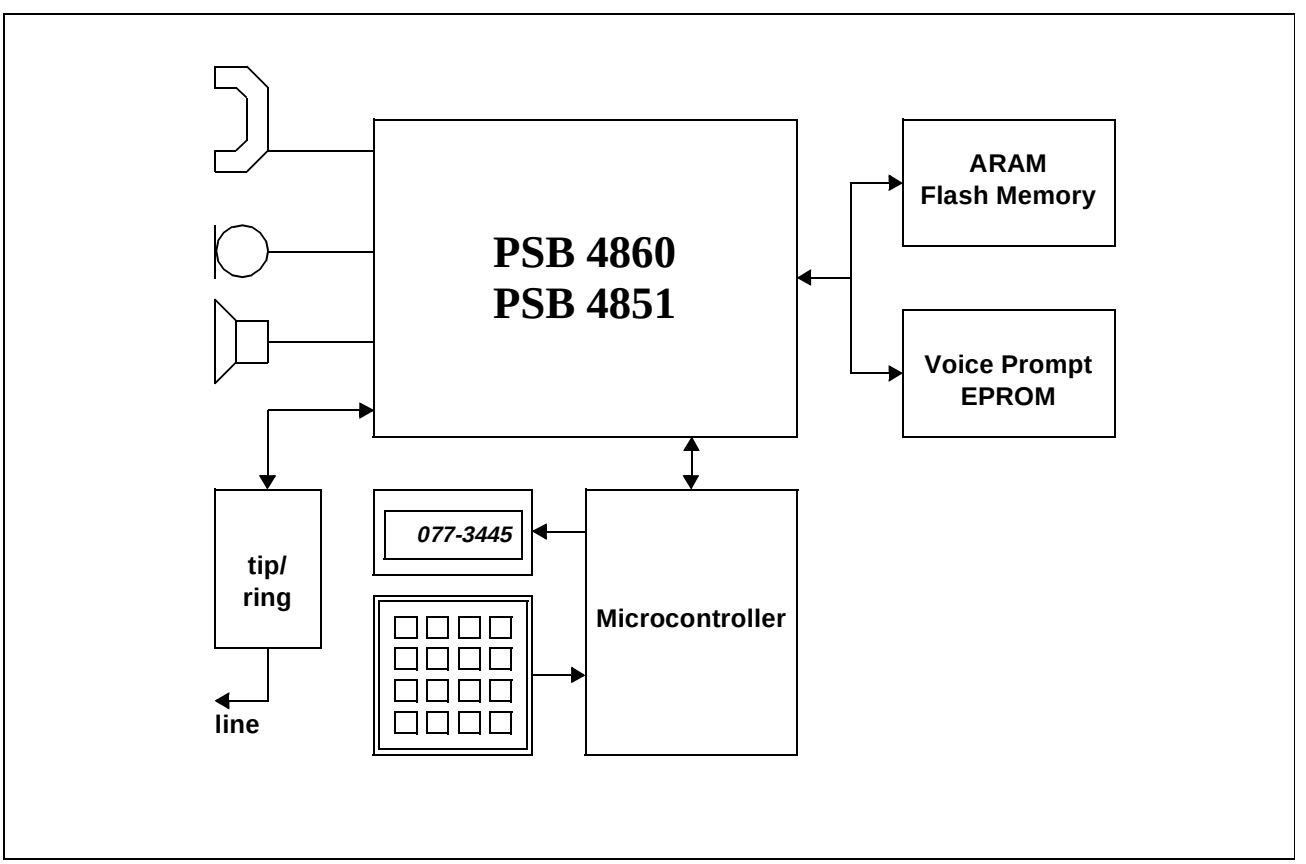


Figure 4 Analog Full Duplex Speakerphone with Digital Answering Machine

1.6.2 Featurephone with Digital Answering Machine for ISDN Terminal

Figure **5** shows an ISDN featurephone that takes full advantage of two simultaneous connections. In this application one channel of the PSB 4851 interfaces to the handset and speakerphone while the other provides an interface for an external analog device (e.g. FAX machine).

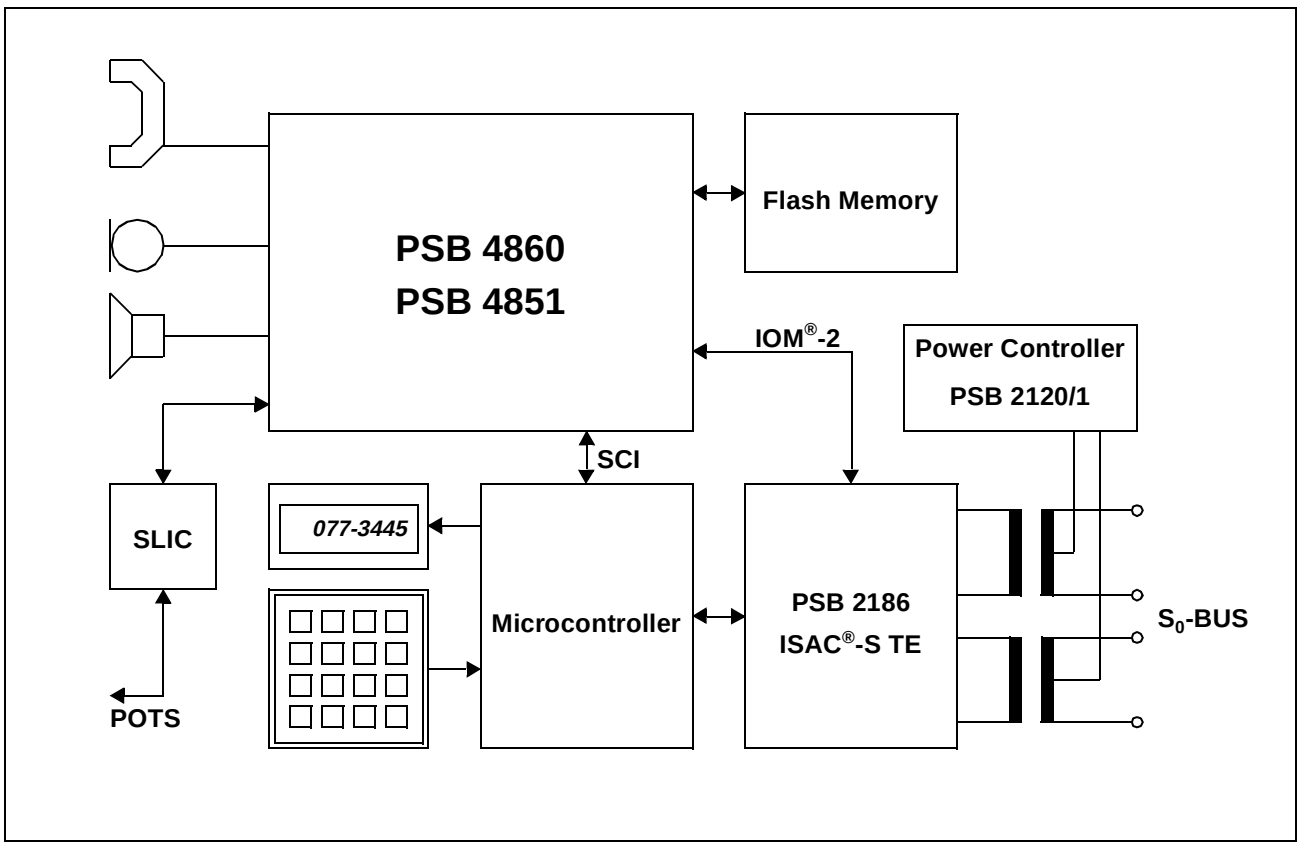


Figure 5 Featurephone with Answering Machine for ISDN Terminal

In addition, the two channels of the PSB 4851 can be used for holding two connections simultaneously. One connection can be switched to the handset and the other to the speakerphone box. Local three party conferences are also possible.

1.6.3 DECT Basestation with Integrated Digital Answering Machine

Figure **6** shows a DECT basestation based on the PSB 4860/PSB 4851 chipset. In this application it is possible to service both an external call and an internal call at the same time. For programming the serial control interface (SCI) is used while voice data is transferred via the strobed serial data interface (SSDI).

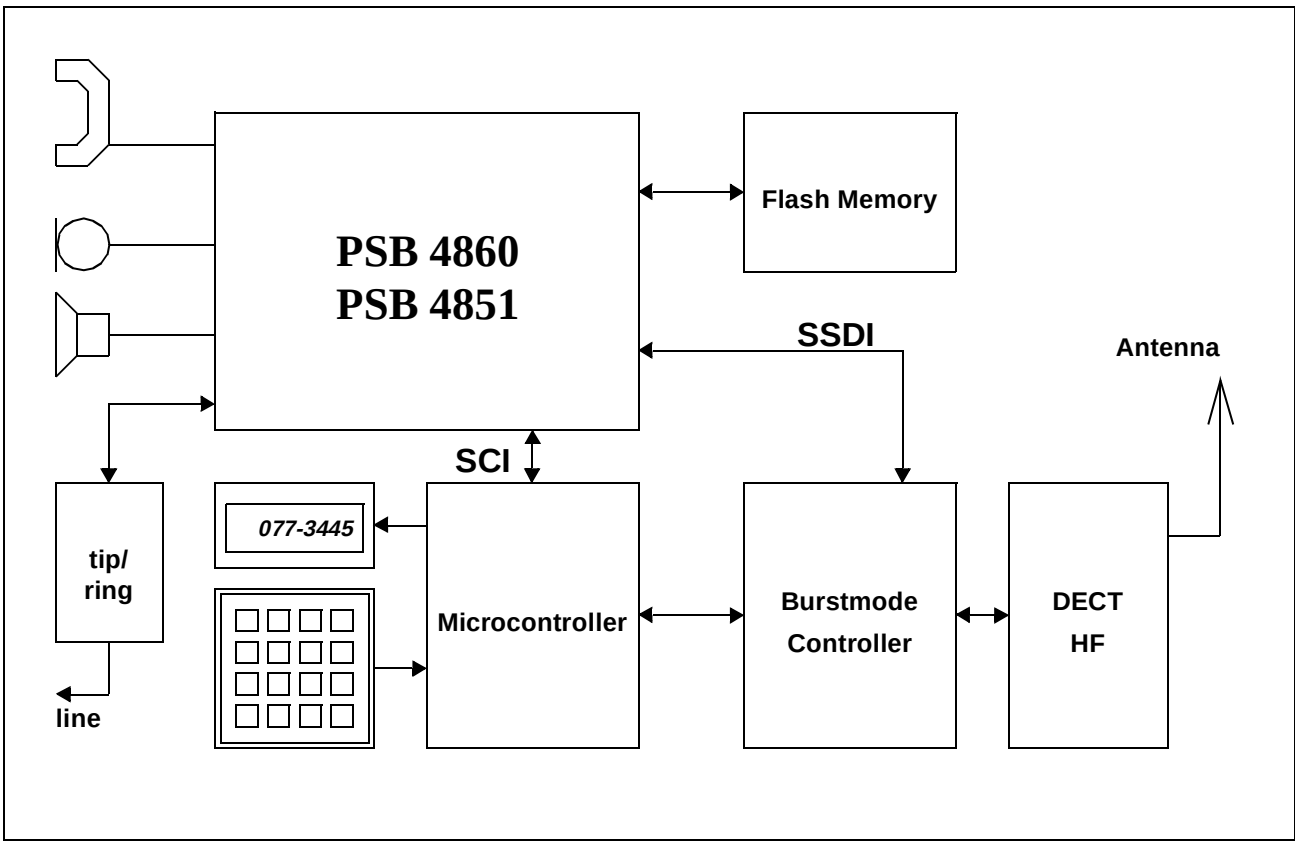


Figure 6 DECT Basestation

1.7 Backward Compatibility

The PSB 4860 V3.1 is backward compatible with the PSB 4860 V2.1 with respect to:

- Pin Configuration
- Supply Voltage
- Signal Levels
- Start-up Sequence after Reset
- Register Definition

All of the additional features of the PSB 4860 V3.1 are enabled by previously unused bits of the Hardware Configuration Registers, the Read/Write Registers or reserved command opcodes. Therefore the PSB 4860 V3.1 can be used as a drop-in replacement for the PSB 4860 V2.1 if the following checklist is observed:

1. Update version register inquiry (if present) for new version
2. Ensure no low level MMU command is used in application
3. Use voice prompt tool (formatter) for V3.1
4. Ensure no invalid (for V2.1) commands, registers or programming values are used
5. Read/Write Data accesses are not used to clear an interrupt

Note: If the current application uses low level MMU commands (e.g. for in-system reloading of voice prompts) then this code must be changed to work properly for V3.1.

2 Functional Description

The PSB 4860 features a unique modular concept for ultimate flexibility. The basic idea is to have a set of independent modules (e.g. a DTMF Detector or a Line Echo Canceller) available within the chip. Each module has signal inputs and signal outputs as appropriate. Any signal input of any module can be connected to any signal output of another module. Therefore modules can be combined as necessary for a particular application. It is, of course, possible to change the interconnection of the modules at any time. Figure **7** shows the available modules.

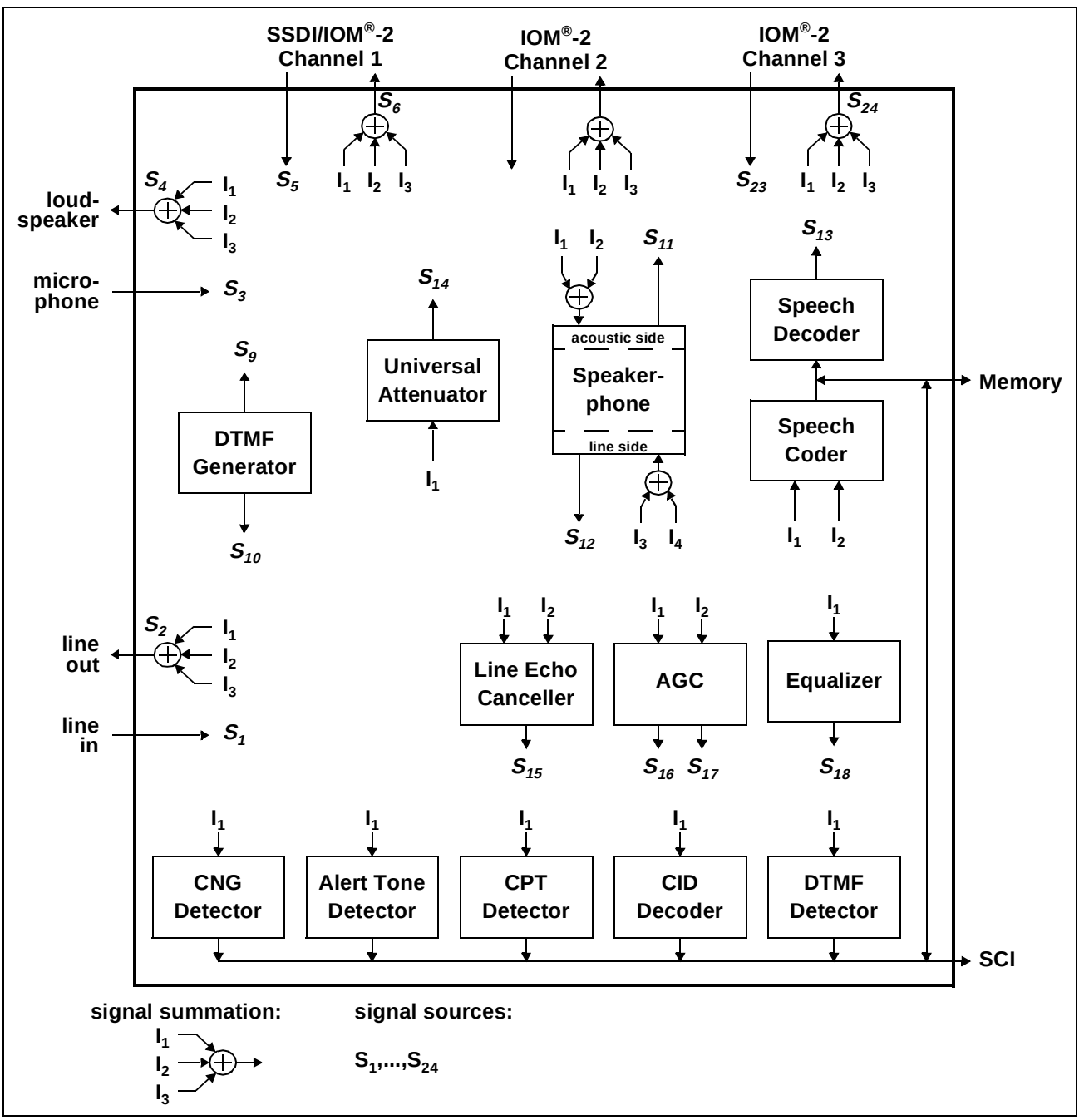


Figure 7 Modular Concept

Each unit has one or more signal inputs (denoted by I). Most units have at least one signal output (denoted by S). Any input I can be connected to any signal output S. In addition to the signals shown in figure **7** there is also the signal S_0 (silence), which is useful at signal summation points. Table **1** lists the available signals within the PSB 4860 according to their reference points.

Table 1

Signal	Description
S_0	Silence
S_1	Analog line input (channel 1 of PSB 4851 interface)
S_2	Analog line output (channel 1 of PSB 4851 interface)
S_3	Microphone input (channel 2 of PSB 4851 interface)
S_4	Loudspeaker/Handset output (channel 2 of PSB 4851 interface)
S_5	Serial interface input, channel 1
S_6	Serial interface output, channel 1
S_7	Serial interface input, channel 2
S_8	Serial interface output, channel 2
S_9	DTMF generator output
S_{10}	DTMF generator auxiliary output
S_{11}	Speakerphone output (acoustic side)
S_{12}	Speakerphone output (line side)
S_{13}	Speech decoder output
S_{14}	Universal attenuator output
S_{15}	Line echo canceller output
S_{16}	Automatic gain control output (after gain stage)
S_{17}	Automatic gain control output (before gain stage)
S_{18}	Equalizer output
S_{23}	Serial interface input, channel 3
S_{24}	Serial interface output, channel 3

The following figures show the connections for two typical states during operation. Units that are not needed are not shown. Inputs that are not needed are connected to S_0 which provides silence. In figure **8** a hands-free phone conversation is currently in progress. The speech coder is used to record the signals of both parties. The alert tone detector is

used to detect an alerting tone of an off-hook caller id request while the CID decoder decodes the actual data transmitted in this case.

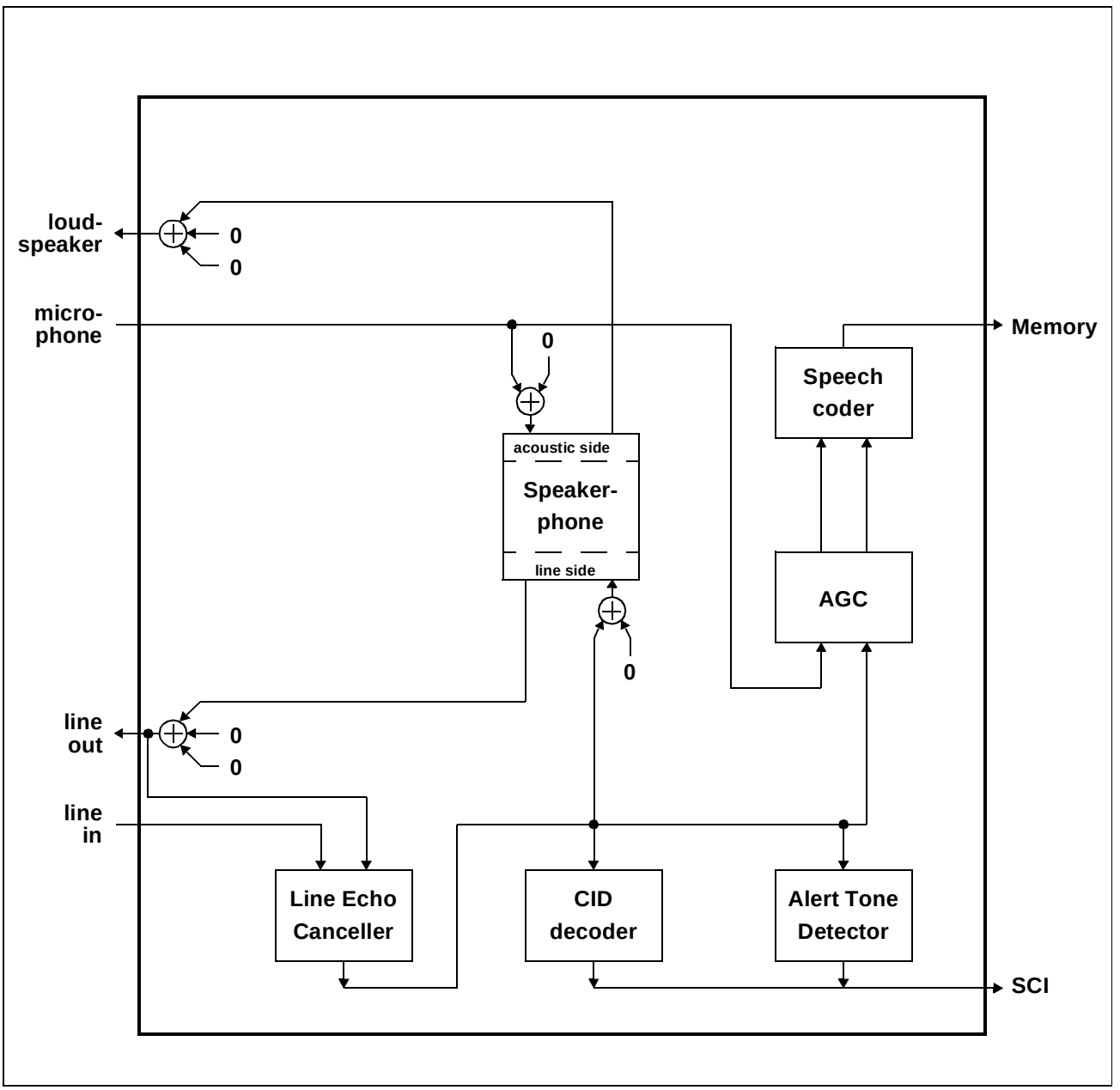


Figure 8 Functional Units - Recording a Phone Conversation

In figure **9** a phone conversation using the speakerphone is in progress. One party is using the base station of a DECT system while the other party is using a mobile handset. At the same time an external call is serviced by the answering machine. In the current state a message is being played back. In this case the DTMF detector is used to detect signals for remote access while the CPT detector is used to determine the end of the external call.

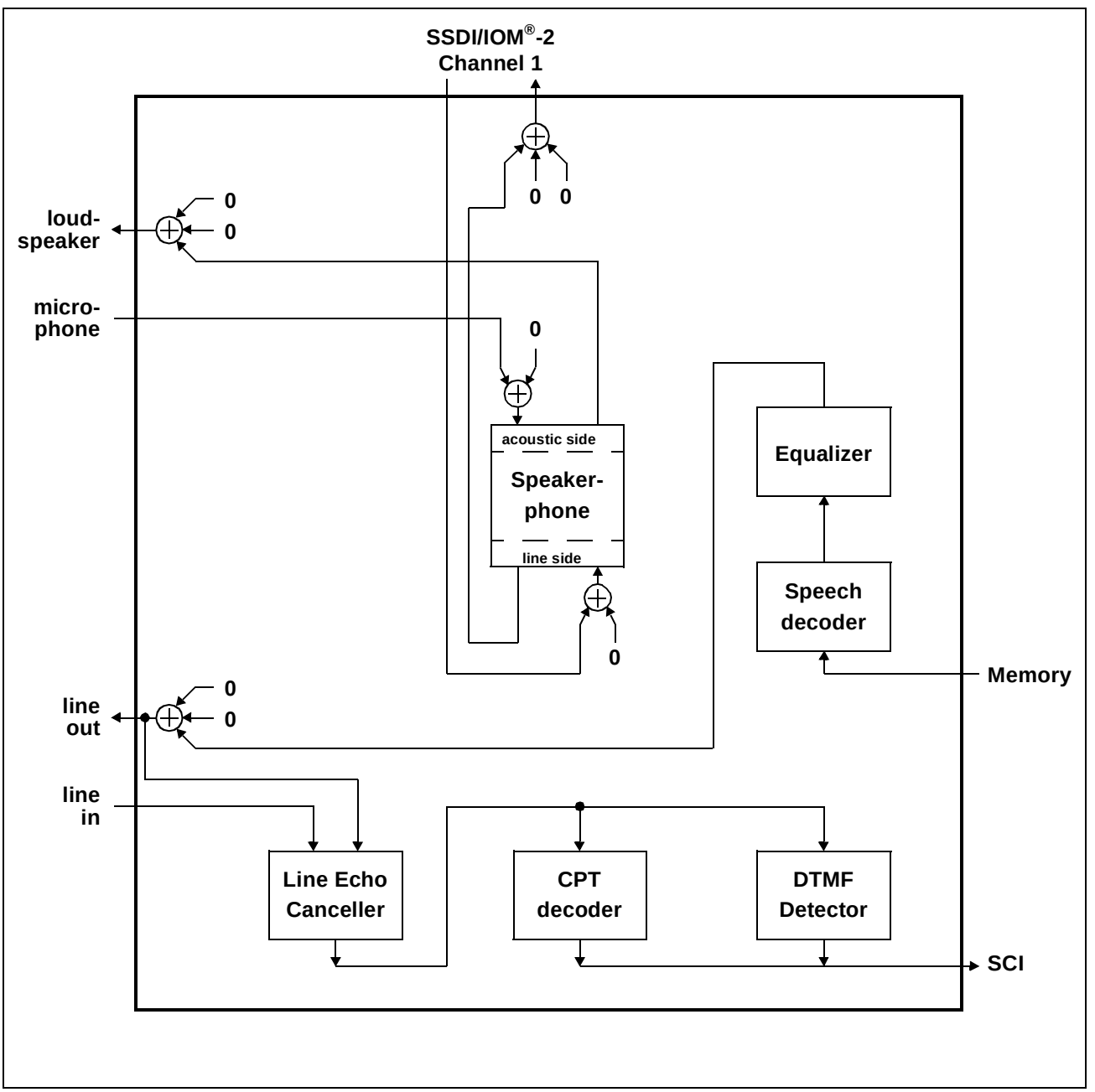


Figure 9 Functional Units - Simultaneous Internal and External Call

The following sections discuss each of the functional units briefly. A complete description can be found in the documentation for the PSB 4860 V2.1.

2.1 Full Duplex Speakerphone

The speakerphone unit (figure **10**) is attached to four signals (microphone, loudspeaker, line out and line in). The two input signals (microphone, line in) are preceded by a signal summation point.

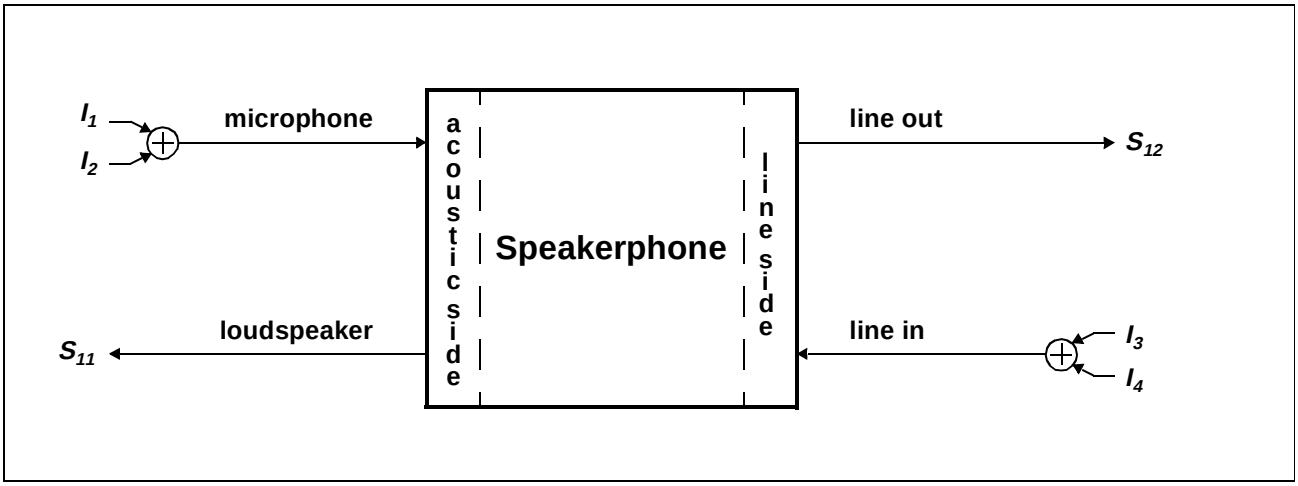


Figure 10 Speakerphone - Signal Connections

Internally, this unit can be divided into an echo cancellation unit and an echo suppression unit (figure **11**). The echo cancellation unit provides the attenuation G_c while the echo suppression unit provides the attenuation G_s. The total attenuation ATT of the speakerphone is therefore $ATT=G_C+G_s$.

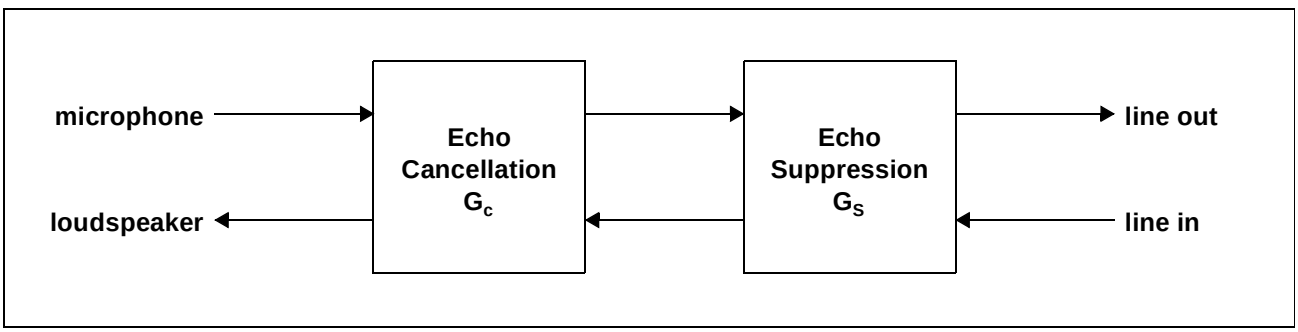


Figure 11 Speakerphone - Block Diagram

The echo suppression unit can be enabled without the echo cancellation unit. If the echo cancellation unit is disabled, the echo suppression unit still provides speakerphone functionality, albeit only half duplex. As the echo cancellation must be disabled during recording or playback of speech data, this option allows for speakerphone operation even if recording or playback is going on. The echo suppression unit is also used to provide additional attenuation if the echo cancellation unit cannot provide all of the required attenuation itself.

2.1.1 Echo Cancellation

A simplified block diagram of the echo cancellation unit is shown in figure **12**.

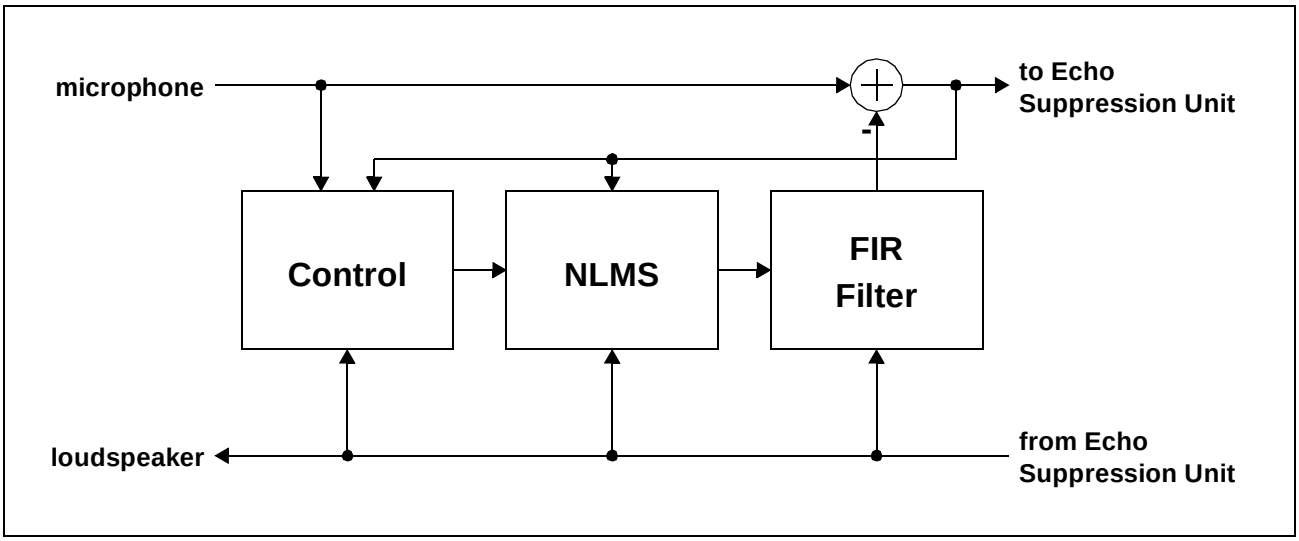


Figure 12 Echo Cancellation Unit - Block Diagram

The echo cancellation unit consists of an finite impulse response filter (FIR) that models the expected acoustic echo, an NLMS based adaption unit and a control unit. The expected echo is subtracted from the actual input signal from the microphone. If the model is exact and the echo does not exceed the length of the filter then the echo can be completely cancelled. However, even if this ideal state can be achieved for one given moment the acoustic echo usually changes over time. Therefore the NLMS unit continuously adapts the coefficients of the FIR filter. This adaption process is steered by the control unit. As an example, the adaption is inhibited as long as double talk is detected by the control unit. Furthermore the control unit informs the echo suppression unit about the achieved echo return loss.

2.2 Line Echo Canceller

The PSB 4860 contains an adaptive line echo cancellation unit for the cancellation of near end echoes. The unit has two modes: normal and extended. In normal mode, the maximum echo length is 4 ms. This mode is always available. In extended mode, the maximum echo length is 24 ms. Extended mode cannot be used while the speech encoder is running or while slow playback.

The line echo cancellation unit is especially useful in front of the various detectors (DTMF, CPT, etc.). A block diagram is shown in figure **13**.

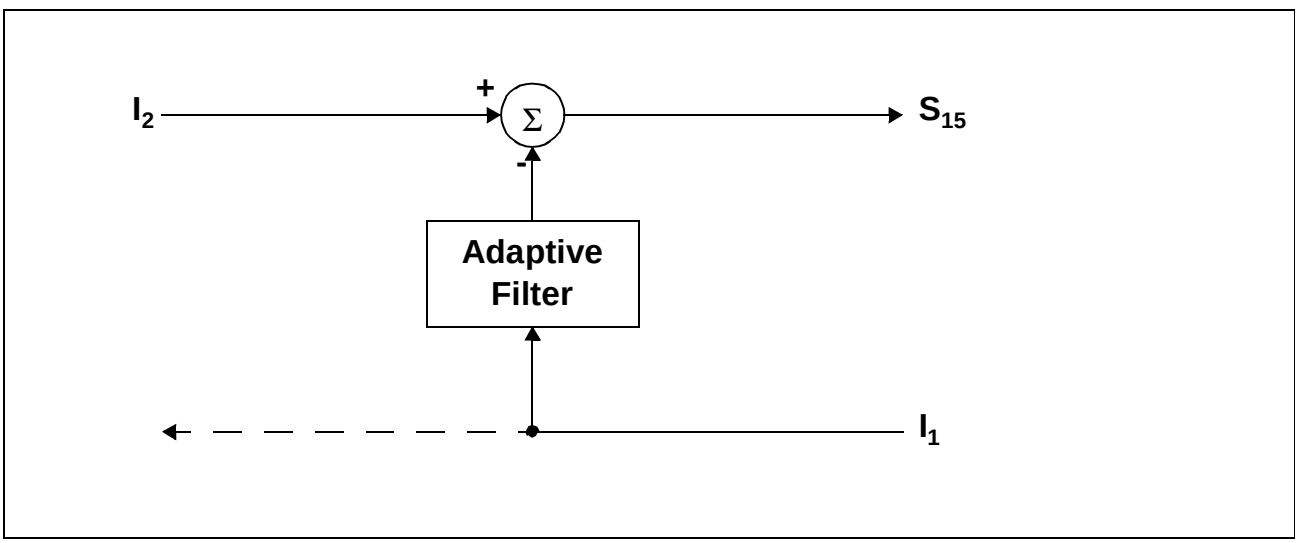


Figure 13 Line Echo Cancellation Unit - Block Diagram

The line echo canceller provides only one outgoing signal (S_{15}) as the other outgoing signal would be identical with the input signal I_1.

2.3 DTMF Detector

Figure **14** shows a block diagram of the DTMF detector. The results of the detector are available in the status register and a dedicated result register that can be read via the serial control interface (SCI) by the external controller. All sixteen standard DTMF tones are recognized.

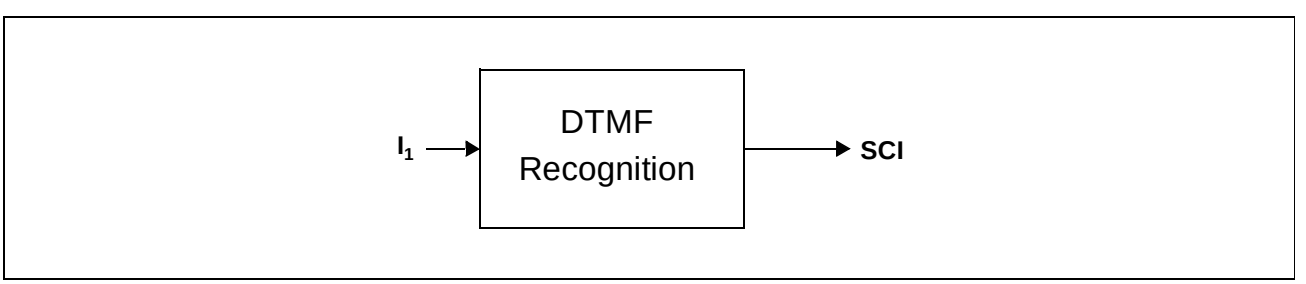


Figure 14 DTMF Detector - Block Diagram

2.4 CNG Detector

The calling tone (CNG) detector can detect the standard calling tones of fax machines or modems. This helps to distinguish voice messages from data transfers. The result of the detector is available in the status register that can be read via the serial control interface (SCI) by the external controller. The CNG detector consists of two band-pass filters with fixed center frequency of 1100 Hz and 1300 Hz.

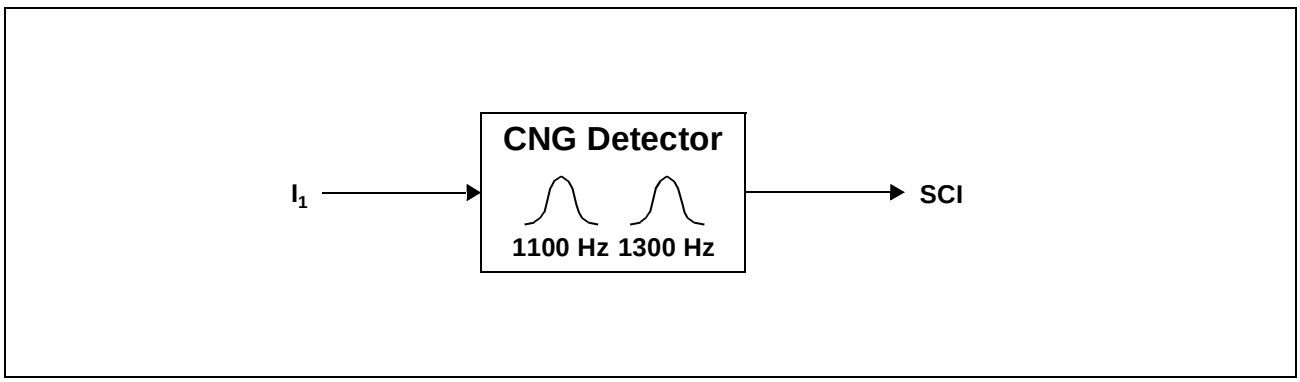


Figure 15 CNG Detector - Block Diagram

2.5 Alert Tone Detector

The alert tone detector can detect the standard alert tones (2130 Hz and 2750 Hz) for caller id protocols. The results of the detector are available in the status register and the dedicated register ATDCTL0 that can be read via the serial control interface (SCI) by the external controller.

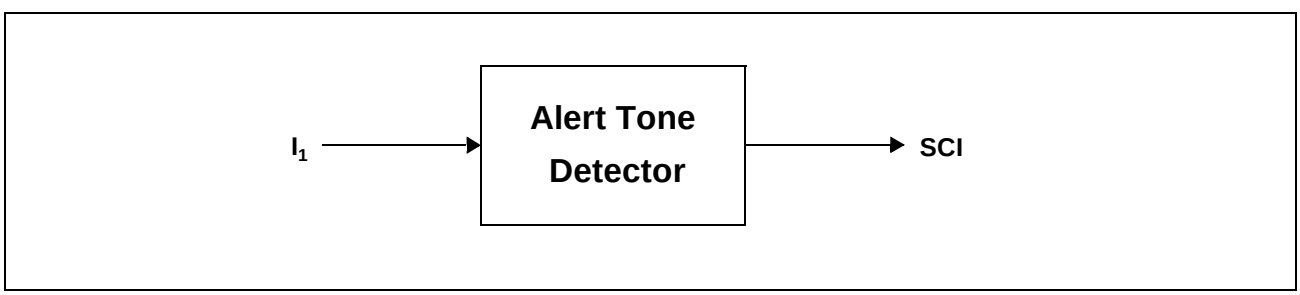


Figure 16 Alert Tone Detector - Block Diagram

2.6 CPT Detector

The selected signal is monitored continuously for a call progress tone. The CPT detector consists of a fixed band-pass followed by an optional timing checker (figure **17**).

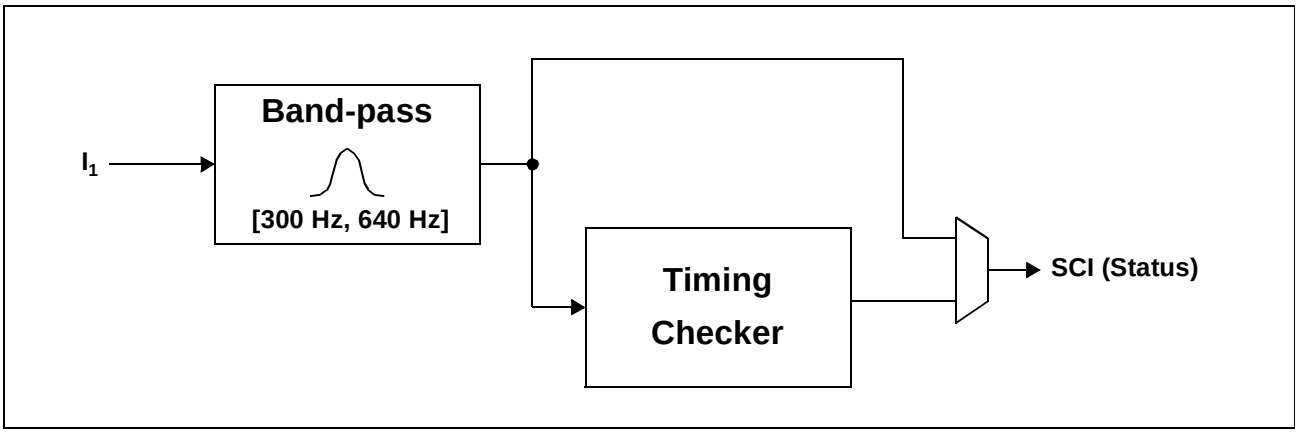


Figure 17 CPT Detector -Block Diagram

The CPT detector can be used in two modes: raw and cooked. In raw mode, the occurrence of a signal within the frequency, time and energy limits is directly reported. The timing checker is bypassed and therefore the does not interpret the length or interval of the signal.

In cooked mode (fixed band-pass only), the number and duration of signal bursts are interpreted by the timing checker. A signal burst followed by a gap is called a cycle. Cooked mode requires a minimum of two cycles. In this mode the CPT is modelled as a sequence of identical bursts separated by gaps with identical length. The PSB 4860 can be programmed to accept a range for both the burst and the gap. It is also possible to specify a maximum aberration of two consecutive bursts (gaps). Figure **18** shows the parameters for a single cycle (burst and gap).

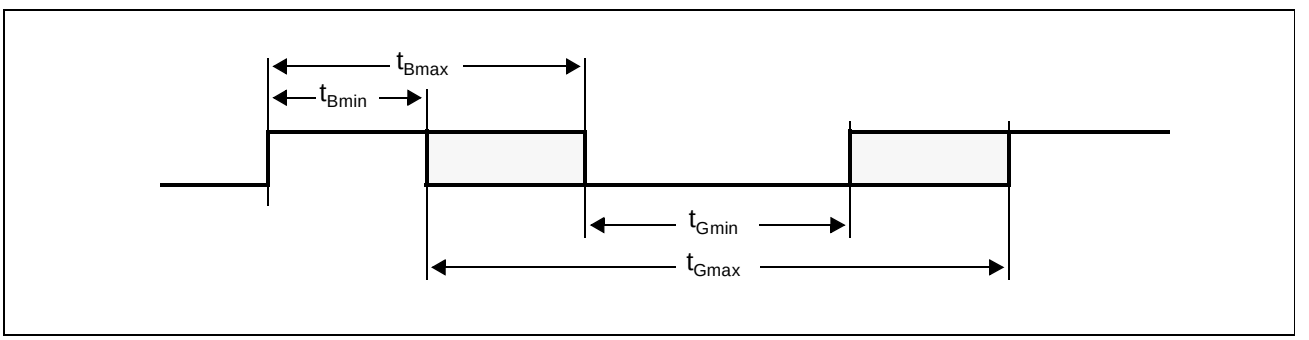


Figure 18 CPT Detector - Cooked Mode

2.7 Caller ID Decoder

The caller ID decoder is basically a 1200 baud modem (FSK, demodulation only). The bit stream is formatted by a subsequent UART and the data is available in a data register along with status information (figure **19**).

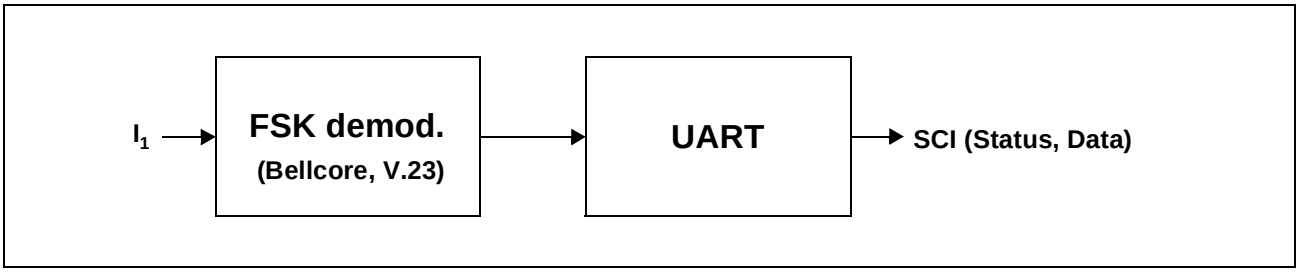


Figure 19 Caller ID Decoder - Block Diagram

The FSK demodulator supports two modes according to table **2**. The appropriate mode is detected automatically.

Table 2

Mode	Mark (Hz)	Space (Hz)	Comment
1	1200	2200	Bellcore
2	1300	2100	V.23

The CID decoder does not interpret the data received. When the CID unit is enabled, it first waits for a channel seizure signal consisting of a series of alternating space and mark signals. The number of spaces and marks that have to be received without errors before the PSB 4860 reports a carrier detect can be programmed.

Channel seizure must be followed by at least 16 continuous mark signals. The first space signal detected is then regarded as the start bit of the first message byte.

The interpretation of the data, including message type, length and checksum is completely left to the controller. The CID unit should be disabled as soon as the complete information has been received as it cannot detect the end of the transmission by itself.

Note: Some caller ID mechanism may require additional external components for DC coupling. These tasks must be handled by the controller.

Note: The controller is responsible for selecting and storing parts of the CID as needed.

2.8 DTMF Generator

The DTMF generator can generate single or dual tones with programmable frequency and gain. This unit is primarily used to generate the common DTMF tones but can also be used for signalling or other user defined tones. A block diagram is shown in figure **20**.

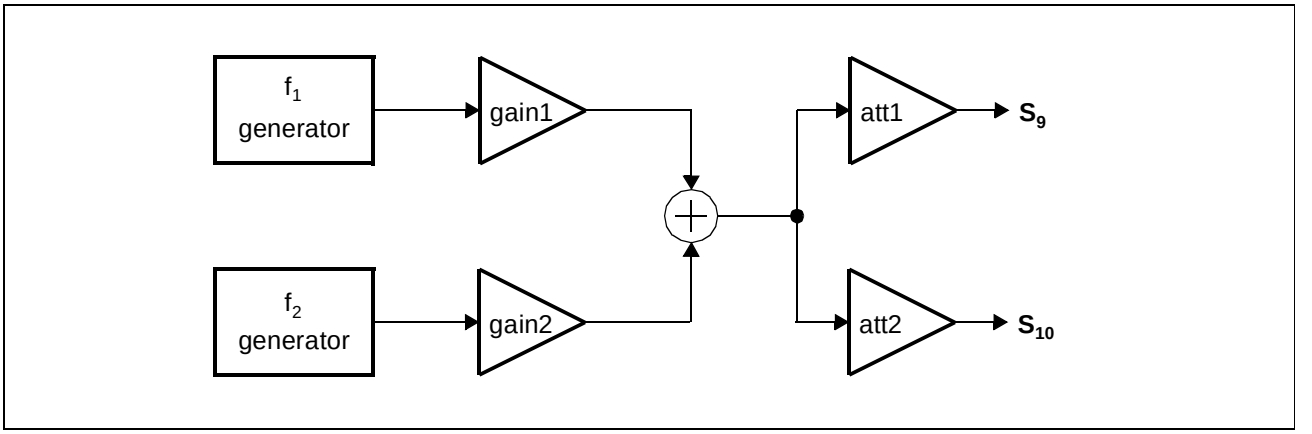


Figure 20 DTMF Generator - Block Diagram

Both generators and amplifiers are identical. There are two modes for programming the generators, cooked mode and raw mode. In cooked mode, DTMF tones are generated by programming a single 4 bit code. In raw mode, the frequency of each generator/ amplifier can be programmed individually by a separate register. The unit has two outputs which provide the same signal but with individually programmable attenuation.

2.9 Speech Coder

The speech coder (figure **21**) has two input signals I_1 and I_2. The first signal (I_1) is fed to the coder while the second signal (I_2) is used as a reference signal for voice controlled recording. The signal I_1 can be coded by either a High Quality coder or a Long Play coder.

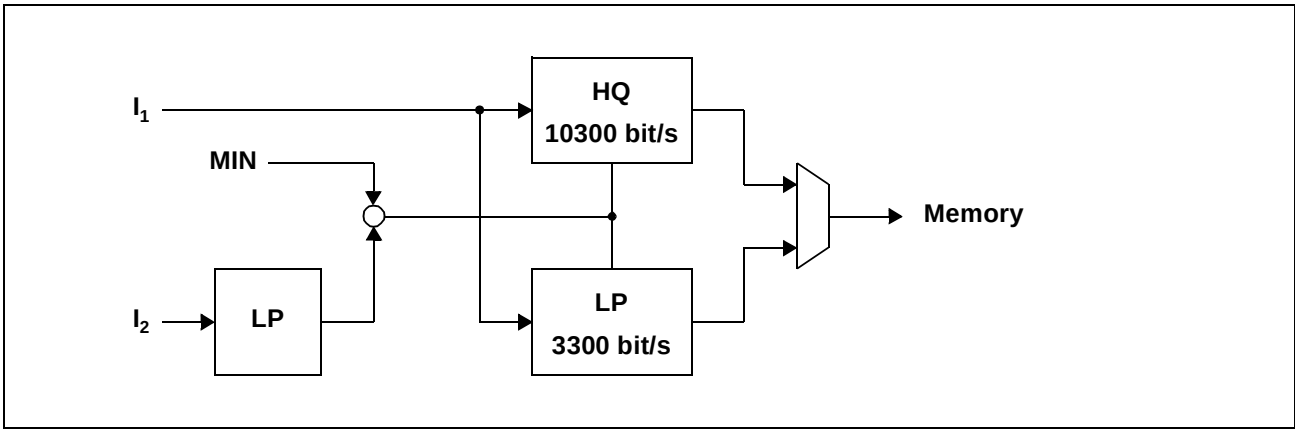


Figure 21 Speech Coder - Block Diagram

In High Quality the output data stream runs at a fixed rate of 10300 bit/s and provides excellent speech quality. In Long Play mode, the output data stream is further reduced to an average of 3300 bit/s while still maintaining good quality.

The coder can be switched on the fly. No audio data is lost during switching.

The signal I_2 is first filtered by a low pass LP1 with programmable time constant and then compared to a reference level MIN. The coder can be enabled in permanent mode or in voice recognition mode. In permanent mode, the coder starts immediately and compresses all input data continuously. The current state of the status bit SD does not affect the coder.

In voice recognition mode, the coder is automatically started on the first transition of the status bit from 0 to 1. Once the coder has started it remains active until disabled.

2.10 Speech Decoder

The speech decoder (figure **22**) decompresses the data previously coded by the speech coder unit and delivers a standard 128 kbit/s data stream.

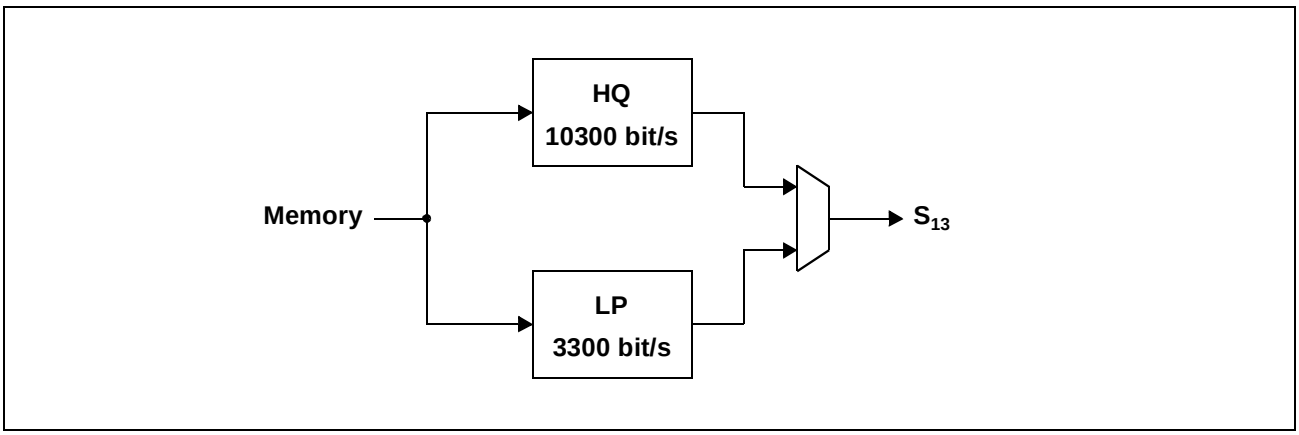


Figure 22 Speech Decoder - Block Diagram

The decoder supports fast (1.5 and 2.0 times) and slow (0.5 times) motion independent of the selected quality. The decoder requests input data as needed at a variable rate. If the end of the file is reached, the decoder is automatically disabled.

2.11 Analog Interface

There are two identical interfaces at the analog side (to PSB 4851) as shown in figure **23**.

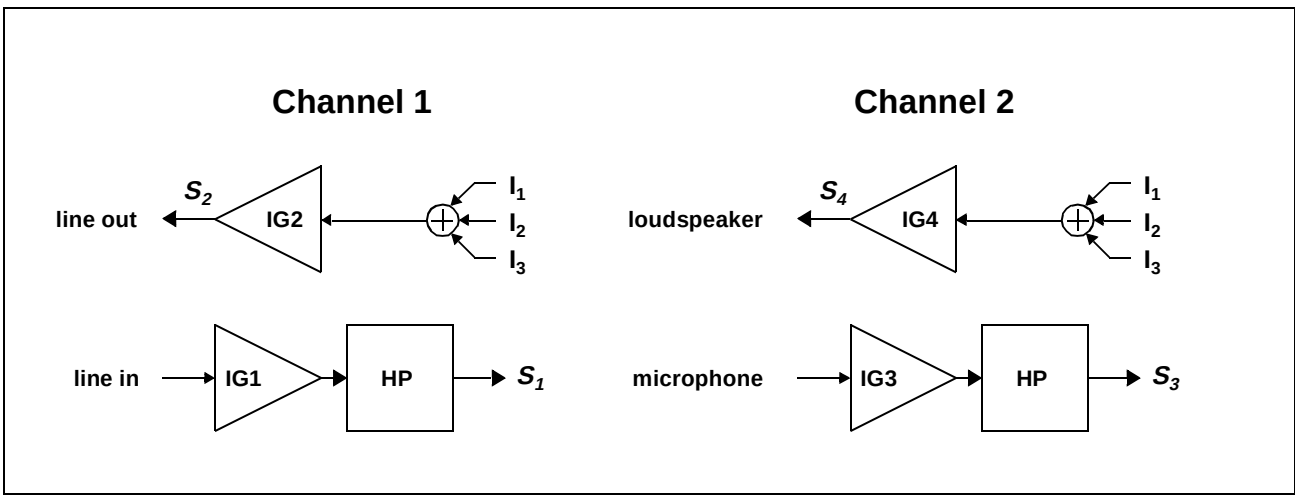


Figure 23 PSB 4851 Interface - Block Diagram

For each signal an amplifier is provided for level adjustment. The ingoing signals can be passed through an optional high-pass (HP). Furthermore, up to three signals can be mixed in order to generate the outgoing signals (S_2,S_4).

2.12 Digital Interface *(Improved in Version 3.1)*

There are *three* almost identical interfaces at the digital side as shown in figure **24**. The only difference between these two interfaces is that only channel 1 supports the SSDI mode.

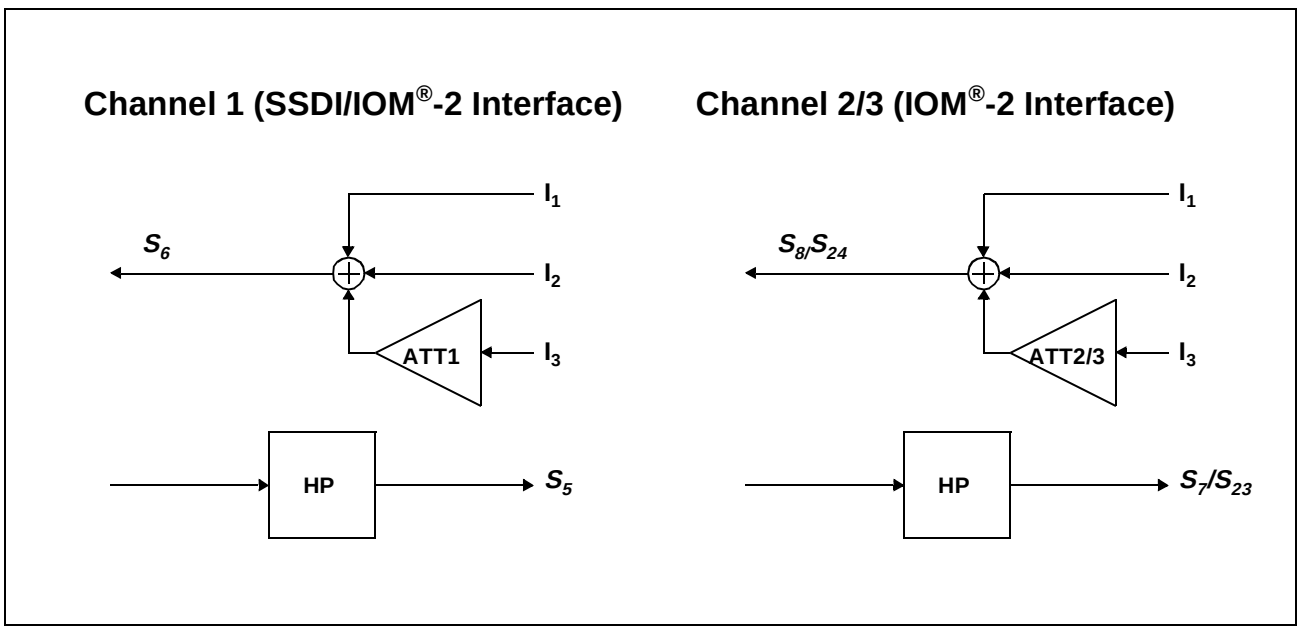


Figure 24 Digital Interface - Block Diagram

Each outgoing signal can be the sum of two signals with no attenuation and one signal with programmable attenuation (ATT). The attenuator can be used for artificial echo loss. Each input can be passed through an optional high-pass (HP).

In V3.1 a third channel (Channel 3) not present in V2.1 has been added. This has been achieved by (optionally) splitting a 16 bit linear channel into two consecutive 8 bit channels with independent data streams (A-law or μ-law). It is therefore possible to use either two 16 bit linear channels, a 16 bit channel and an 8 bit channel, a 16 bit channel and two 8 bit channels or three 8 bit channels.

2.13 Universal Attenuator

The PSB 4860 contains an universal attenuator that can be connected to any signal (e.g. for sidetone gain).

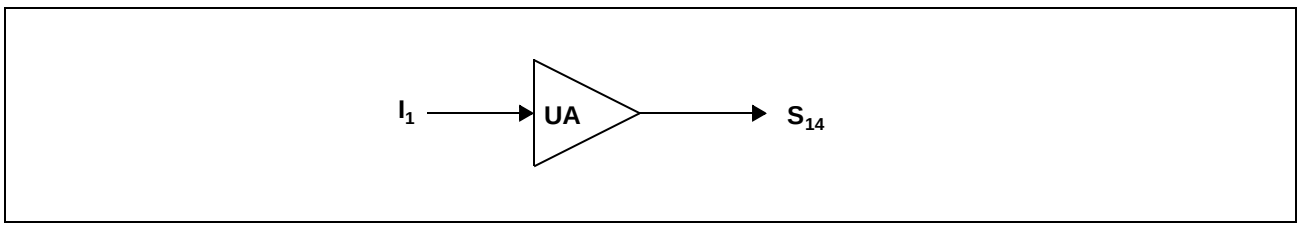


Figure 25 Universal Attenuator - Block Diagram

2.14 Automatic Gain Control Unit

In addition to the universal attenuator with programmable but fixed gain the PSB 4860 contains an amplifier with automatic gain control (AGC). The AGC is preceded by a signal summation point for two input signals. One of the input signals can be attenuated.

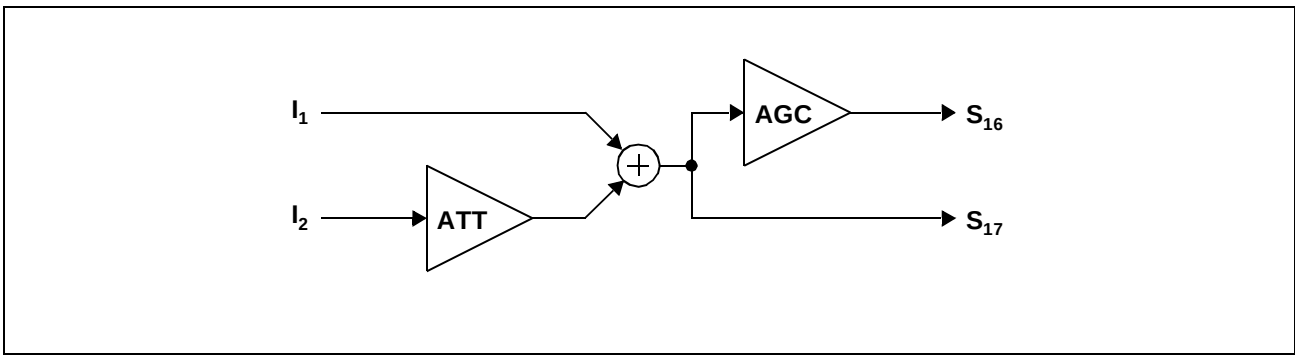


Figure 26 Automatic Gain Control Unit - Block Diagram

Furthermore the signal after the summation point is available. Besides providing a general signal summation (S_{16} not used) this signal is especially useful if the AGC unit provides the input signal for the speech coder. In this case S_{17} can be used as a reference signal for voice controlled recording.

2.15 Equalizer

The PSB 4860 also provides an equalizer that can be inserted into any signal path. The main application for the equalizer is the adaption to the frequency characteristics of the microphone, transducer or loudspeaker.

The equalizer consists of an IIR filter followed by an FIR filter as shown in figure **27**.

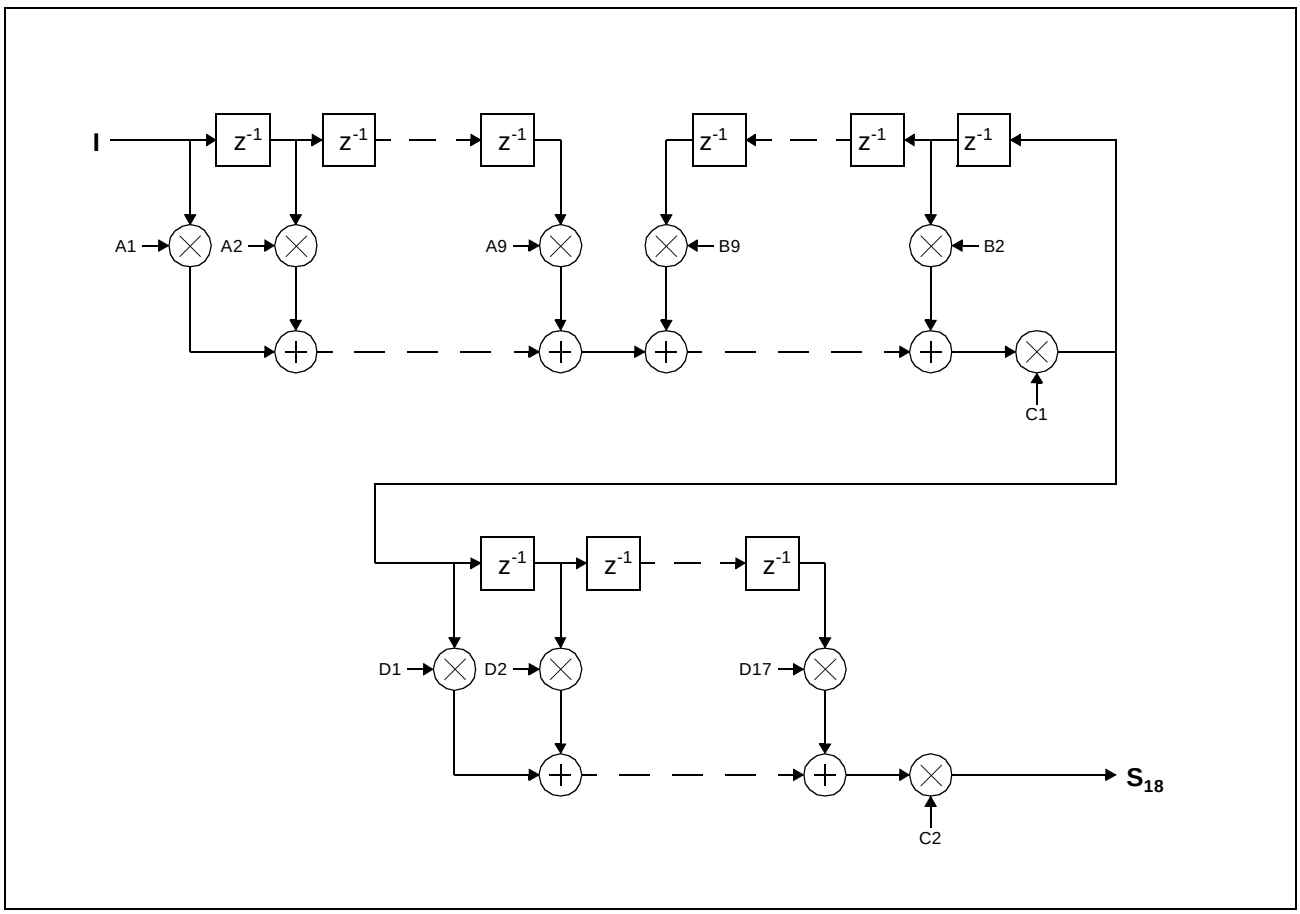


Figure 27 Equalizer - Block Diagram

The coefficients A_1-A_9, B_2-B_9 and C_1 belong to the IIR filter, the coefficients D_1-D_{17} and C_2 belong to the FIR filter.

2.16 Miscellaneous

2.16.1 Real Time Clock

The PSB 4860 supplies a real time clock which maintains time with a resolution of a second and a range of up to a year. The auxiliary oscillator must be running.

2.16.2 SPS Control Register

The two SPS outputs (SPS_0, SPS_1) can be used as either general purpose outputs, speakerphone status outputs, extended address outputs for Voice Prompt EPROM or as status register outputs. When used as status register outputs, the status register bit at position POS appears at SPS_0 and the bit at position POS+1 appears at SPS_1.

2.16.3 Reset and Power Down Mode

The PSB 4860 can be in either reset mode, power down mode or active mode. During reset the PSB 4860 clears the hardware configuration registers and stops both internal and external activity. The address lines MA_0-MA_{15} provide a weak low until they are actually used as address lines (strong outputs) or auxiliary port pins (I/O). In reset mode the hardware configuration registers can be read and written. With the first access to a read/write register the PSB 4860 enters active mode. In this mode the main oscillator is running and normal operation takes place. By setting the power down bit (PD) the can be brought to power down mode.

In power down mode the main oscillator is stopped. Depending on the configuration (ARAM/DRAM, APP) the PSB 4860 may still generate external activity (e.g. refresh). The PSB 4860 enters active mode again upon an access to a read/write register. Figure **28** shows a state chart of the modes of the PSB 4860.

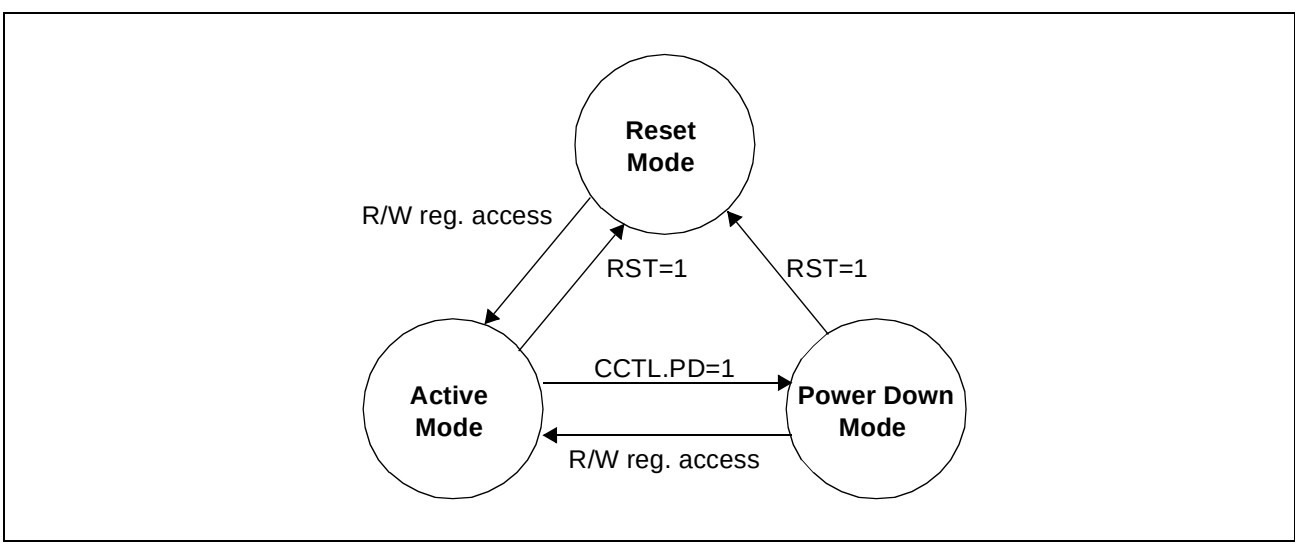


Figure 28 Operation Modes - State Chart

2.16.4 Interrupt

The PSB 4860 can generate an interrupt to inform the host of an update of the STATUS register An interrupt mask register (INTM) can be used to disable or enable the interrupting capability of each bit of the STATUS register except ABT individually. The interrupt is cleared when the host reads the STATUS register.

2.16.5 Abort

If the PSB 4860 detects a corrupted configuration (e.g. due to a transient loss of power) it stops operation and initializes all read/write registers to their reset state. After that it sets the ABT bit of the STATUS register, generates an interrupt and goes into power down mode. The discards all commands with the exception of a write command to the revision register while ABT is set. Only after the write command to the revision register (with any value) the ABT bit is reset and a reinitialization can take place.

2.16.6 Revision Register

The PSB 4860 contains a revision register. This register is read only and does not influence operation in any way. A write to the revision register clears the ABT bit of the STATUS register but does not alter the content of the revision register.

2.16.7 Hardware Configuration

The PSB 4860 can be adapted to various external hardware configurations by four special registers: HWCONFIG0 to HWCONFIG3. These registers are usually only written once during initialization and must not be changed while the PSB 4860 is in active mode.

2.16.8 AFECLK Tracking

The PSB 4860 can adjust AFECLK and AFEFSC dynamically to a slightly varying FSC if AFECLK and AFEFSC are derived from the main oscillator (XTAL). This mode requires that both AFEFSC and FSC are nominally running at the same frequency (8 kHz).

3 Memory Management

This section describes the memory management provided by the PSB 4860. As figure **29** shows, three units can access the external memory. During recording, the speech coder can write compressed speech data into the external memory. For playback, the speech decoder reads compressed speech data from external memory. In addition, the microcontroller can directly access the memory by the SCI interface.

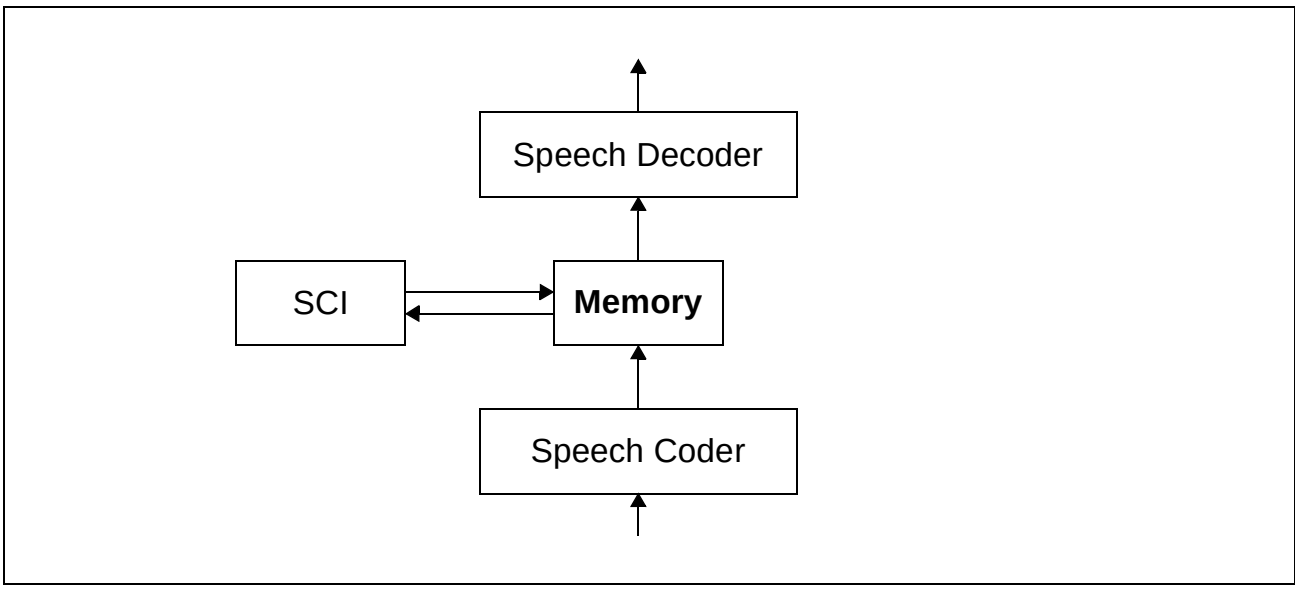


Figure 29 Memory Management - Data Flow

The memory is organized as a file system. For each memory space (R/W-memory and voice prompt memory) the PSB 4860 maintains a directory with 255 file descriptors (figure **30**).

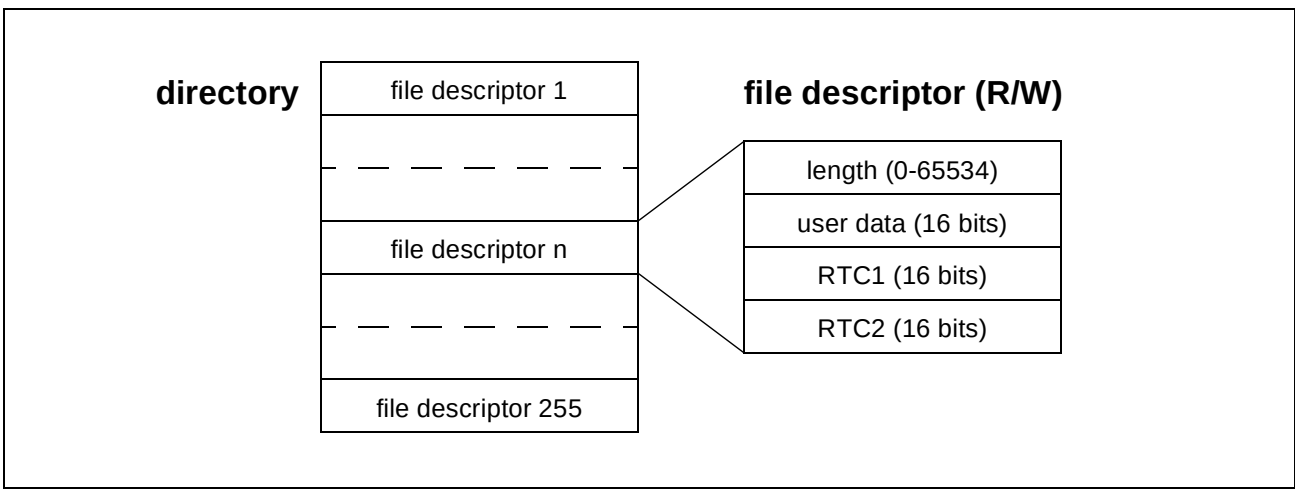


Figure 30 Memory Management - Directory Structure

The directories must be created after each power failure for volatile R/W-memory. All file descriptors are cleared (all words zero). For non-volatile memory, the directories have to

be created only once. If the directories already exist, the memory has just to be activated after a reset. The file descriptors are not changed in this case.

3.1 File Definition and Access

A file is a linear sequence of units and can be accessed in two modes: binary and audio. In binary mode, a unit is a word. In audio mode, a unit is a variable number of words representing 30 ms of uncompressed speech. A file can contain at most 65535 units. Figure **31** shows an audio file containing 100 audio units. The length of the message is therefore 3 s.

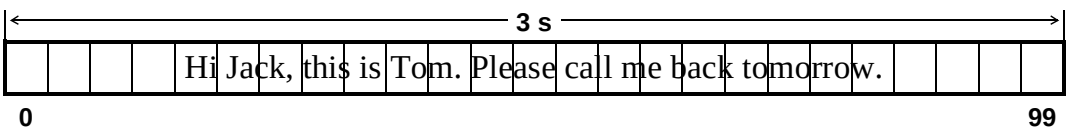


Figure 31 Audio File Organization - Example

Figure **32** shows a binary file of 11 words containing a phonebook (with only two entries).

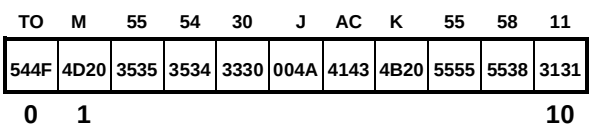


Figure 32 Binary File Organization - Example

There is one special file in the voice prompt directory (referenced by file number 255) which is intended for a large number of phrases and hence has a different organization.This file exists only in the directory for the voice prompt memory. It consists of up to 2048 phrases of arbitrary individual length. The actual number of units within an individual phrase is determined during creation and cannot be altered afterwards. Phrases can be combined in any sequence without intermediate noise or gaps.

Figure **33** shows a phrase file containing a total of five phrases.

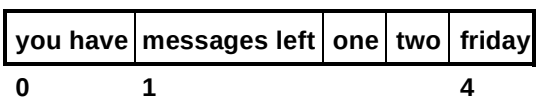


Figure 33 Phrase File Organization - Example

3.2 User Data Word

The user data word consists of 12 bits that can be read or written by the user, one bit (R) that is reserved for future use and three bits (D,M, U) which indicate the status of a file.

15					0
D	M	U	R	User Definable	

3.3 High Level Memory Management Commands

This section gives a brief overview of the high level memory management commands.

3.3.1 Initialize

This command creates a directory, sets the external memory configuration and delivers the size of usable memory in 8 kB blocks. Furthermore the voice prompt memory space is scanned for a valid directory. The PSB 4860 can either create a completely empty directory from scratch or leave the first n files of an existing directory untouched while clearing the remaining files. The latter option is useful if due to an unexpected event like a sudden power loss during recording some data is corrupted. In that case vital system information can still be recovered provided that it has been stored in the first files (e.g. file 1).

3.3.2 Activate

This command activates an existing directory, sets the external memory configuration and delivers the size of usable memory in 8 kB blocks. Furthermore the voice prompt memory space is scanned for a valid directory. Upon activation the PSB 4860 checks (in case of ARAM/DRAM only) the consistency of the directory in R/W memory space. It returns the first file that contains corrupted data (if any). If corrupted data is detected an initialization should be performed with the same file number as an input parameter.

3.3.3 Open File *(Improved in Version 3.1)*

A specific file is opened for subsequent accesses with the specified access mode. Opening a new file automatically closes the currently open file and clears the file pointer. Opening file number 0 can be used to close all physical files. If the TS flag is set, the current content of the real time clock is written to the appropriate fields of the file descriptor in order to provide a timestamp.

Optionally, the User Data Word can be written.

3.3.4 Open Next Free File *(Improved in Version 3.1)*

The next free file is opened for subsequent write accesses with the specified access mode. The search starts at the specified file number. If the TS flag is set, the current

content of the real time clock is written to the appropriate fields of the file descriptor in order to provide a timestamp. If a free file has been found, the file is opened and the file number is returned. Otherwise an error is reported.

Optionally, the User Data Word can be written.

3.3.5 Seek

The file pointer of the currently opened file is set to the specified position. If the current file is the phrase file the PSB 4860 starts the speech decoder immediately after the seek is finished. This is done by simply enabling the decoder. All other settings of the decoder remain unaffected. When the phrase is finished, the decoder is automatically disabled again.

3.3.6 Cut File *(Improved in Version 3.1)*

All units after the unit addressed by the file pointer are removed from the file. If all units are deleted the file is marked for deletion (see user data word). However, the associated file descriptor and memory space are released only after a subsequent garbage collection.

The memory space freed by a partial cut (e.g. tail-cut) is also recovered. In Version 2.1 memory was only recovered if the complete file was deleted.

3.3.7 Compress File

An audio file that has been recorded in HQ mode can be recoded using LP mode. This reduces the file size to approximately one third of the original size. The speech quality, however, is somewhat lower compared to a signal that has been recorded in LP mode in the first place. This command can be aborted at any time an resumed later without loss of information.

3.3.8 Memory Status

This command returns the number of available 8 kB blocks in R/W memory space.

3.3.9 Garbage Collection *(Improved in Version 3.1)*

This command initiates a garbage collection. Until a garbage collection files that are marked for deletion still occupy the associated file descriptor and memory space. After the garbage collection these file descriptors and the associated memory space are available again. This command can optionally remap the directory. In this mode the remaining file descriptors are remapped to form a contiguous block starting with file number 1. The original order is preserved. This command requires that all files are closed, i.e. file 0 is opened. Independently of the selected directory only the read/write directory is used.

This command can be aborted any time in V3.1 and resumed later on.

3.3.10 Access File Descriptor *(Improved in Version 3.1)*

By this command the length, user data word and RTC1/RTC2 of a file descriptor can be read. The file or the other entries of the file descriptor are not affected by this command.

Unlike in version 2.1 this command can also be used with another file being currently open. It is no longer necessary to open the file itself prior to reading the file descriptor.

3.3.11 Read Data

This command can be used in binary access mode only. A single word is read at the position given by the file pointer. The file pointer is advanced by one word automatically.

3.3.12 Write Data

This commands can be used in binary access mode only. A single word is written at the position of the file pointer. The file pointer is advanced by one word automatically.

3.4 Low Level Memory Management Commands

These commands allow the direct access of any location (single word) of the external memory. Additionally it is possible to erase any block in case of a flash device. These commands should not be used during normal operation as the may interfere with the file system.

3.4.1 Set Address

This command sets the 24 bit address pointer APTR. Only the address bits A_8-A_{23} are set, the address bits A_0-A_7 are automatically cleared.

3.4.2 DMA Read

This command reads a single word addressed by APTR. After the read access APTR is automatically incremented by one.

3.4.3 DMA Write

This command writes a single word to the location addressed by APTR. After the write access APTR is automatically incremented by one. Possible error conditions:

3.4.4 Block Erase

This command erases the physical block which includes the address given by APTR. The actual amount of memory erased by this command depends on the block size of the flash device.

Note: The data structure of V3.1 is not compatible with the data structure used by V2.1.

4 Interfaces

This section briefly discusses the interfaces of the PSB 4860 V3.1 For details please refer to the documentation of the PSB 4860 V2.1.

4.1 IOM®-2 Interface

The data stream is partitioned into packets called frames. Each frame is divided into a fixed number of timeslots. Each timeslot is used to transfer 8 bits. Figure **34** shows a commonly used terminal mode (three channels ch_0, ch_1 and ch_2 with four timeslots each).

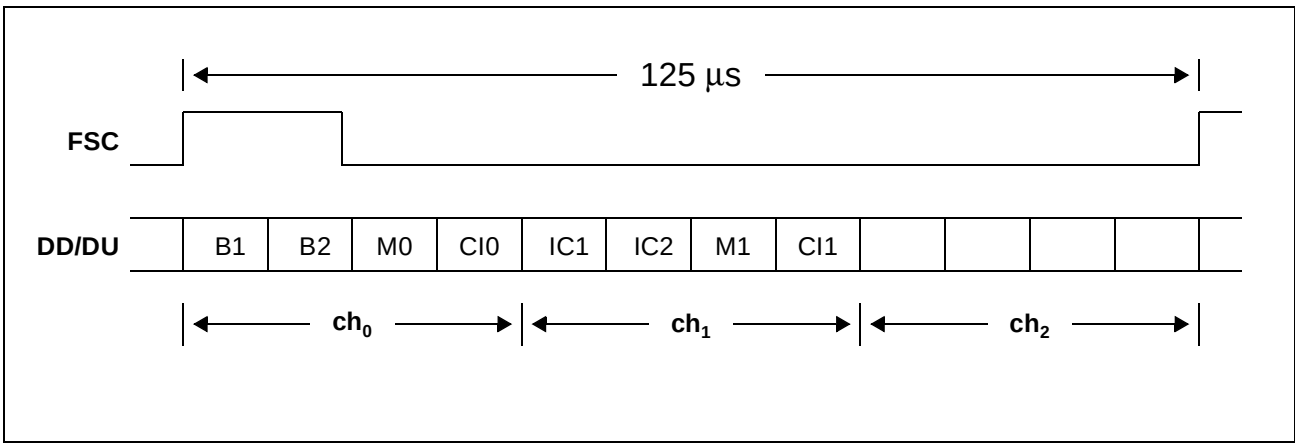


Figure 34
IOM®-2 Interface - Frame Structure

The PSB 4860 supports both single clock mode and double clock mode. In single clock mode, the bit rate is equal to the clock rate. Bits are shifted out with the rising edge of the first clock cycle and sampled with the falling edge of the second clock cycle.

4.2 SSDI Interface

The SSDI interface is intended for seamless connection to low-cost burst mode controllers (e.g. PMB 27251) and supports a single channel in each direction. The data stream is partitioned into frames. Within each frame one 16 bit value can be sent and received by the PSB 4860. The start of a frame is indicated by the rising edge of FSC. Data is always latched at the falling edge of DCL and output at the rising edge of DCL.

The SSDI transmitter and receiver are operating independently of each other except that both use the same FSC and DCL signal.

4.3 Analog Front End Interface

The uses a four wire interface similar to the IOM®-2 interface to exchange information with the analog front end (PSB 4851). The main difference is that all timeslots and the channel assignments are fixed.

4.4 Serial Control Interface *(Improved in Version 3.1)*

The serial control interface (SCI) uses four lines: SDR, SDX, SCLK and $\overline{CS}$. Data is transferred by the lines SDR and SDX at the rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of an access. Data is sampled by the PSB 4860 at the rising edge of SCLK and shifted out at the falling edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$. The accesses to the PSB 4860 can be divided into *four* classes:

1. Configuration Read/Write
2. *Normal Status Read*/Data Read
3. Register Read/Write
4. *Status Read without Interrupt Acknowledge*

With the PSB 4860 V3.1 it is possible to read the STATUS register either with or without an interrupt acknowledge. With the PSB 4860 V2.1 all accesses to the STATUS register automatically acknowledge an interrupt (if present). Therefore the controller has to check the STATUS register everytime it is read, even if not in the interrupt routine.

With the PSB 4860 V3.1 only the dedicated Status Register Read Command with Interrupt Acknowledge clears the interrupt.

Furthermore it is now possible to abort any command at any time. With the PSB 4860 V2.1 an aborted command could result in false register programming.

Table **3** shows the formats of the different command words. All other command words are reserved.

Table 3
Command Words for Register Access

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Status Register or Data Read Access	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Read Register[1)]	0	1	0	1	REG											
Write Register[1)]	0	1	0	0	REG											
Read Configuration Reg.	0	1	1	1	0	0	R	0	0	0	0	0	0	0	0	0
Write Configuration Reg.	0	1	1	0	0	0	W		DATA							
Read Status Register or Data Read Access (no Interrupt Acknowledge)	*1*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*

1) Does not acknowledge interrupt anymore.

4.5 Memory Interface *(Improved in Version 3.1)*

The PSB 4860 supports either Flash Memory or ARAM/DRAM as external memory for storing messages. If ARAM/DRAM is used, an EPROM can be added optionally to support read-only messages (e.g. voice prompts). Table **4** summarizes the different configurations supported.

Table 4

Mbit	Type	Bank 0 (D_0-D_3)	Bank 1 (D_4-D_7)	Comment
1	ARAM/DRAM	256kx4	-	
2	ARAM/DRAM	256kx4	256kx4	
4	ARAM/DRAM	1Mx4	-	
4	*ARAM/DRAM*	*4Mx1*	-	*only MD_0 is used*
4	ARAM/DRAM	512kx8		
8	ARAM/DRAM	1Mx4	1Mx4	
16	ARAM/DRAM	4Mx4	-	2k or 4k refresh
16	ARAM/DRAM	16Mx1	-	*only MD_0 is used*
16	ARAM/DRAM	2Mx8		2k refresh
32	ARAM/DRAM	4Mx4	4Mx4	2k or 4k refresh
32	ARAM/DRAM	2x2Mx8		2k refresh
64	ARAM/DRAM	16Mx4	-	4k or 8k refresh
64	ARAM/DRAM	8Mx8		4k or 8k refresh
128	ARAM/DRAM	16Mx4	16Mx4	4k or 8k refresh
4-128	FLASH			KM29N040
16-128	FLASH			KM29N16000
4-16	*FLASH*			*TC58A040*
4-16	*FLASH*			*AT45DB041*
8-32	*FLASH*			*AT45DB081*

If ARAM/DRAM is used, the total amount of memory must be a power of two and all devices must be of the same type. The pin FRDY must be tied high.

For flash devices, the PSB 2168 supports in-circuit programming of voice prompts by releasing the control lines during reset and (optionally) power down. Instead of actively driving the lines $\overline{\text{FCS}}$, $\overline{\text{FOE}}$, $\overline{\text{FWE}}$, FCLE and ALE these lines are pulled high by a weak pullup during reset and (optionally) power down.

4.5.1 ARAM/DRAM Interface *(Improved in Version 3.1)*

The PSB 4860 supports up to two banks of memory which may be either *1 bit*, 4 bit or 8 bit wide (Figure **35**). If both banks are used they must be populated identically.

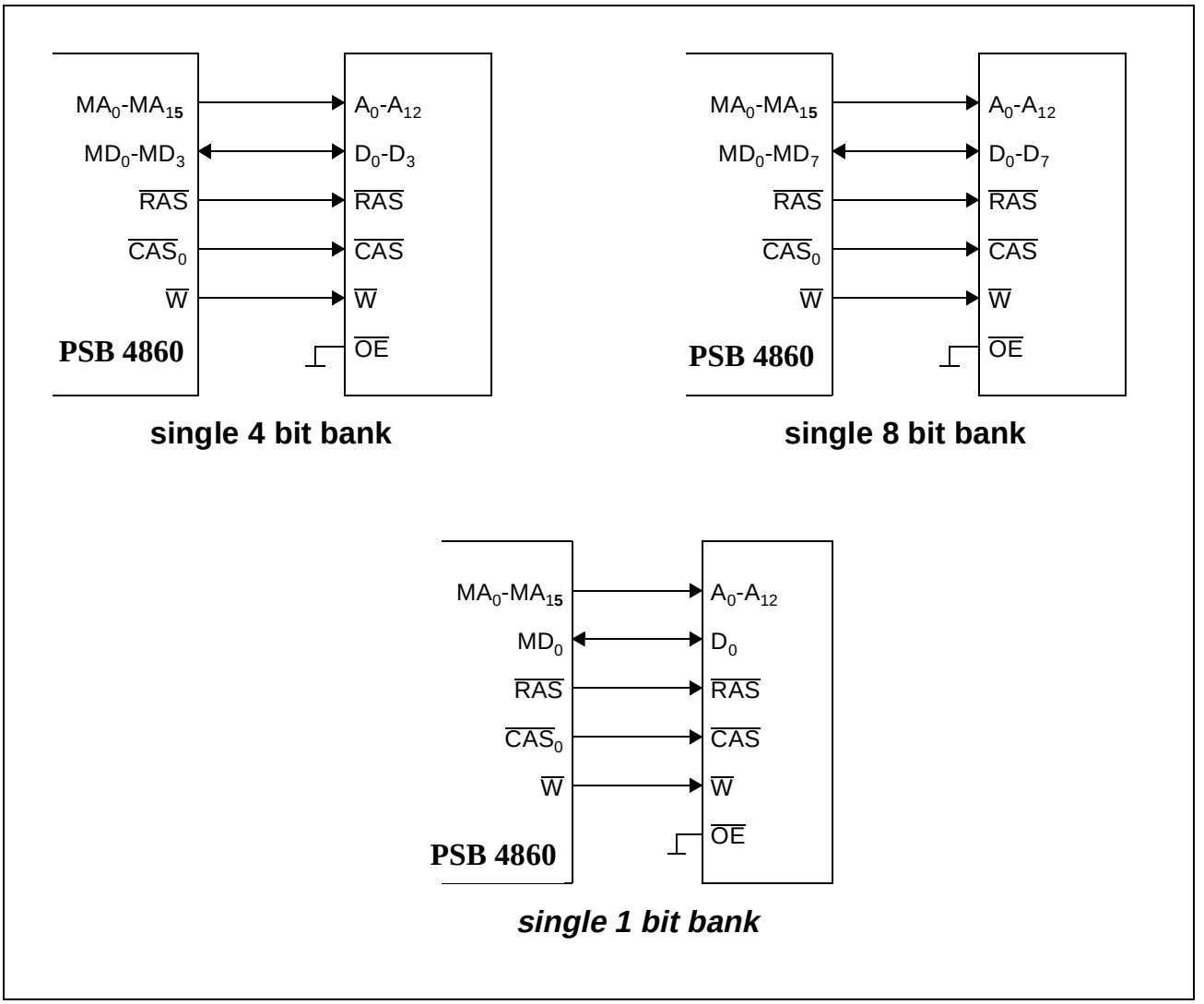


Figure 35 ARAM/DRAM Interface - Connection Diagram

For power-down refresh, two modes are available. The normal mode ensures a refresh rate of 64 kHz while the battery backup mode uses 8 kHz for low power ARAMs/DRAMs. The battery backup mode can only be used with the auxiliary oscillator running.

4.5.2 EPROM Interface

The supports an EPROM in parallel with ARAM/DRAM. This interface is always 8 bits wide and supports a maximum of 256 kB. Figure **36** shows a connection diagram.

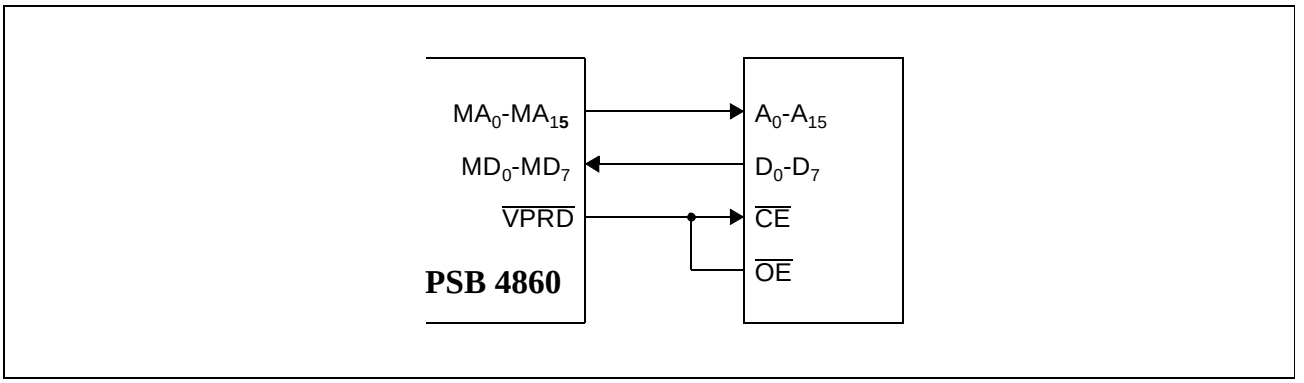


Figure 36 EPROM Interface - Connection Diagram

4.5.3 Samsung Flash Memory Interface

The PSB 4860 has special support for the KM29N040 and KM29N16000. No external components are required for up to four devices. Figure **37** shows the connection diagram for a single device.

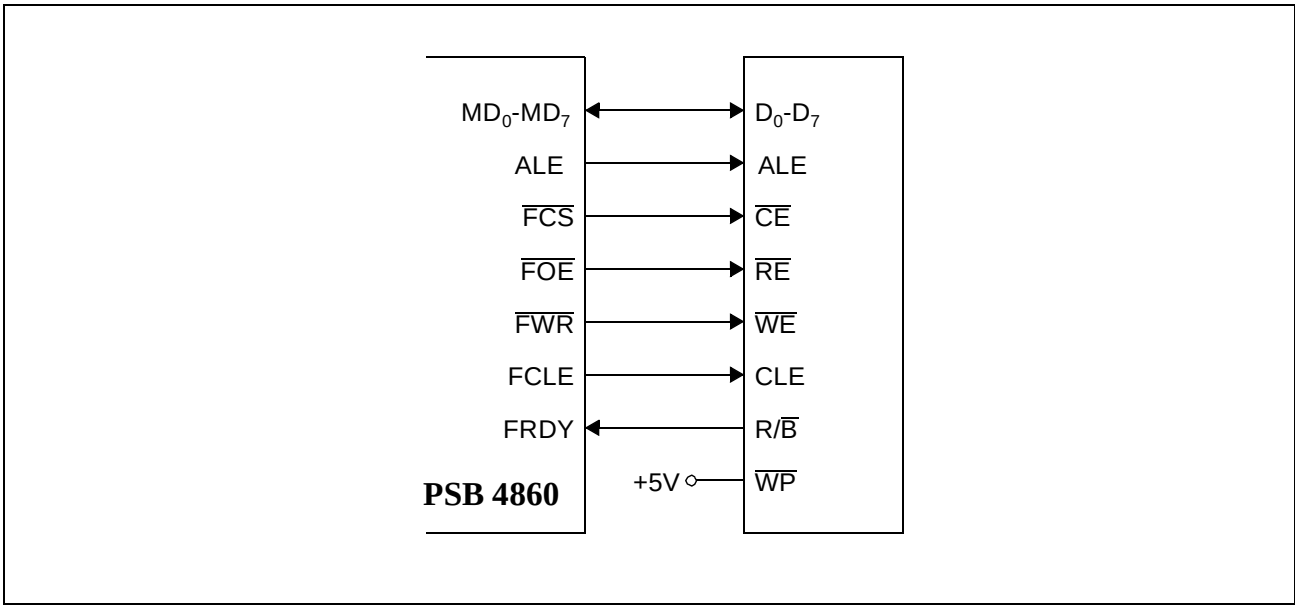


Figure 37 Flash Memory Interface - Connection Diagram

Figure **38** shows an application with three KM29N040 devices.

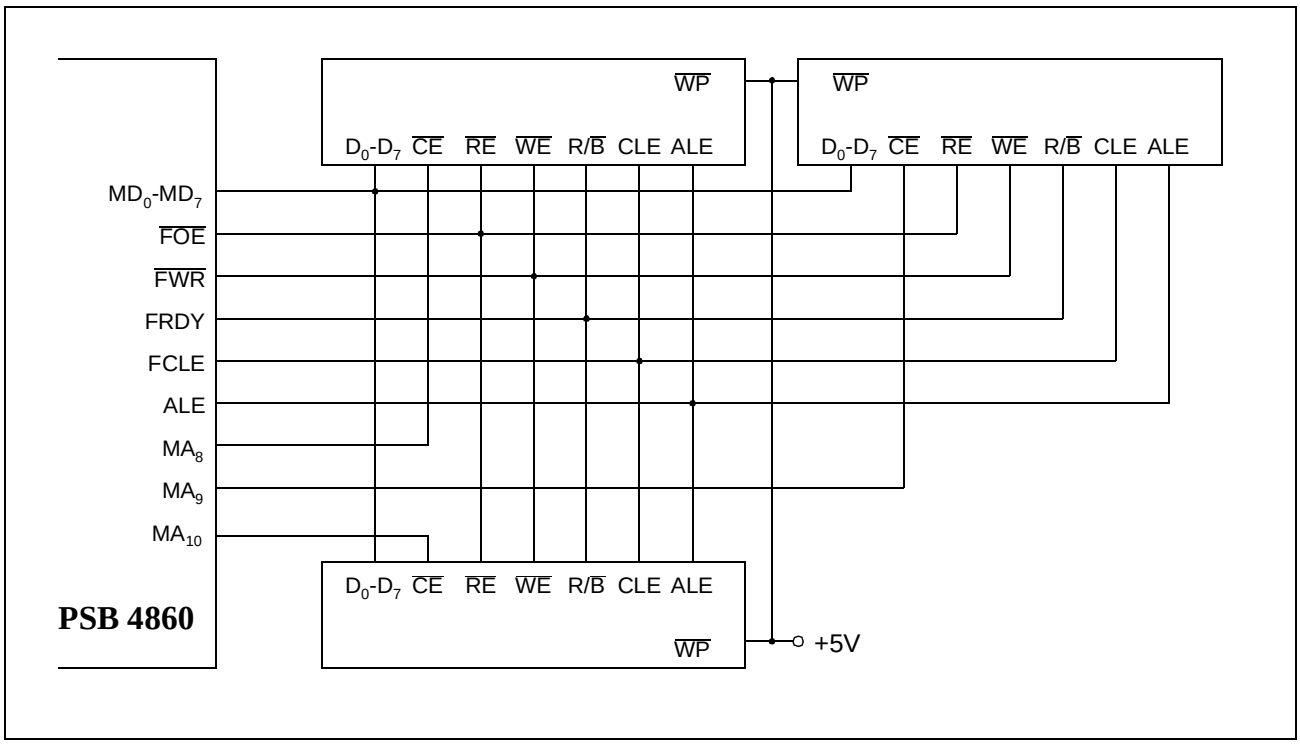


Figure 38 Flash Memory Interface - Multiple Devices

4.5.4 Serial Flash Memory Interface *(New in Version 3.1)*

*The PSB 4860 supports up to four identical devices. It can detect the number of devices connected automatically. The controller must provide the information about the type of the devices connected. Table **5** shows the pins that are used order to support serial flash devices.*

Table 5

Pin Nr.	Name	Comment
42	MD_0/SCLK	Clock output for serial interface
43	MD_1/SDI	Data in from flash device
44	MD_2/SDO	Data out from PSB 2168 V3.1
46	$MD_4/\overline{CS}_0$	Chip select for first device
47	$MD_5/\overline{CS}_1$	Chip select for second device
50	$MD_6/\overline{CS}_2$	Chip select for third device
51	$MD_7/\overline{CS}_3$	Chip select for fourth device

The following figures show the connection diagrams for various configurations.

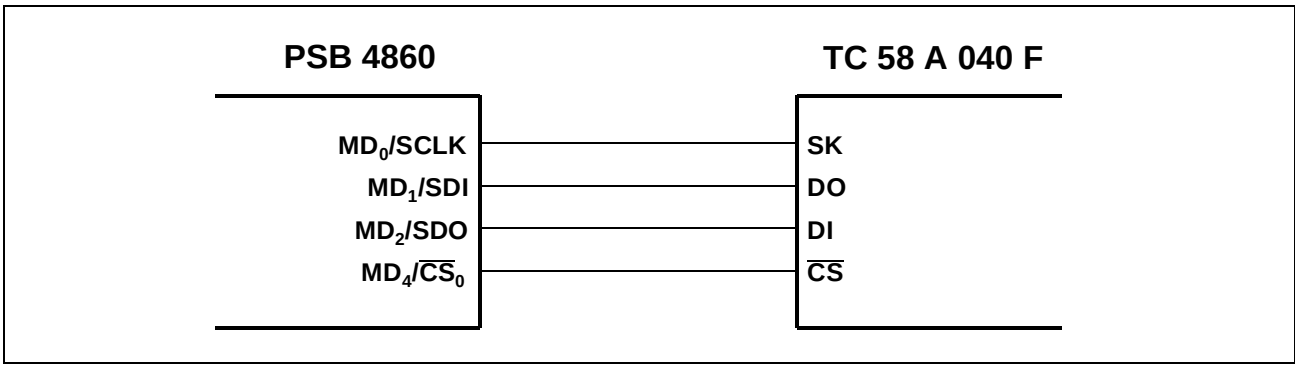


Figure 39 Connection to Single TC 58 A 040 F

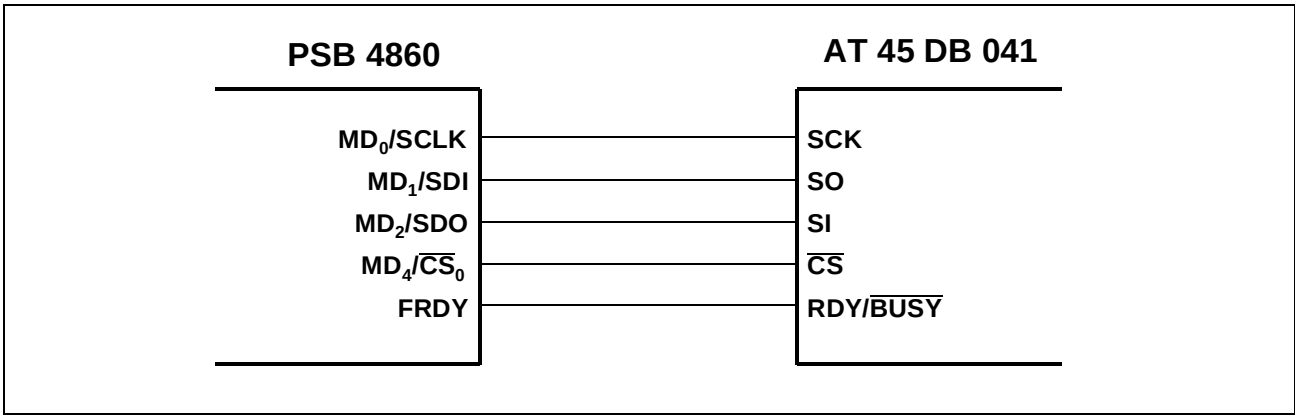


Figure 40 Connection to Single AT 45 DB 041

*In each case multiple devices can be connected by sharing the lines MD_0/SCLK, MD_1/SDI and MD_2/SDO as shown in figure **41**.*

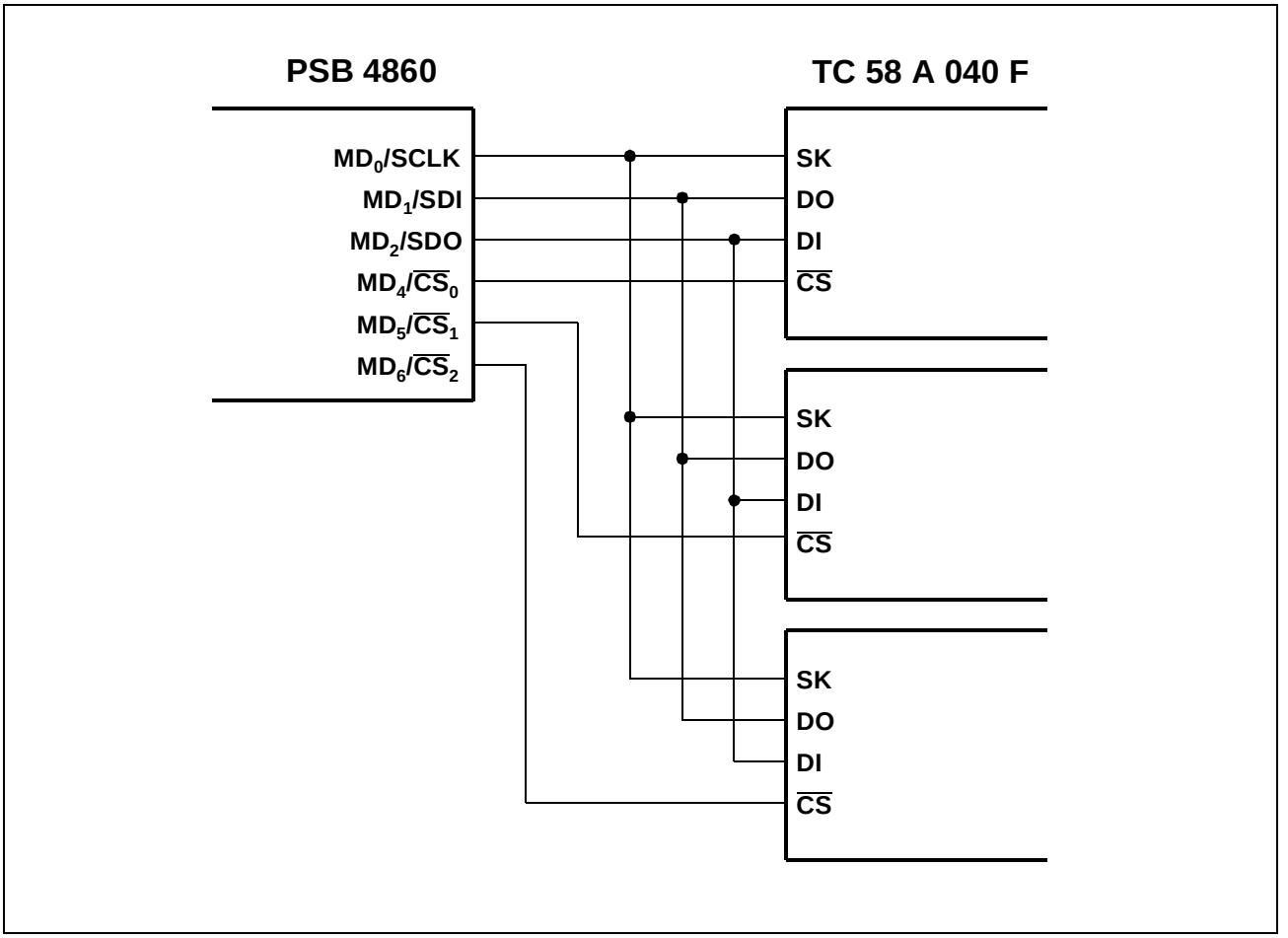


Figure 41 Connection to Multiple TC 58 A 040 F

4.6 Auxiliary Parallel Port *(Improved in Version 3.1)*

The PSB 4860 provides an auxiliary parallel port if flash memory is used. In this case the lines MA_0 to MA_{15} are not needed for the memory interface and can therefore be used for an auxiliary parallel port. This port has two modes: static mode and multiplex mode.

Unlike in V2.1 the auxiliary port can also be used if more than one Samsung flash device is connected. In this case the lines MA_8, MA_9, MA_{10} and MA_{11} are configured as the chip select lines for the flash devices while the remaining pins can be used as inputs or outputs.

4.6.1 Static Mode

In static mode all pins of the auxiliary parallel port interface have identical functionality. Any pin can be configured as an output or an input. Pins configured as outputs provide

a static signal as programmed by the controller. Pins configured as inputs are monitoring the signal continuously without latching. The controller always reads the current value.

4.6.2 Multiplex Mode

In multiplex mode, the PSB 4860 uses MA_{12}-MA_{15} to distinguish four timeslots. Each timeslot has a duration of approximately 2 ms. The timeslots are separated by a gap of approximately 125 µs in which none of the signals at MA_{12}-MA_{15} are active. The PSB 4860 multiplexes three more output registers to MA_0-MA_{11} in timeslots 0, 1 and 2. In timeslot 3 the direction of the pins can be programmed. For input pins, the signal is latched at the falling edge of MA_{15}. Figure **42** shows the timing diagram for multiplex mode.

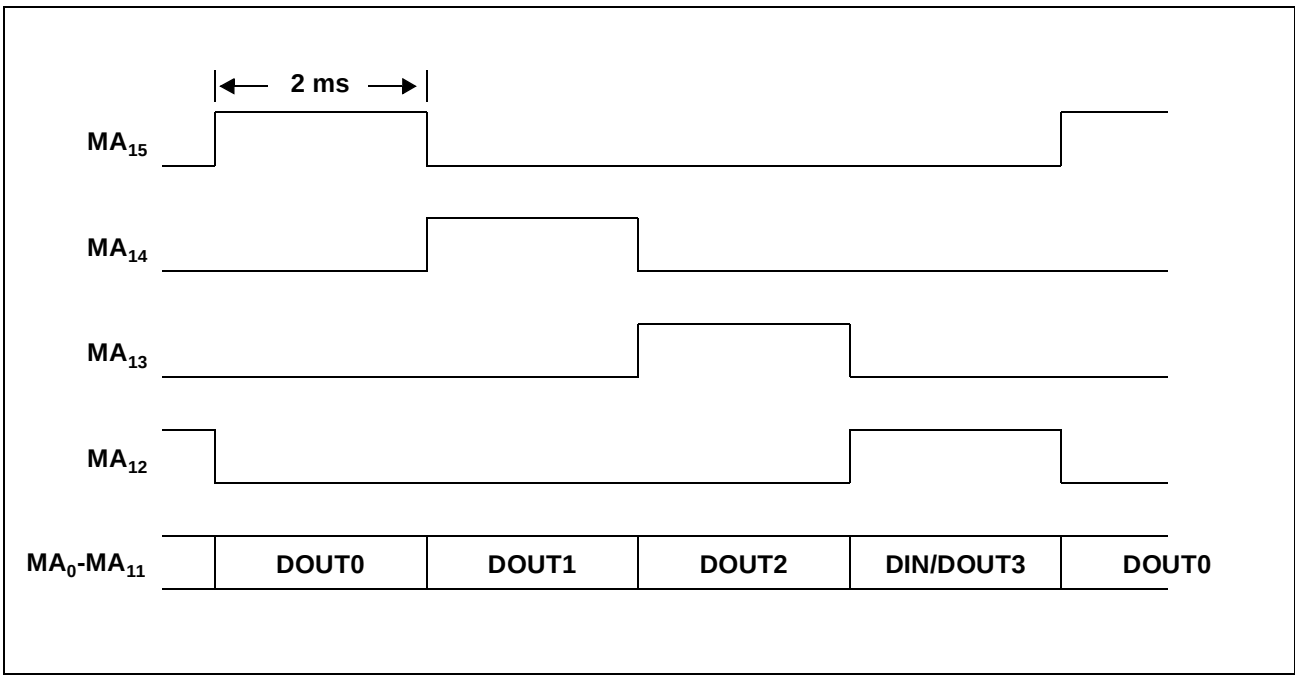
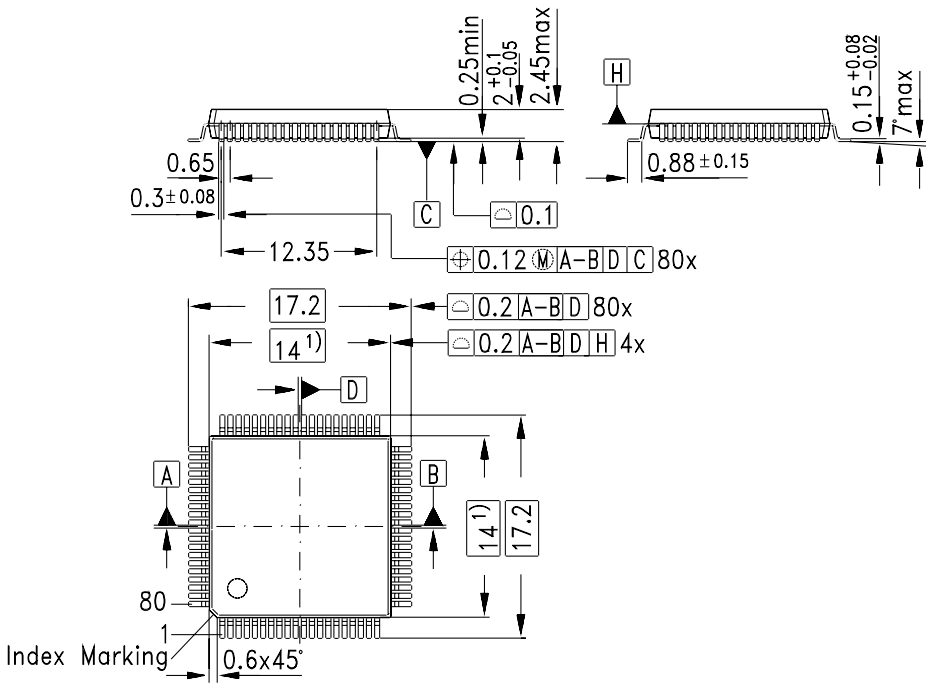


Figure 42 Auxiliary Parallel Port - Multiplex Mode

5 Package Outlines

Plastic Package, P-MQFP-80 (SMD)
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusions of 0.25 max per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm